Semiconductor industry – Challenges and Opportunities

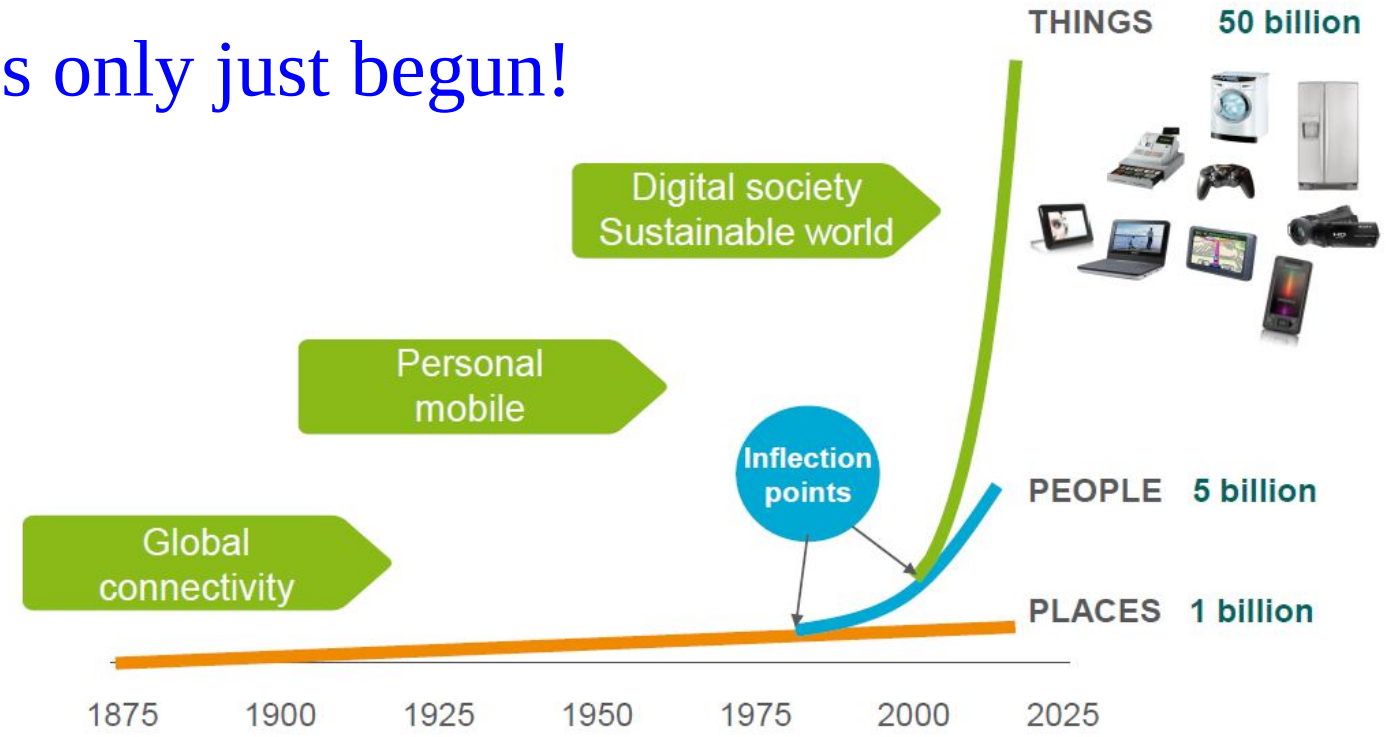
Yogesh S. Chauhan
Assistant Professor and Ramanujan Fellow
Nanolab, Department of Electrical Engineering
IIT Kanpur
Email: chauhan@iitk.ac.in
Homepage – http://home.iitk.ac.in/~chauhan/

Outline

- Hyperconnected Age
  - Role of semiconductors
- What is semiconductor
  - MOSFET and Scaling
  - Multigate Transistors
    - FinFET
    - Thin-Body Transistor
- Compact Modeling of FinFET and UTB FET
- What next?

Hyperconnected Age

- We are living in an unprecedented era of hyperconnectivity that is redefining our societies, cultures, and communications.
- And it has only just begun!



Hyperconnected Age

- Present
  - Facebook has more than 1.4 billion users worldwide, creating a hyperconnected, global social network
  - Human to Device interaction
- Future
  - Device to Human interaction
  - Device to Device interaction

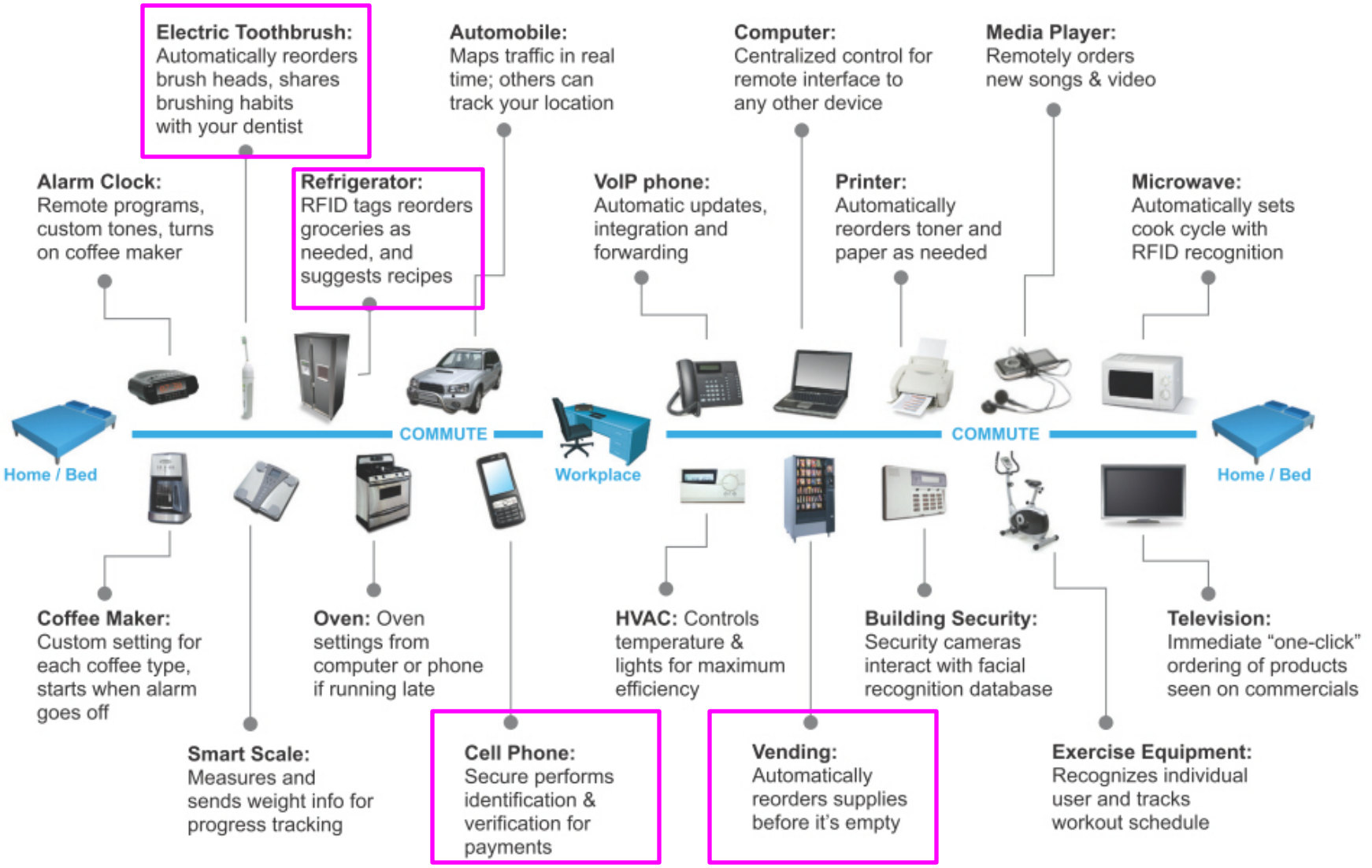
CISCO – By 2020, there will be 50 billion networked devices.

Electronics industry

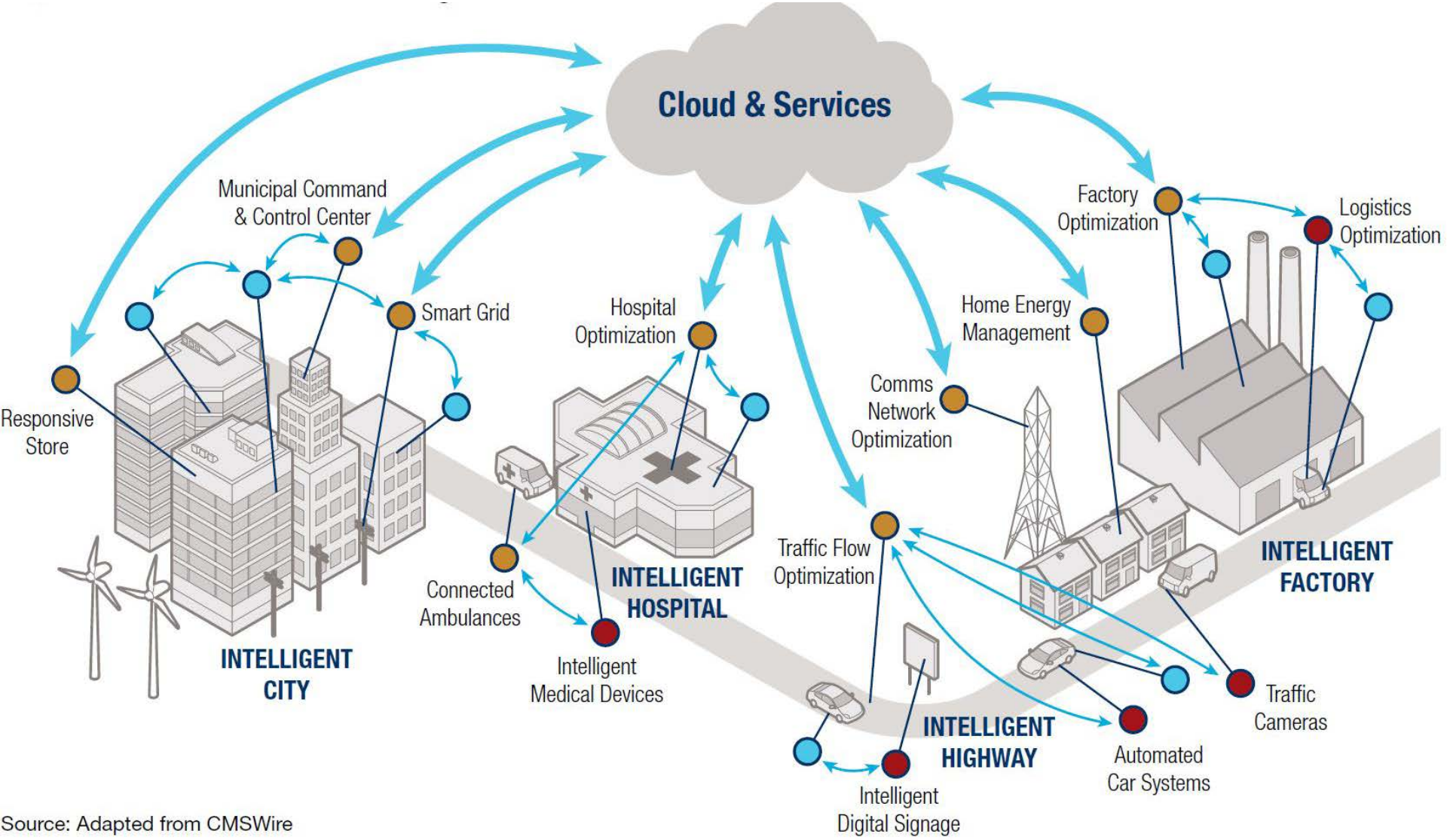
- Playing important role in making this planet smarter!
- Key enabling technologies
  - Internet of things
  - Cloud
  - Healthcare
  - Robotics
  - Automobile
  - Food

Source: European Commission

Internet of things

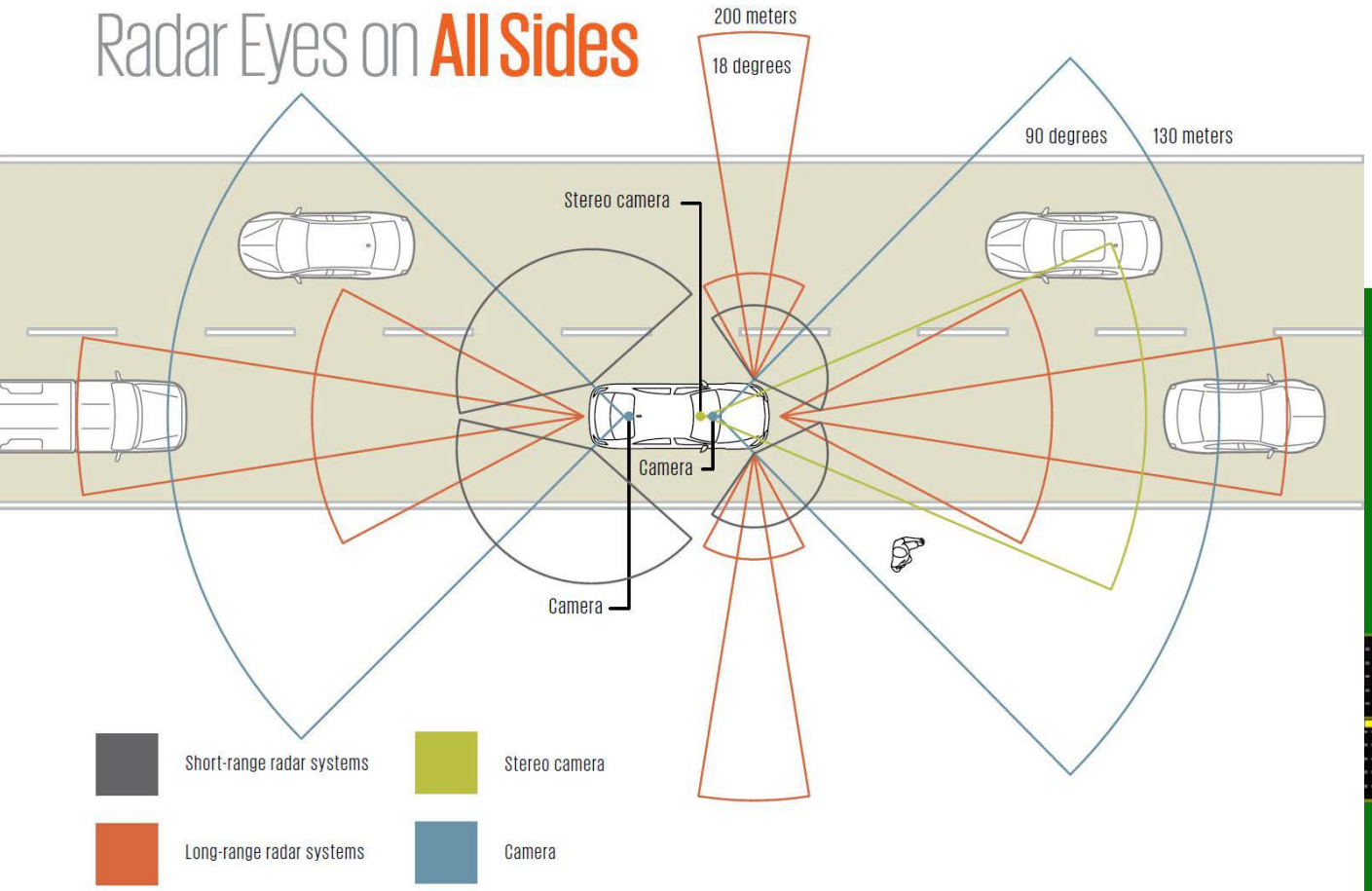


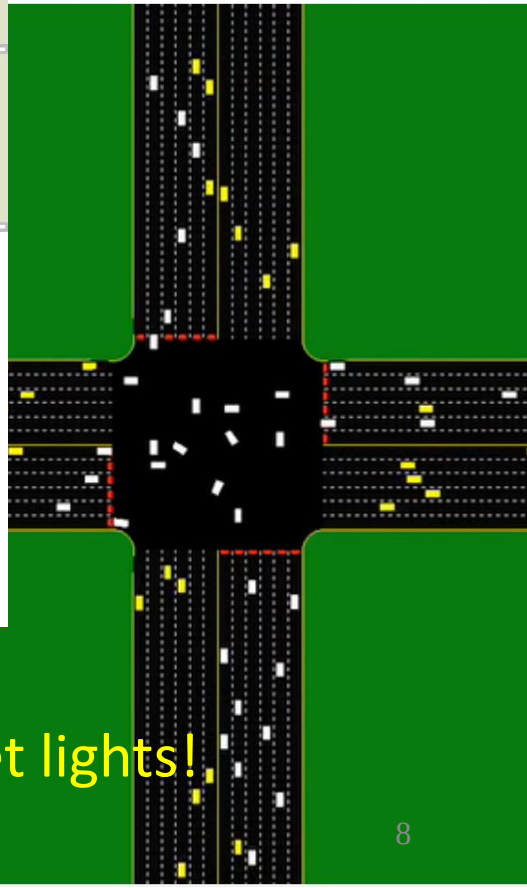
IoT & Cloud – Data and Computation



Source: Adapted from CMSWire

Automobile – Driverless car



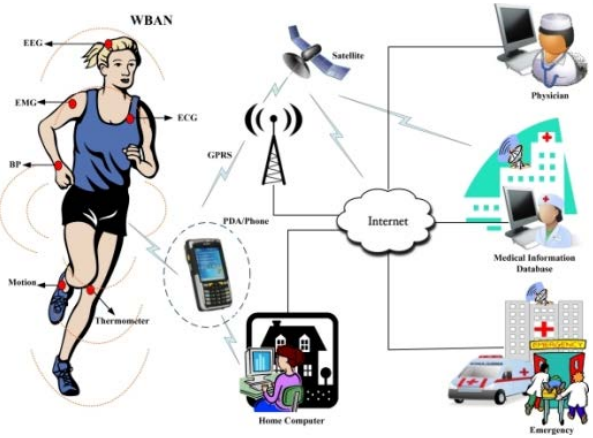


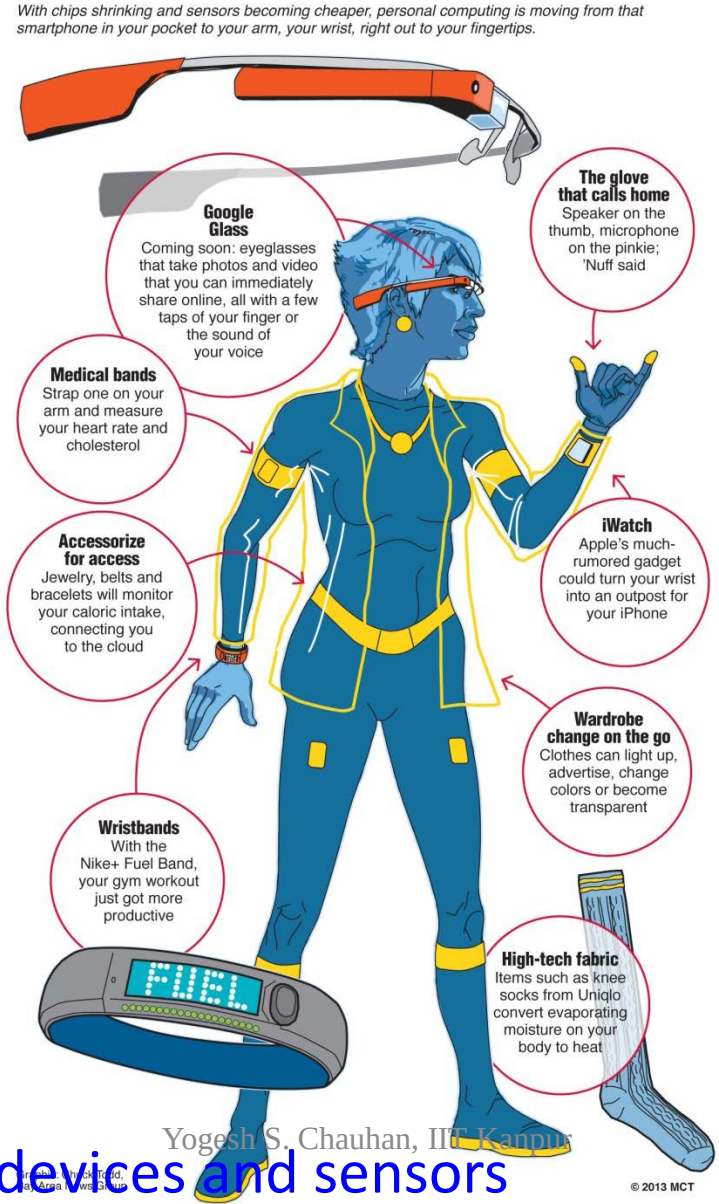
No street lights!

Source: IEEE Spectrum, Aug. 2014

Wearable Electronics

Smart Watch

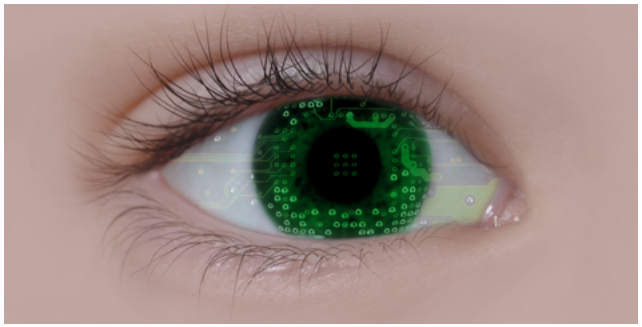


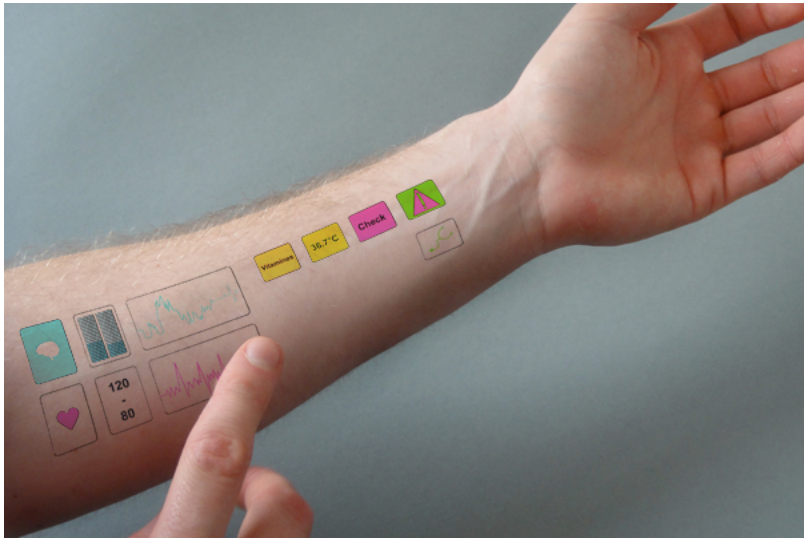


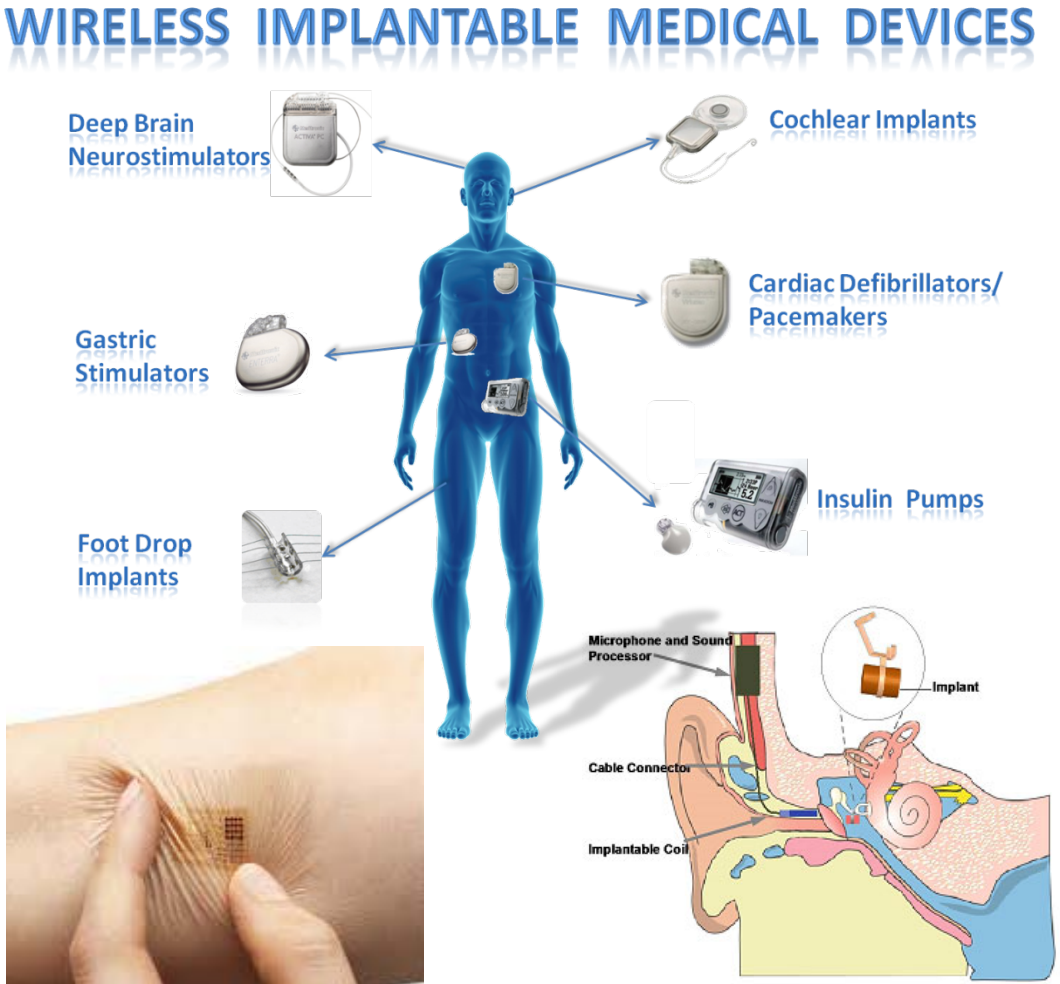
Google Glass

Need ultra-low power devices and sensors

Healthcare – Implantable Electronics

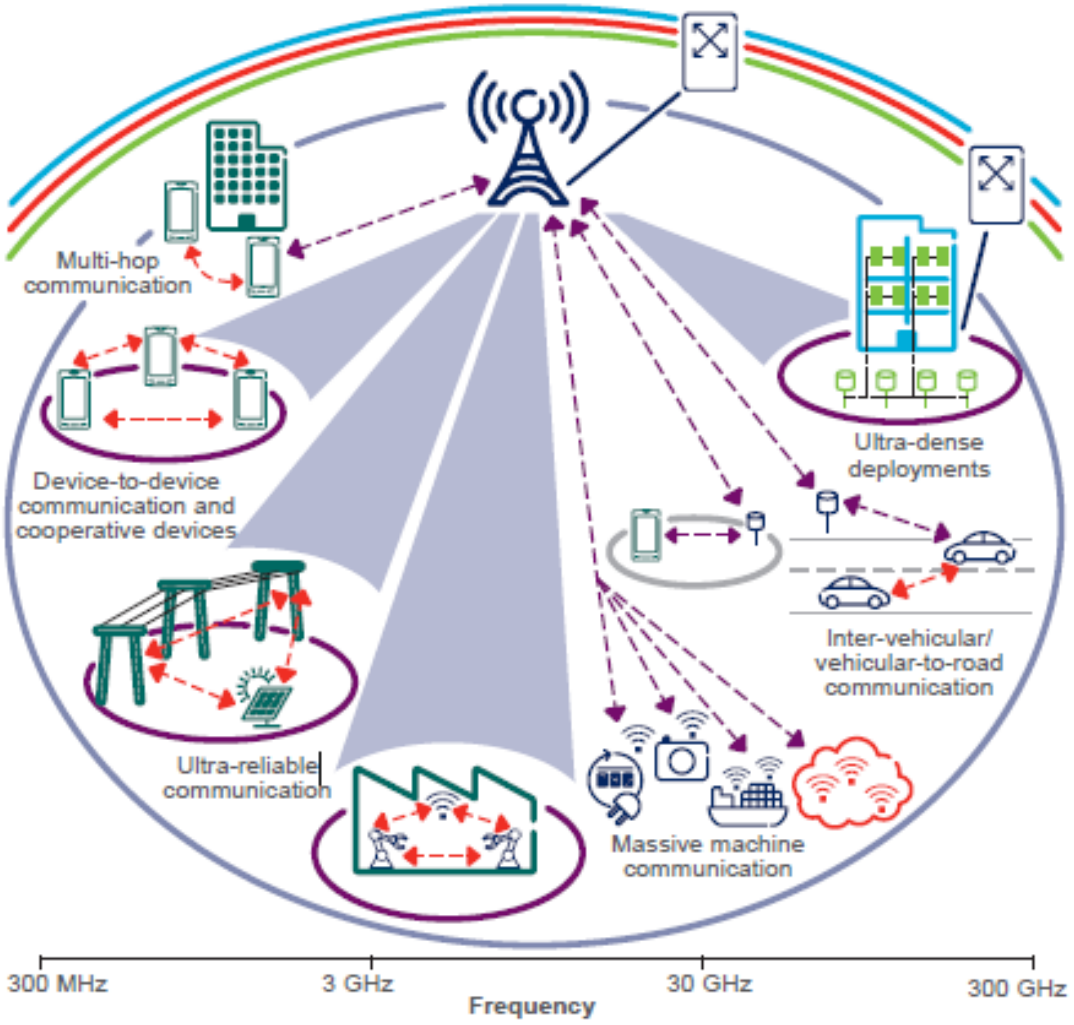




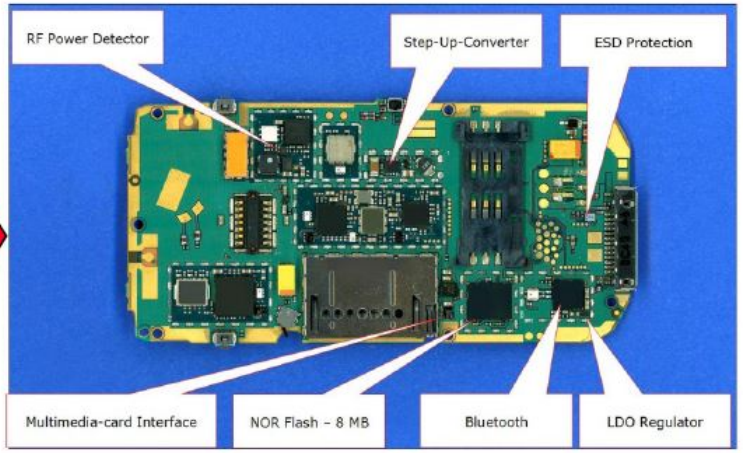


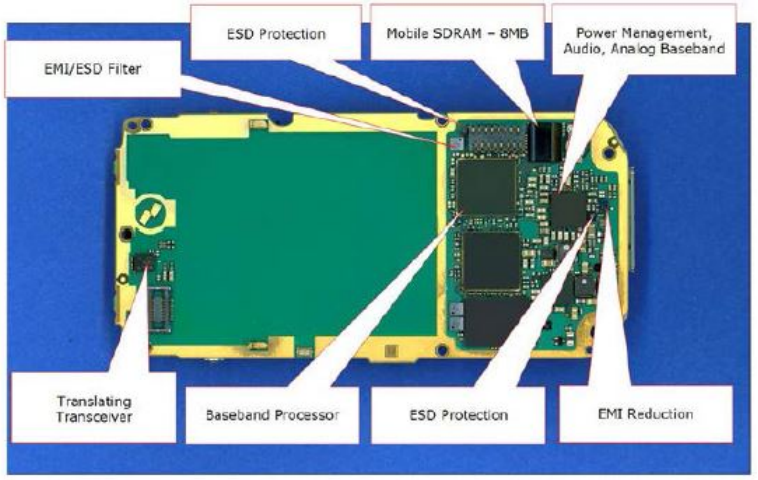
5G –Machine communication

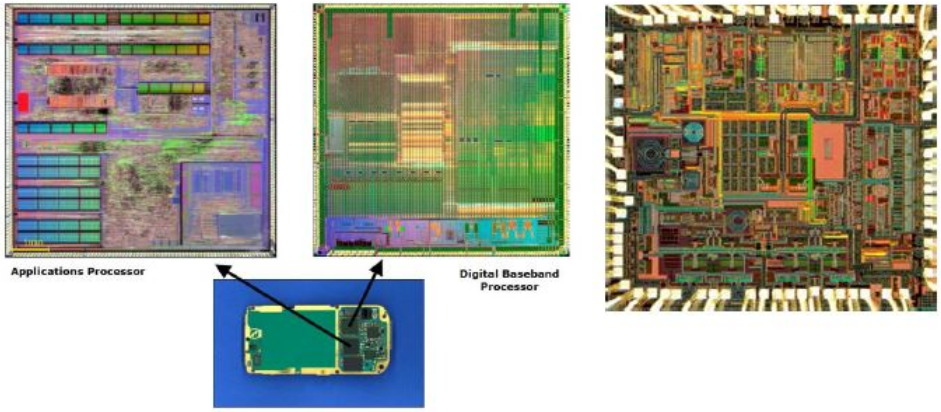
- Communication
  - Device to device
  - Machine to machine
  - Vehicle to vehicle
- UHD live video



The Deconstructed Cell Phone







Hint: It's All About the Microelectronics!

Semiconductors – Heart of technological progress and innovation

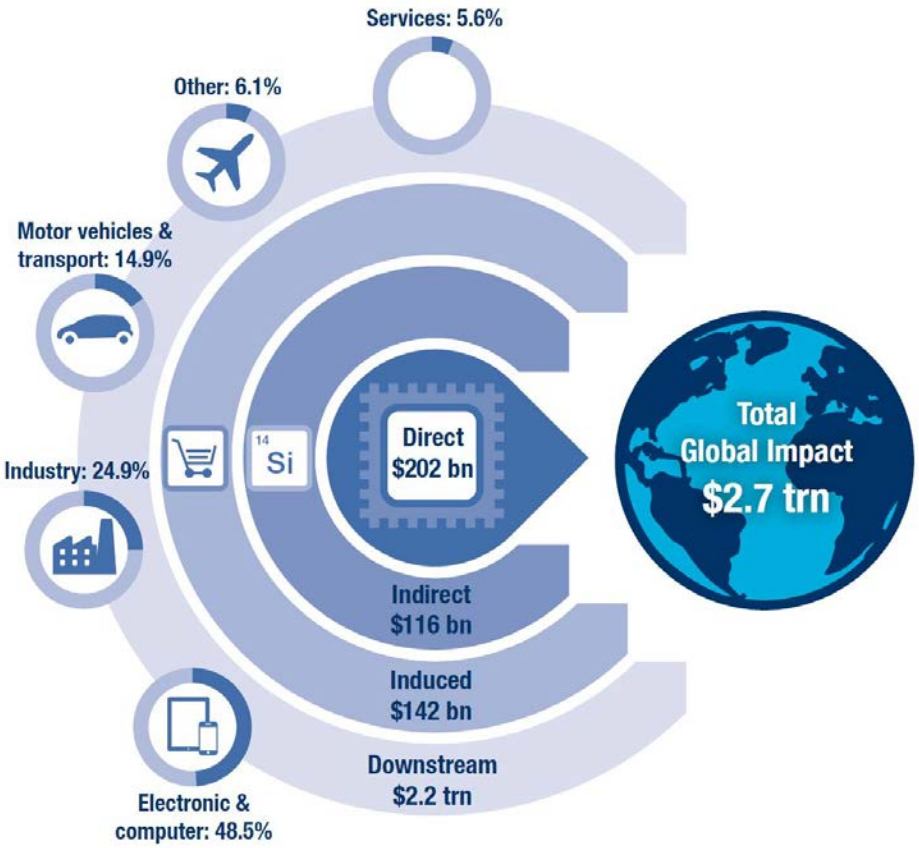
- The semiconductor is one of the most pervasive and powerful inventions in human history.

Nobel Prize in Physics 2014
"invention of efficient blue LEDs"

Economic impact of semiconductors

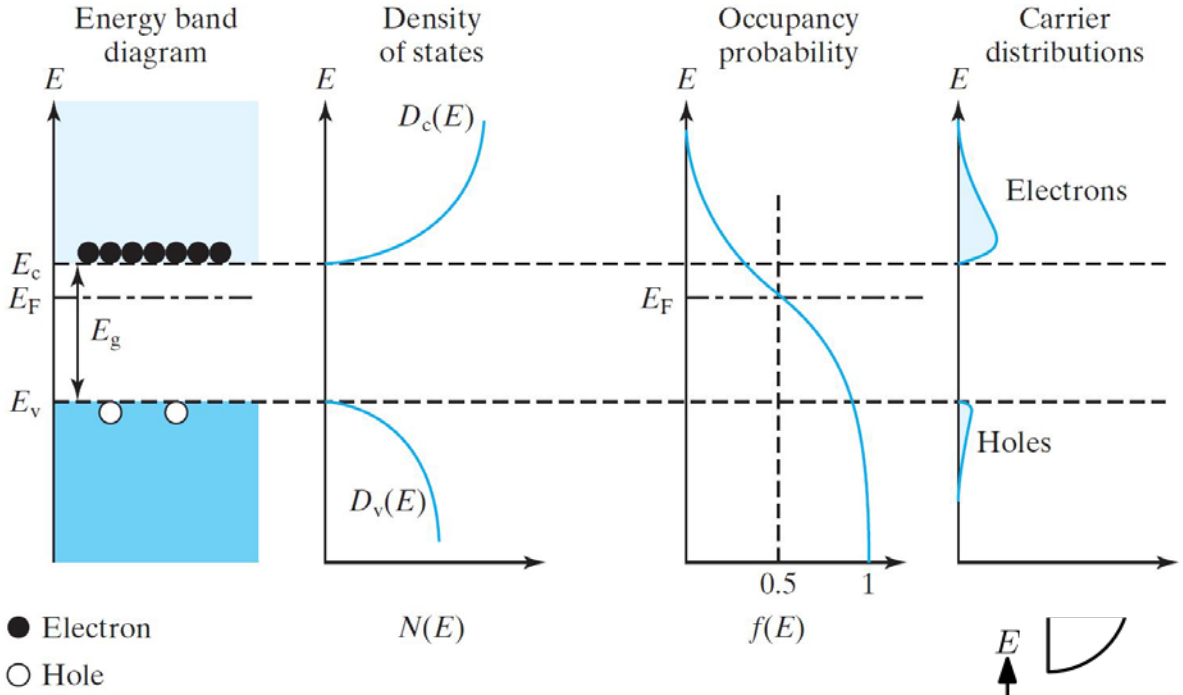
- Semiconductors touch every sphere of economic activity.

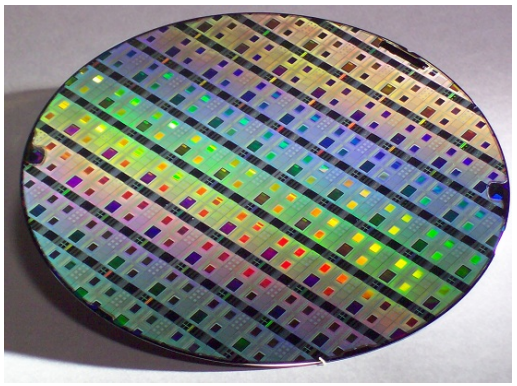
- Direct: ~$300 bn
- Indirect
  - Material/equipment
- Induced
  - consumer market
- Downstream
  - Other industry

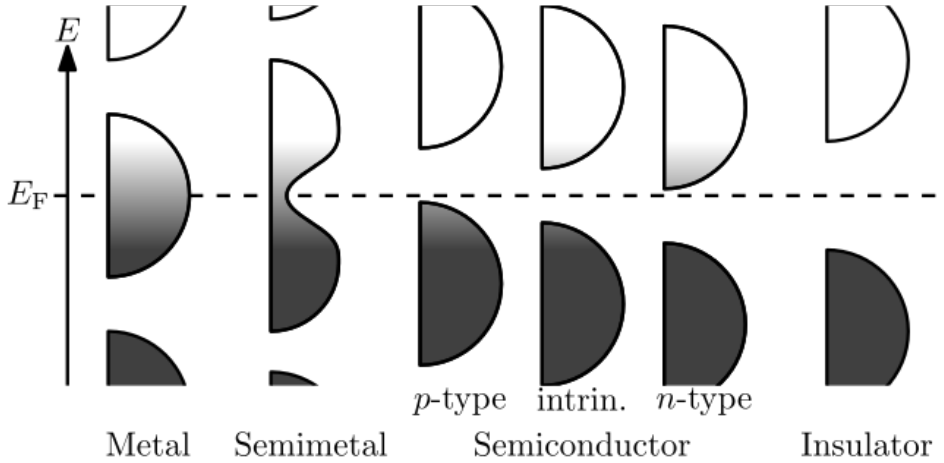


Source: Global Semiconductor Alliance and Oxford Economics

What is semiconductor?

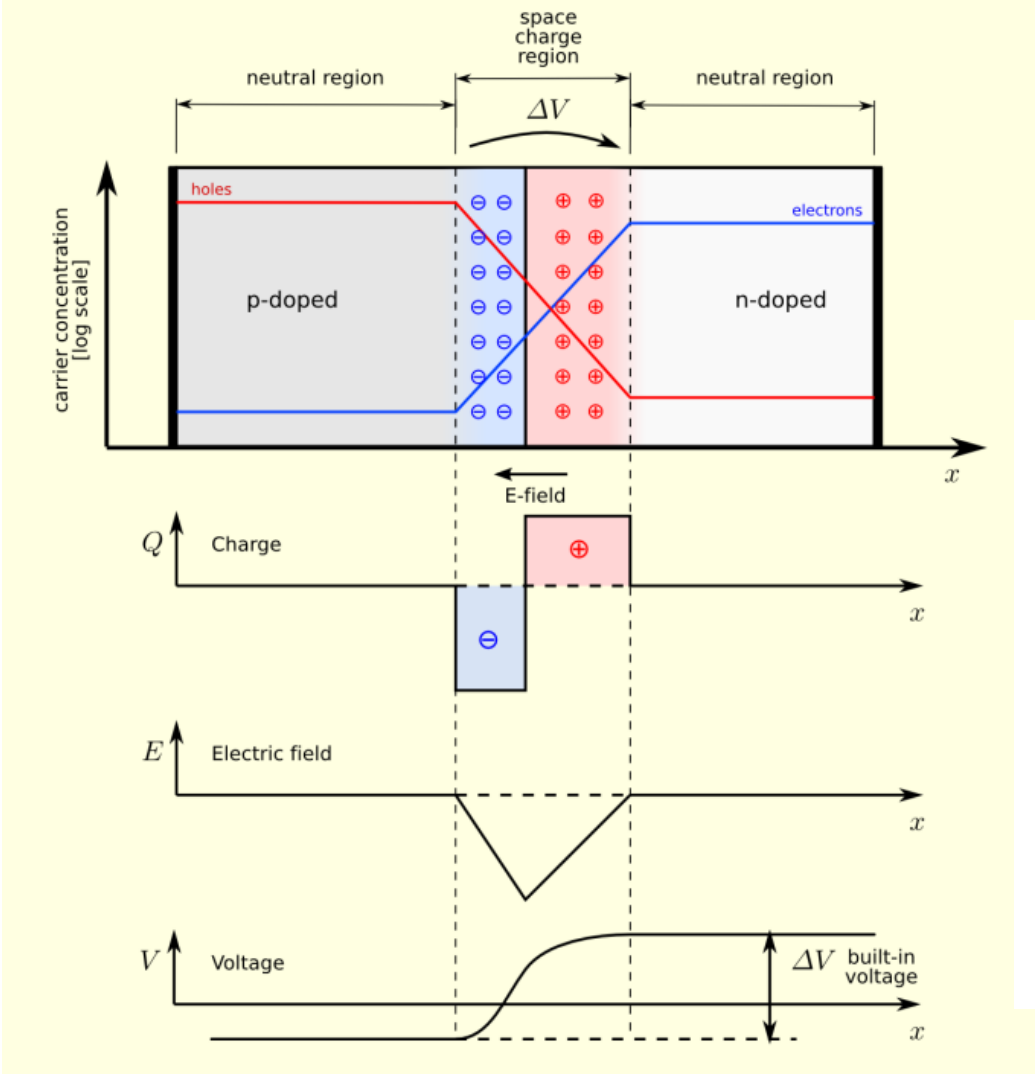




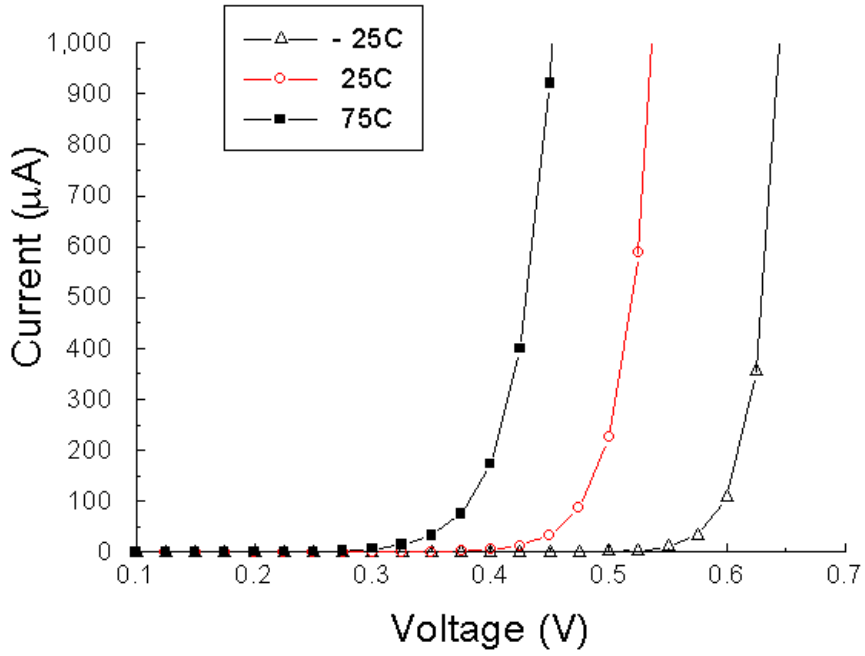


Source: Anandtech

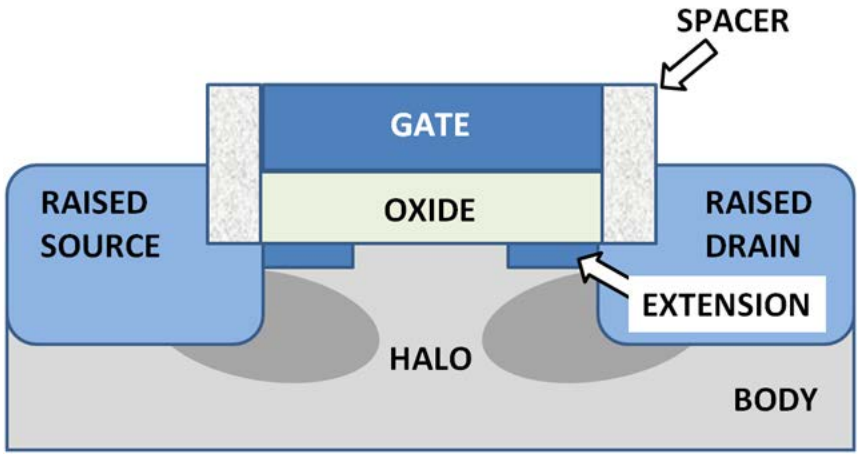
Semiconductor Devices – Junction

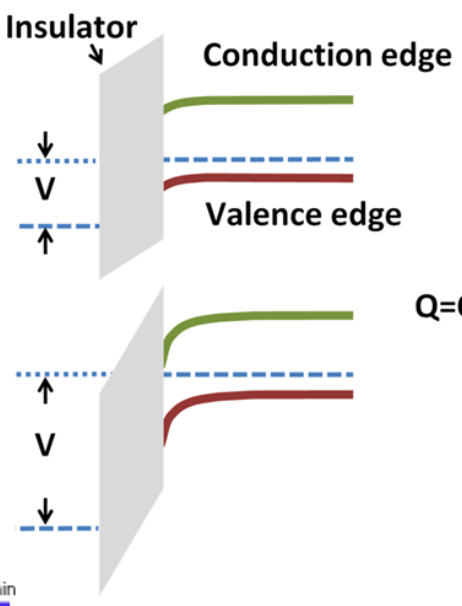


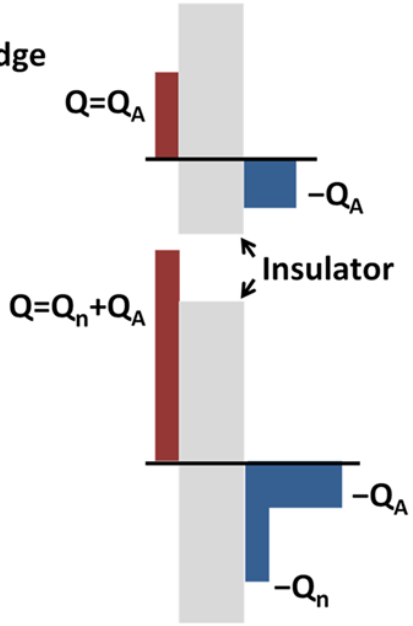
- Doping
- Junction

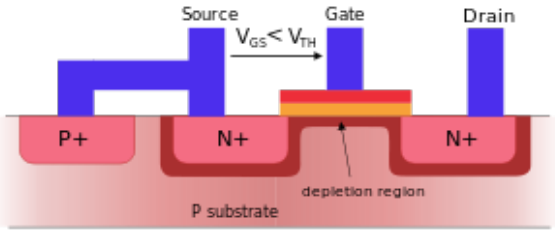


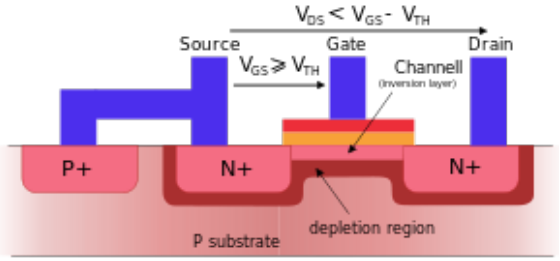
Semiconductor Devices – MOSFET



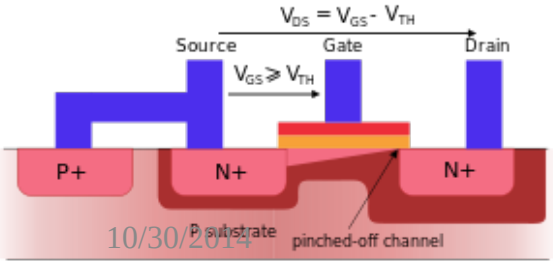




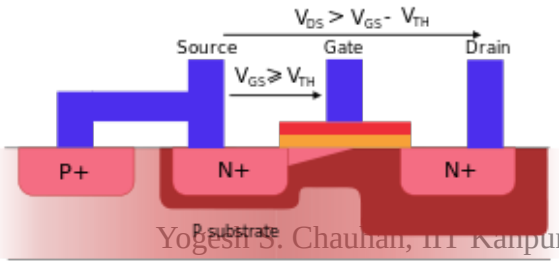




Linear operating region (ohmic mode)



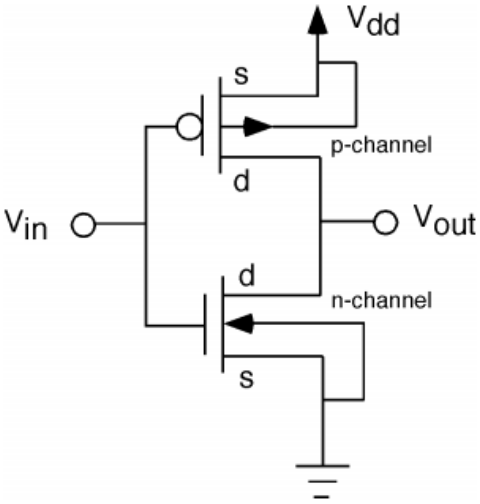
Saturation mode at point of pinch-off



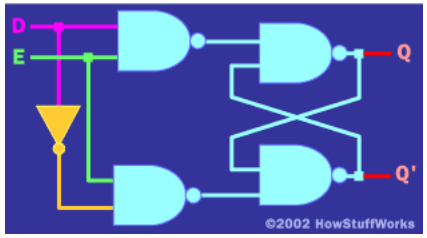
Saturation mode

Semiconductor devices to circuits

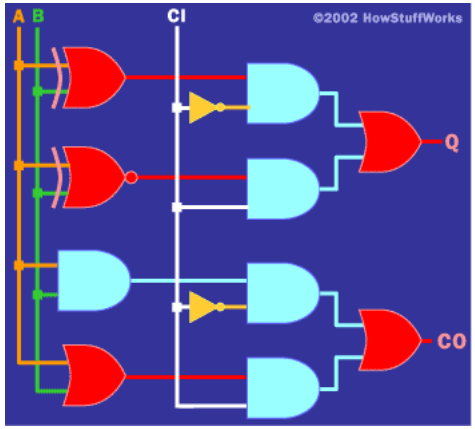
NOT gate



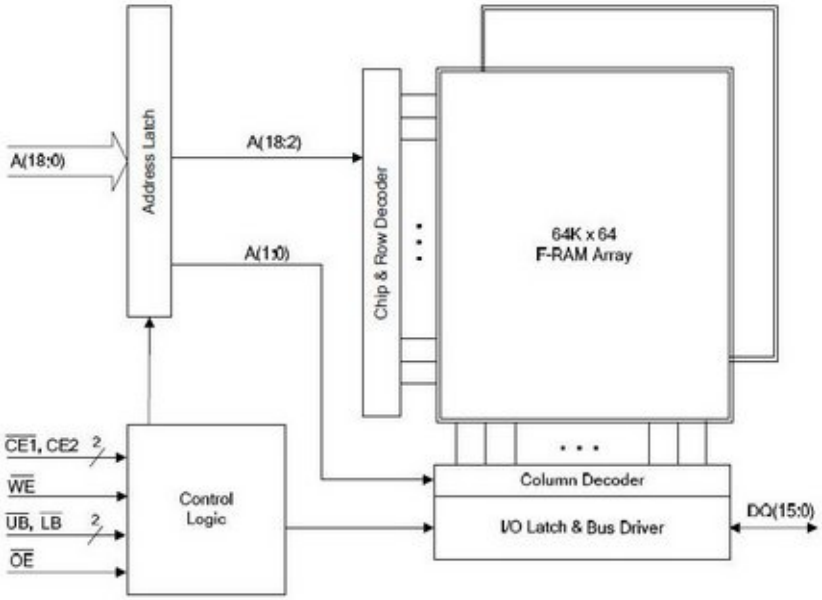
Flip-flop



Full Adder

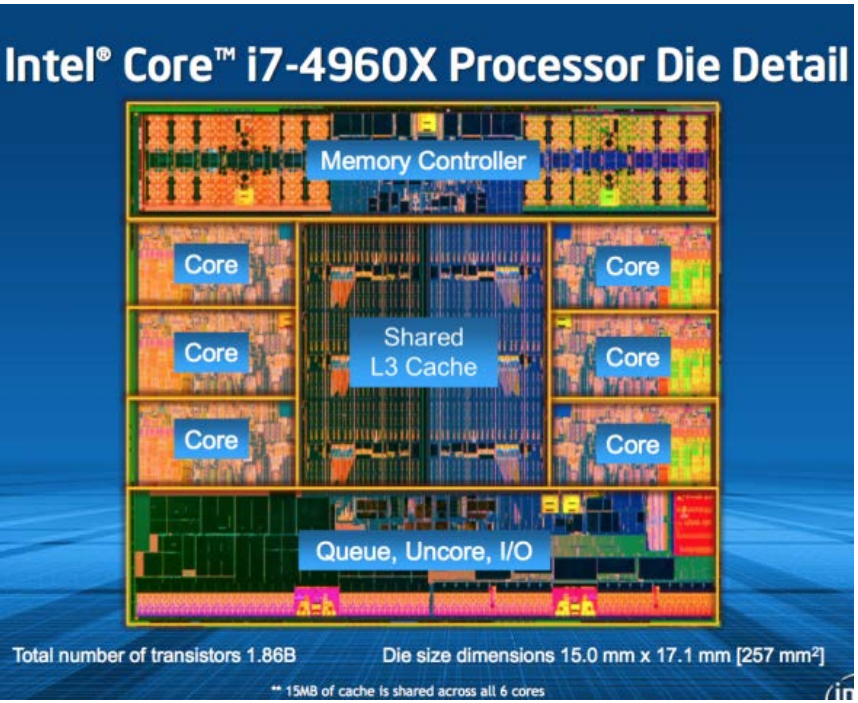


Memory



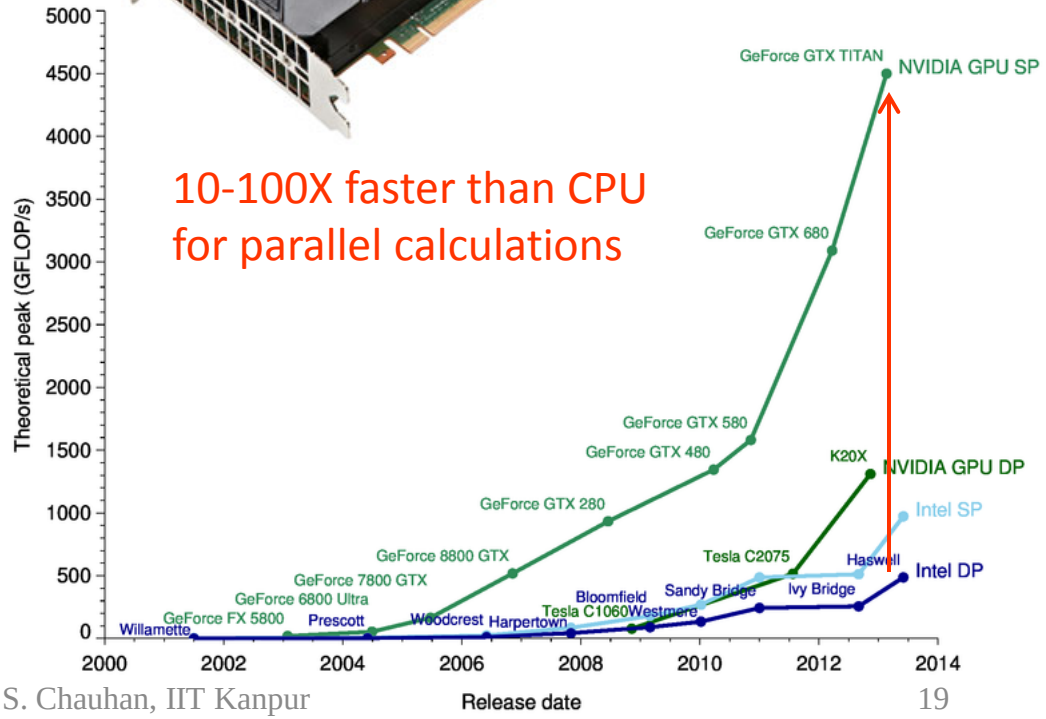
Semiconductor circuits to Products

CPU



GPU – Graphics Processing Unit

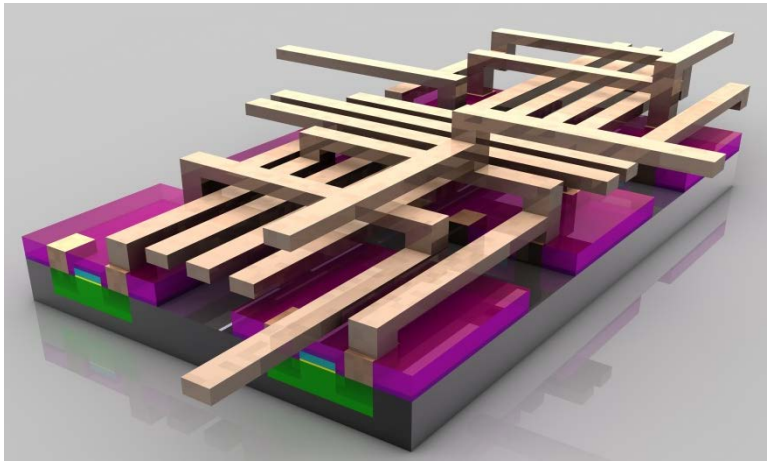
10-100X faster than CPU
for parallel calculations



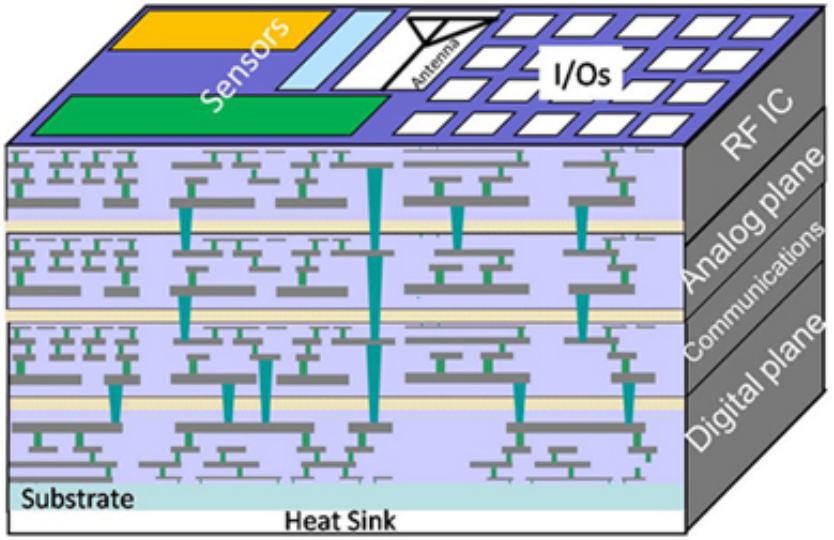
Source: Anandtech, Intel, Nvidia

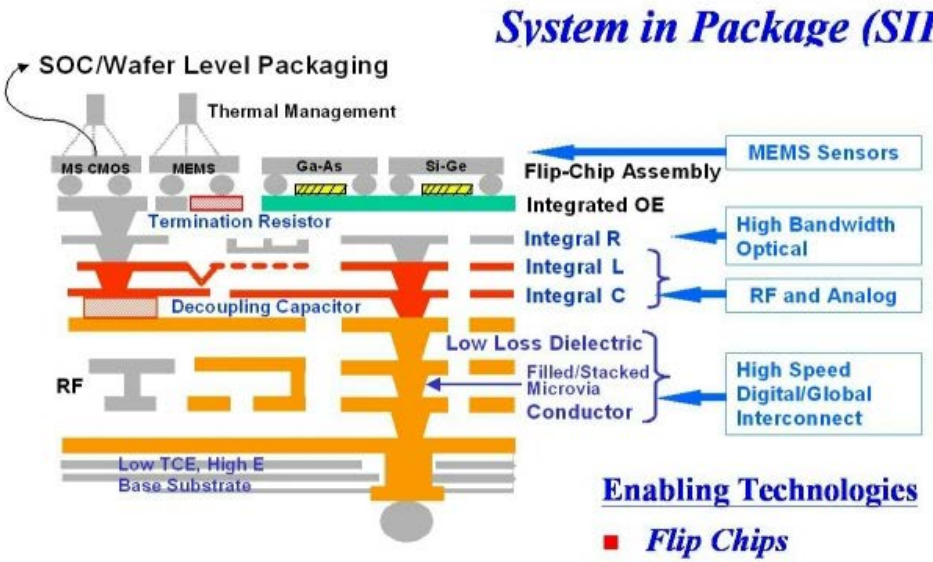
Today's ICs

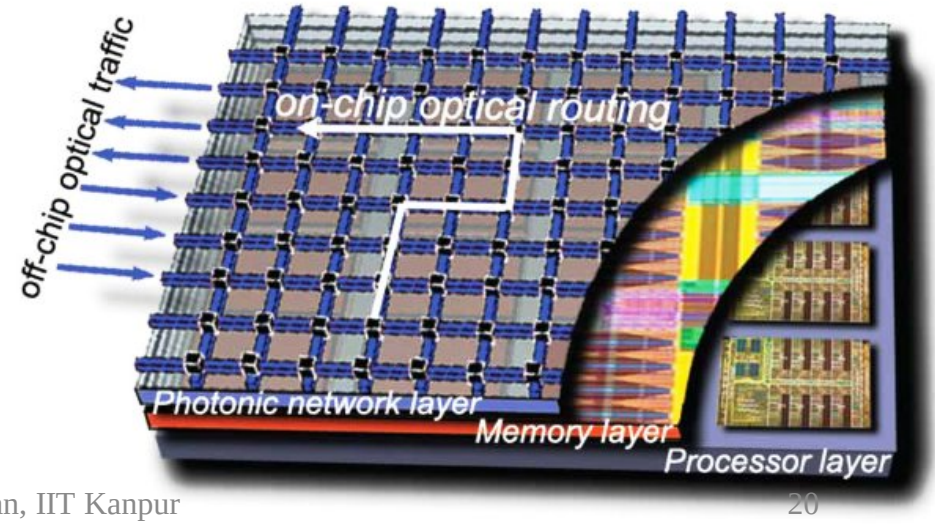
Multiple metal layers



3D ICs





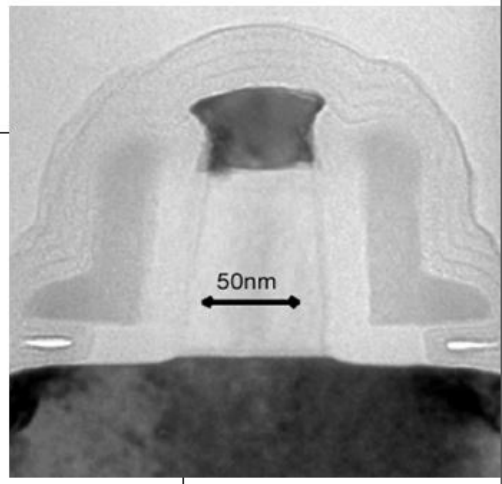


How do you make these?

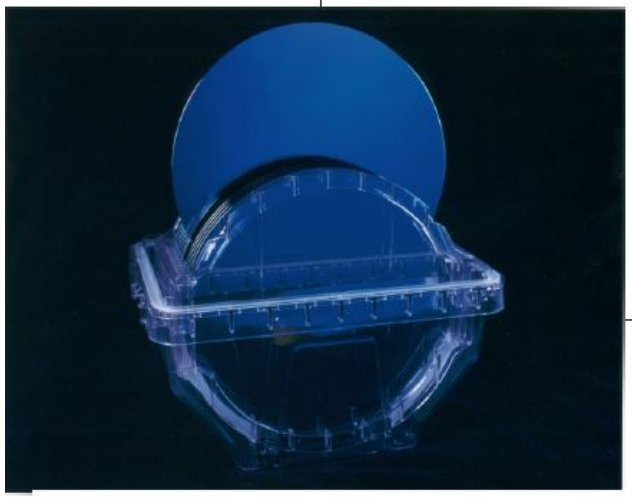
Start

Silicon Crystals

Bunny Suits!

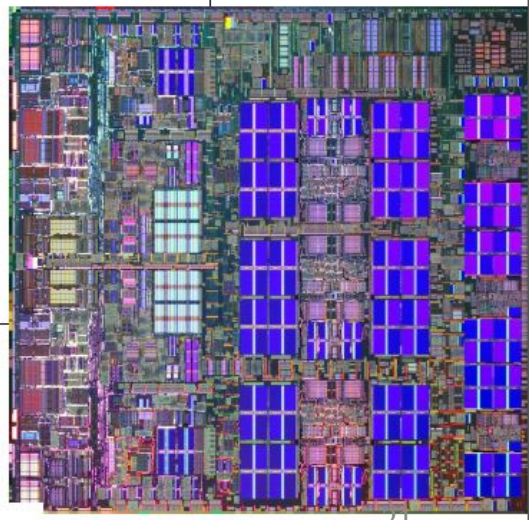


10B Transistors per cm^2



Silicon "Wafers"

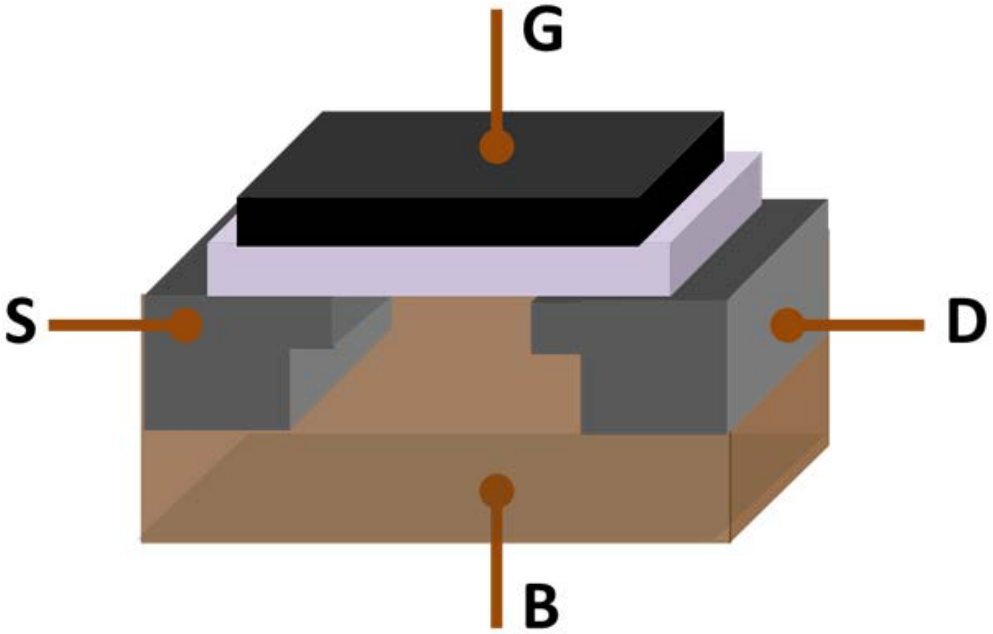
$5B Fabrication Facility



Finish

Building block – (tiny) MOSFET!

- MOSFET is a transistor used for amplifying or switching electronic signals.



Invention of Transistor

- First Transistor (1947-1948) at AT&T's Bell Labs
  - Point Contact Transistor
  - First transistor was bipolar contact transistor
  - Material – Germanium

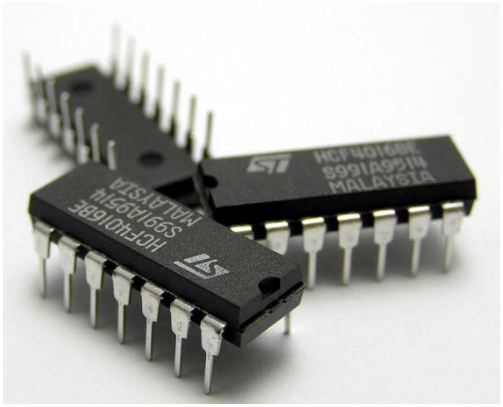
Invention of Transistor

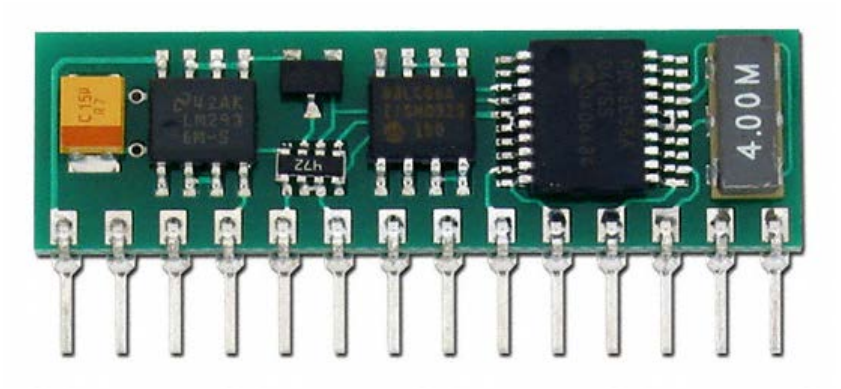
William Shockley

- Worked on theory of Diode, Transistor, Thyristor etc.
  - Invented First transistor at Bell Labs
  - Received Nobel Prize in 1956
- Formed Shockley semiconductor in Mountain View, California in 1956
- Employees of Shockley semiconductor (Robert Noyce, Gordon Moore, ….)
  - These employees opened 65 companies in next 20 years including Intel, AMD, Fairchild,…

Integrated Circuit (IC)

- IC – Electronic circuit manufactured on the surface of a thin substrate of semiconductor material.
- Additional materials are deposited and patterned to form interconnections between semiconductor devices.



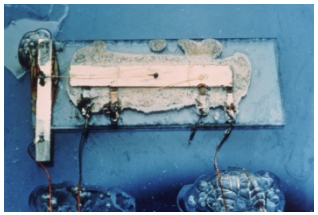


- ICs are used in virtually all electronic equipment today and have revolutionized the world of electronics.

Invention of Integrated Circuits

- Jack Kilby (at *Texas Instruments*) demonstrated first working IC in 1958.
  - Jack Kilby was awarded the Nobel Prize in Physics 2000.
  - Kilby's work was named an IEEE Milestone in 2009.

First IC

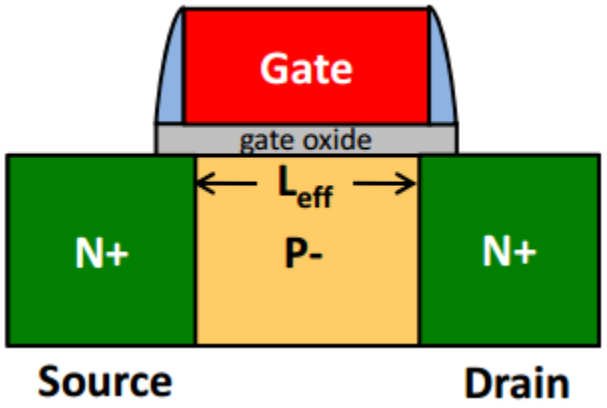


First handheld Calculator

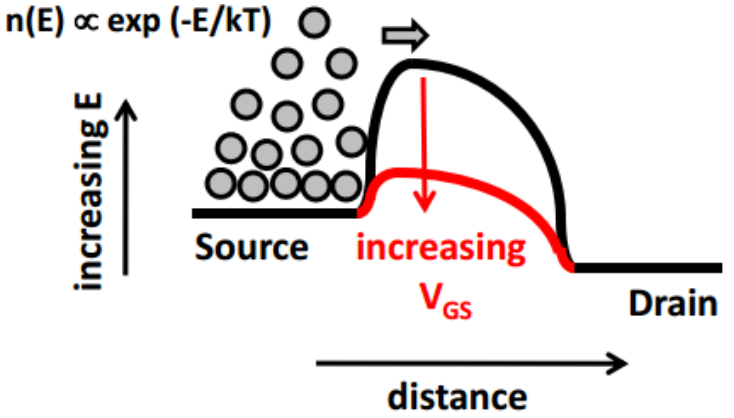
- Robert Noyce (at *Fairchild Semiconductor*) also invented IC separately six months later than Kilby.
  - It was made of silicon, whereas Kilby's chip was made of germanium.
  - Fairchild Semiconductor was also home of the first silicon gate IC technology with self-aligned gates, which stands as the basis of all modern CMOS computer chips.

Bulk MOSFET

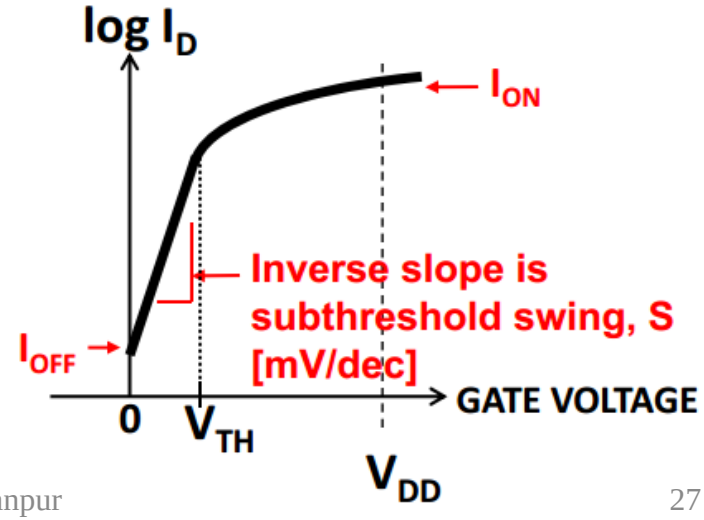
Schematic Cross Section



Barrier height is controlled by gate voltage



I_{DS} controlled by V_{GS}



Desired

- **High I_{ON}**
- **Low I_{OFF}**

Figures: T.Liu, SRC/GRC e-Workshop, November 2012

Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

- Drain current in MOSFET (OFF operation)

$$I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)}$$

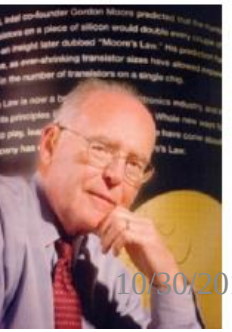
$C_{ox}=\varepsilon_{ox}/t_{ox}$=oxide cap.
S – Subthreshold slope

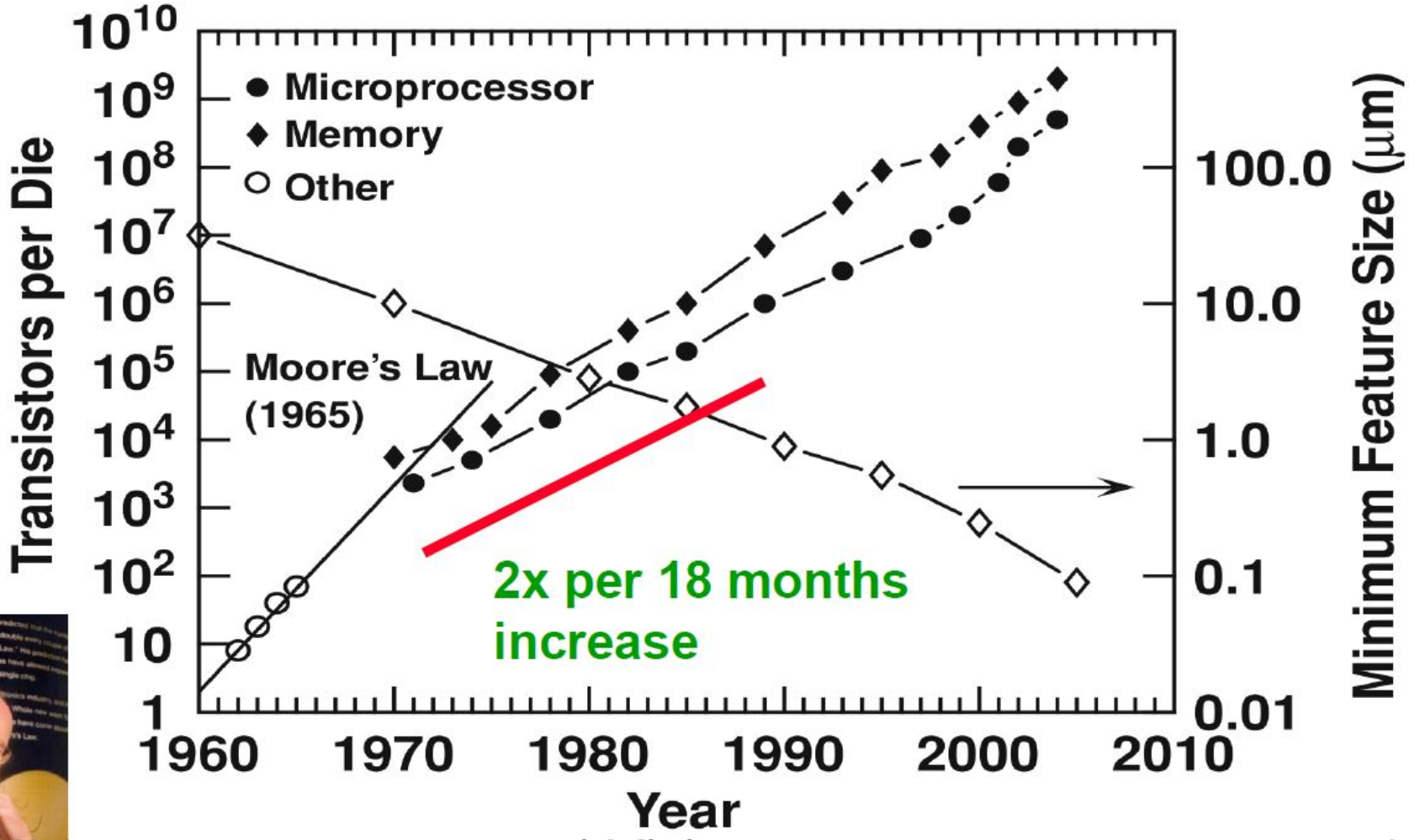
- **Desired**
- **High I_{ON} (↓L, ↑Cox, ↑V_{DD}-V_{TH})**
- **Low I_{OFF} (↑V_{TH}, ↑S)**

Moore's Law:

The defining features of the integrated circuit technology (size, speed, cost) follow an exponential growth pattern over time

Moral: Computing power ⬆ while cost ⬇ exponentially!





Technology Scaling drives down the cost

- **Scaling:** At each new node, all geometrical features are reduced in size to 70% of the previous node.
- **Reward:** Reduction of *circuit size by half*.
  - Twice number of circuits on each wafer
  - Cost per circuit is reduced significantly.

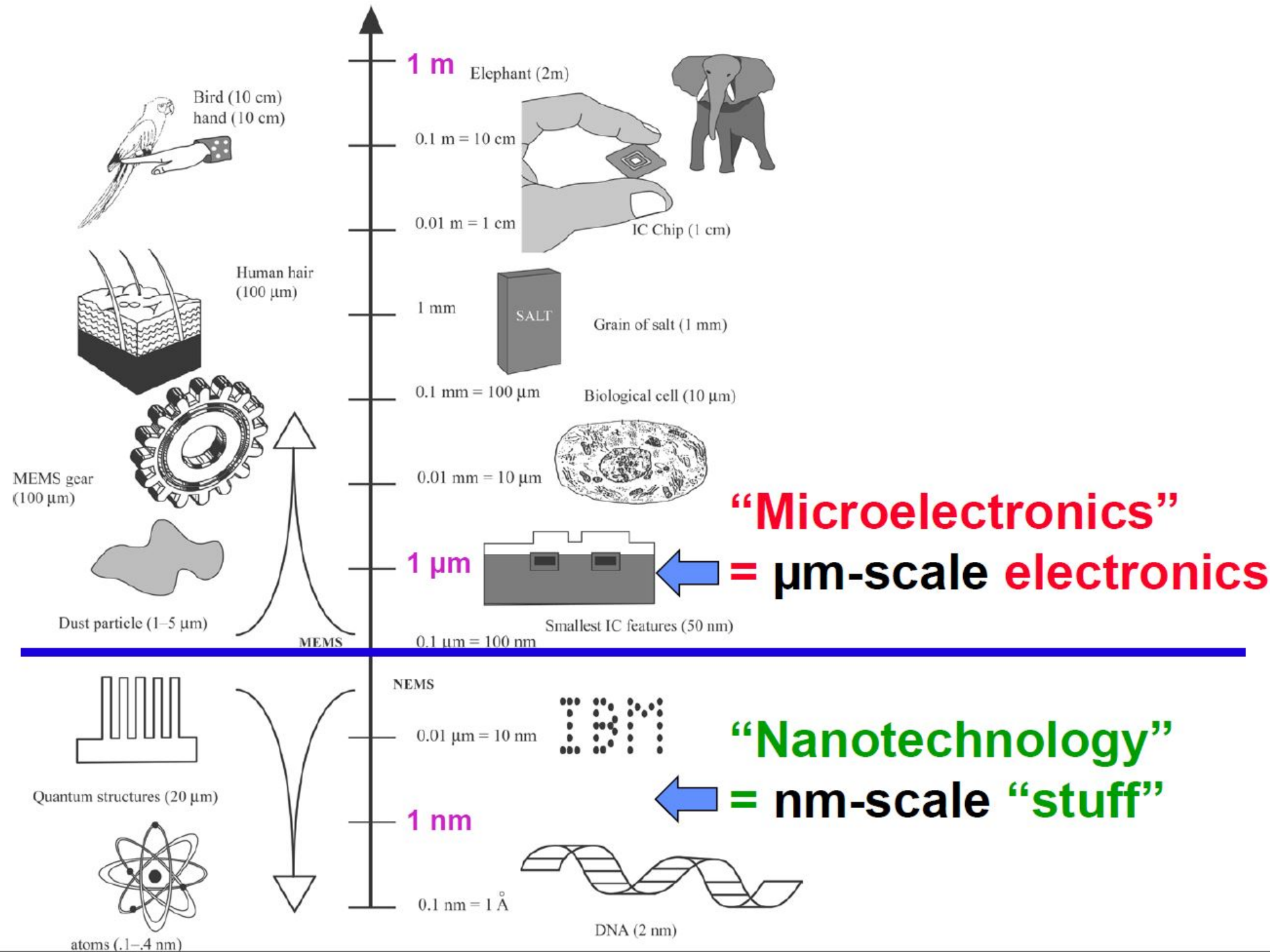
$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

Moore's Law

It's not technology! → It's economy.

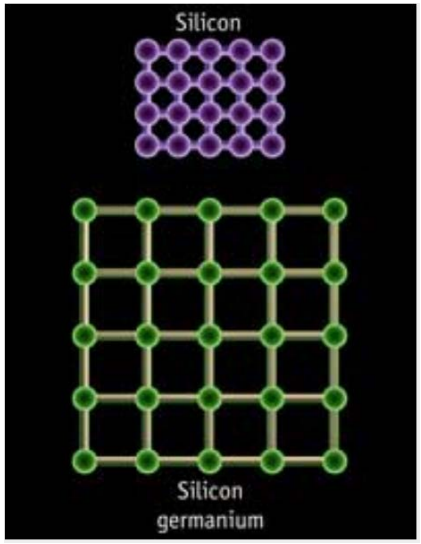
In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore's Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.

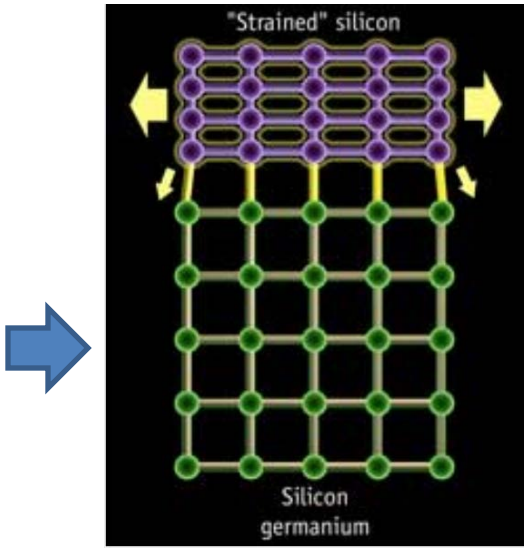
- Ways to Huge Profits
  - High performance and Low Cost
  - Achieved by making everything SMALLER

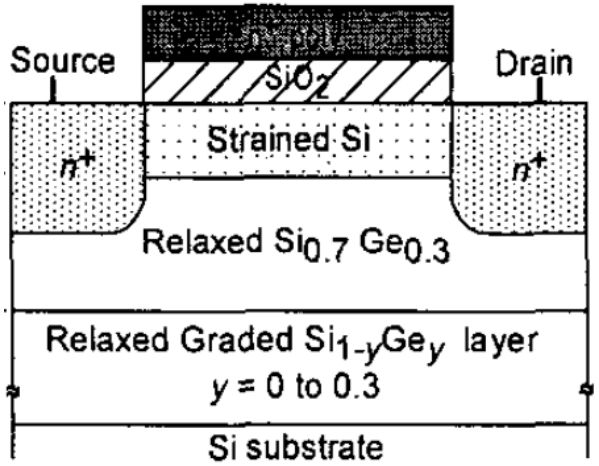

1 m
Elephant (2m)
Bird (10 cm)
hand (10 cm)
0.1 m = 10 cm
0.01 m = 1 cm
IC Chip (1 cm)
Human hair
(100 µm)
1 mm
SALT
Grain of salt (1 mm)
0.1 mm = 100 µm
Biological cell (10 µm)
MEMS gear
(100 µm)
0.01 mm = 10 µm
1 µm
Dust particle (1–5 µm)
MEMS
Smallest IC features (50 nm)
0.1 µm = 100 nm
NEMS
0.01 µm = 10 nm
IBM
Quantum structures (20 µm)
1 nm
atoms (.1–.4 nm)
0.1 nm = 1 Å
DNA (2 nm)
"Microelectronics"
= µm-scale electronics
"Nanotechnology"
= nm-scale "stuff"

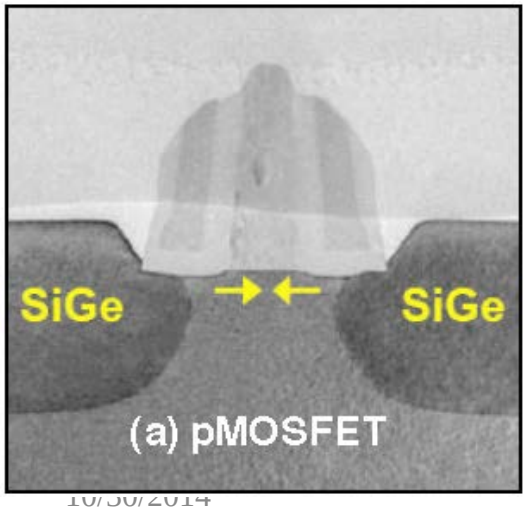
Strained Silicon $I_{ON} = \mu \frac{W}{L} C_{ox}(V_{DD} - V_{TH})^2$

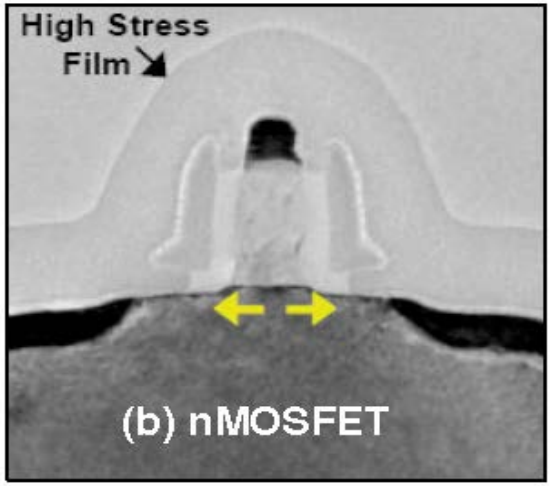
Silicon is placed on substrate having large atomic spacing











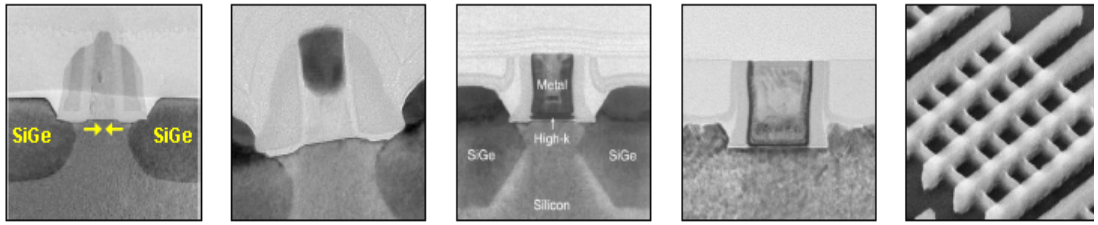
Methods of straining

-Burried SiGe –Biaxial

-Uniaxial Stress S/D SiGe

Technology Trend

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



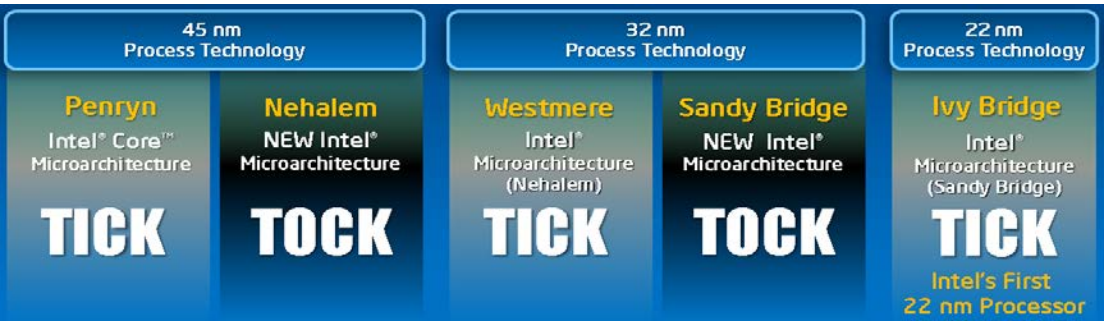
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

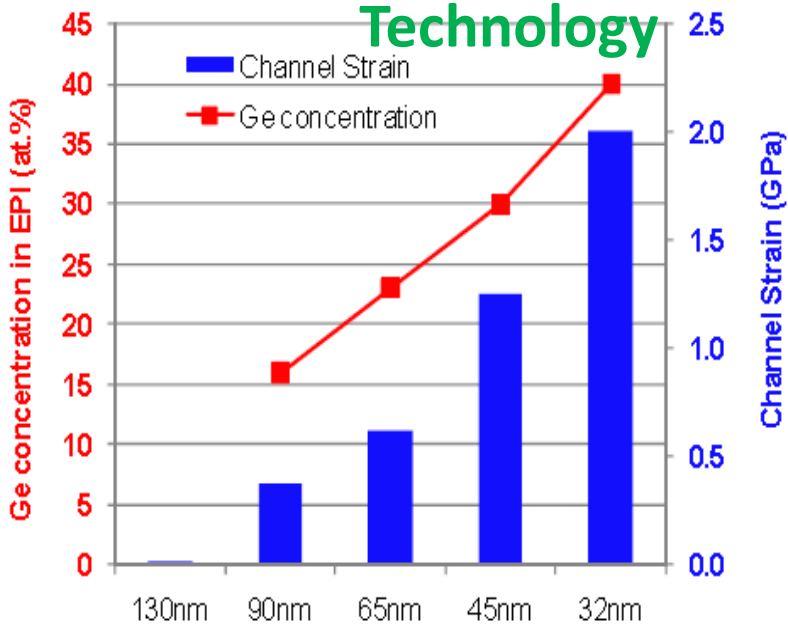
High-k Metal Gate

Tri-Gate

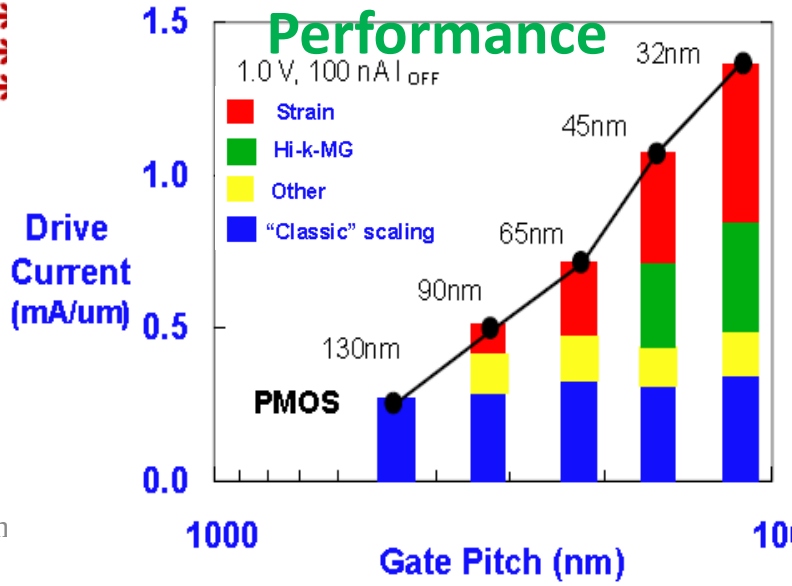
Product



Technology

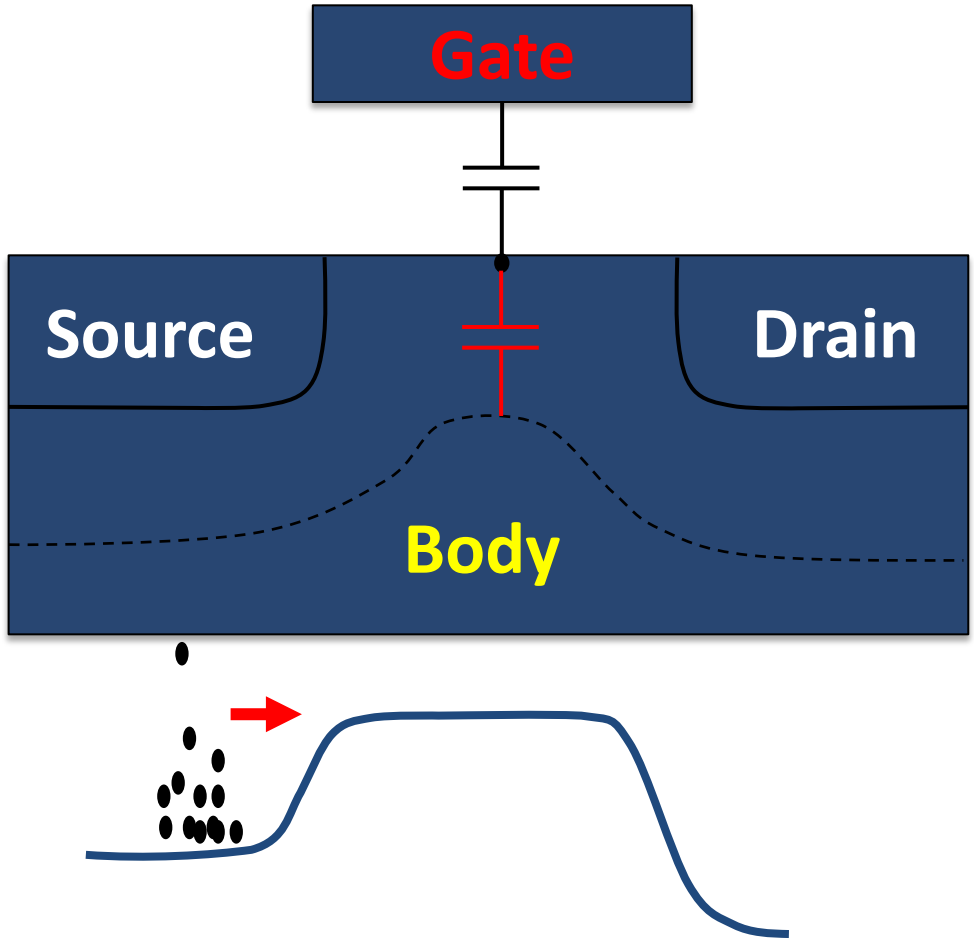


Performance



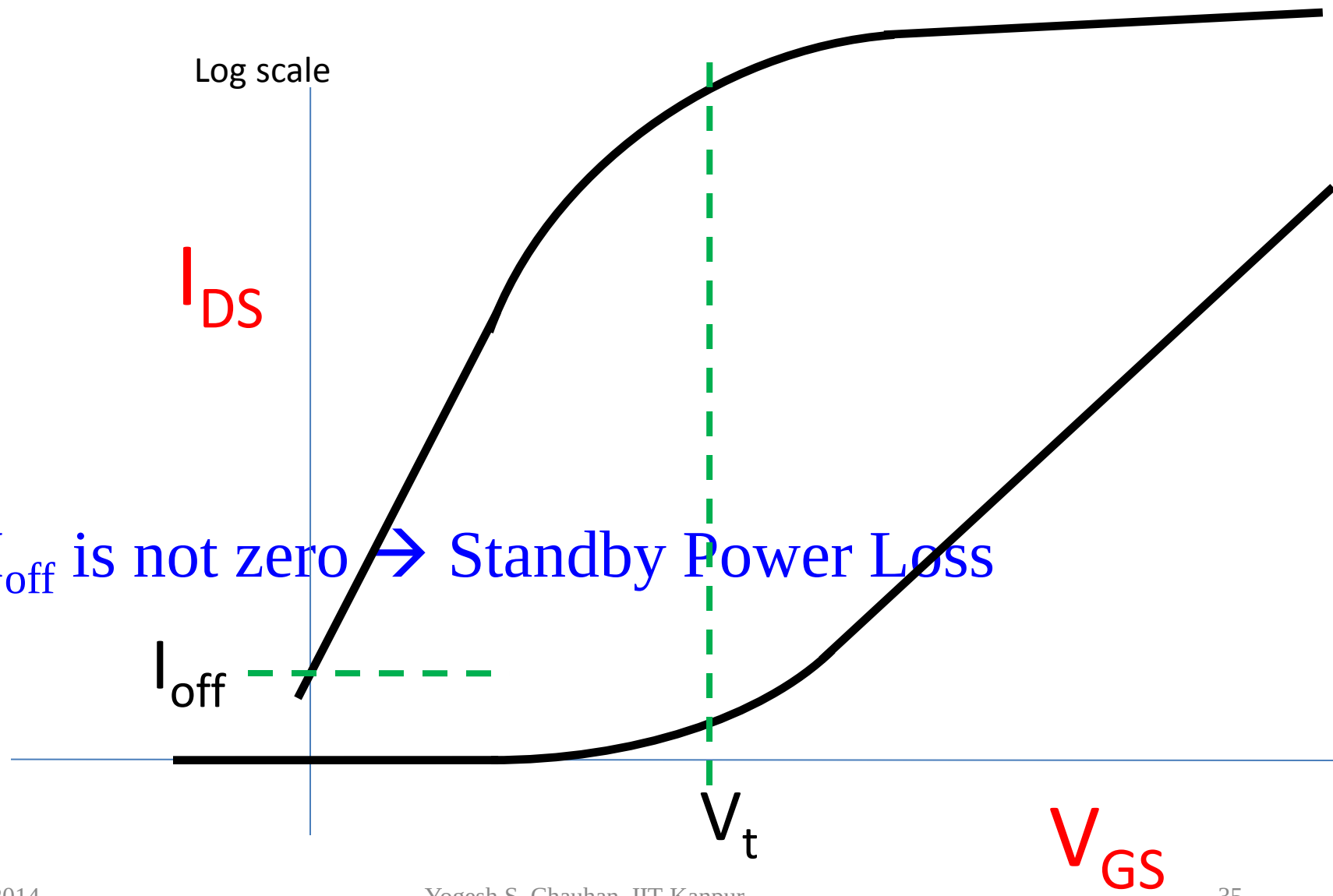
Source : www.intel.com

Thin Depletion Layer - Problem



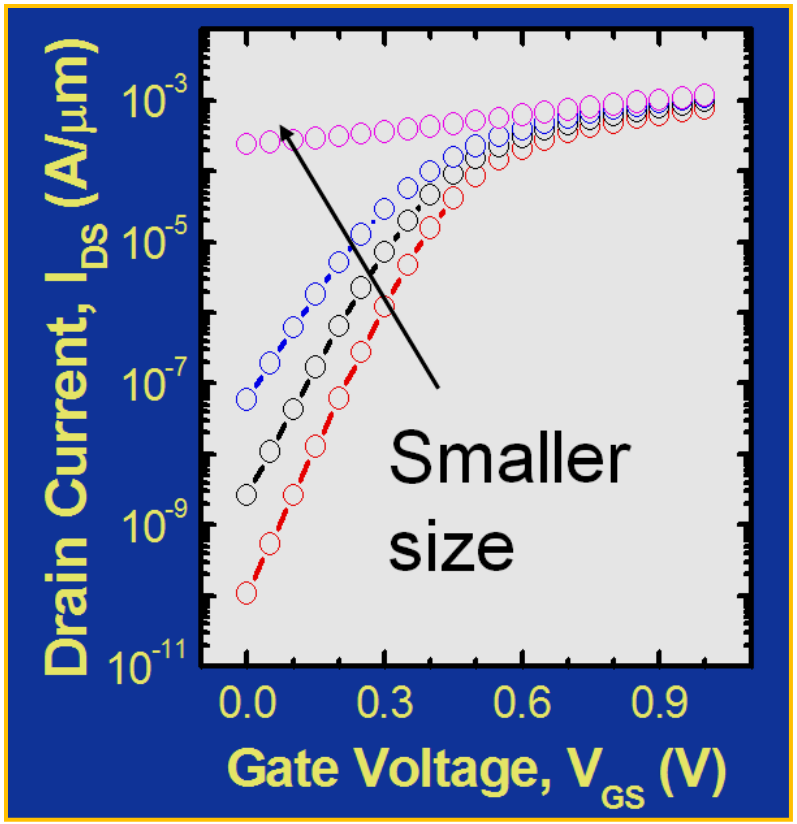
- $Q_G = Q_i + Q_b$
- Charge sharing

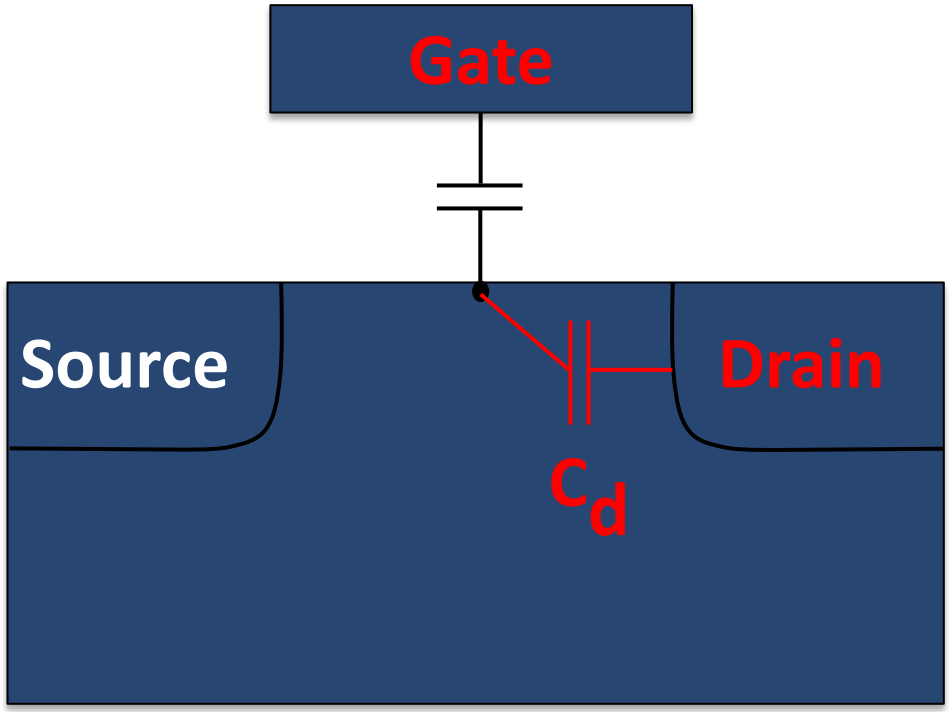
Current in MOSFET



- I_{off} is not zero → Standby Power Loss

Short Channel – Big Problem

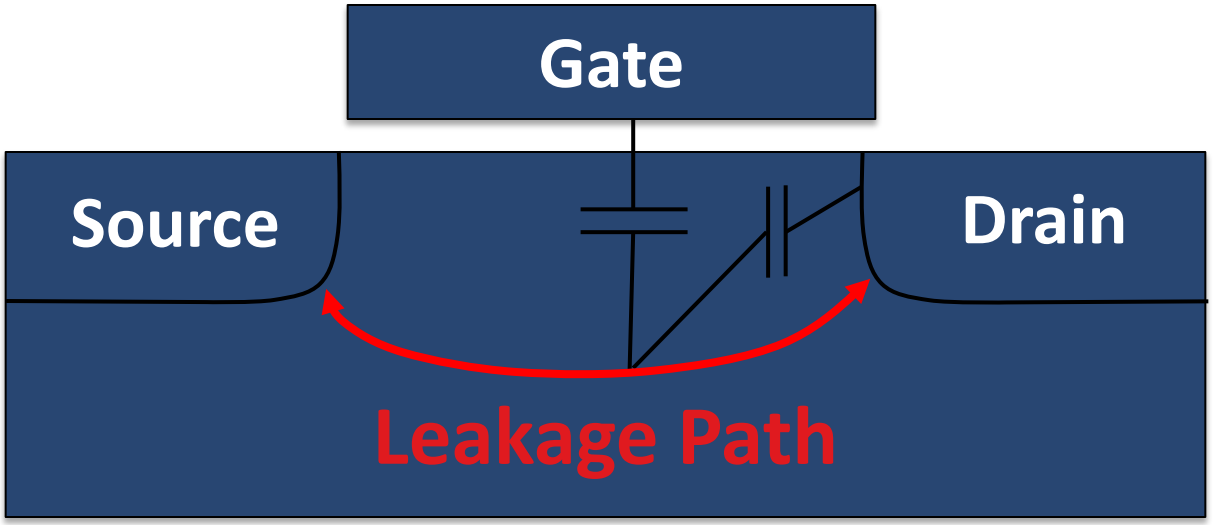




MOSFET becomes "resistor" at small L.

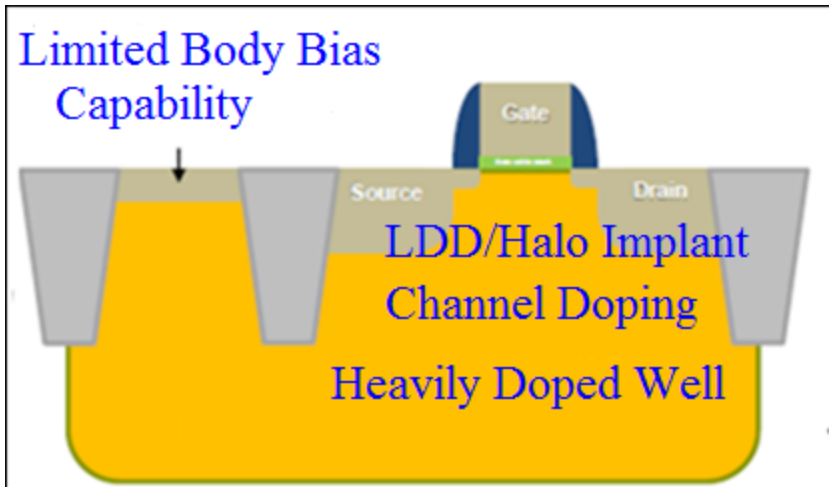
Chenming Hu, "Modern Semiconductor Devices for ICs" 2010, Pearson

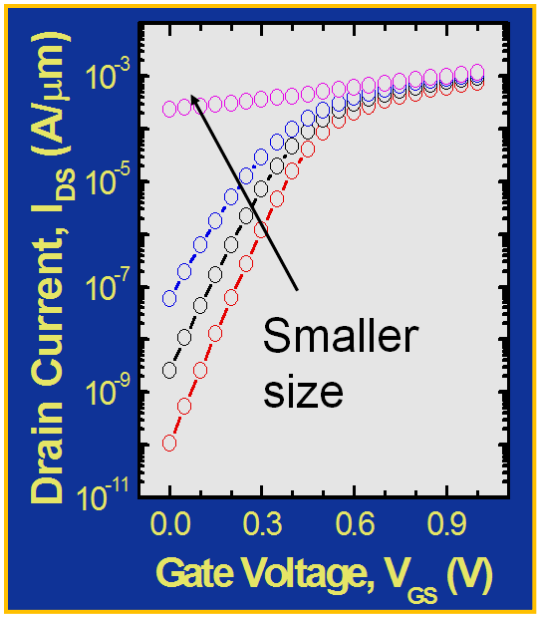
Making Oxide Thin is Not Enough

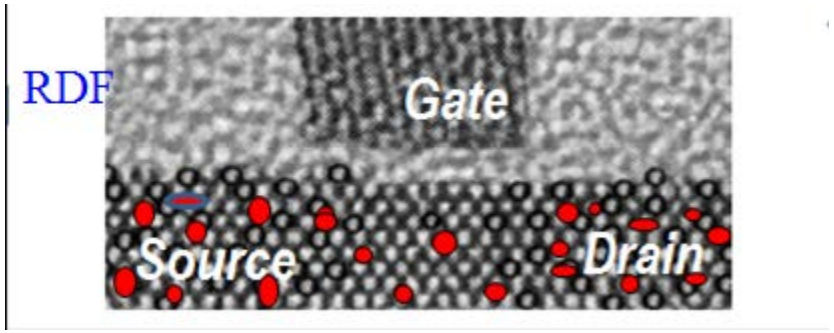


Gate cannot control the leakage current paths that are far from the gate.

Good Old MOSFET has reached its Limits



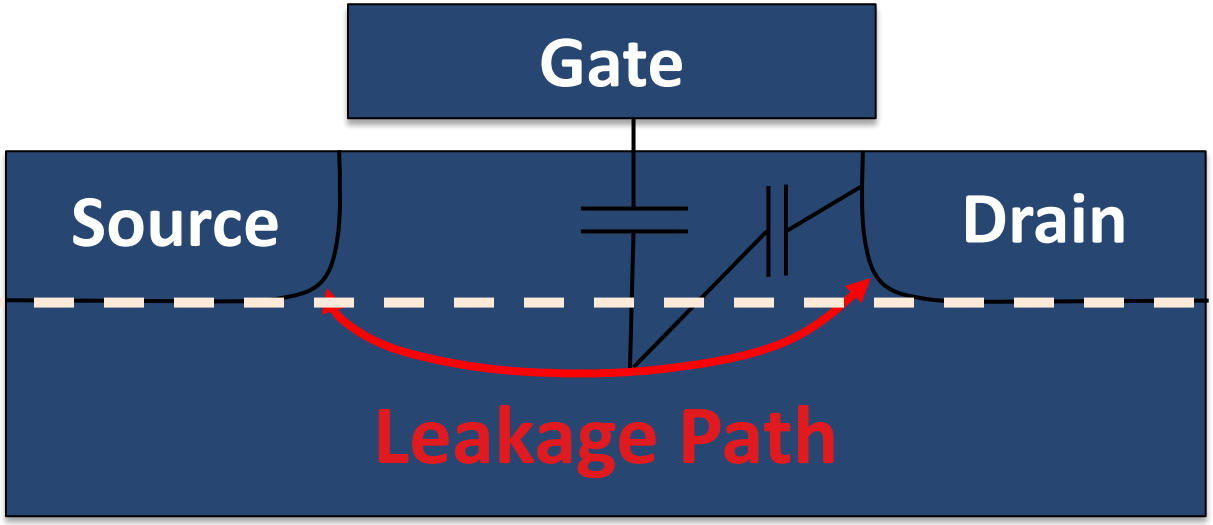




- **Ioff is bad**
- **Size and dopant variations**

High Vdd, Power, Design Cost

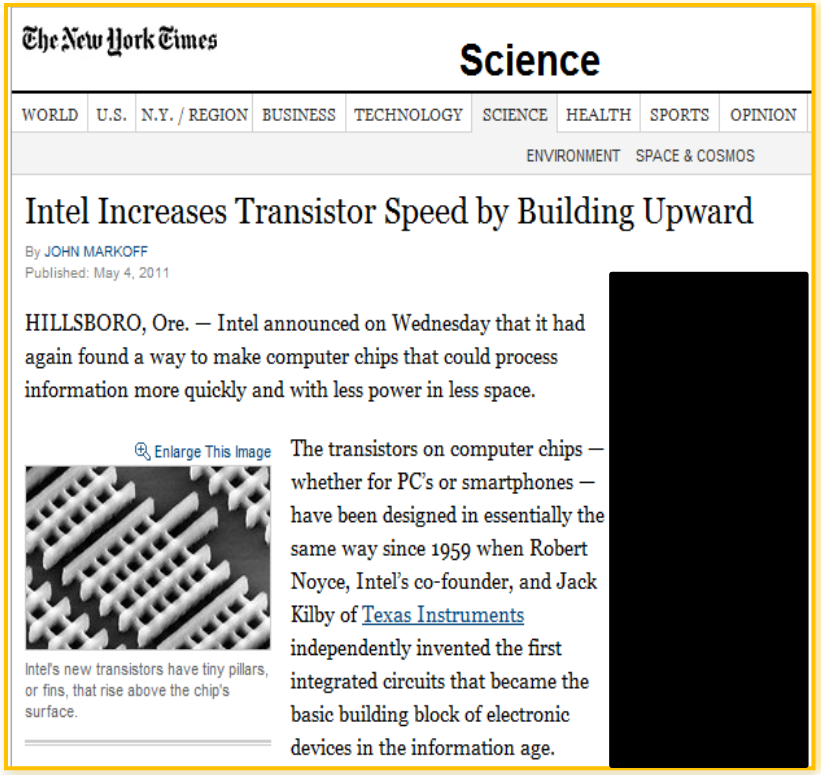
What can we do?



May 4, 2011

The New York Times Front Page

- **Intel will use 3D FinFET at 22nm**
- **Most radical change in decades**
- **There is a competing SOI technology**



The New York Times

Science

WORLD | U.S. | N.Y. / REGION | BUSINESS | TECHNOLOGY | SCIENCE | HEALTH | SPORTS | OPINION

ENVIRONMENT | SPACE & COSMOS

Intel Increases Transistor Speed by Building Upward

By JOHN MARKOFF
Published: May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

Enlarge This Image

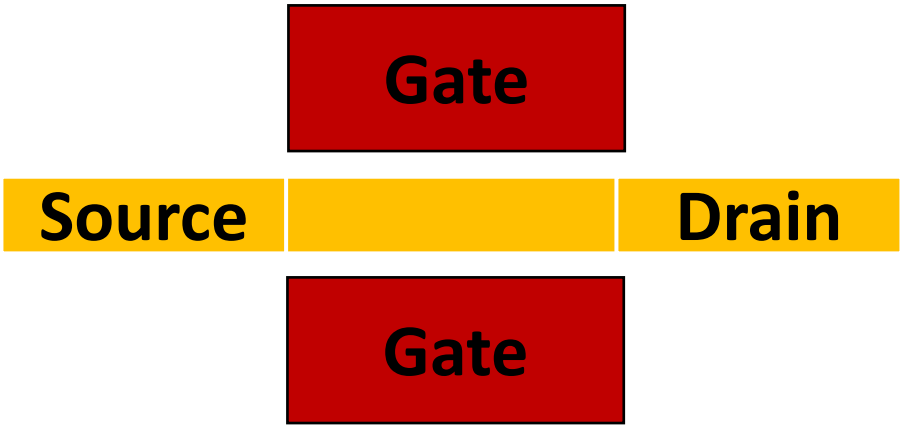
Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

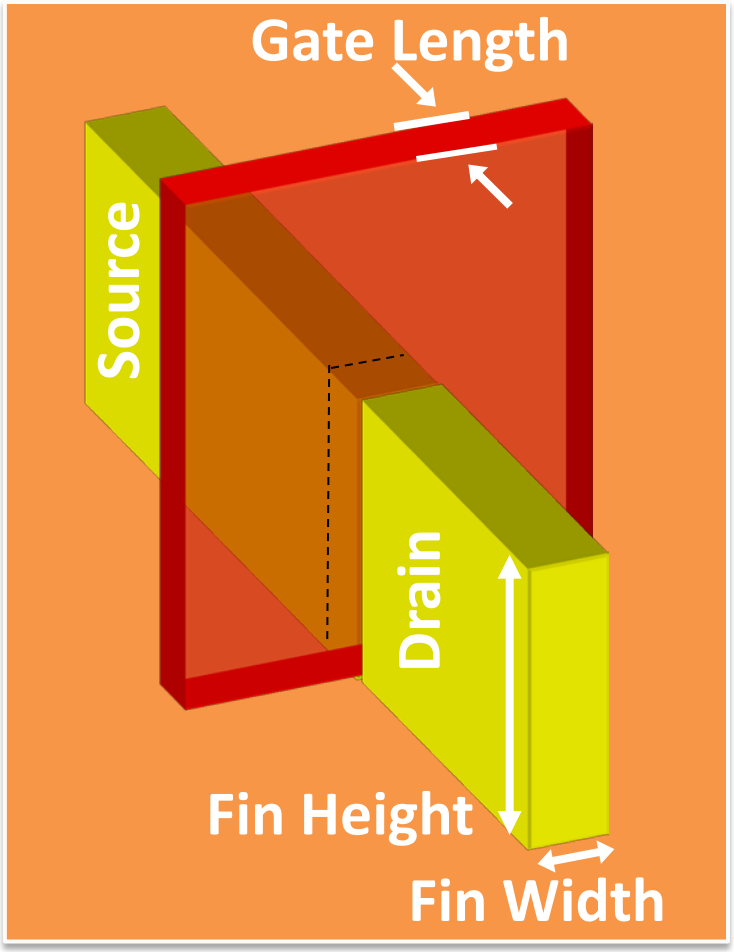
One Way to Eliminate Si Far from Gate

Thin body controlled

By multiple gates.



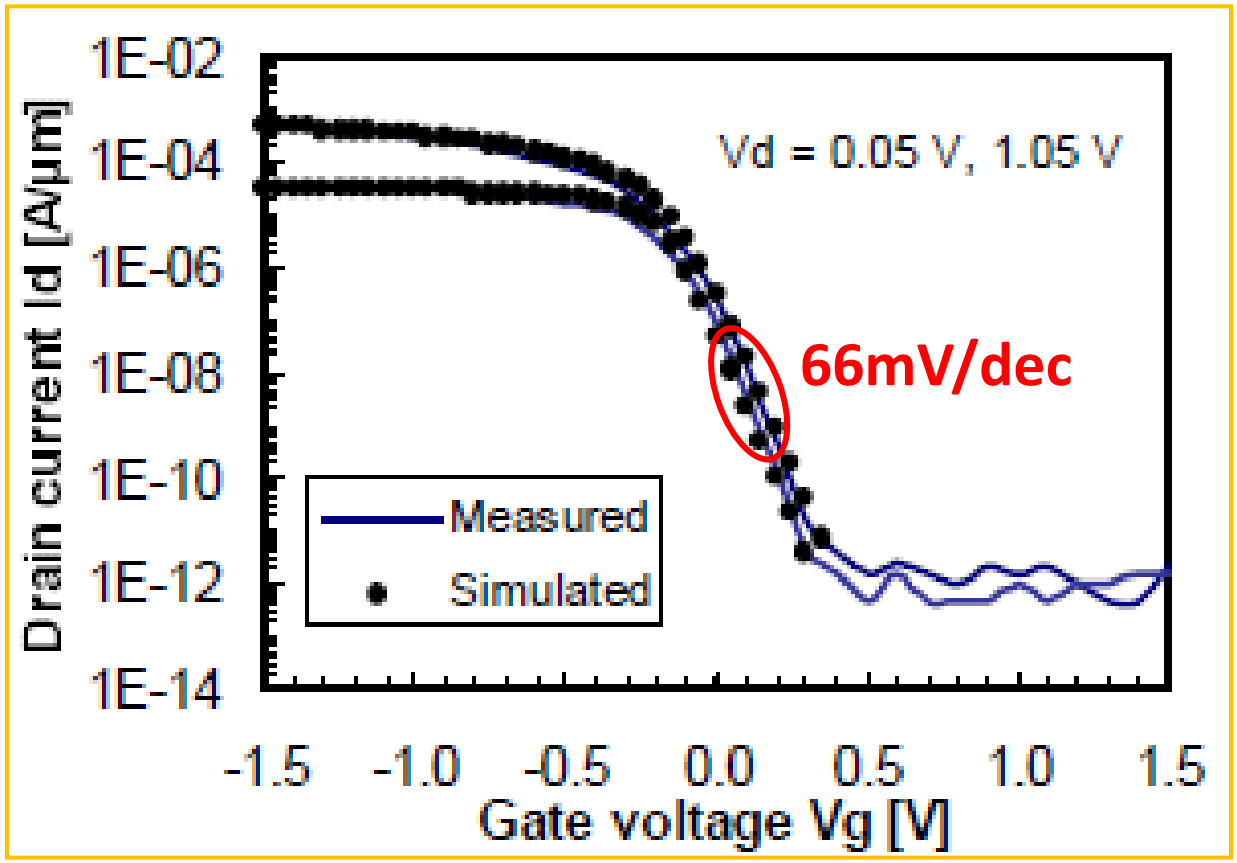
FinFET body is a thin Fin.



N. Lindert et al., DRC paper II.A.6, 2001

40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.



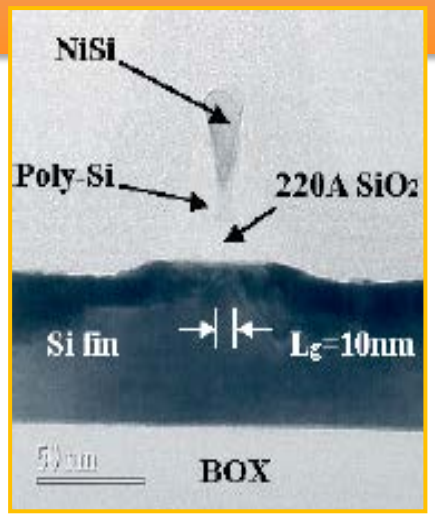
X. Huang et al., IEDM, p. 67, 1999

Introduced New Scaling Rule

Leakage is well suppressed if

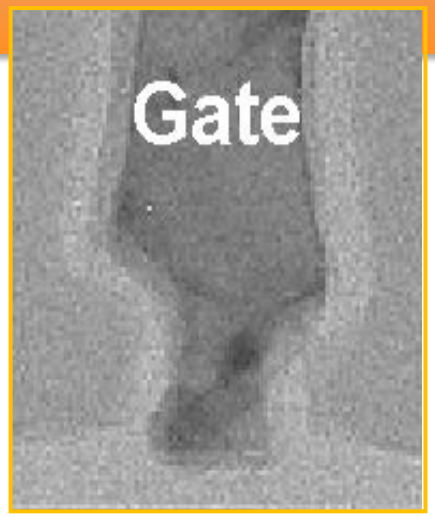
Fin thickness < Lg

10nm Lg AMD 2002 IEDM

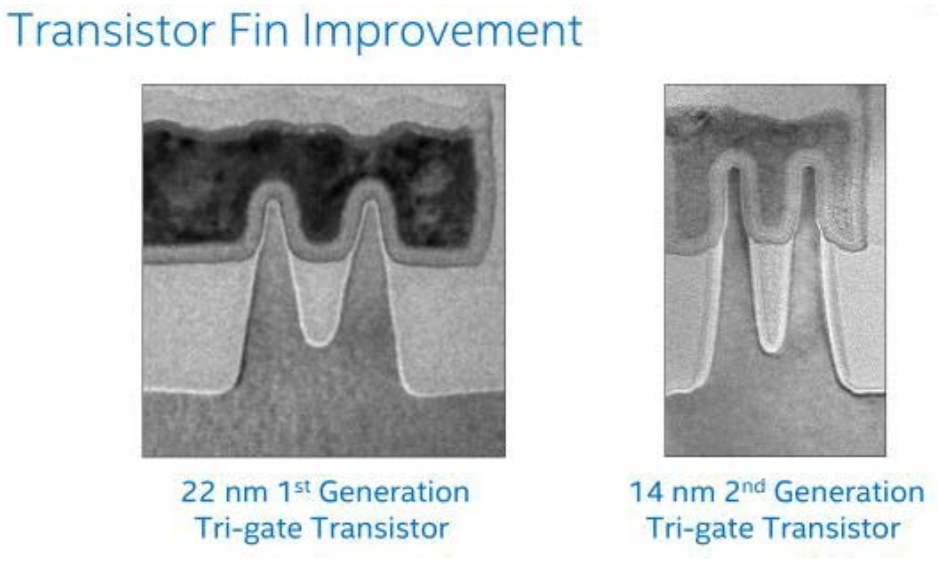


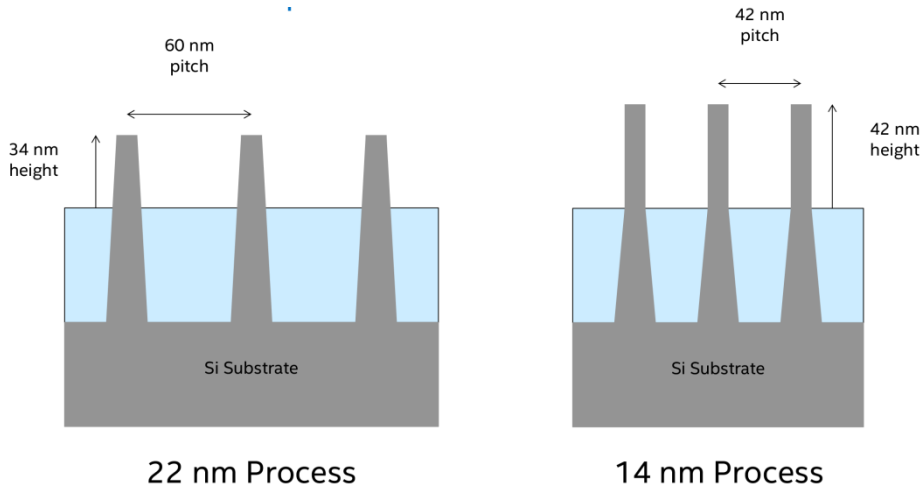
5nm Lg TSMC 2004 VLSI

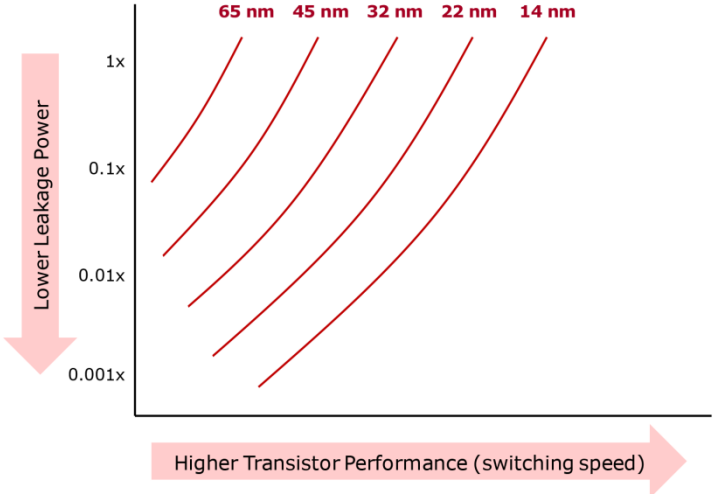
3nm Lg KAIST 2006 VLSI



State-of-the-Art **14nm** FinFET





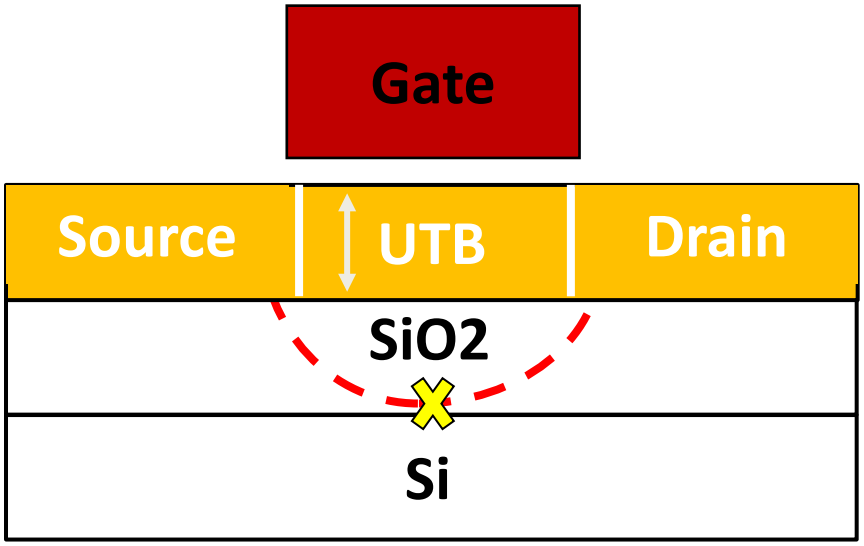


Taller and Thinner Fins for increased drive current and performance

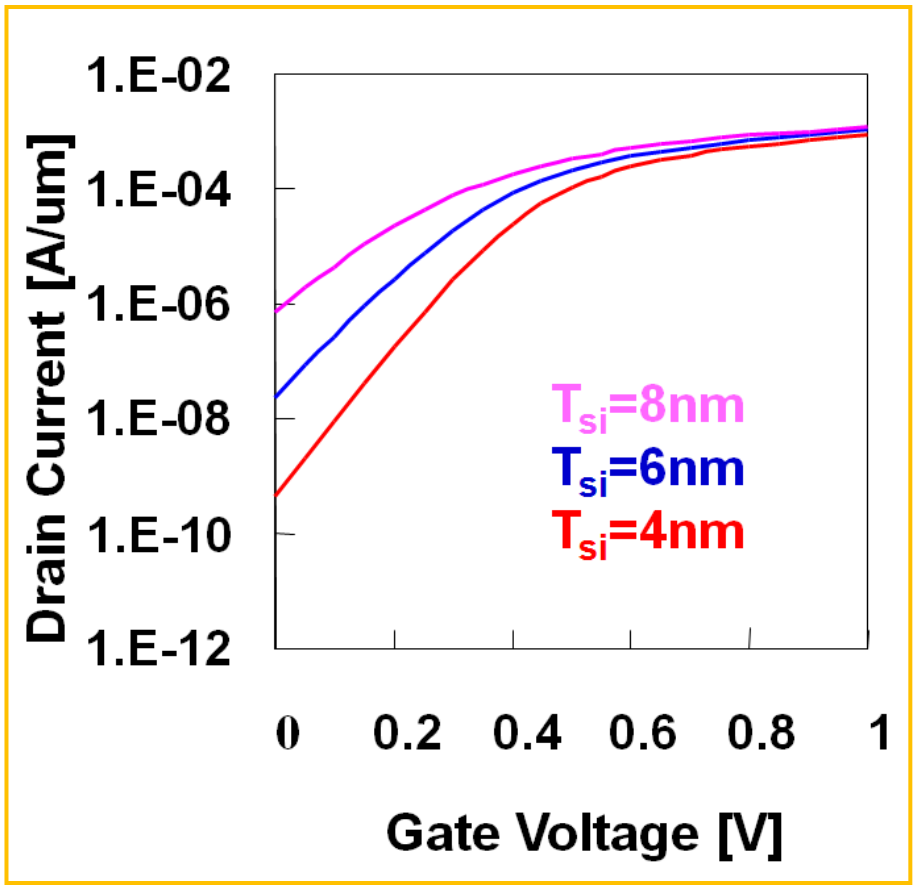
Source: Anandtech

2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI)

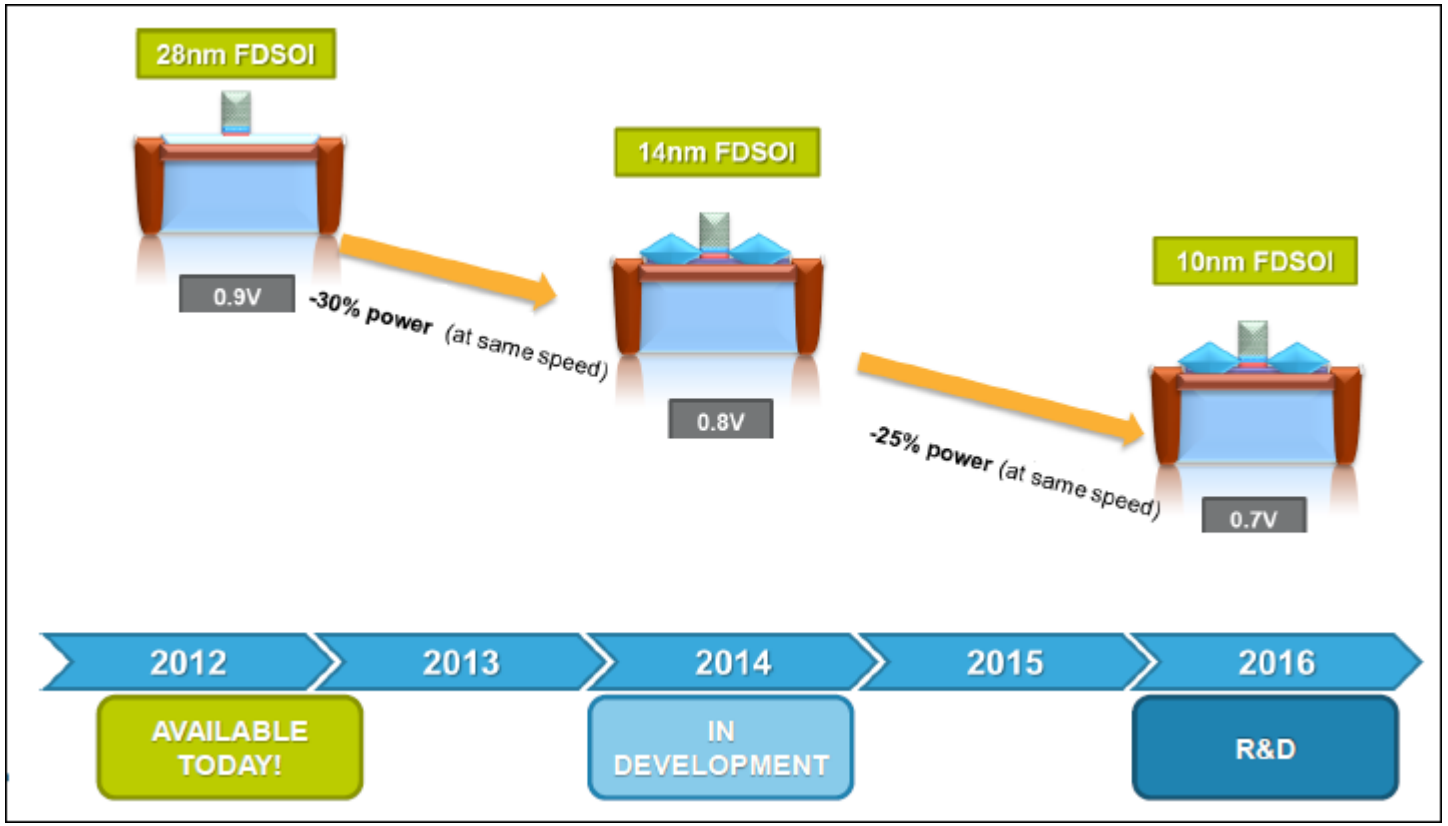


Y-K. Choi, IEEE EDL, p. 254, 2000



FDSOI Roadmap

- From a global cooperation ST-IBM-LETI have enabled an FD-SOI 3-node roadmap.



Design, Automation & Test in Europe Conference & Exhibition (DATE), 2013
http://cmp.imag.fr/events/FDSOI_DATE_2013/FDSOI_DATE_2013.html

Main Differences

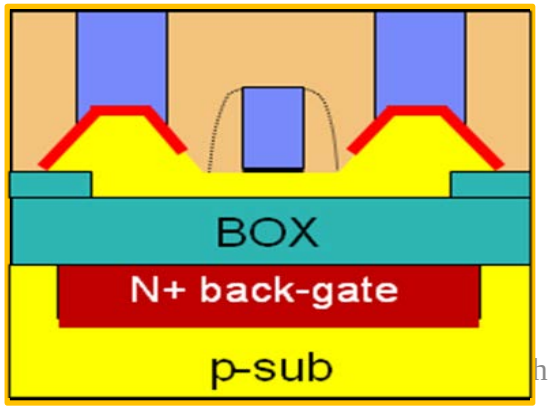
FinFET

- Body thickness <Lg
- Investment by fab
- Has larger Ion

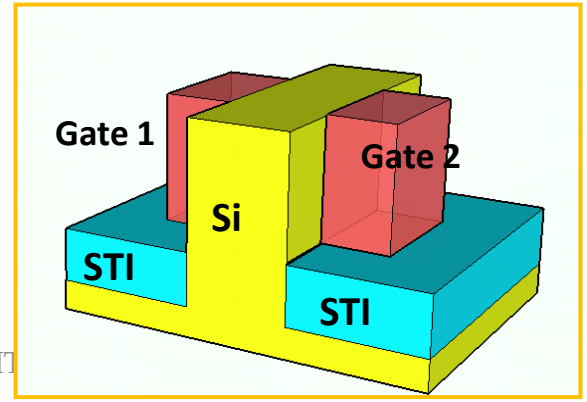
UTB-SOI

- Thickness <1/3Lg
- Investment by SOI suppliers
- Has good back-gate bias option

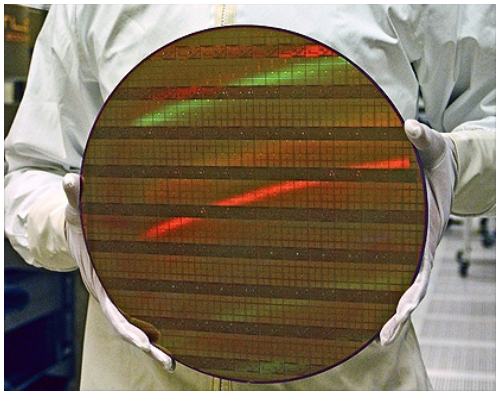
UTB-SOI



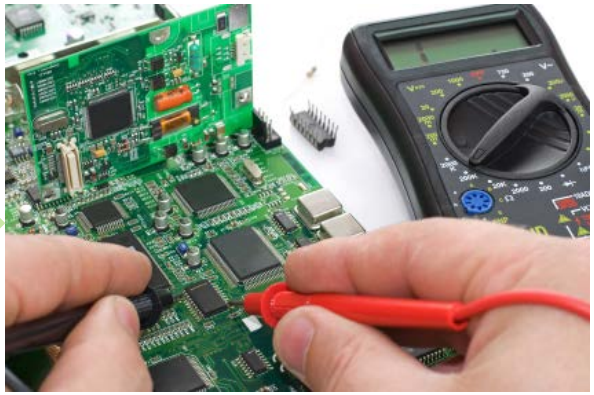
FinFET



Compact Modeling or SPICE Modeling



Medium of information exchange



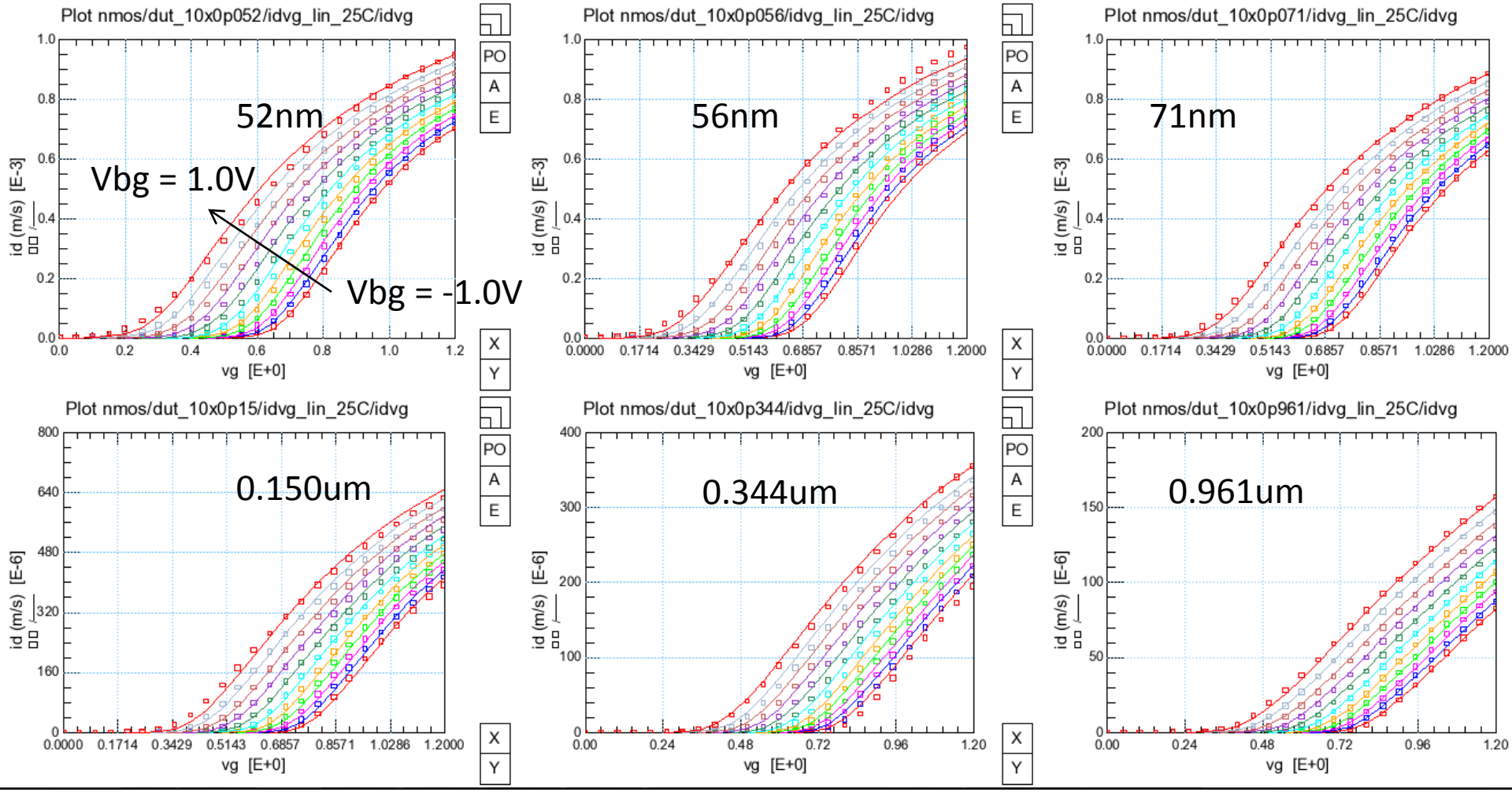
- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~μs*ec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

BSIM-CMG and BSIM-IMG

- **Berkeley Short-channel IGFET Model**
- **First industry standard SPICE model for IC simulation**
- **Used by hundreds of companies for IC design since 1997**
- **BSIM FinFET model became industry standard in March 2012**

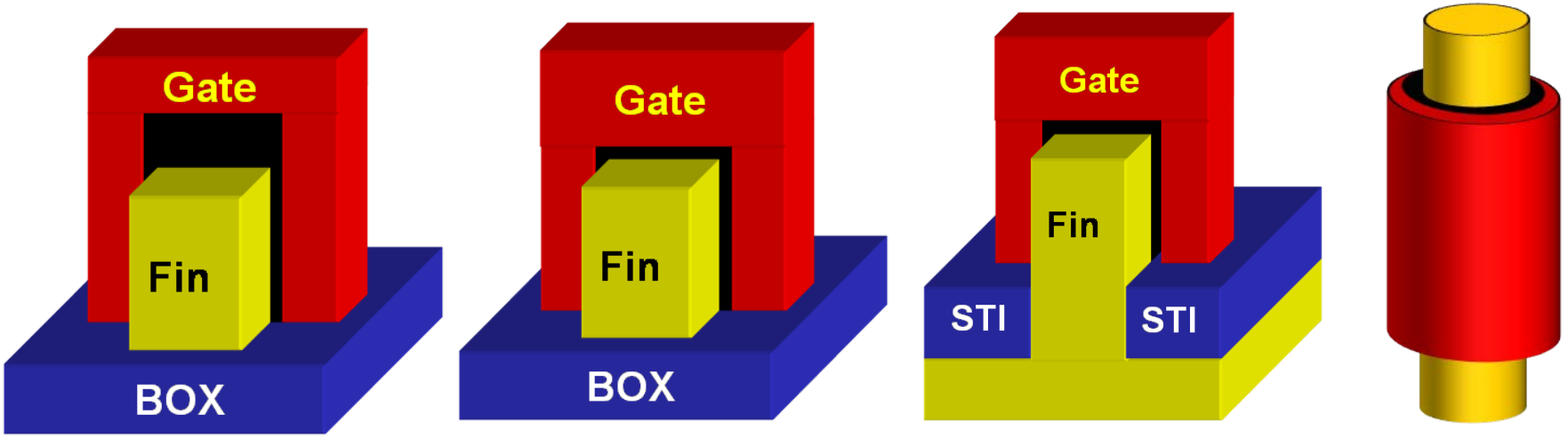
BSIM-IMG: Length scaling@low Vds



UTBBSOI FET, Tsi=12nm

Common-Multi-Gate Modeling

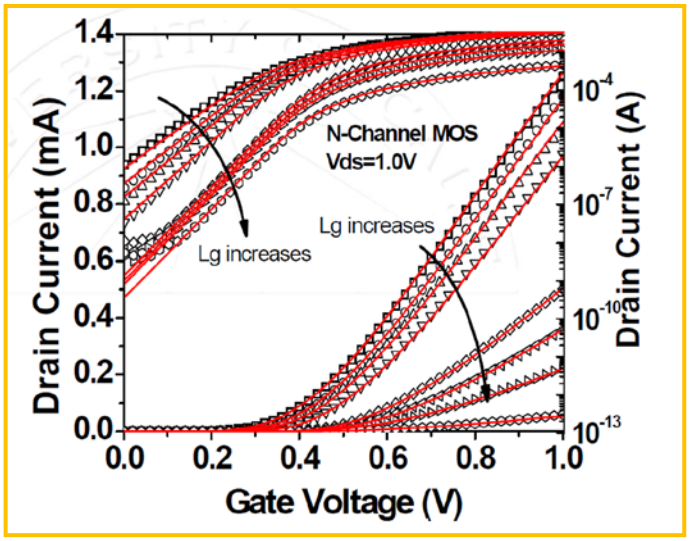
- Common Multi-gate (BSIM-CMG):
  - All gates tied together

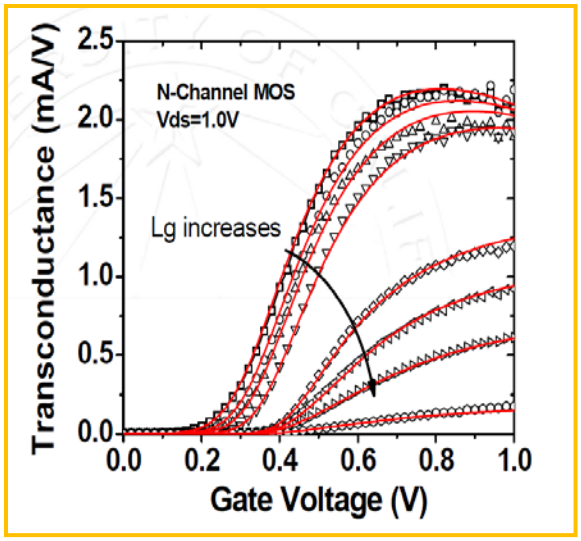


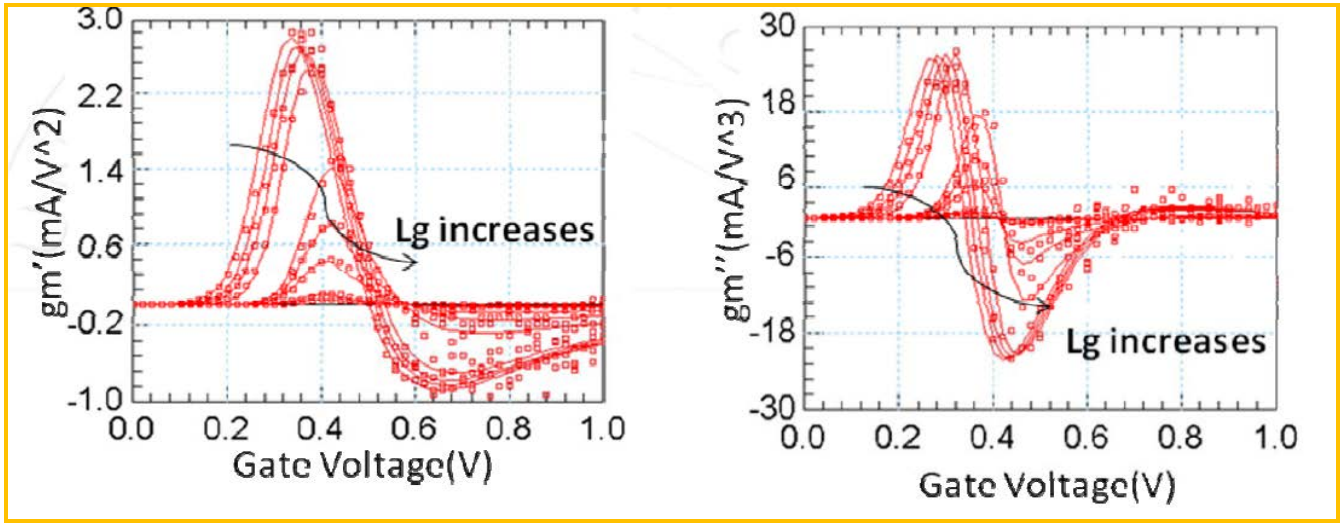
  - Surface-potential-based core I-V and C-V model
  - Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates

BSIM-CMG

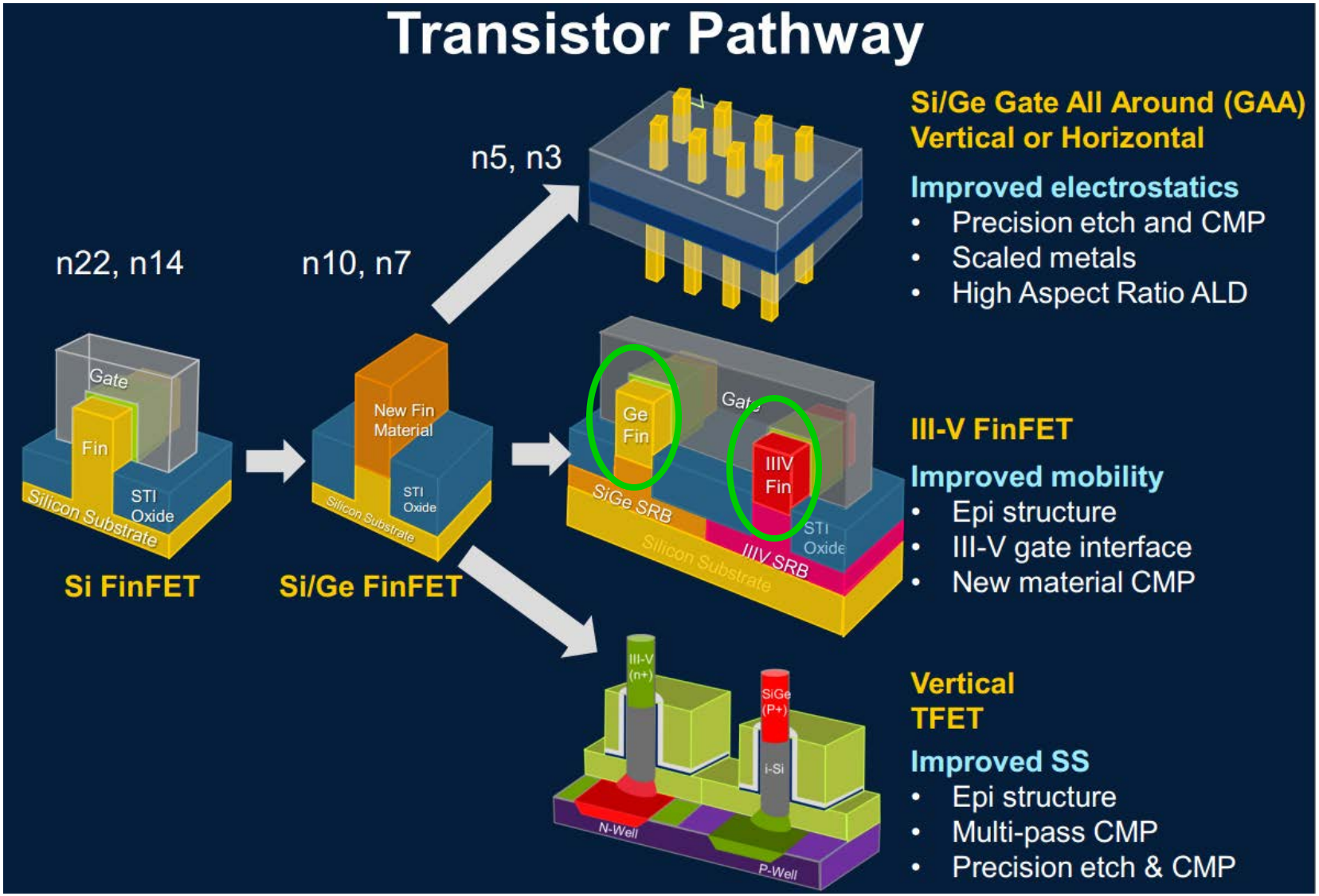
Global fitting with 30nm–10µm FinFETs







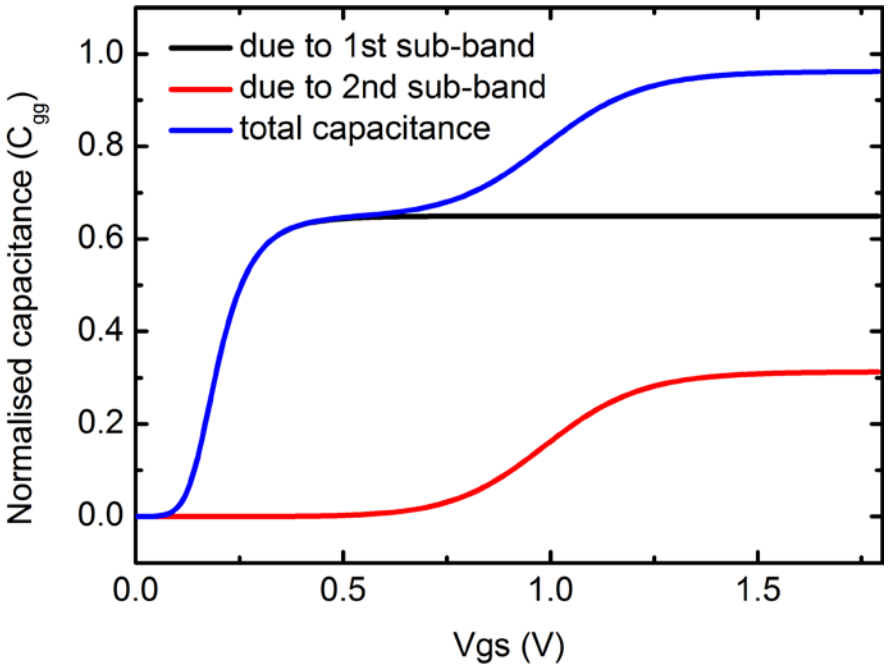
What Next?

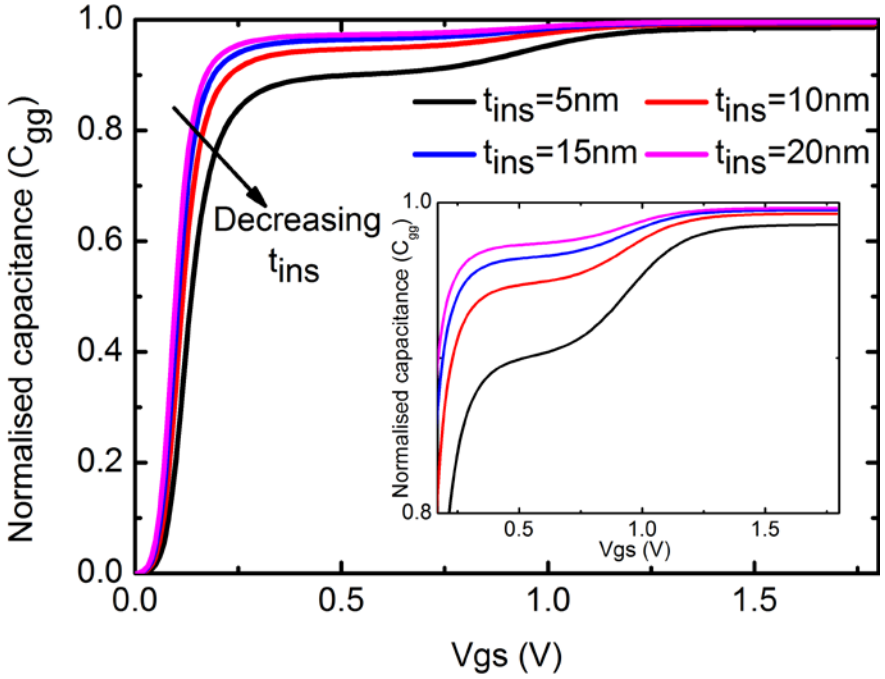


Source: Applied Materials

Modeling of III-V FinFET

Quantum Capacitance Modeling





Avirup Dasgupta et. al., "Analysis and Modeling of Quantum Capacitance in III-V Transistors", submitted in ICEE Bangalore, 2014.

Modeling of III-V FinFET

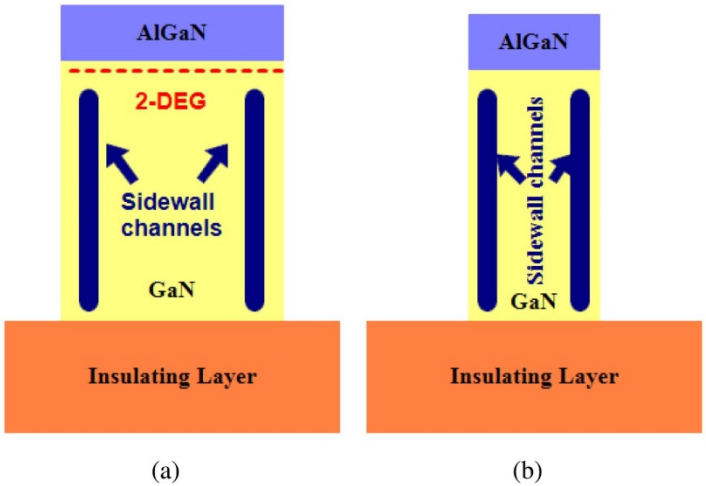


Fig. 1. Schematic showing sidewall channels and 2-DEG channel in AlGaN/GaN based FinFET devices; (a) Wide fin-width device, (b) Narrow fin-width device [12].

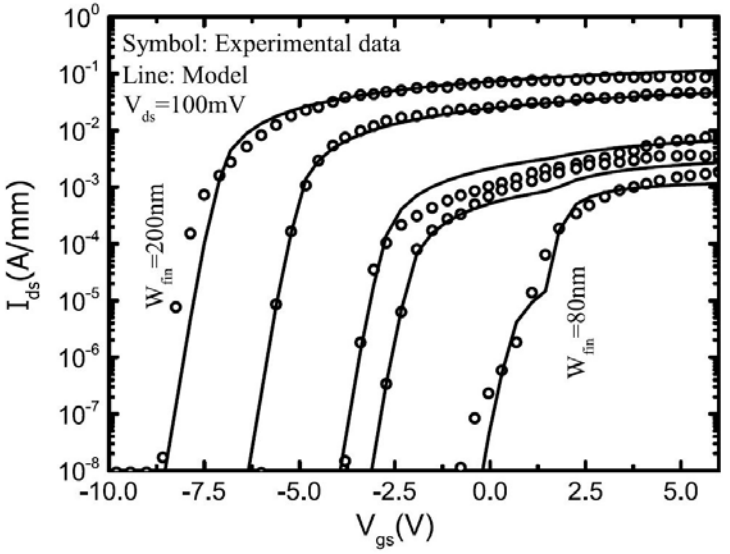
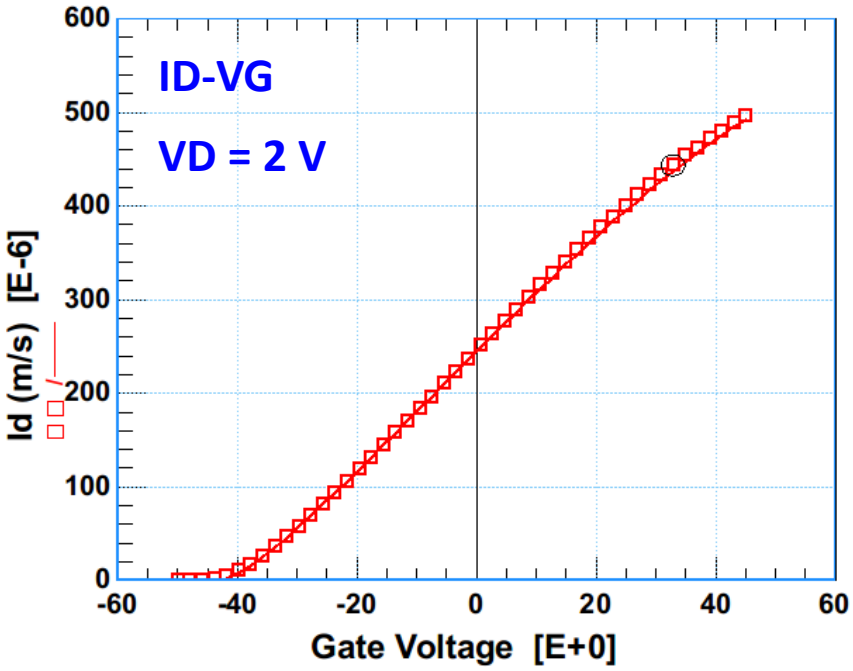
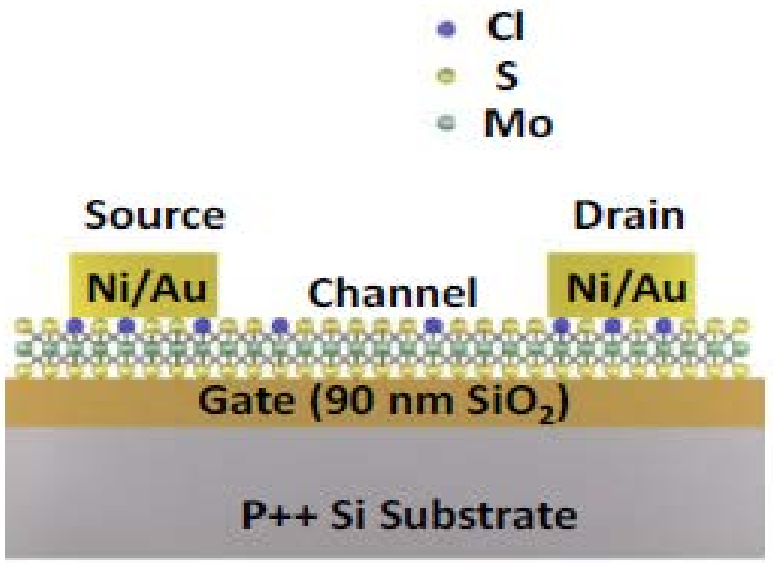


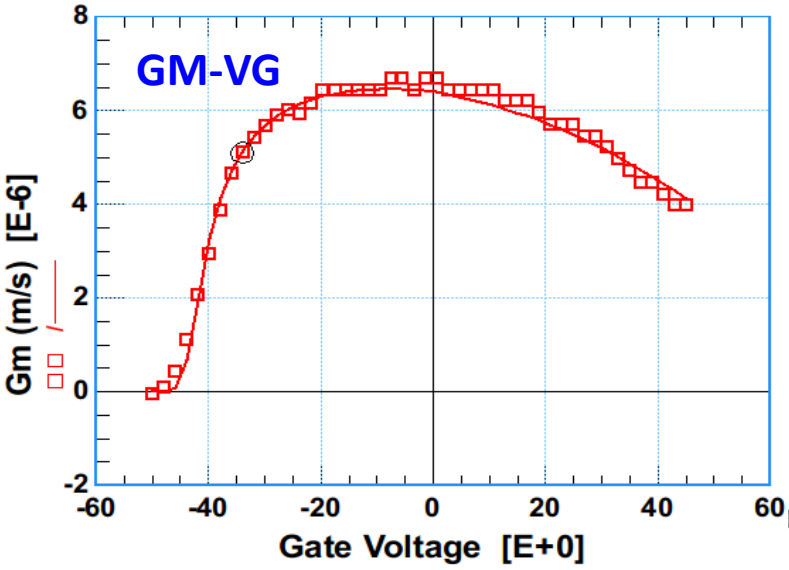
Fig. 3. Subthreshold behaviour of model with experimental data [12], for W_{fin}=80nm, 120nm, 140nm, 180nm and 200nm and $Lg = 1.0\mu m$. Drain current is normalized with total gate width $(W_{fin} + 2H_{fin})$, where $H_{fin} = 120nm$.

- Chandan Yadav et. al., “Modeling of GaN-Based Normally-Off FinFET”, IEEE ELECTRON DEVICE LETTERS, June 2014.

Forward Looking Modeling of 2D Semiconductor FET

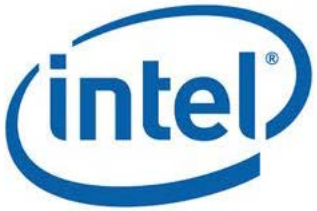






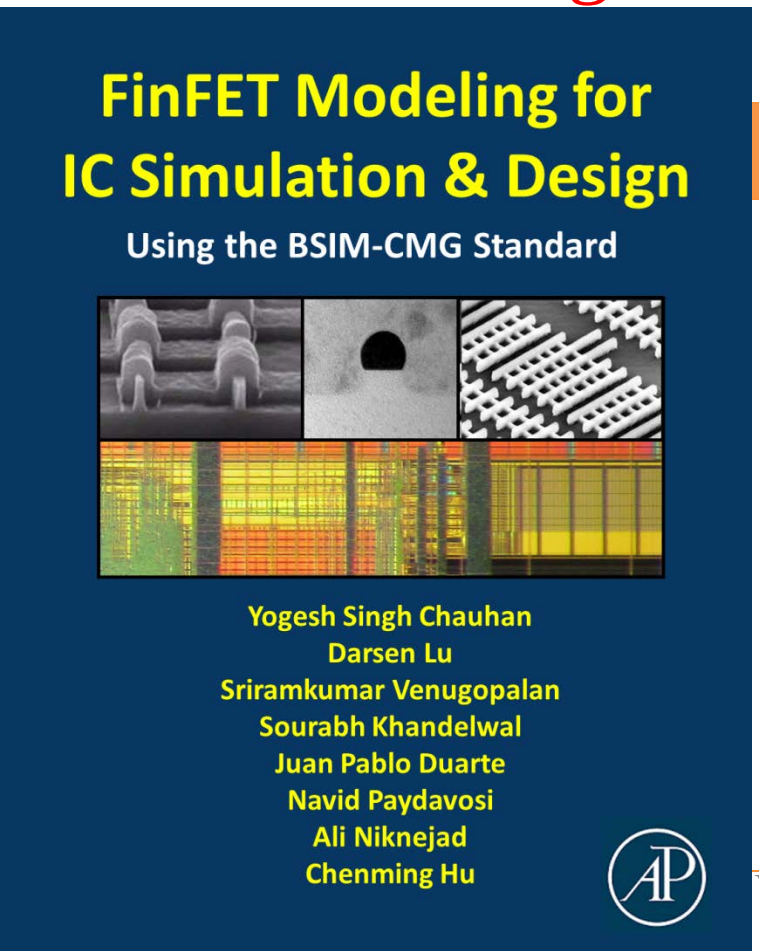
Joint Development & Collaboration

- Working closely with universities/companies on model development and support



Upcoming Book on FinFET Model

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

Summary

- Future is beyond imagination.
- Challenges
  - Technology – Hardware and Software
  - Need Innovation
- Opportunities
  - Entrepreneurship
  - Research
  - Jobs (private/public)
- Knowledge economy

Are you ready?

Present

Future