High Performance Transistors: Present & Future trends

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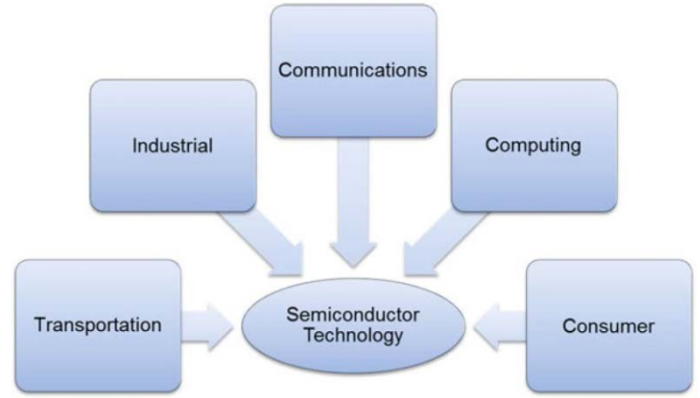
Outline

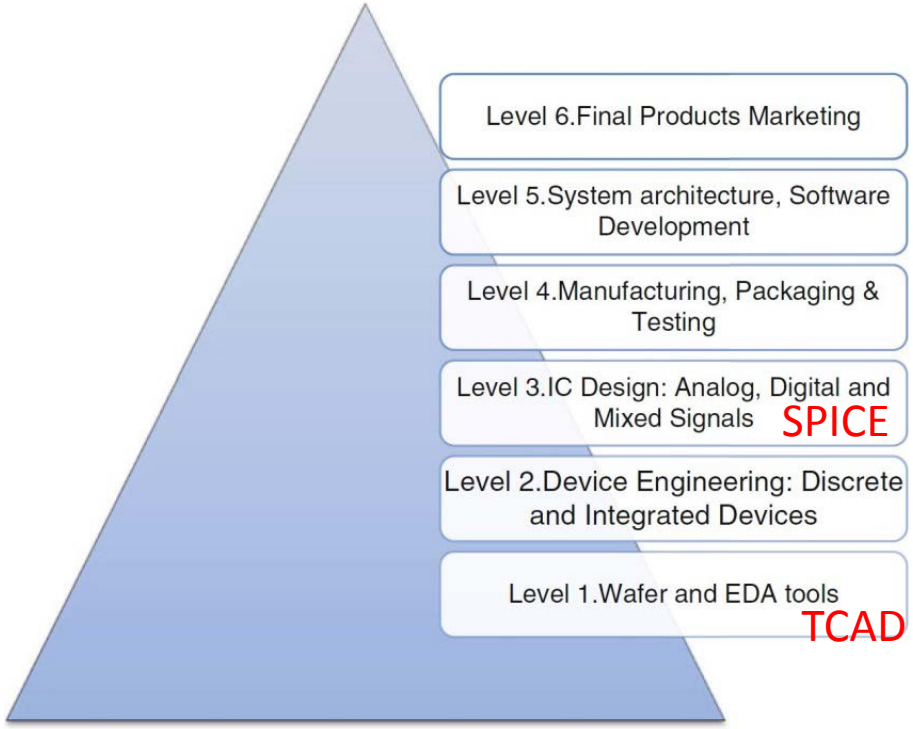
- Semiconductor industry
- What is semiconductor
  - MOSFET and Scaling
  - Multigate Transistors
    - FinFET
    - Thin-Body Transistor
- Compact Modeling of FinFET and UTB FET
- What next?

Semiconductor Industry

- One of the key driving force in today's global economy.
- >$300 billion industry.



.1 Semiconductor technology and some of its applications



Semiconductor industry – pyramid structure

Integrated Device Manufacturers (IDMs)	• Integrated Device Manufacturers (IDMs) have their own fabs to fully or partially support their product manufacturing.
Fabless Companies	• Fabless companies have no manufacturing capabilities, and have to outsource all the manufacturing activities from foundries.
Pure-players (Foundries)	• Pure-players (foundries) have no intention to design their own ICs, even though they may also design some simple IP blocks, and ESD devices for I/O.

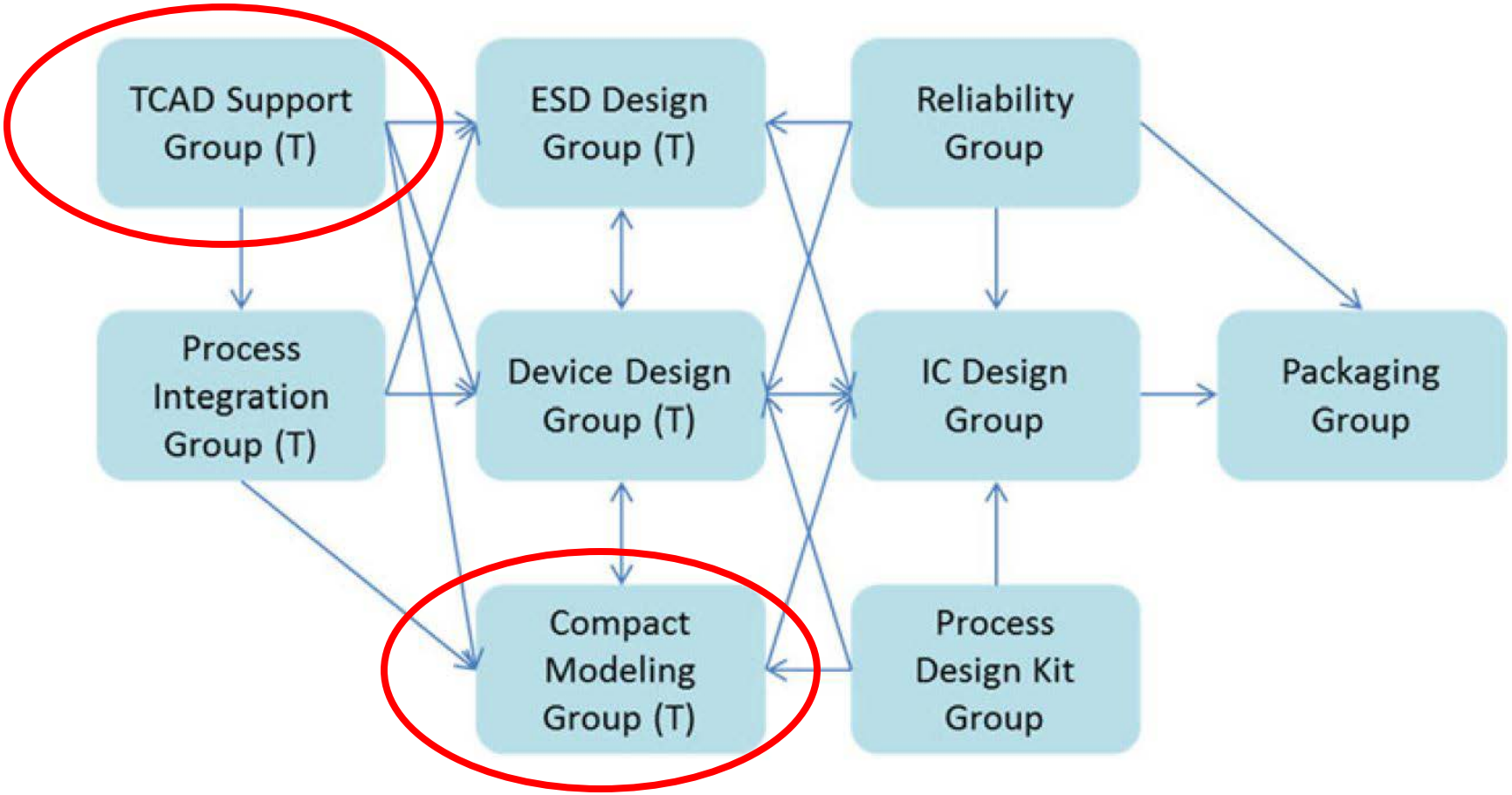
Types of semiconductor companies

Source: S. Li and Y. Fu, 3D TCAD Simulation for Semiconductor Processes, Devices and Optoelectronics, Springer

Global semiconductor companies ranking (2013) – dynamic industry!

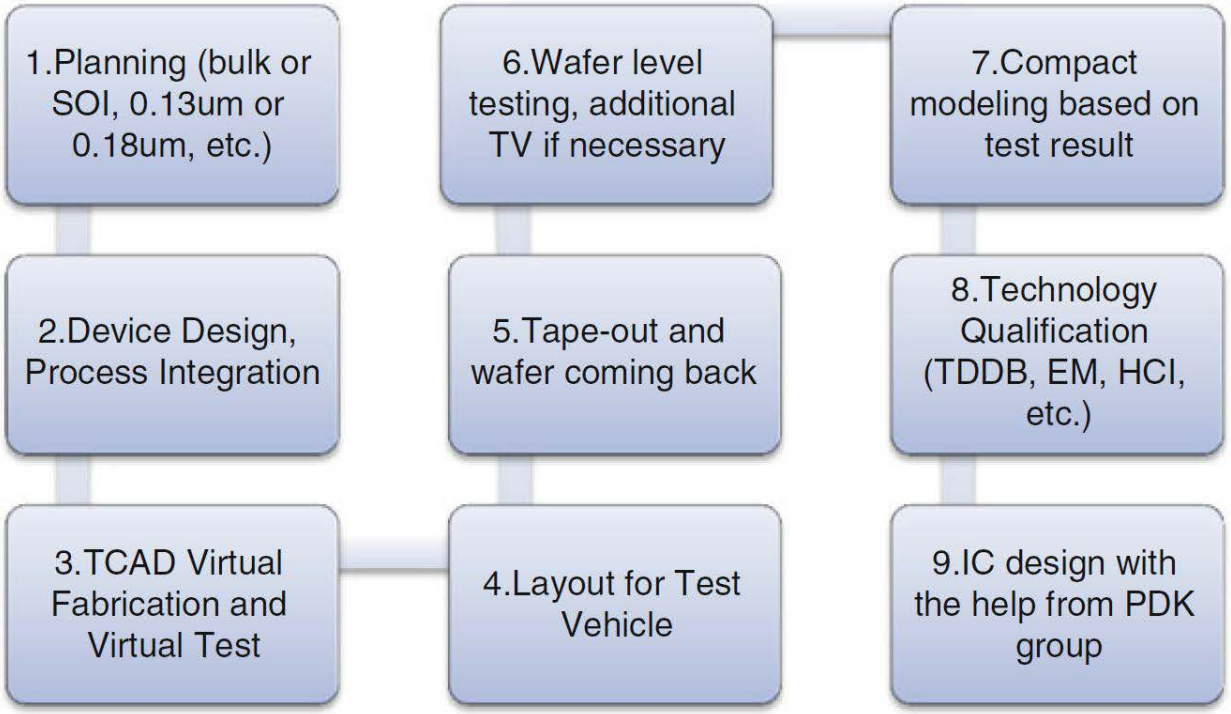
Rank	Company	Headquarters	Type	Revenue
1	Intel	U.S.	IDM	~$48B
2	Samsung	South Korea	IDM	~$33B
3	TSMC	Taiwan	Foundry	~$19B
4	Qualcomm	U.S.	Fabless	~$17B
5	SK Hynix	South Korea	IDM	~$13B
6	Toshiba	Japan	IDM	~$12B
7	TI	U.S.	IDM	~$11B
8	Micron	U.S.	IDM	~$10B
9	ST	Europe	IDM	~$8B
10	Broadcom	U.S.	Fabless	~$8B
11	Renesas	Japan	IDM	~$8B
12	Infineon	Europe	IDM	~$5B
13	AMD	U.S.	Fabless	~$5B

Device engineering groups in a typical IDM



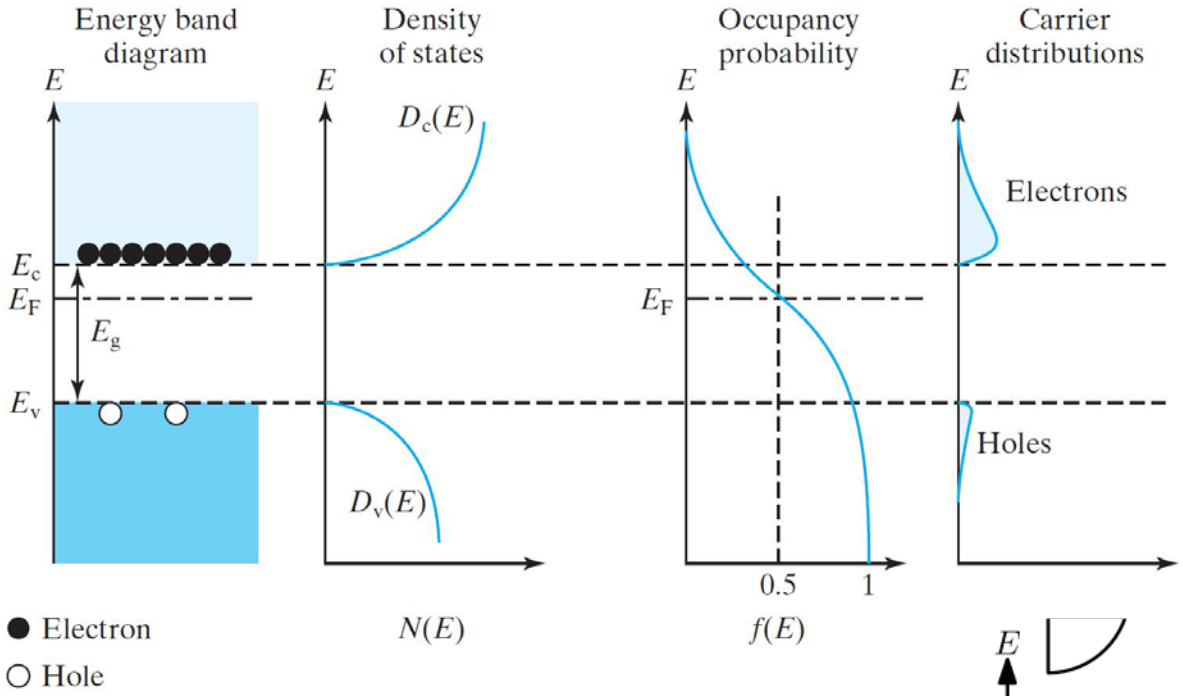
T-TCAD users

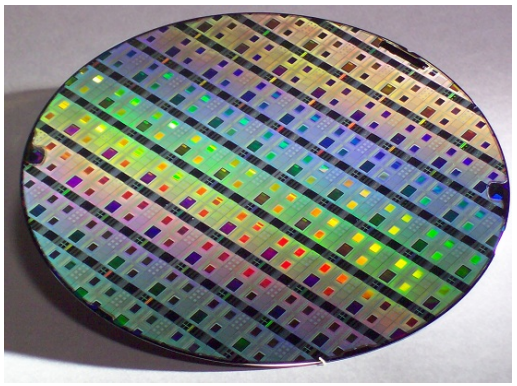
Process flow of analog and power technology development

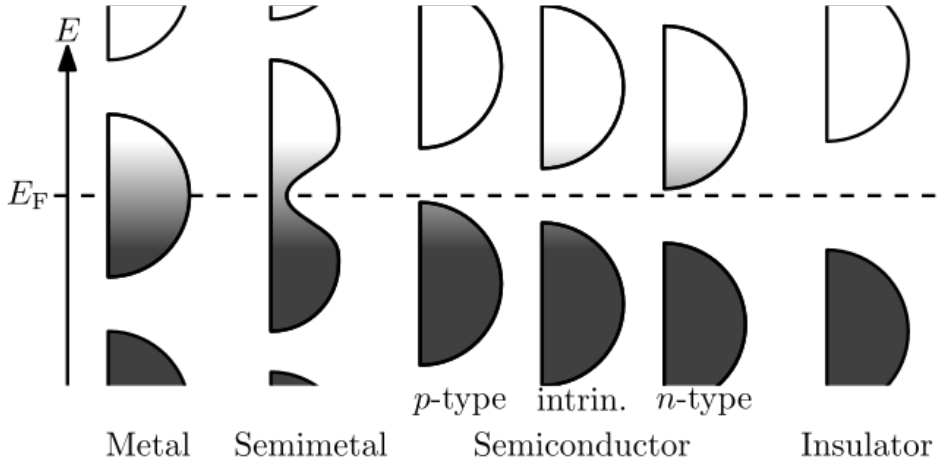


- Results from previous technologies and other measurements can serve as a guideline.
- Engineers should foresee the future need (2–5 years), to make sure the new technology is neither too advanced (costly!) nor too conservative (obsolete even before release!).
- Keep applications in mind.
- **The choice of technology node is an important but risky task.**

What is semiconductor?

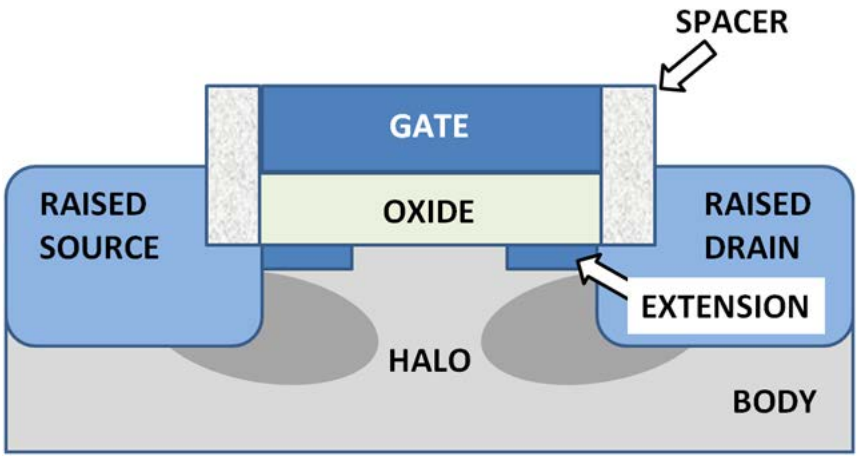


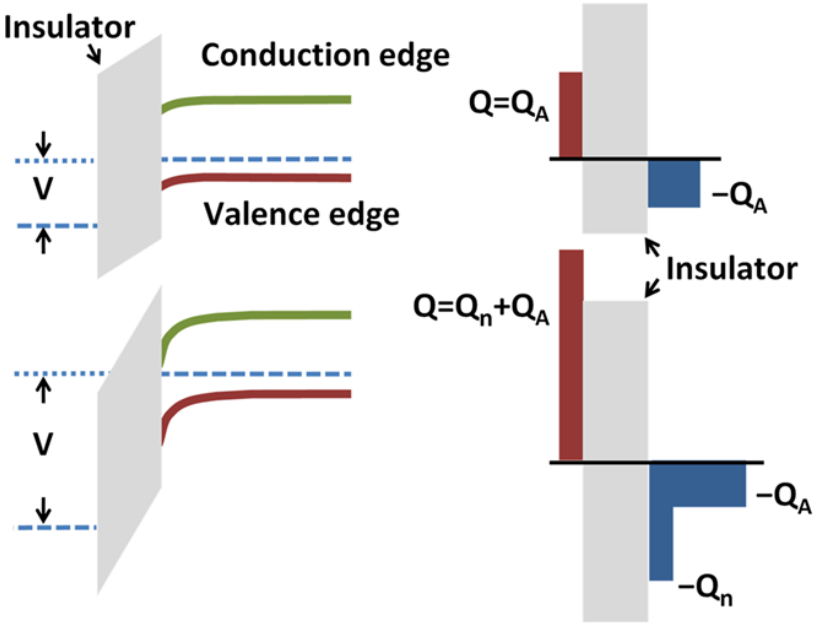




Source: Anandtech

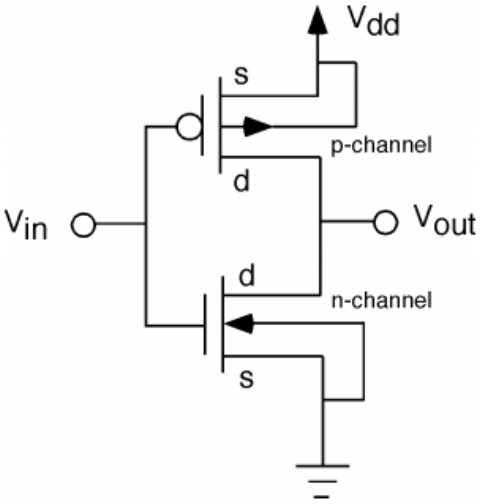
Semiconductor Devices – MOSFET



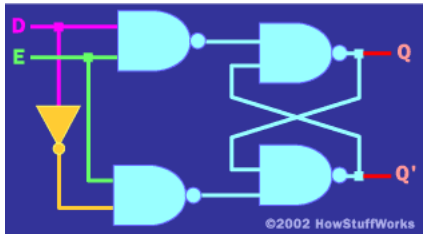


Devices to circuits

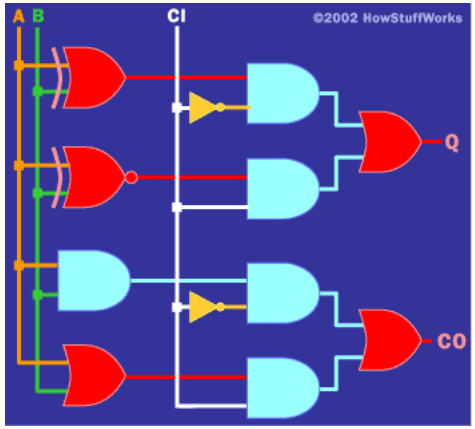
NOT gate



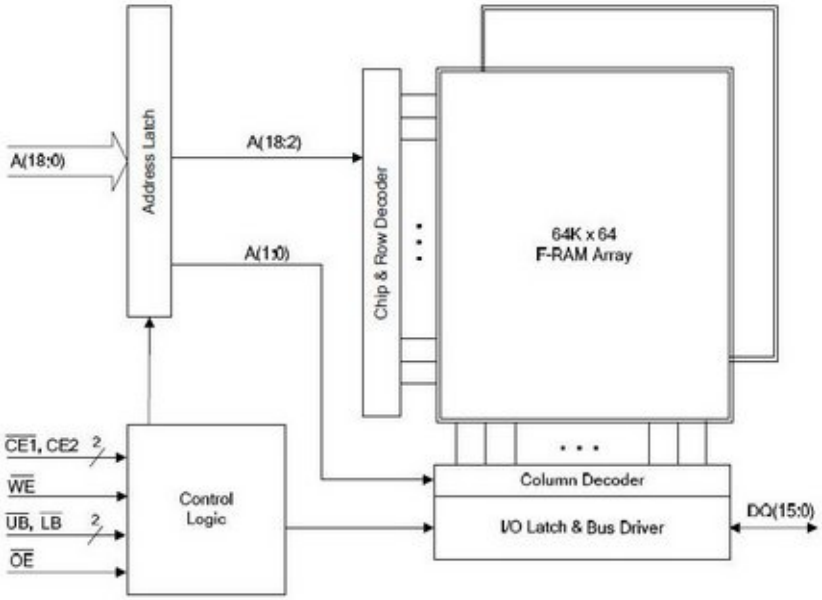
Flip-flop



Full Adder

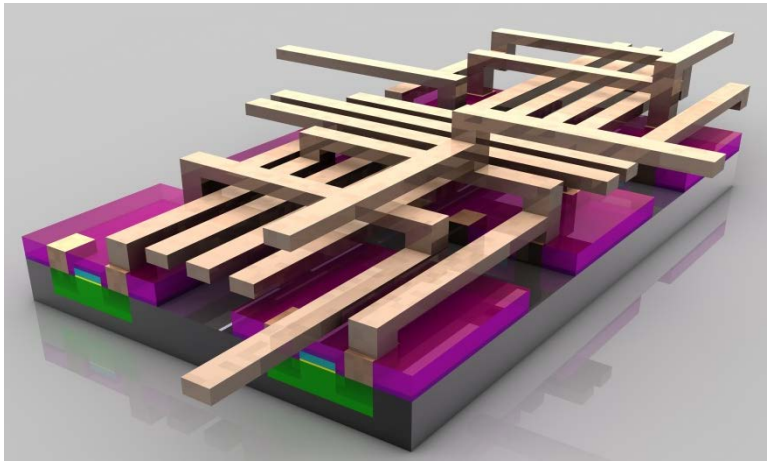


Memory

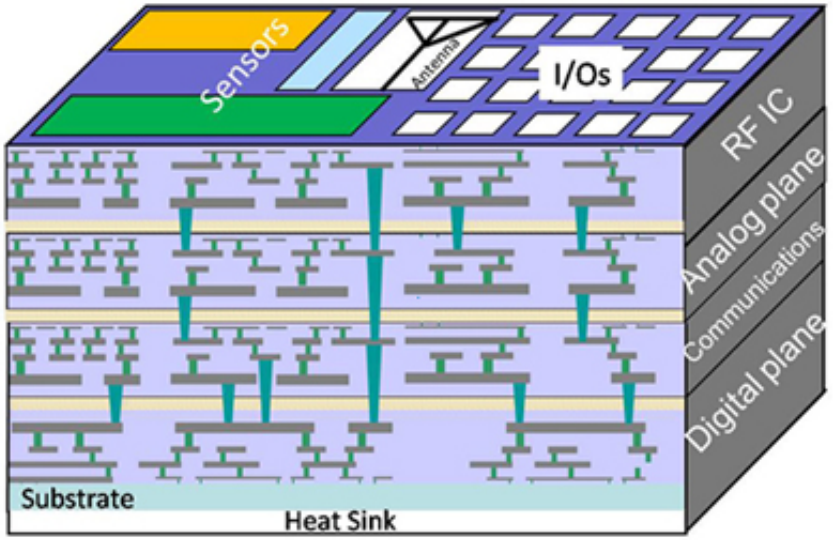


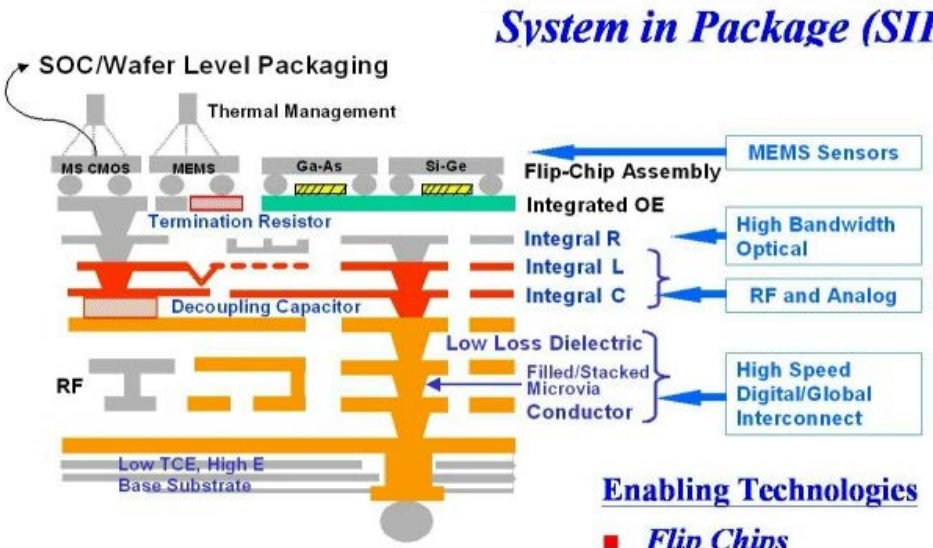
Today's ICs

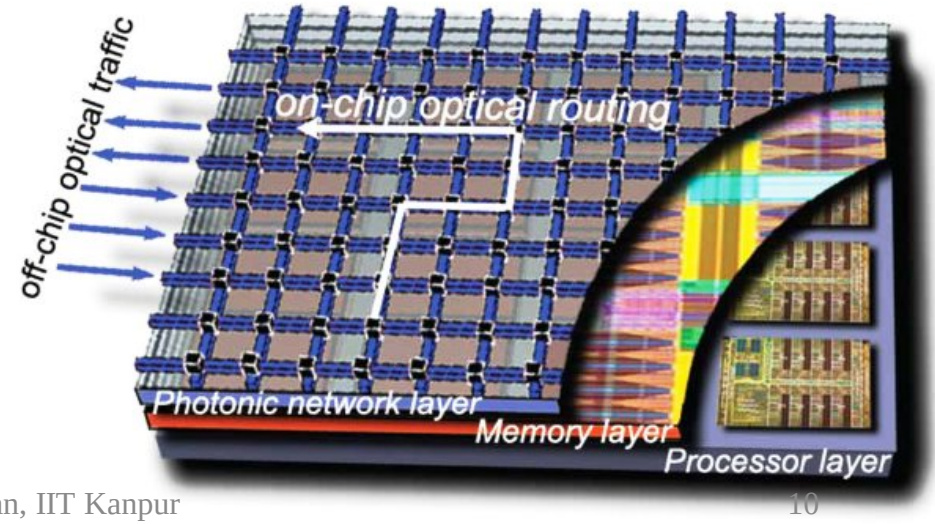
Multiple metal layers



3D ICs





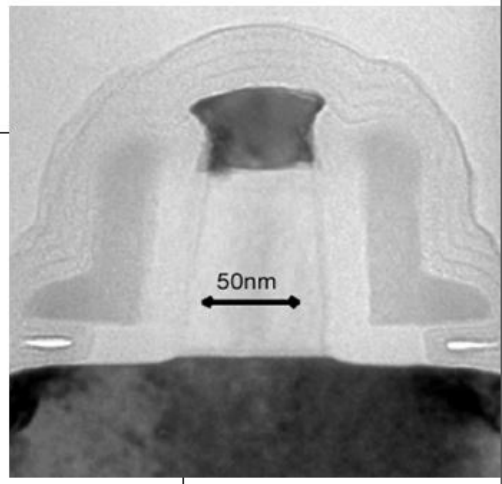


How do you make these?

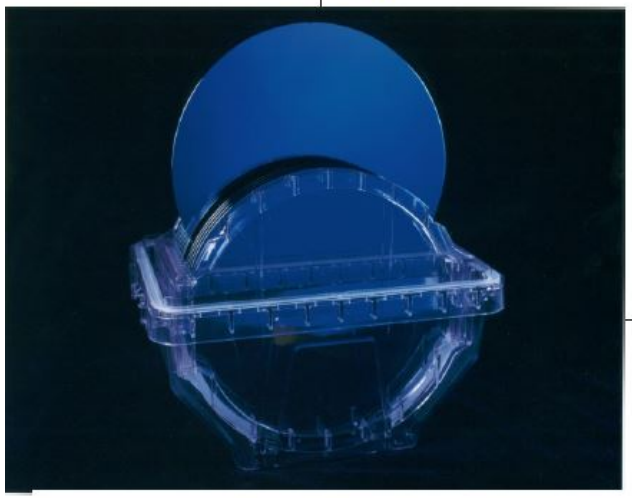
Start

Silicon Crystals

Bunny Suits!

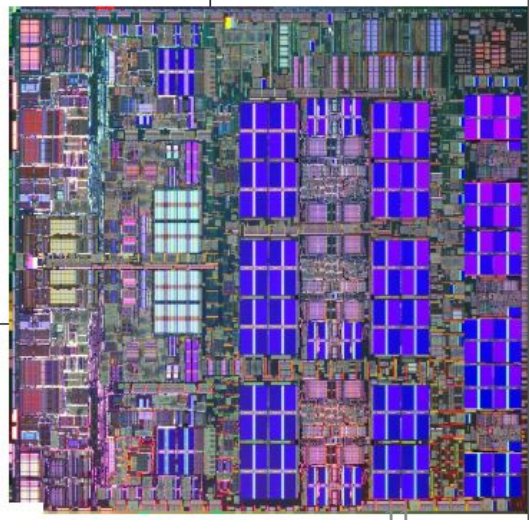


10B Transistors per cm^2



Silicon "Wafers"

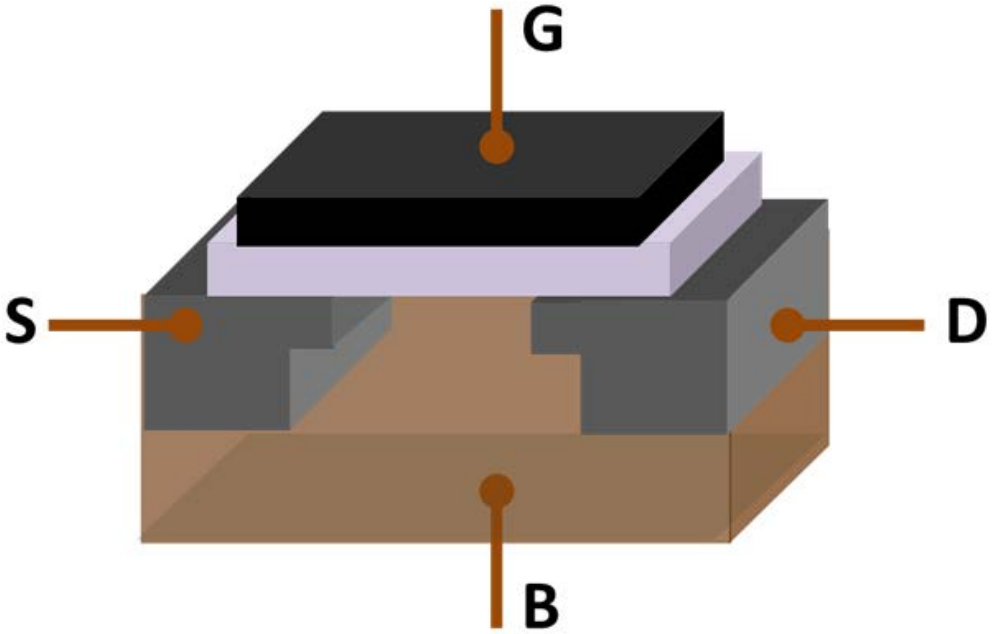
$5B Fabrication Facility



Finish

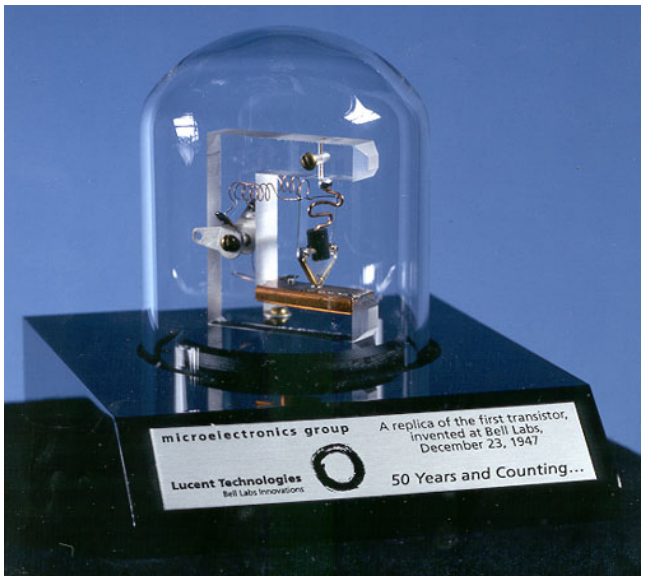
Building block – (tiny) MOSFET!

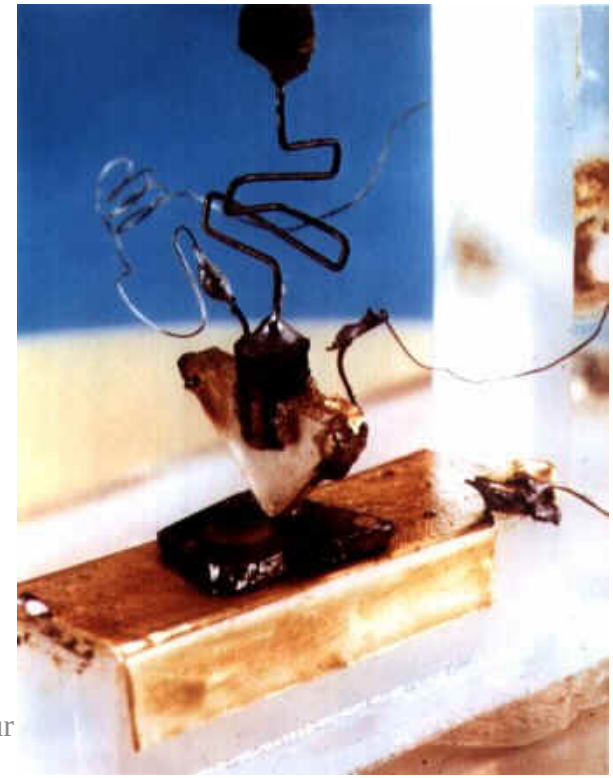
- MOSFET is a transistor used for amplifying or switching electronic signals.



Invention of Transistor

- First Transistor (1947-1948) at AT&T's Bell Labs
  - Point Contact Transistor
  - First transistor was bipolar contact transistor
  - Material – Germanium



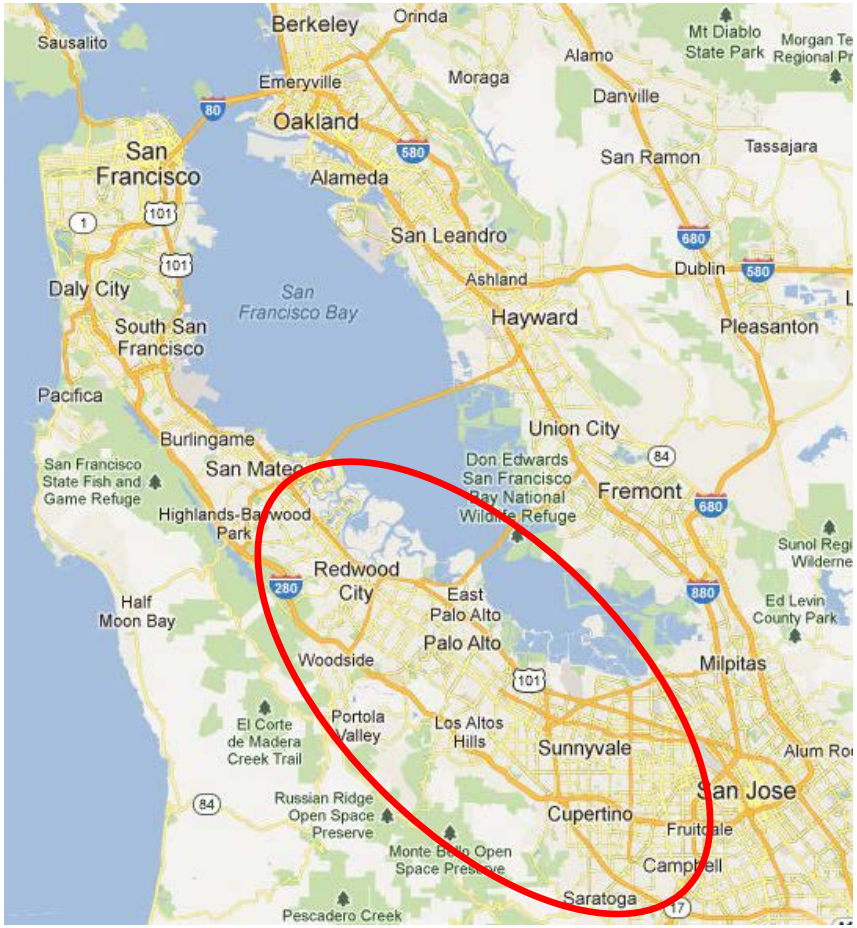


Invention of Transistor

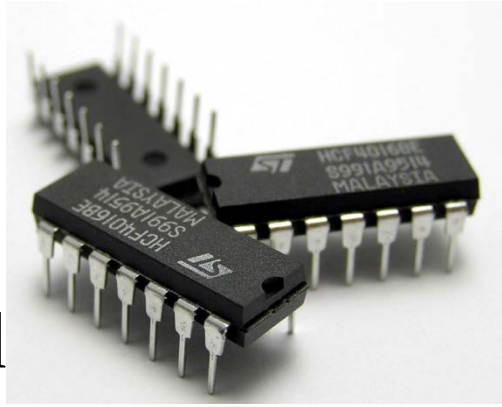
- Inventors
  - Walter H. Brattain (1902–1987)
  - John Bardeen (1908–1991)
  - William B. Shockley (1910–1988)

Silicon Valley

- Started with Shockley Semiconductor in 1956



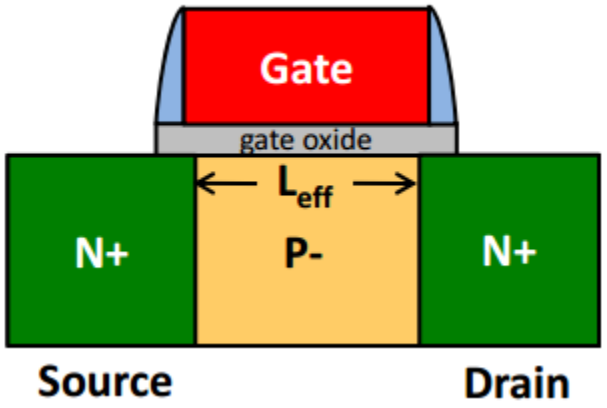
Integrated Circuit (IC)



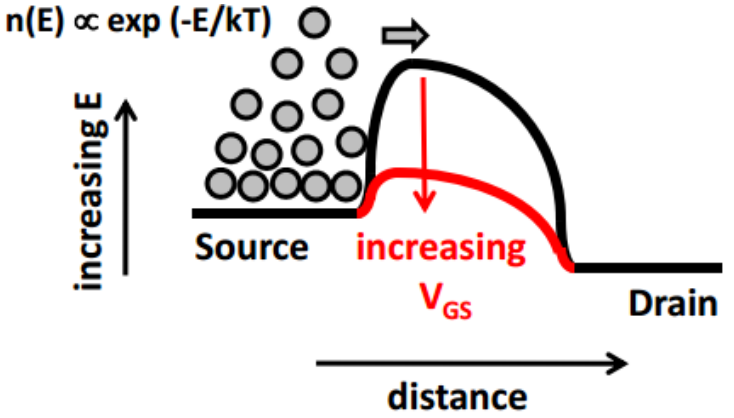
- IC – Electronic circuit manufactured on the surface of a thin substrate of semiconductor material.
- Additional materials are deposited and patterned to form interconnections between semiconductor devices.
- Jack Kilby (at *Texas Instruments*) demonstrated first working IC in 1958.
  - Jack Kilby was awarded the Nobel Prize in Physics 2000.

Building Block – Tiny MOSFET!

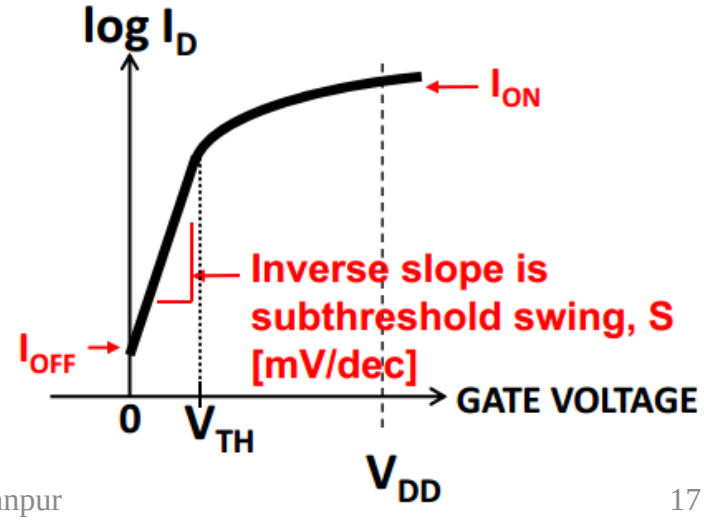
Schematic Cross Section



Barrier height is controlled by gate voltage



I_{DS} controlled by V_{GS}



Desired

- **High I_{ON}**
- **Low I_{OFF}**

Figures: T.Liu, SRC/GRC e-Workshop, November 2012

Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

- Drain current in MOSFET (OFF operation)

$$I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)}$$

$C_{ox}=\varepsilon_{ox}/t_{ox}$=oxide cap.
S – Subthreshold slope

- **Desired**
- **High I_{ON} (↓L, ↑Cox, ↑V_{DD}-V_{TH})**
- **Low I_{OFF} (↑V_{TH}, ↑S)**

Technology Scaling

- Each time the minimum line width is reduced, we say that a new ***technology node*** is introduced.

- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.

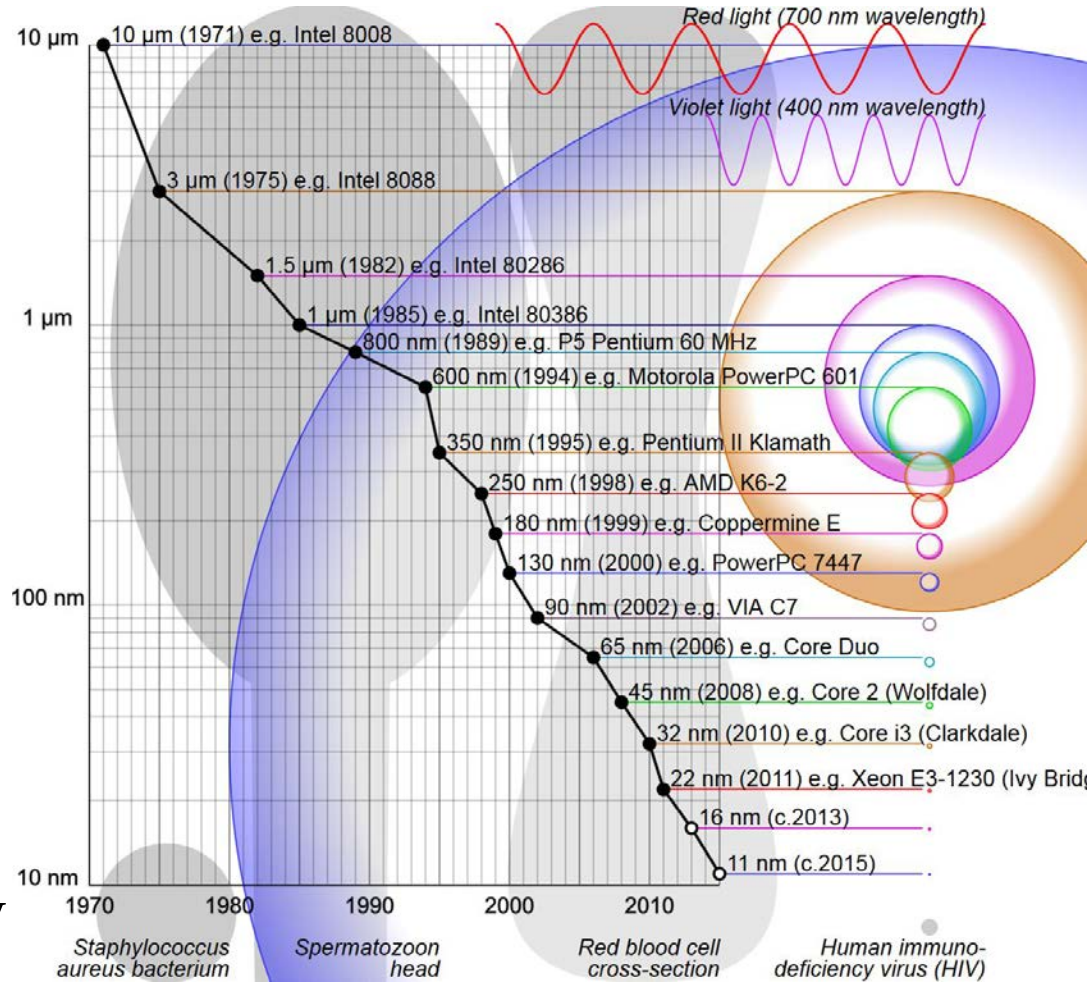


Figure source - Wikipedia

Technology Scaling

- Scaling – At each new node, all geometrical features are reduced in size to 70% of the previous node.
- Reward – Reduction of *circuit size by half*. (~50% reduction in area, i.e., $0.7 \times 0.7 = 0.49$.)
  - Twice number of circuits on each wafer
  - Cost per circuit is reduced significantly.

- Ultimately – **Scaling drives down the cost of ICs.**

Scaling and Moore's Law

- Number of components per IC function will double every two years – April 19, 1965 (Electronics Magazine)
- Shorthand for rapid technological change!

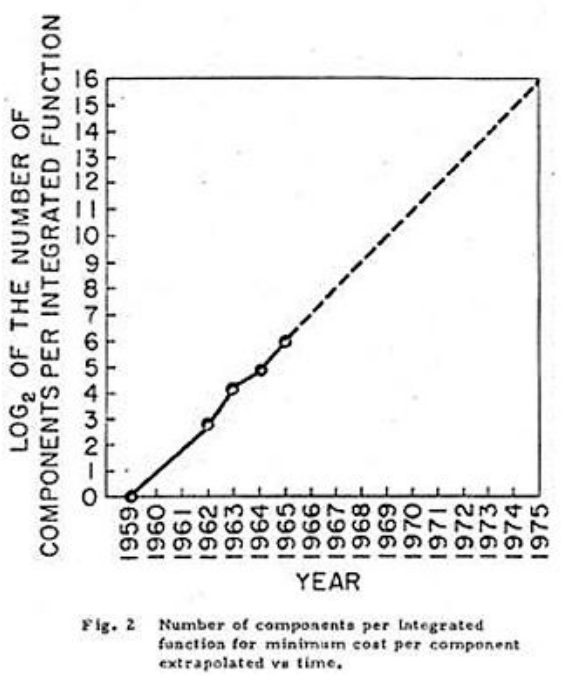
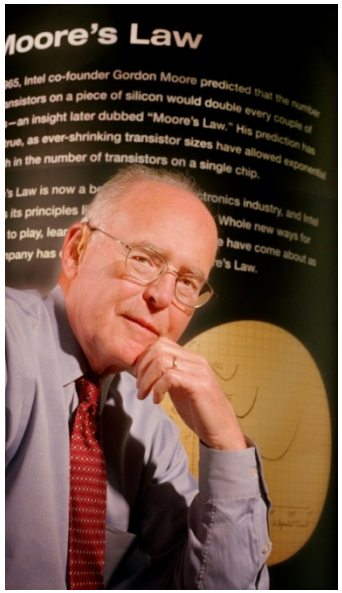
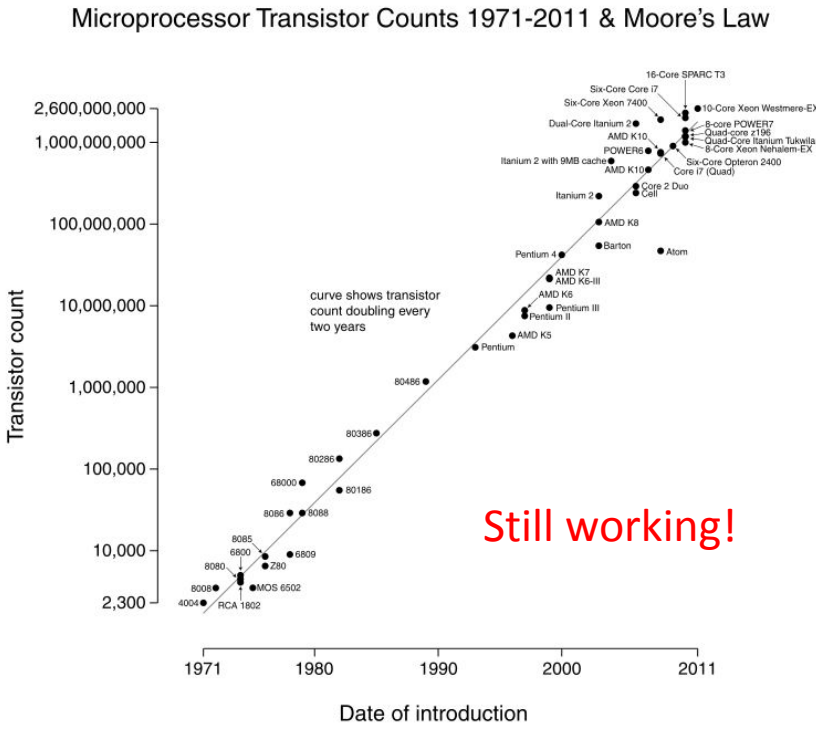


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.



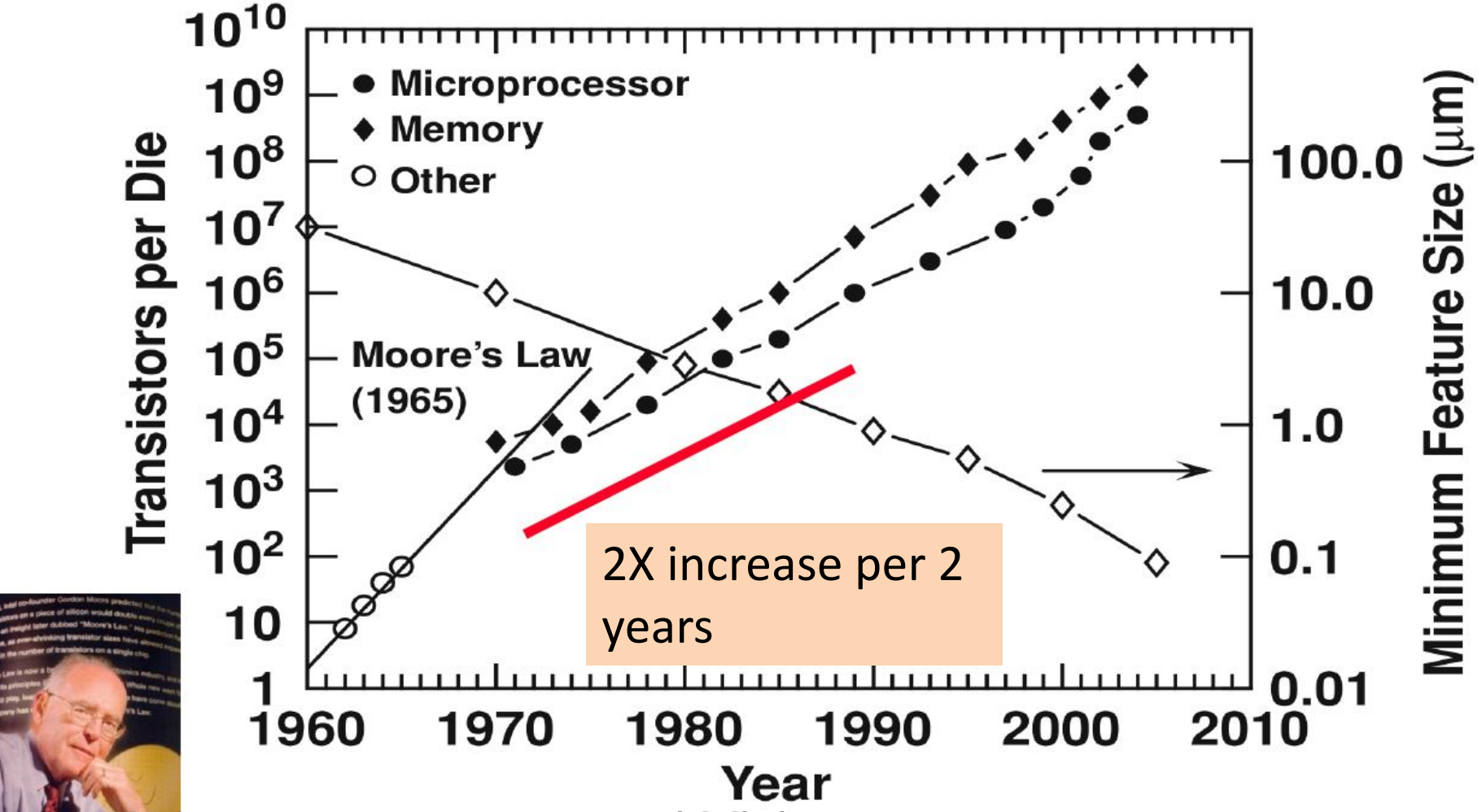


Source: http://www.intel.com/pressroom/kits/events/moores_law_40th/

Moore's Law:

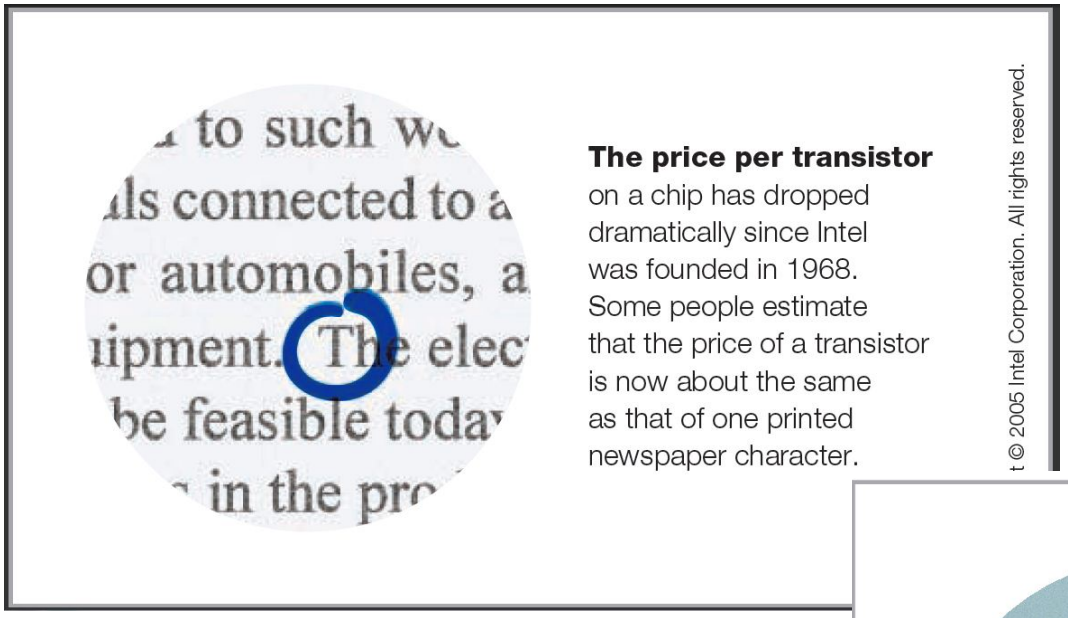
The defining features of the integrated circuit technology (size, speed, cost) follow an exponential growth pattern over time

Moral: Computing power ⬆ while cost ⬇ exponentially!



Moore's Law

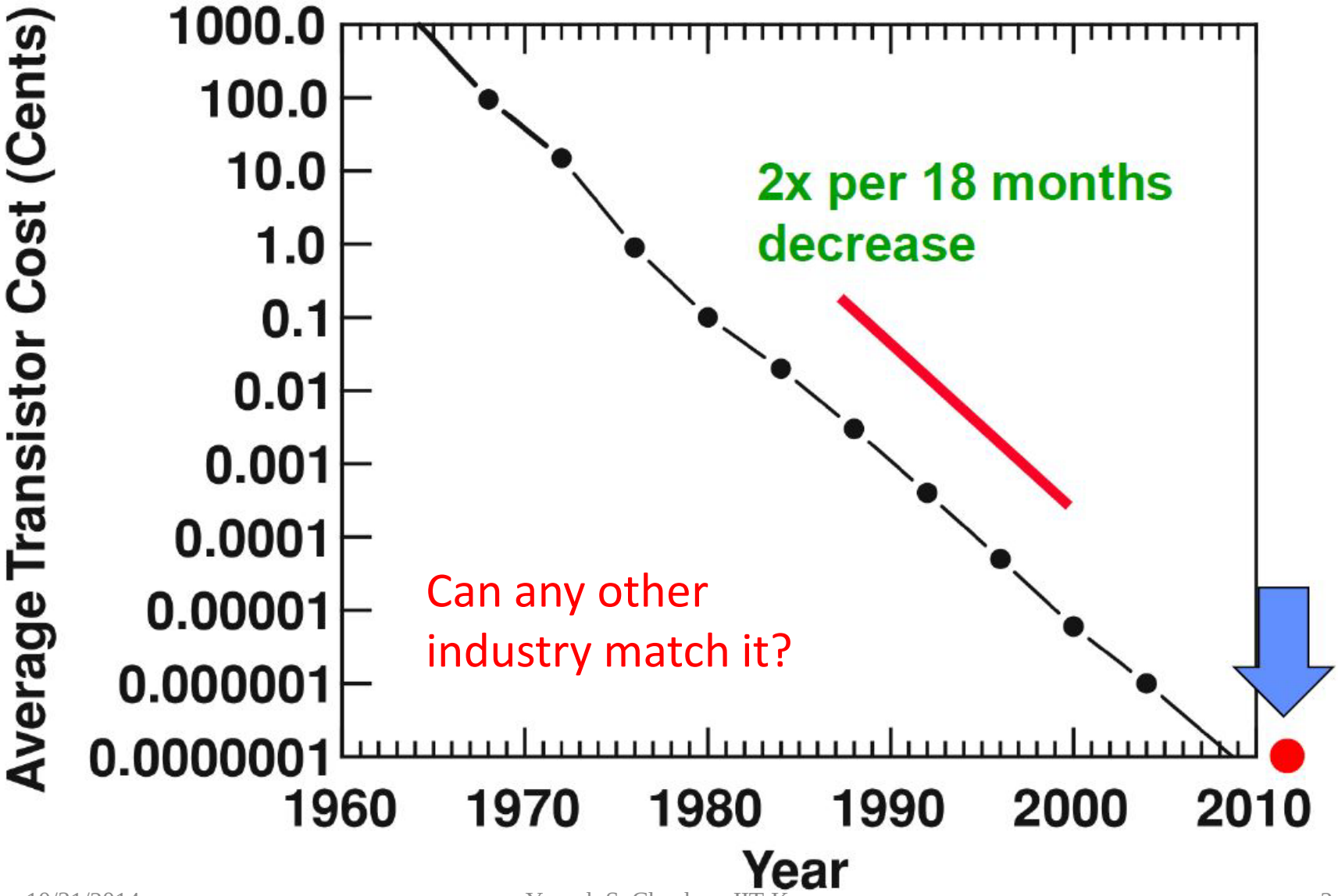
It's not technology! → It's economy.



- Ways to Huge Profits
  - High performance and Low Cost
  - Achieved by making everything SMALLER

In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore's Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.

1 Nano-$ / Transistor!



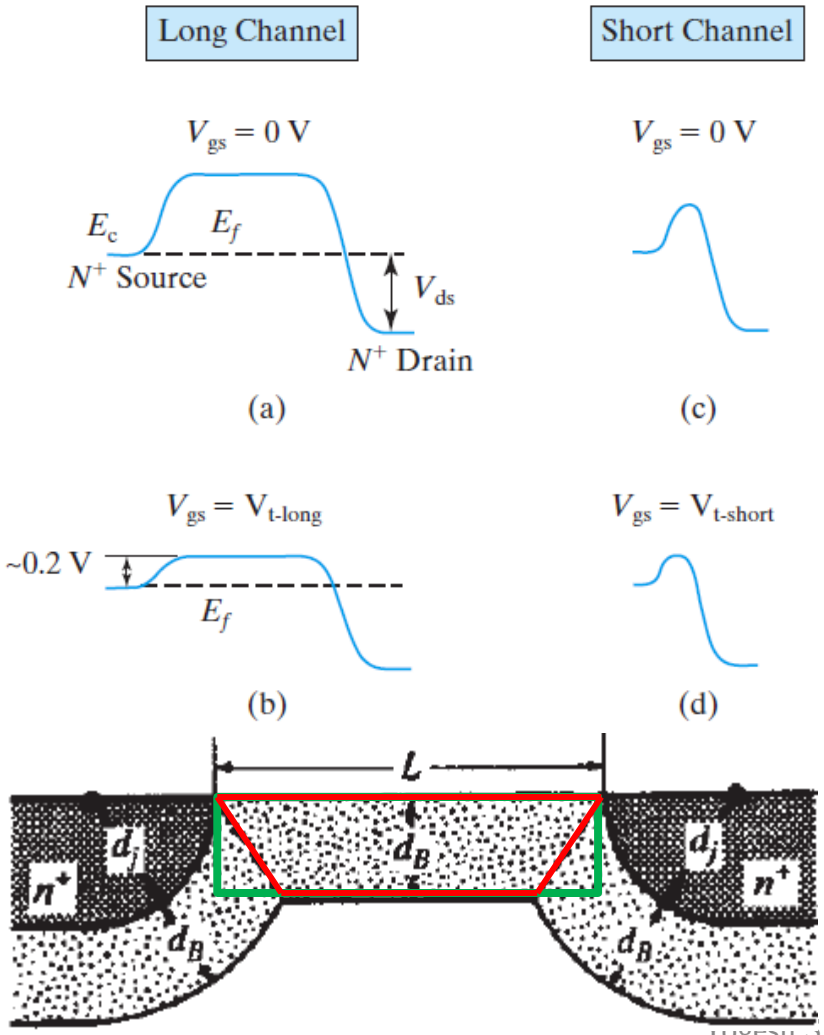
Ways to drive performance & decrease cost?

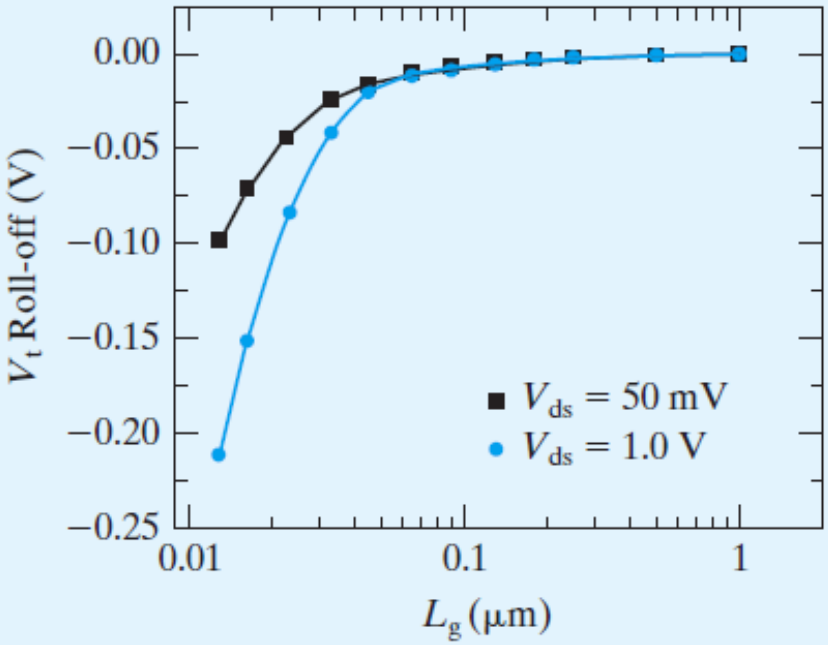
- Closer distance between elements – *Pitch*
- *Faster* signal transfer and processing rate
- For the same Chip size (thus material cost), *more functionality*
- *Mass production*
  - Wafer size is doubled every 10years.
  - Currently it's 300mm.
- Use less energy (or *less power*) to achieve the same function

Technology Scaling (Cost, Speed & Power Consumption)

- In the last 45 years since 1965
- *Price* of memory/logic gates has dropped 100 million times.
  - Rapid price drop has stimulated *new applications*.
- The primary engine that powered the proliferation of electronics is "*miniaturization*".
- More circuits on each wafer → cheaper circuits.
- Miniaturization has also been instrumental to the improvements in *speed and power consumption* of ICs.

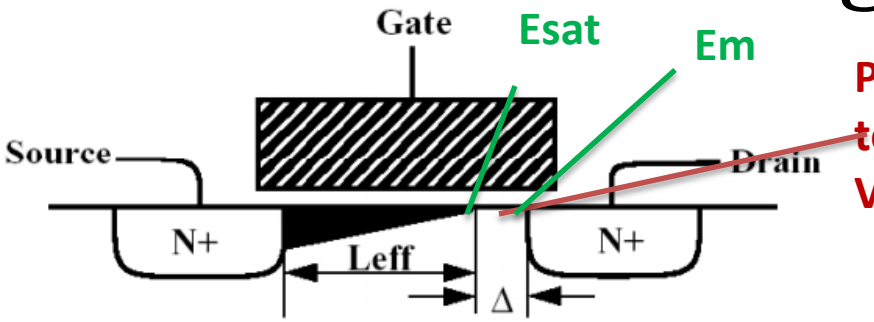
Threshold Voltage Roll-Off





Vt decreases at very small Lg. It determines the minimum acceptable Lg because Ioff is too large when Vt becomes too low or too sensitive to Lg.

Channel Length Modulation



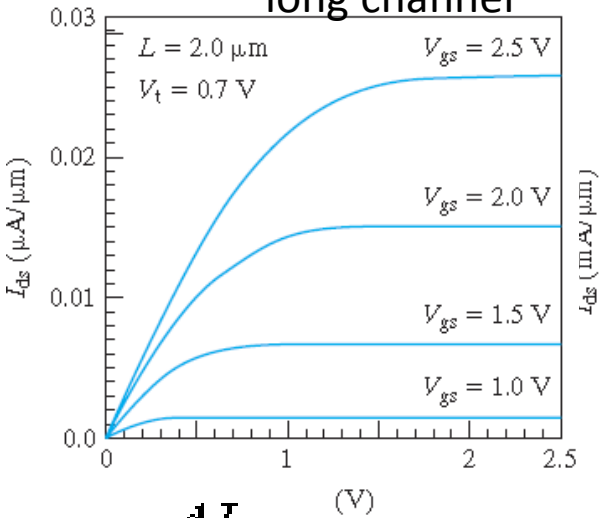
Pinch off point moves towards the source as V_{ds} increases

$$\Delta \propto V_{DS} - V_{DSsat}$$

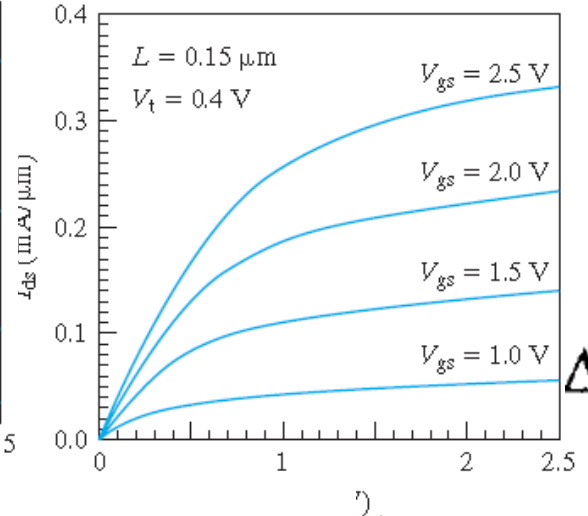
$$I_{Dsat} \propto \frac{1}{L-\Delta L} \cong \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$$

$$I_{Dsat} = I_{Dsat0}\left(1+\frac{\Delta L}{L}\right) = I_{Dsat0}\left(1+\frac{V_{ds}-V_{dsat}}{V_A}\right)$$

long channel



Short channel



This model is simple and acceptable for some digital applications

More Accuracy for better gds

$$\Delta L = l \ln\left(\frac{(V_{ds}-V_{dsat}}{lE_{sat}} + \frac{Em}{E_{sat}}\right)$$

$$g_{ds} = \frac{dI_{dsat}}{dV_{ds}}$$

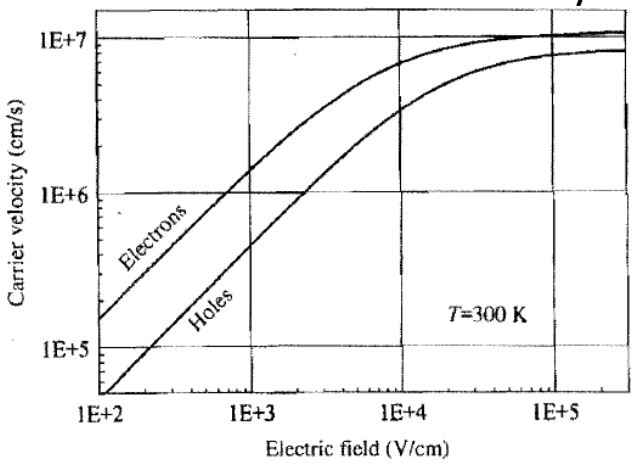
g_{ds} ↑ A_v reduces

C.Hu, Modern Semiconductor Devices for IC, 2009 Prentice Hall

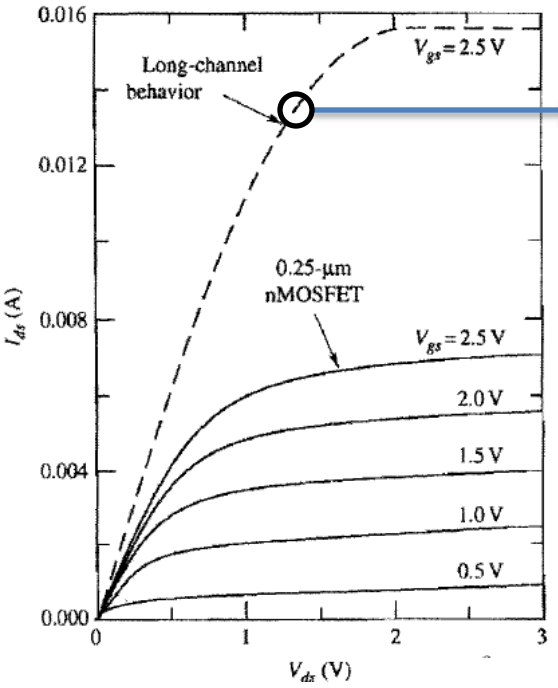
Velocity Saturation

State of the art MOSFET, channels are short enough to cause velocity saturation

Measured carrier velocity



Y.Taur, Fundamentals of Modern VLSI Devices, 2009 Cambridge Press



Long channel current is well predicted by model

For short channel, current is saturated well below V_{dsat}

Modeling

$$v = \frac{\mu_{eff}\mathscr{E}}{\left[1+(\mathscr{E}/\mathscr{E}_c)^n\right]^{1/n}}$$

$E<E_c$, $v = \mu E$: For low field, velocity is proportional to mobility

$E>E_c$, $v=\mu E_c = V_{sat}$

High $E_{vertical}$ ---> Low μ--> High E_c

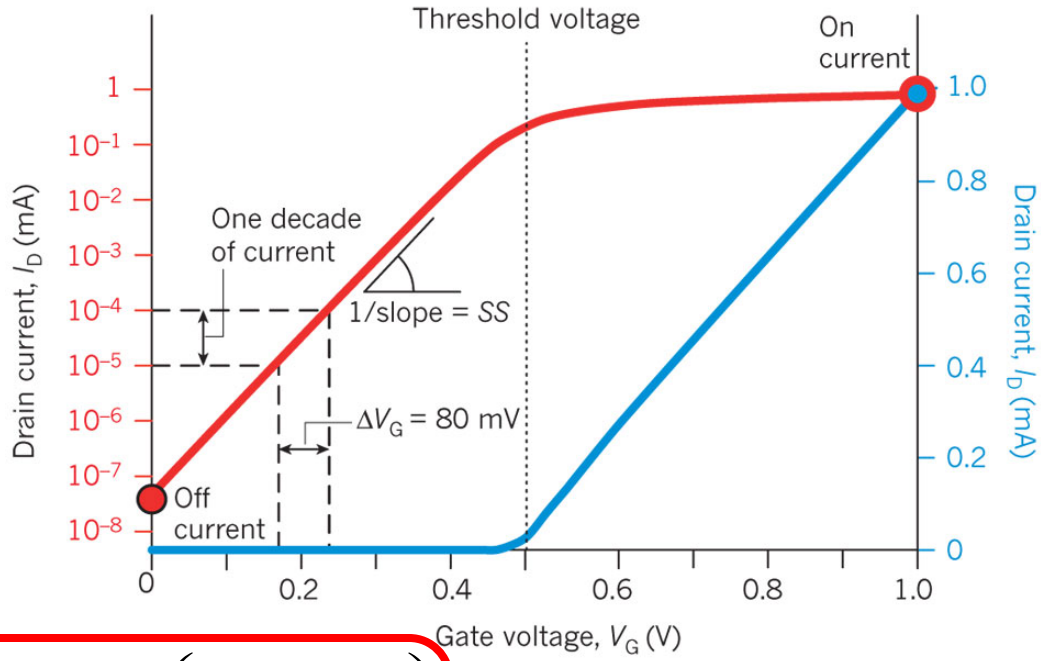
Y.S.Chauhan et.al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET," Transaction on Electron Devices, 2014

Subthreshold slope

- It is defined as the amount of gate voltage required to change the gate current by 1-decade.

$$S = \frac{dV_{GS}}{d\left(\log I_{ds}\right)}$$

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_{dep}}{C_{ox}}\right)$$



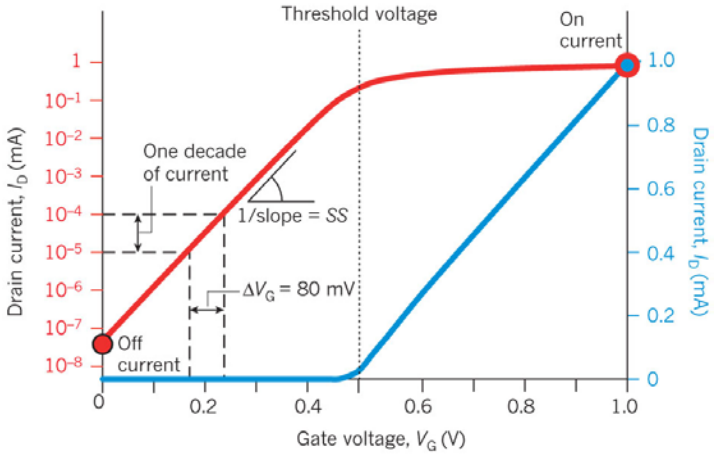
At room temperature

$$S = (25.85)(2.30)\left(1+\frac{C_{dep}}{C_{ox}}\right) \approx 60mV\left(1+\frac{C_{dep}}{C_{ox}}\right)$$

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_{dep}}{C_{ox}}\right)$$

Subthreshold slope

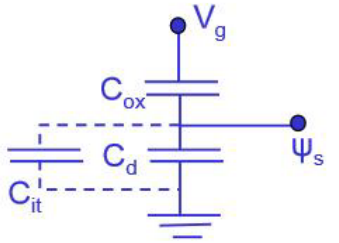
- Minimum value of S is 60mV/decade.
- I_{off} is determined by VTH and S
- If I_{ds} at V_{TH} is $100nA\frac{W}{L}$



$$I_{ds}(nA) = 100\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{nkT/q}} = 100\frac{W}{L}10^{\frac{V_{GS}-V_{TH}}{S}}$$

$$I_{off}(nA) = 100\frac{W}{L}10^{-\frac{V_{TH}}{S}}$$

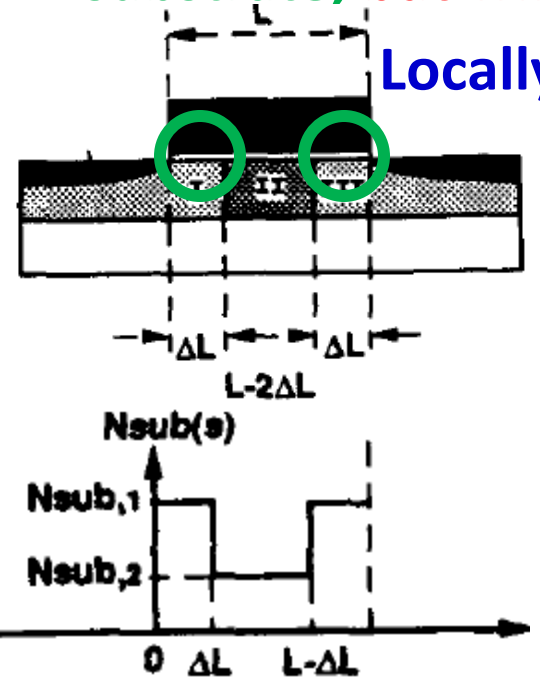
- To minimize I_{off}
  - Increase V_{TH} – Not good as I_{ON} decreases (low speed!)
  - Reduce S
    - Increase Cox – Thin oxide
    - Decrease Cdep (Increase Wdep) – Use substrate bias or low doping
    - Decrease Temperature – cost?



Channel Engineering : Lateral Non Uniform Doping

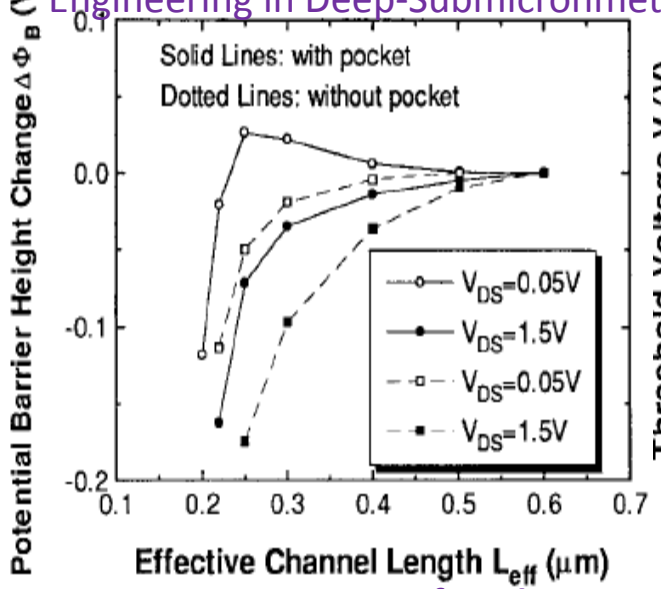
The encroachment of depletion layer in the channel is the prime cause of Vt Roll off

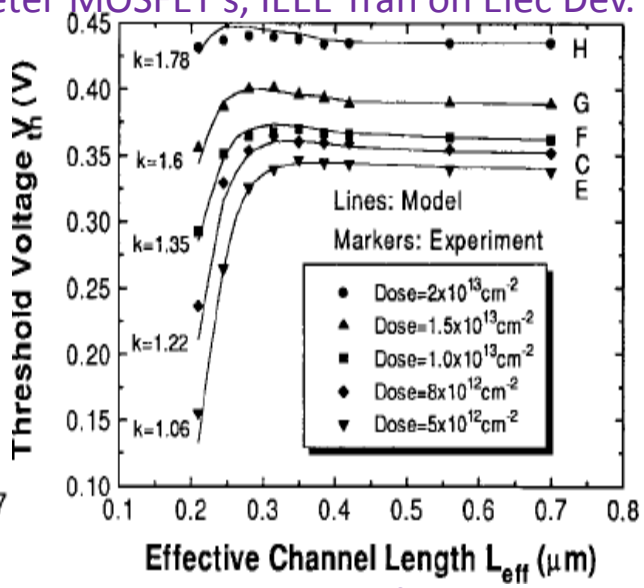
Sol: Control depletion region by increasing doping of the substrate, but will have adverse effect on other parameters



Locally increase doping near S/D : Halo doping

Bin Yu et al, Short-Channel Effect Improved by Lateral Channel Engineering in Deep-Submicronmeter MOSFET's, IEEE Tran on Elec Dev. 1997



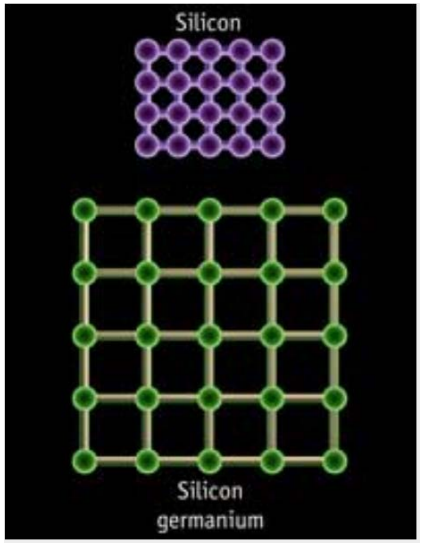


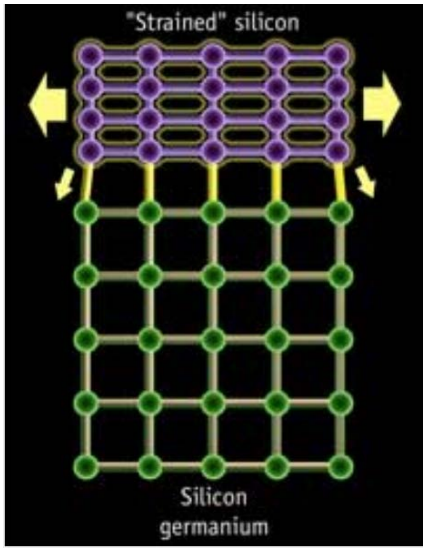
Okumura et al, "Novel Source to Drain Non Uniformly Doped channel MOSFET for High Current Drivability and Threshold Voltage Controllability", IEDM, 1990

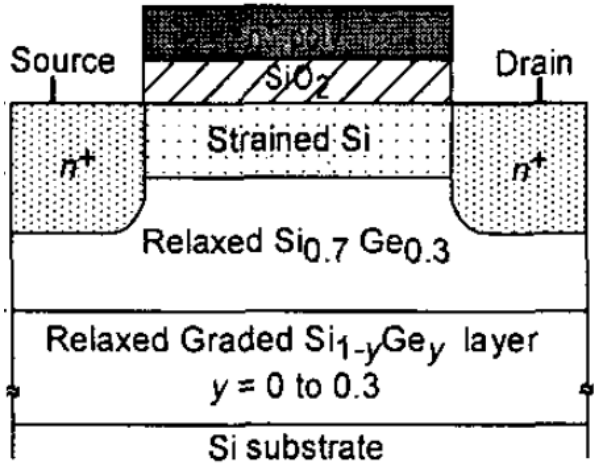
Strained Silicon

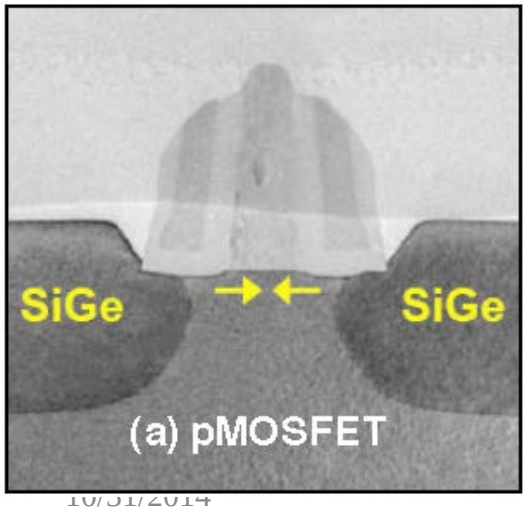
$$I_{ON} = \mu \frac{W}{L} C_{ox}(V_{DD} - V_{TH})^2$$

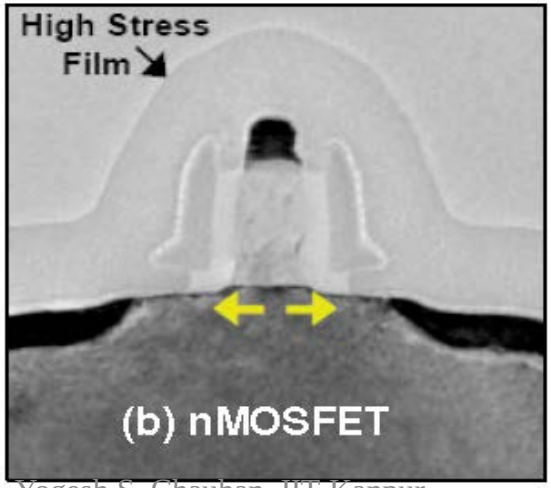
Silicon is placed on substrate having large atomic spacing











Methods of straining

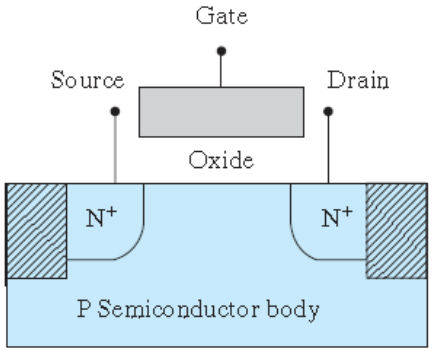
-Burried SiGe –Biaxial

-Uniaxial Stress S/D SiGe

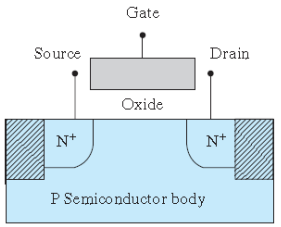
High-K Metal Gate Technology

- **"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"- Moore**

What is HKMG



scaling



Lateral and vertical dimensions squeezed

$$C_{OX} = \frac{\varepsilon_{ox}.\varepsilon_0}{T_{ox}}$$

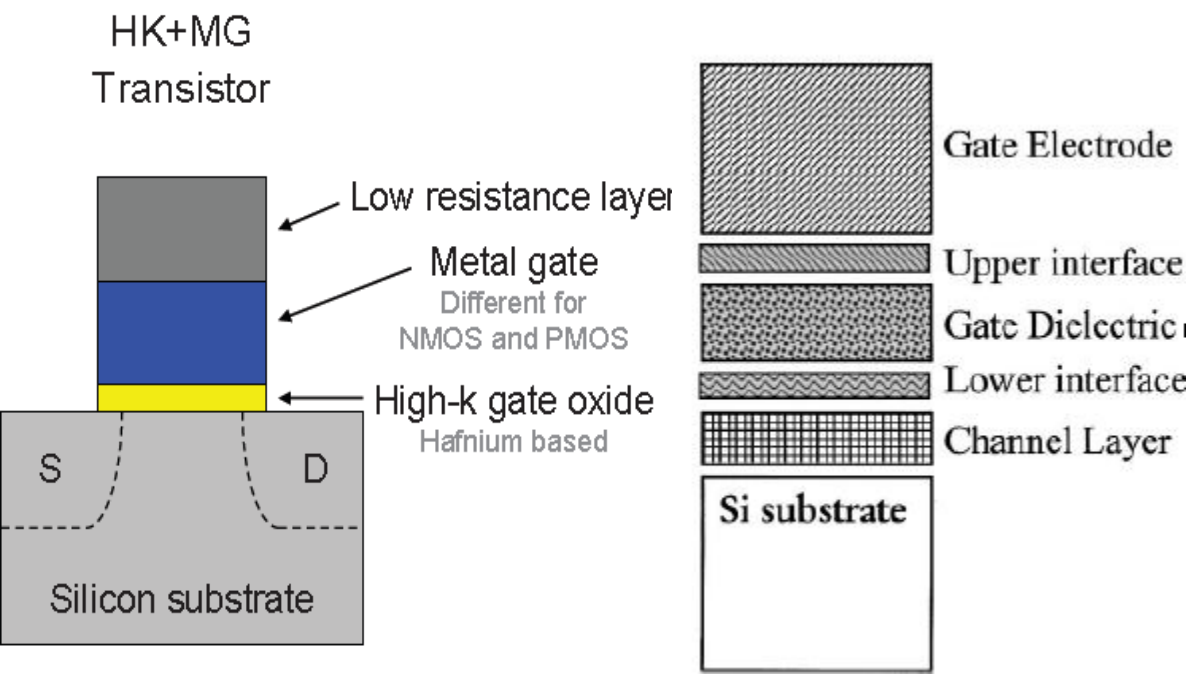
T_{ox} ⬇ , C_{ox} increases

: **Better Gate Control** ✓

: **Gate Leakage Increases** ✗

C_{ox} can alternatively be increased by using high K material : **HKMG**

High-K Metal Gate Technology



$$EOT = \frac{3.9}{\kappa} t_{phys}$$

EOT @ 45nm = 1.0nm
@ 32nm=0.9nm

Metal Gate

- Increases the gate field effect

High-k Dielectric

- Increases the gate field effect
- Allows use of thicker dielectric layer to reduce gate leakage

HK + MG Combined

- Drive current increased >20% (>20% higher performance)
- Or source-drain leakage reduced >5x
- Gate oxide leakage reduced > 10x

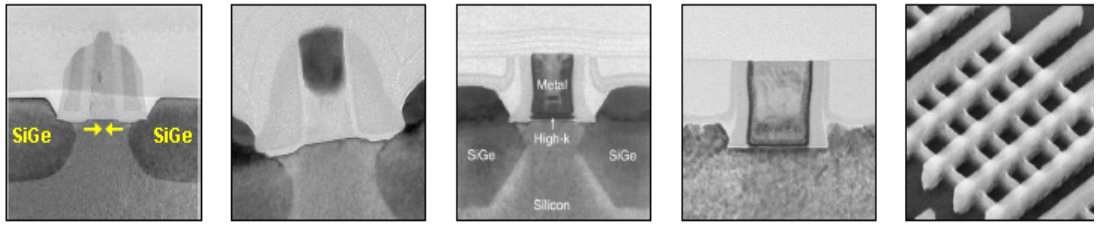
Requires interface engineering

High K Material used – HfO_2

Intel began volume production of HKMG in 2008 at 45nm

Technology Trend

2003	2005	2007	2009	2011
90 nm	65 nm	45 nm	32 nm	22 nm



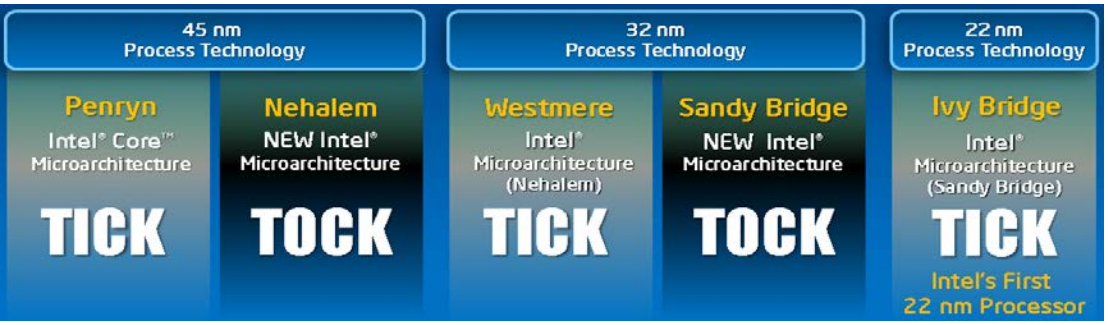
Invented SiGe Strained Silicon	2nd Gen. SiGe Strained Silicon	Invented Gate-Last High-k Metal Gate	2nd Gen. Gate-Last High-k Metal Gate	First to Implement Tri-Gate

Strained Silicon

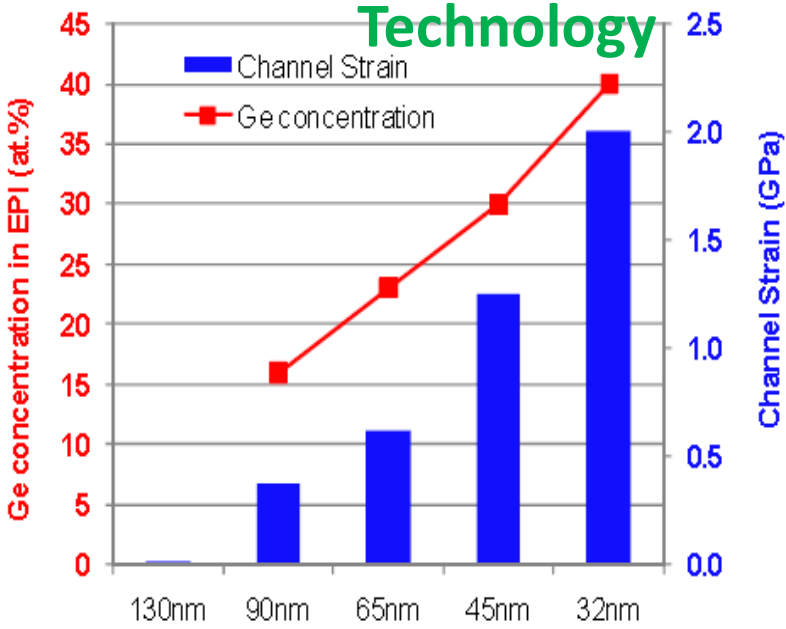
High-k Metal Gate

Tri-Gate

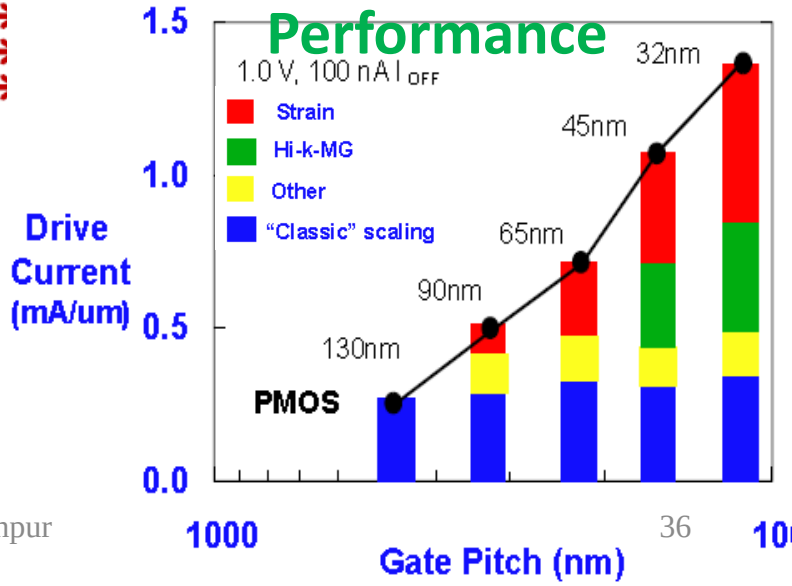
Product



Technology



Performance



Source : www.intel.com

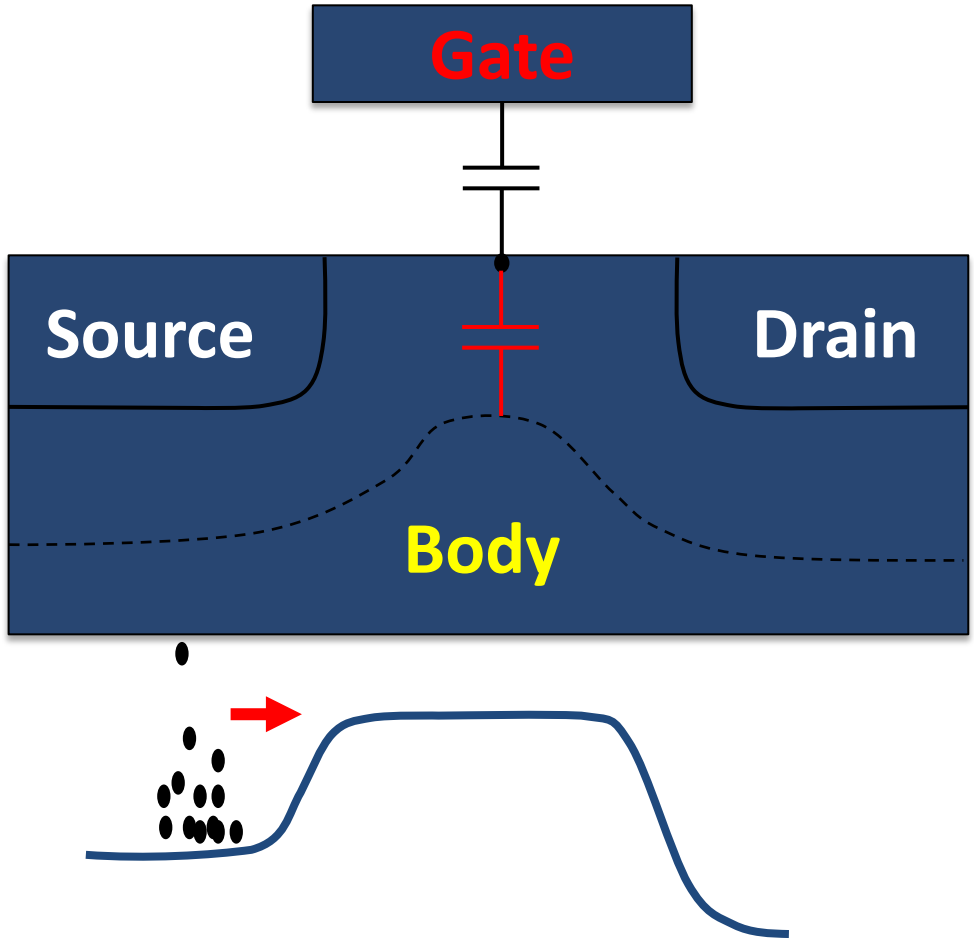
Wasn’t that smooth ride?

- Where is the bottleneck?

$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

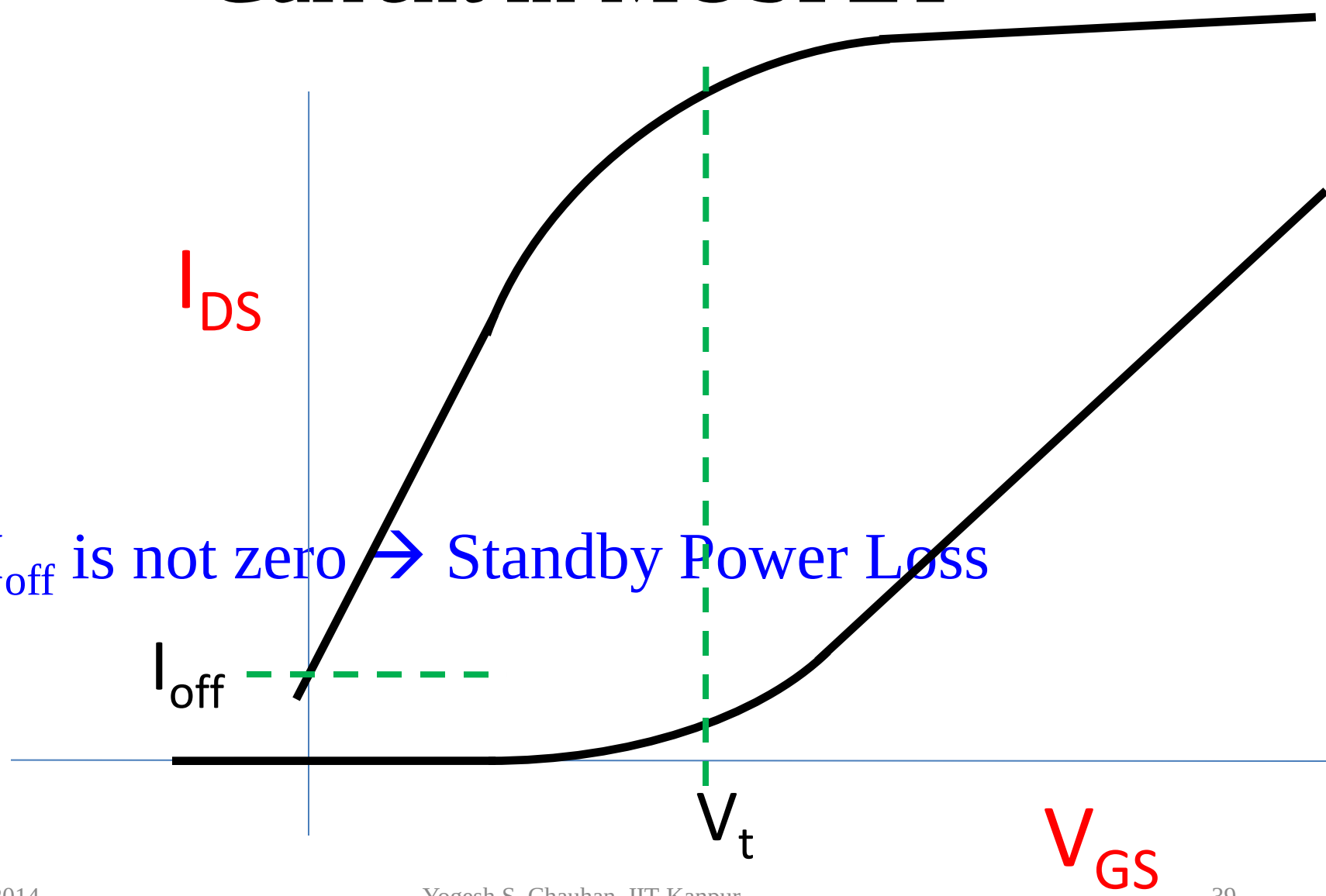
- V_{TH} can’t be decreased – why?

Thin Depletion Layer - Problem



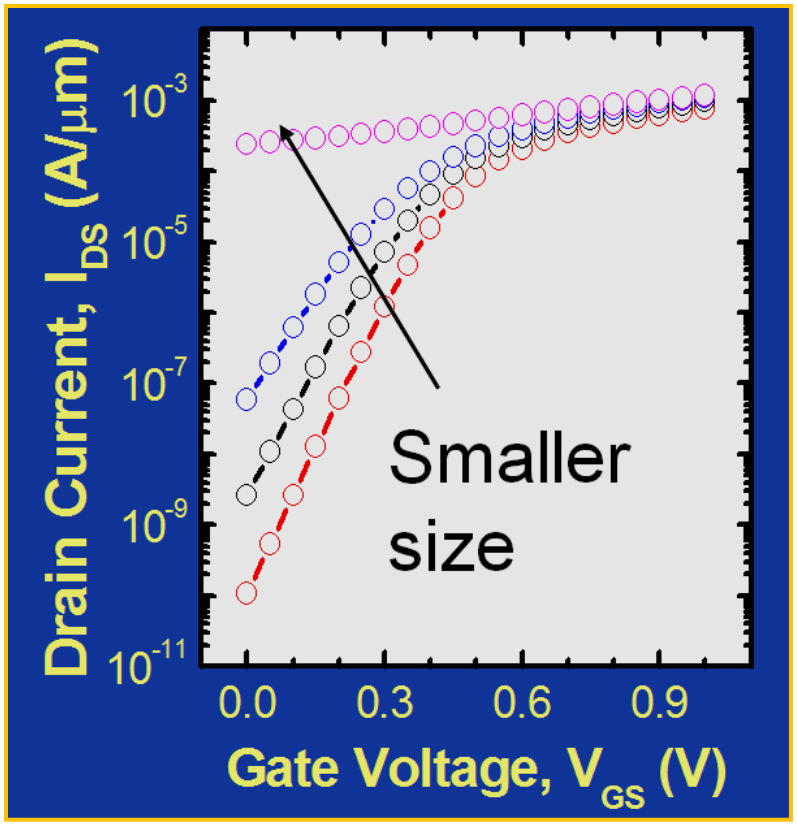
- $Q_G = Q_i + Q_b$
- Charge sharing

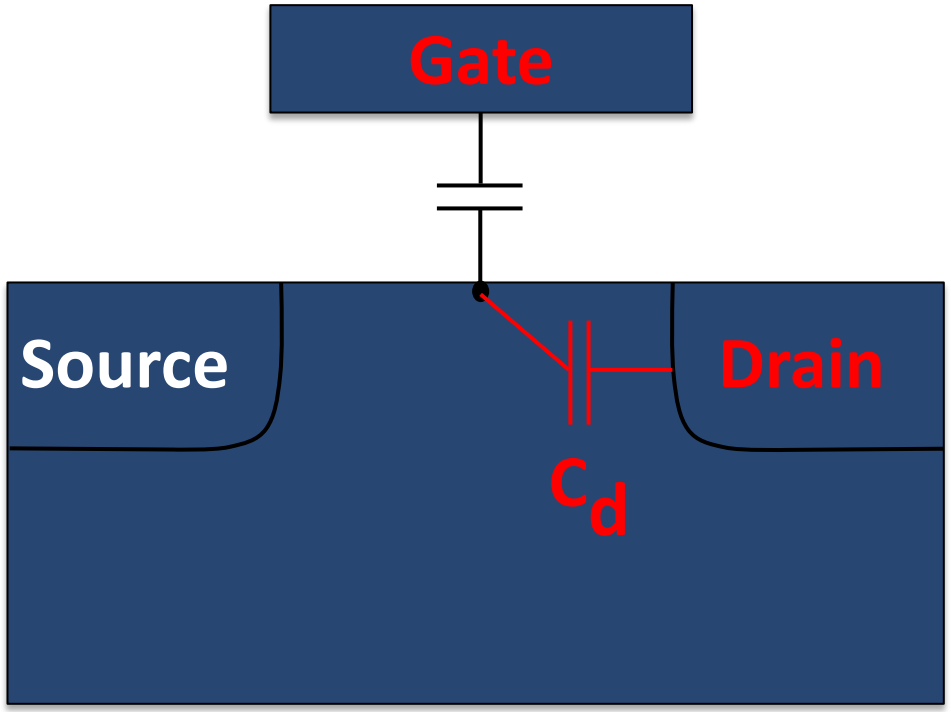
Current in MOSFET



- I_{off} is not zero → Standby Power Loss

Short Channel – Big Problem

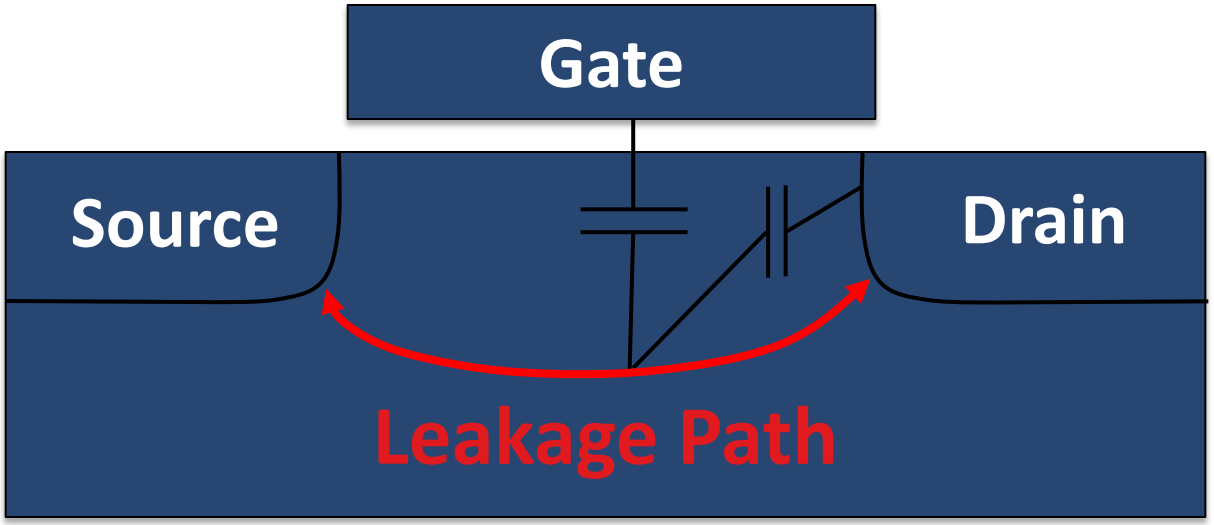




MOSFET becomes "resistor" at small L.

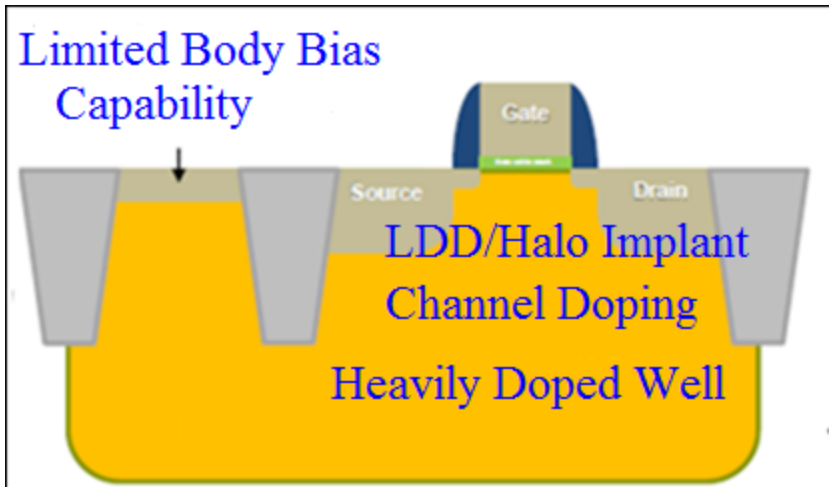
Chenming Hu, "Modern Semiconductor Devices for ICs" 2010, Pearson

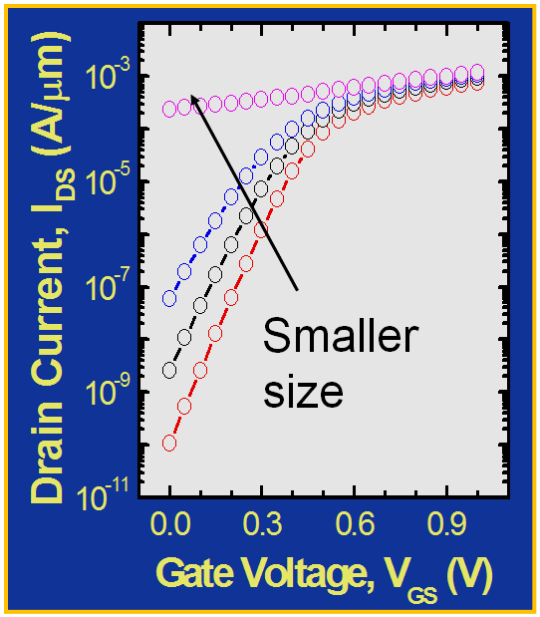
Making Oxide Thin is Not Enough

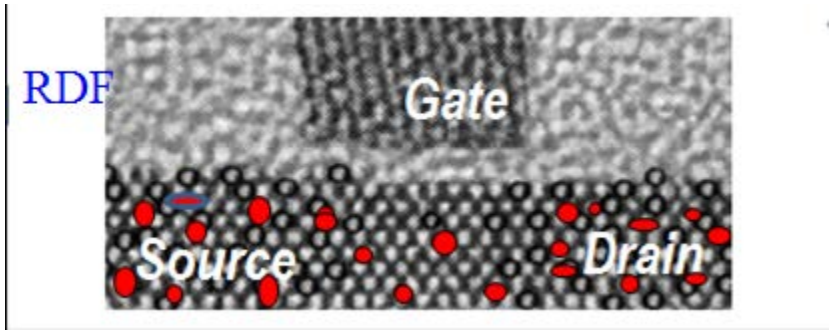


Gate cannot control the leakage current paths that are far from the gate.

Good Old MOSFET has reached its Limits



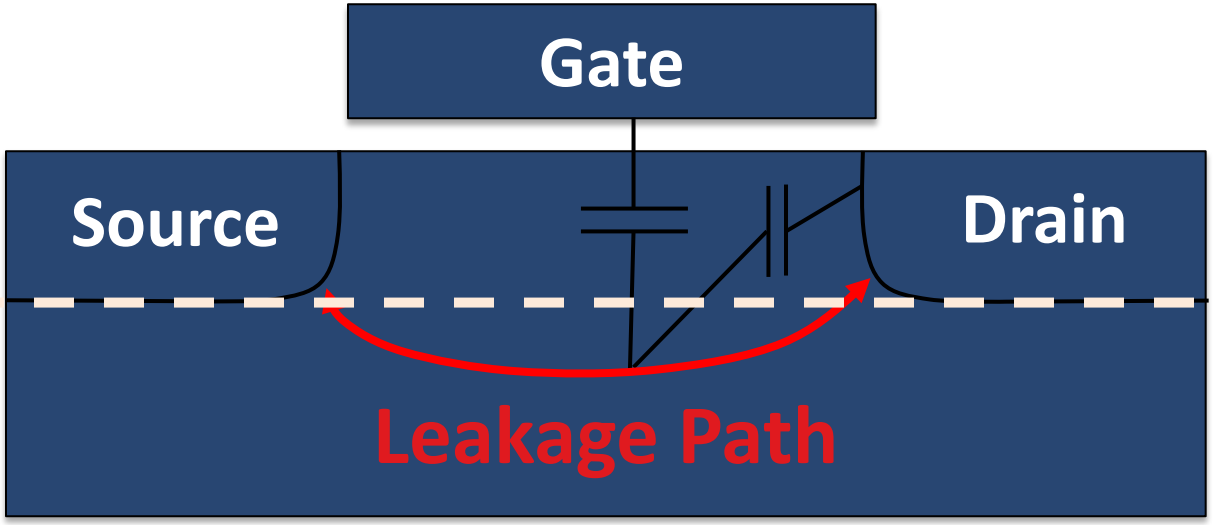




- **Ioff is bad**
- **Size and dopant variations**

High Vdd, Power, Design Cost

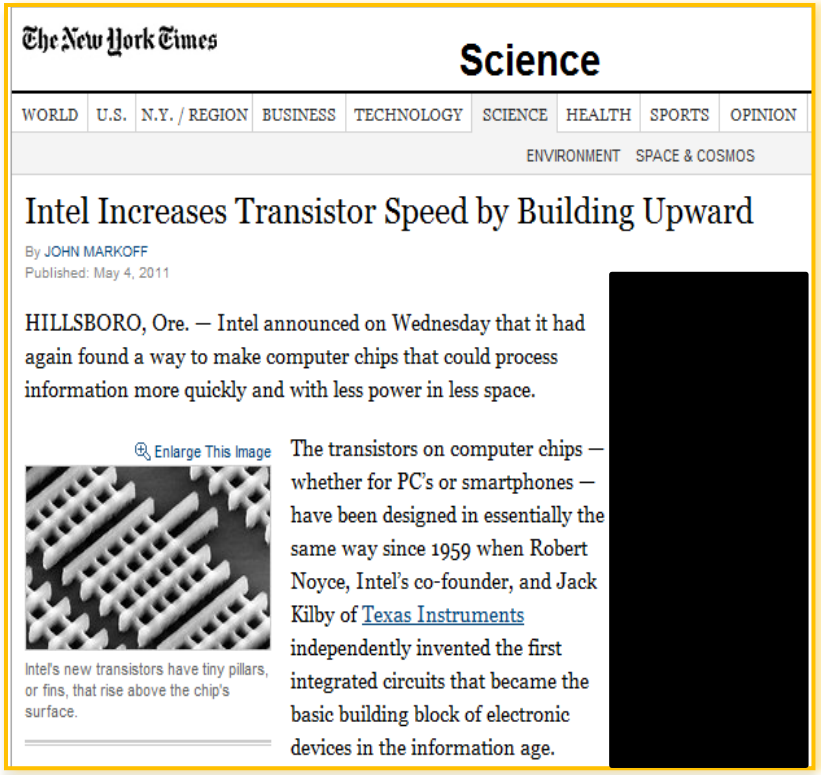
What can we do?



May 4, 2011

The New York Times Front Page

- **Intel will use 3D FinFET at 22nm**
- **Most radical change in decades**
- **There is a competing SOI technology**



The New York Times

Science

WORLD | U.S. | N.Y. / REGION | BUSINESS | TECHNOLOGY | SCIENCE | HEALTH | SPORTS | OPINION

ENVIRONMENT | SPACE & COSMOS

Intel Increases Transistor Speed by Building Upward

By JOHN MARKOFF
Published: May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

Enlarge This Image

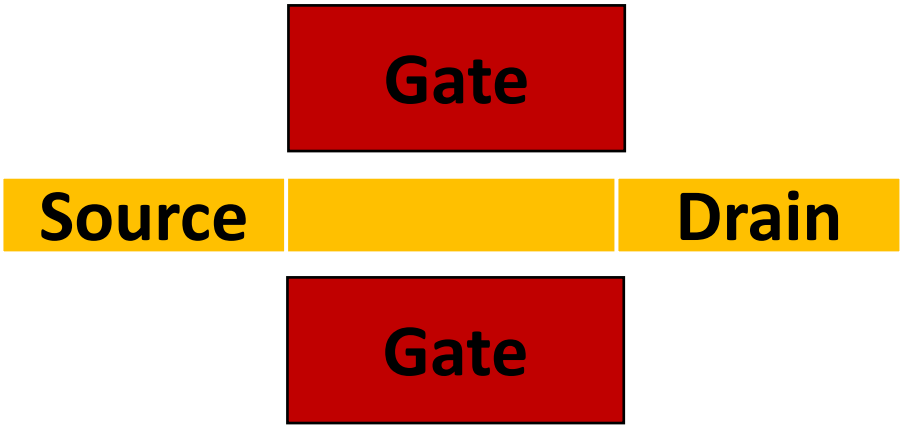
Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

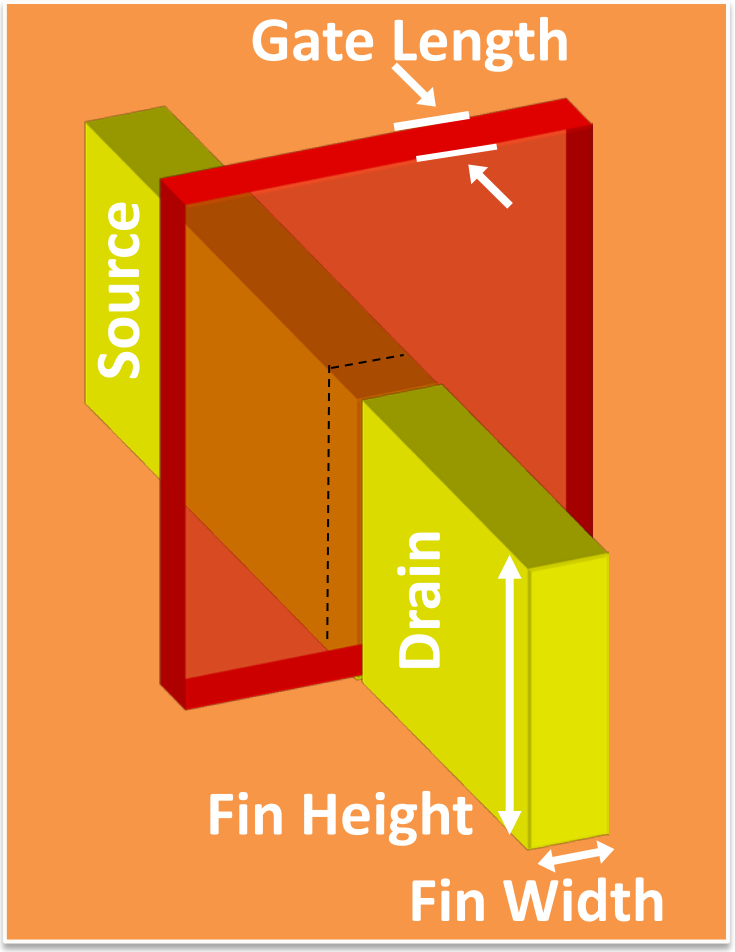
One Way to Eliminate Si Far from Gate

Thin body controlled

By multiple gates.



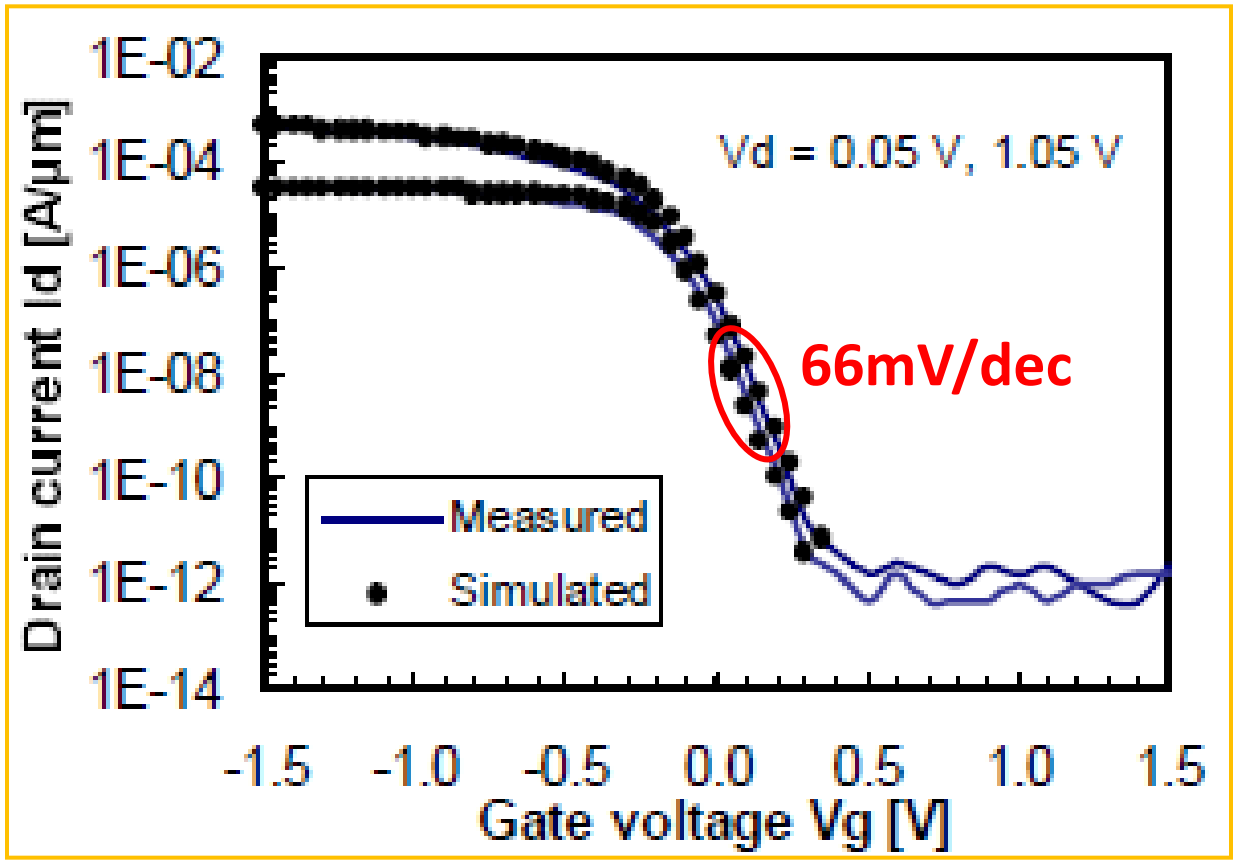
FinFET body is a thin Fin.



N. Lindert et al., DRC paper II.A.6, 2001

40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.



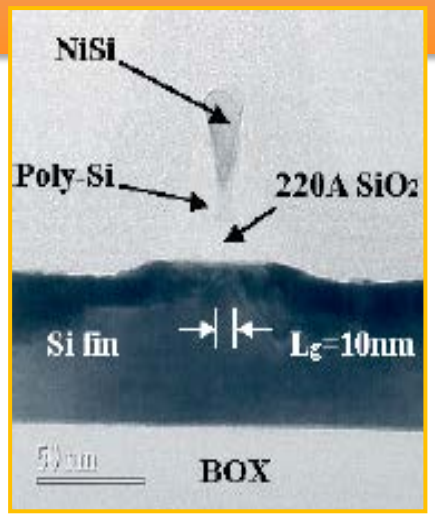
X. Huang et al., IEDM, p. 67, 1999

Introduced New Scaling Rule

Leakage is well suppressed if

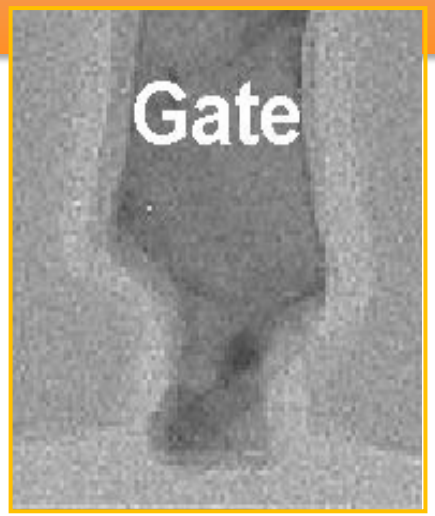
Fin thickness < Lg

10nm Lg AMD
2002 IEDM



5nm Lg TSMC
2004 VLSI

3nm Lg KAIST
2006 VLSI



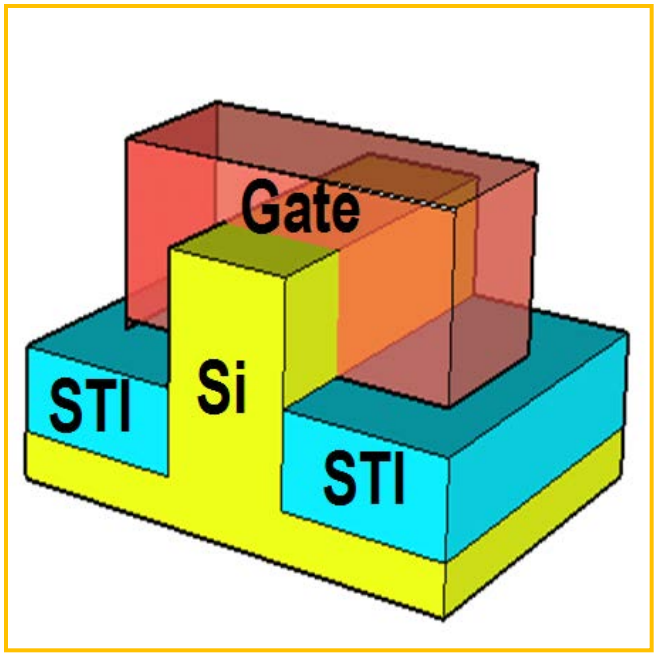
Two Improvements Since 1999

- **2002 FinFET with thin oxide on Fin top**

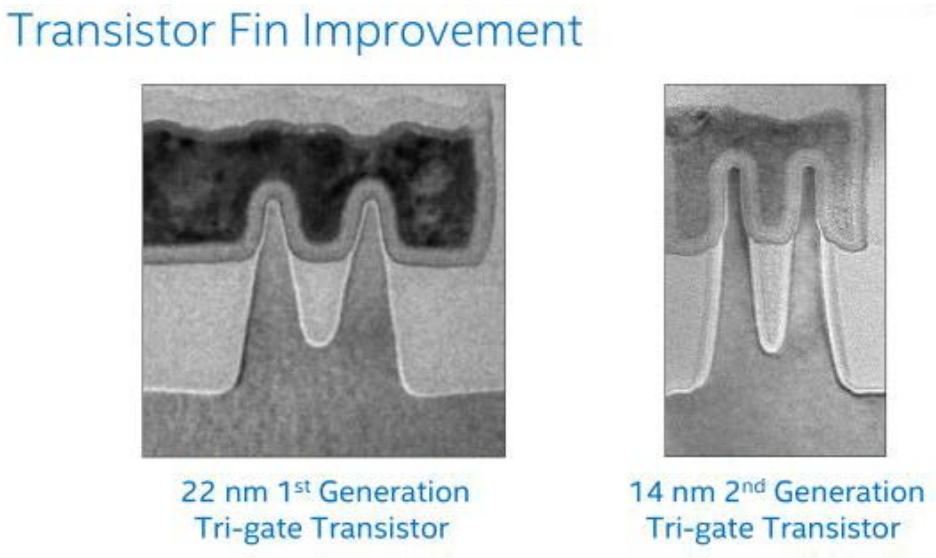
  F.L.Yang et al. (TSMC) 2002 IEDM, p. 225.

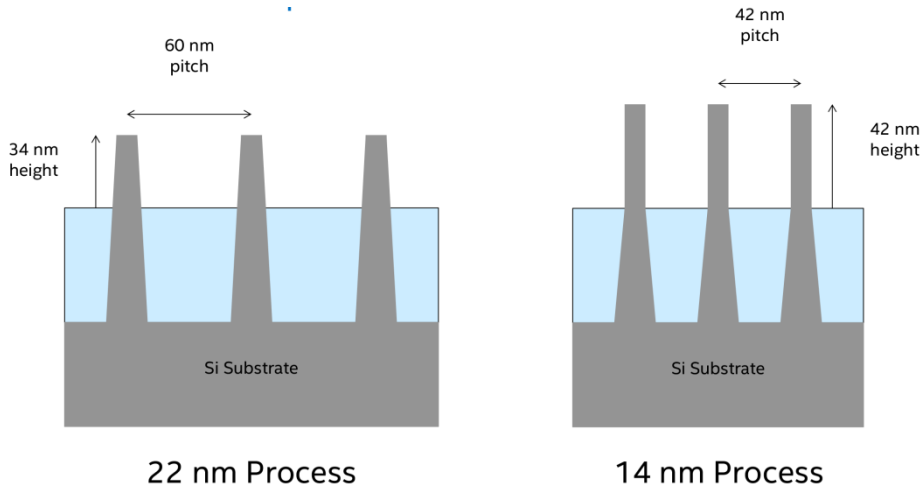
- **2003 FinFET on bulk substrate**

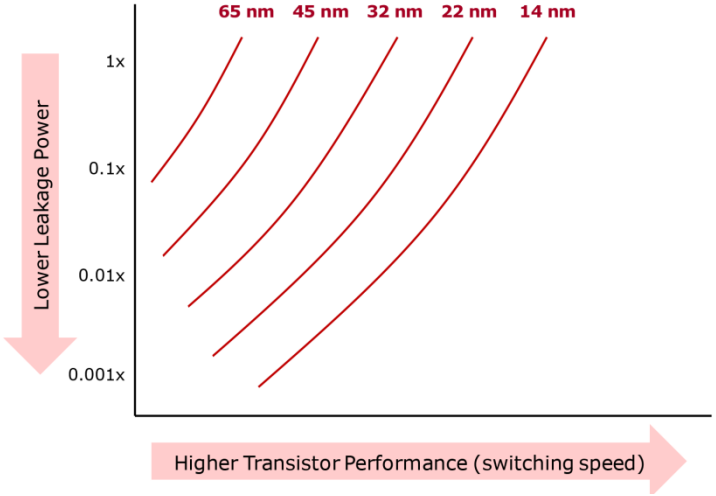
  T. Park et al. (Samsung) 2003 VLSI Symp. p. 135.



State-of-the-Art **14nm** FinFET





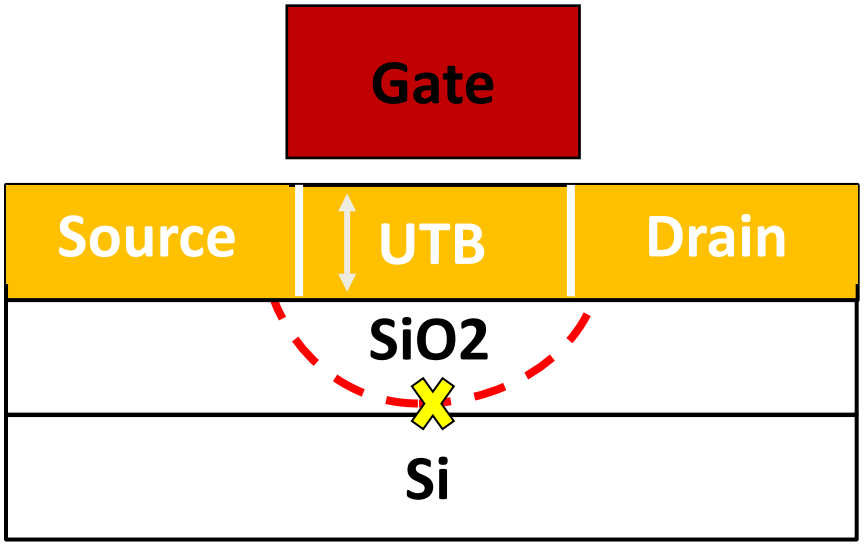


Taller and Thinner Fins for increased drive current and performance

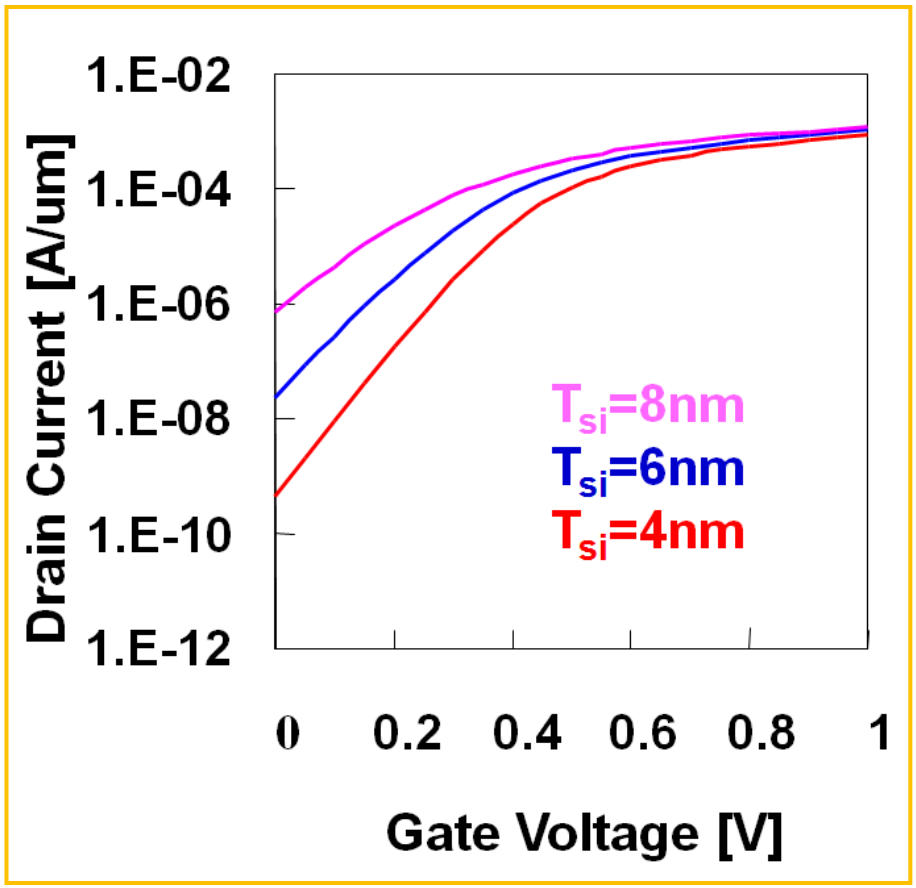
Source: Anandtech

2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI)



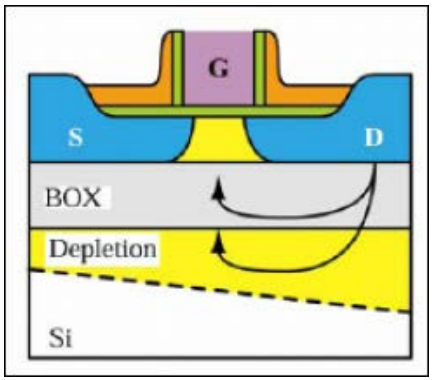
Y-K. Choi, IEEE EDL, p. 254, 2000

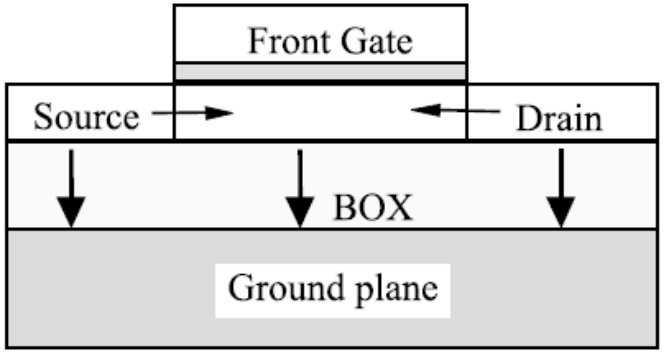


Ultra Thin Body on Thin Box

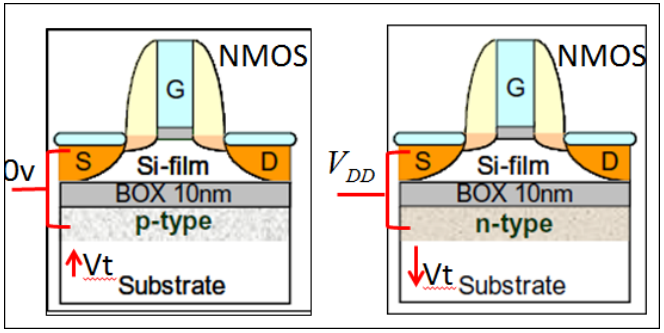
- Problem in thin BOX without Back-Plane: Depleted zone can extend under the BOX.
  - Increased short channel effects compared to Bulk devices.

- Benefit of Thin BOX with Back-Plane:
  - Doped & Biased Back Plane eliminates this depletion effect under the BOX.





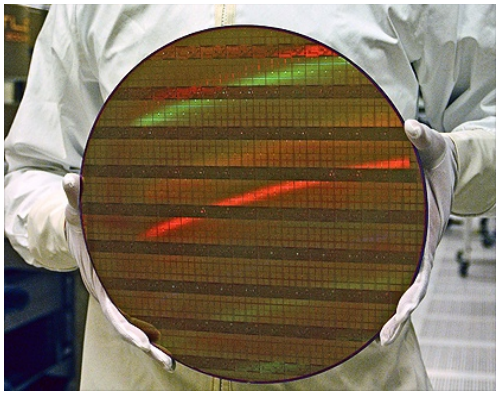
T. Ernst, Volume 46, Issue 3, March 2002, Pages 373–378



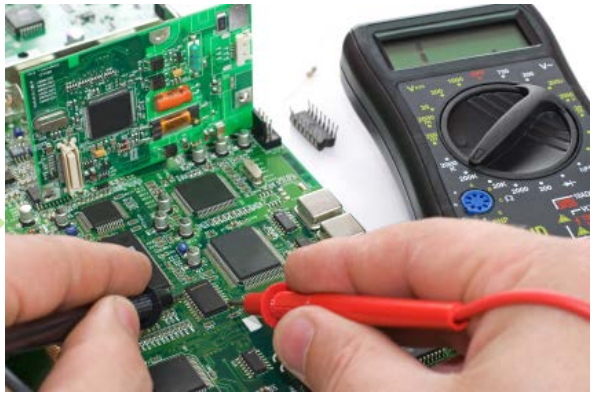
J.-P. Noel et.al,Solid State Device Research Conf, 2009

High K-$HfZrO_2$, EOT=1.4nm, Lg=32nm, L_{spacer}=10nm, $N_{bp}=10^{19}cm^{-3}$, Tsi=7nm

Compact Modeling or SPICE Modeling



Medium of information exchange



- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~μs*ec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

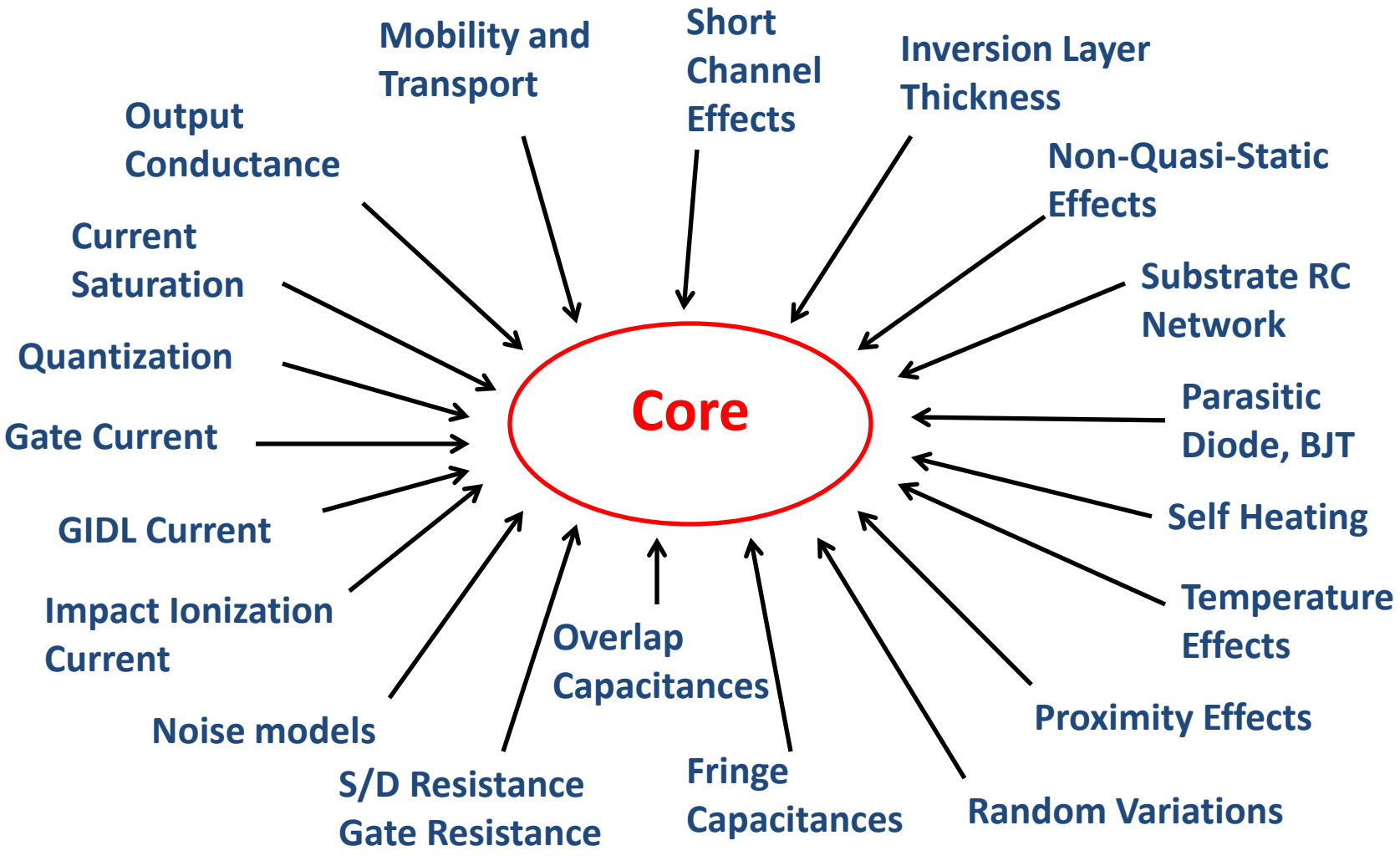
Industry Standard Compact Models

- Standardization Body – Compact Model Coalition
- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia
- CMC is by the industry and for the industry

BSIM-CMG and BSIM-IMG

- **Berkeley Short-channel IGFET Model**
- **First industry standard SPICE model for IC simulation**
- **Used by hundreds of companies for IC design since 1997**
- **BSIM FinFET model became industry standard in March 2012**

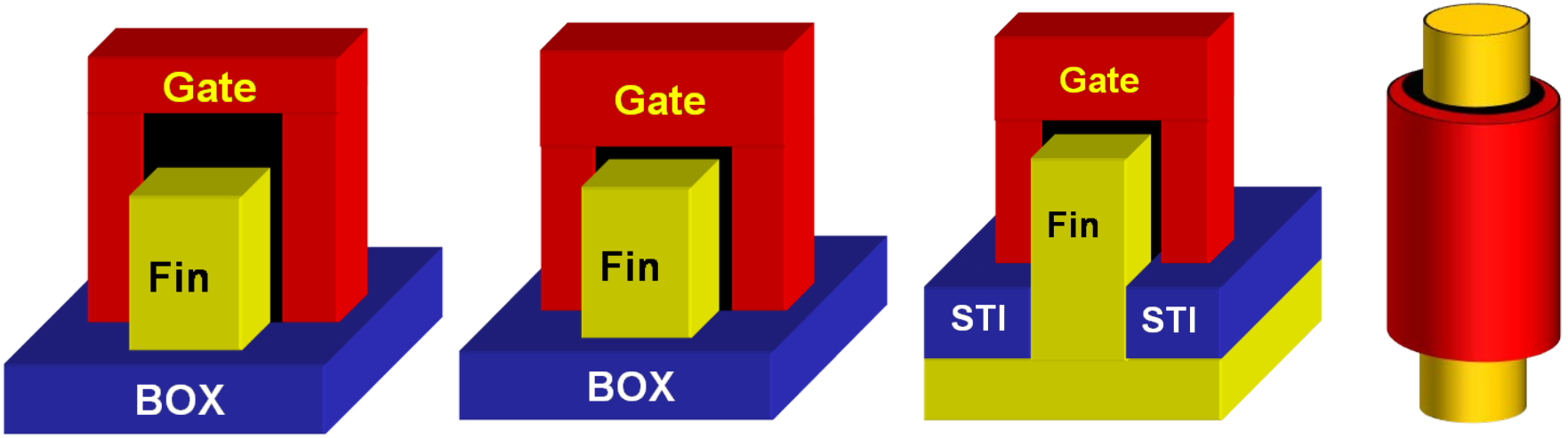
Compact Model is Art Based on Science



Y. S. Chauhan et.al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET," IEEE TED, 2014

Common-Multi-Gate Modeling

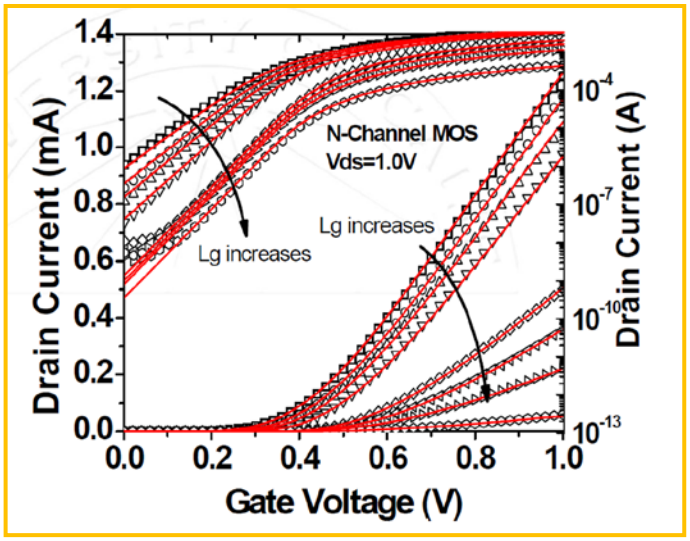
- Common Multi-gate (BSIM-CMG):
  - All gates tied together

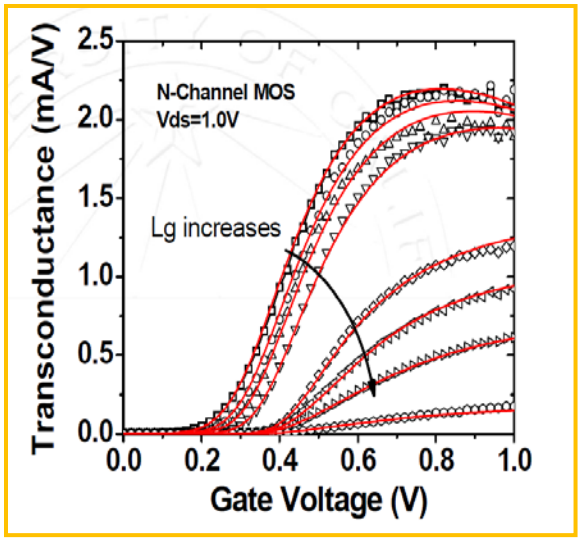


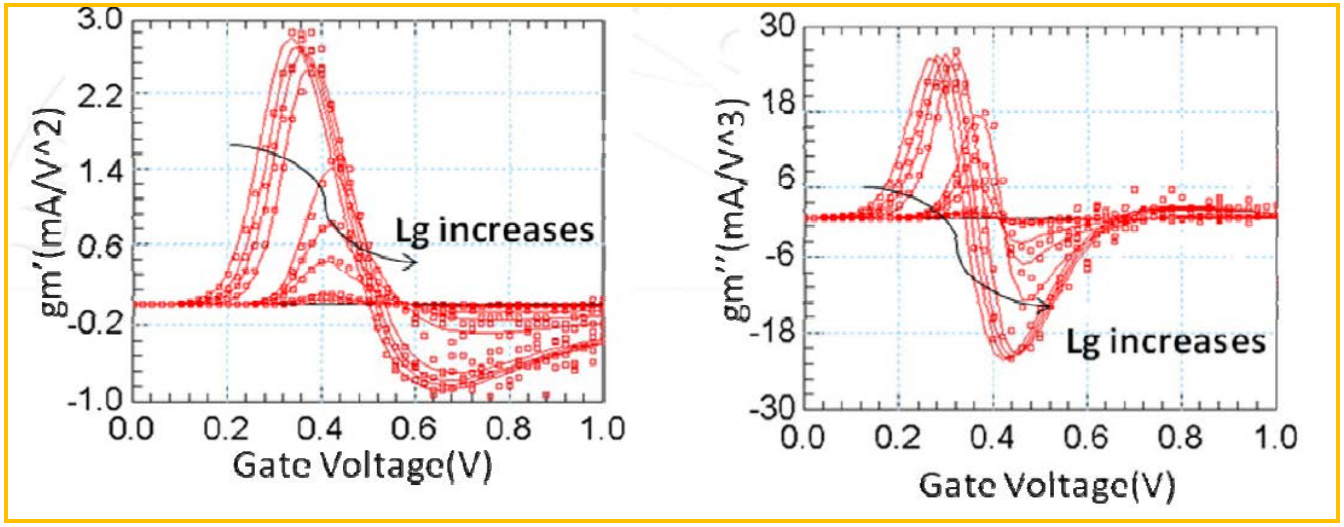
  - Surface-potential-based core I-V and C-V model
  - Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates

BSIM-CMG

Global fitting with 30nm–10μm FinFETs



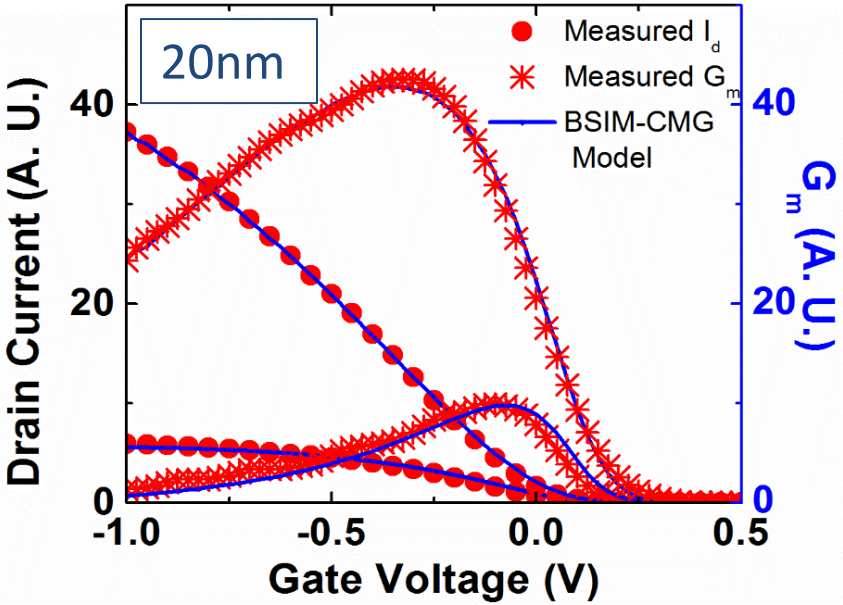


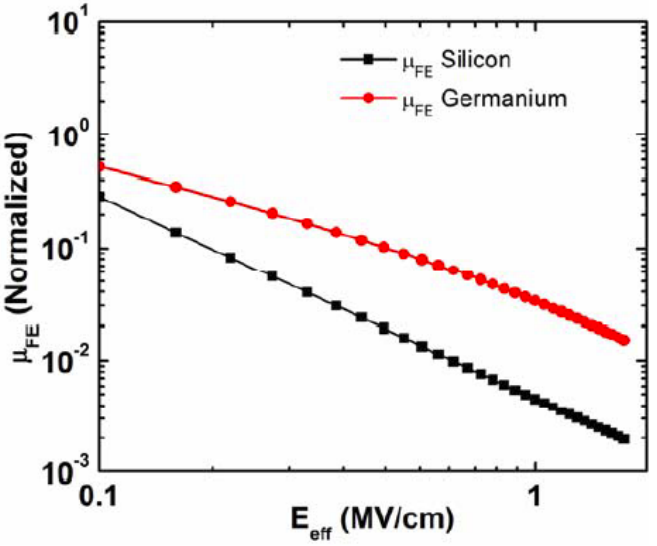


Modeling of Germanium FinFETs @10nm

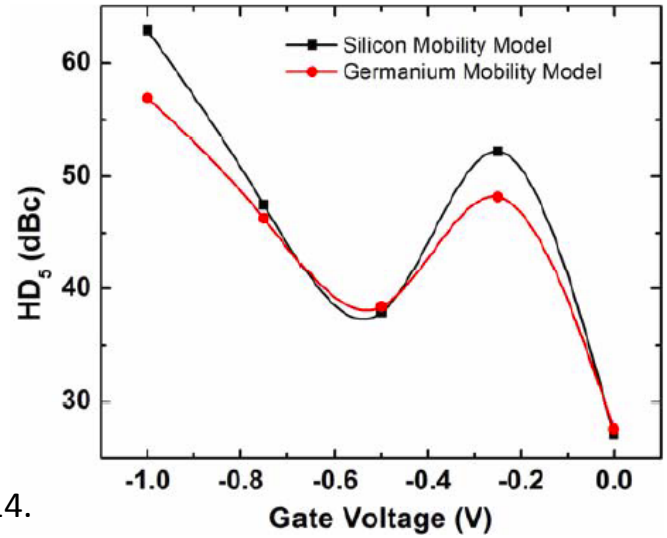
- Ge FinFET may be used in 10nm node for better P-FinFET.
- Industry standard BSIM FinFET model can now model Ge FinFET.
- Early availability of a unified Si/Ge FinFET model facilitates technology-circuits co-development.

Verification of Ge FinFET Model





- Due to the lower *m** of holes in Ge the charge-centroid is farther away from the oxide interface resulting in a weaker SR scattering.
- Ge mobility has a weaker dependence on E_{eff} up-to ~0.5 MV/cm as the impact of SR scattering is only seen at much higher E_{eff} in Ge as compared to Si.

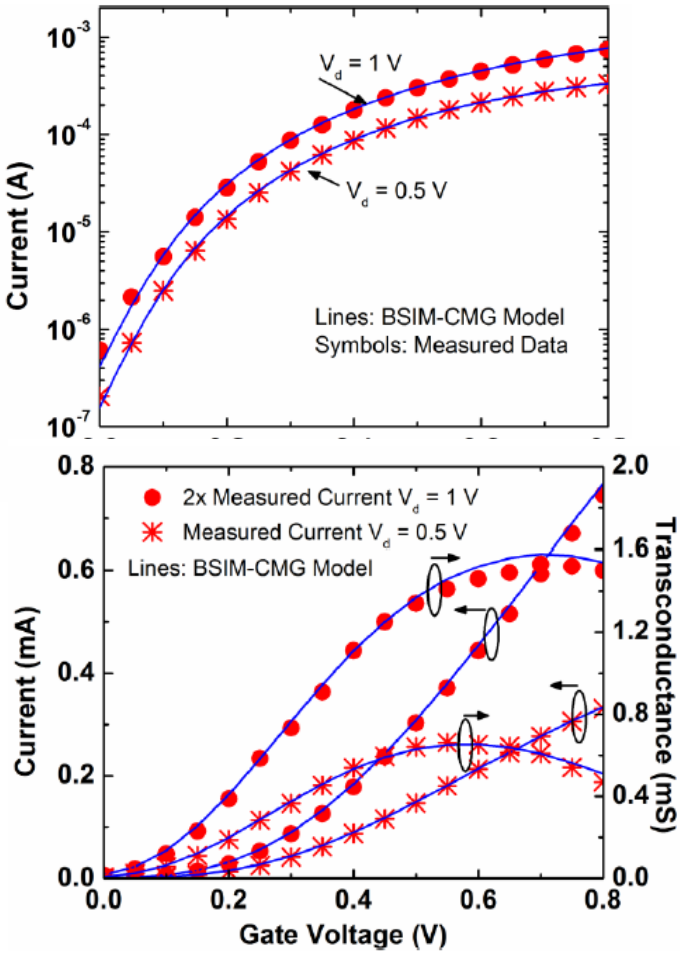


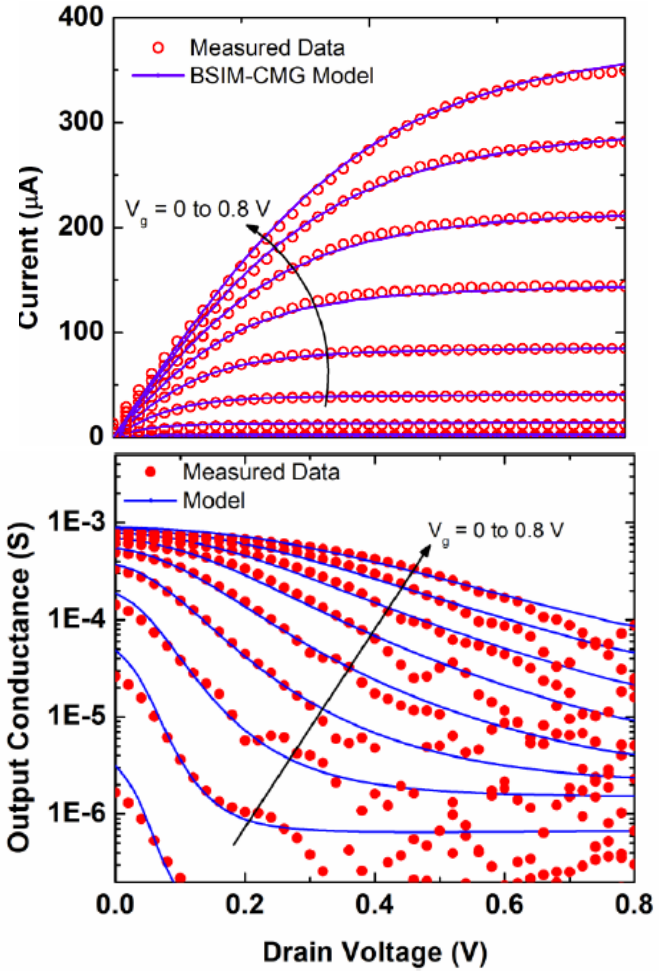
S. Khandelwal et. al., "Modeling 20nm Germanium FinFET with the Industry Standard FinFET Model", IEEE Electron Device Letters, Vol. 35, Issue 7, July 2014.

Modeling of InGaAs FinFET @10nm

L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.

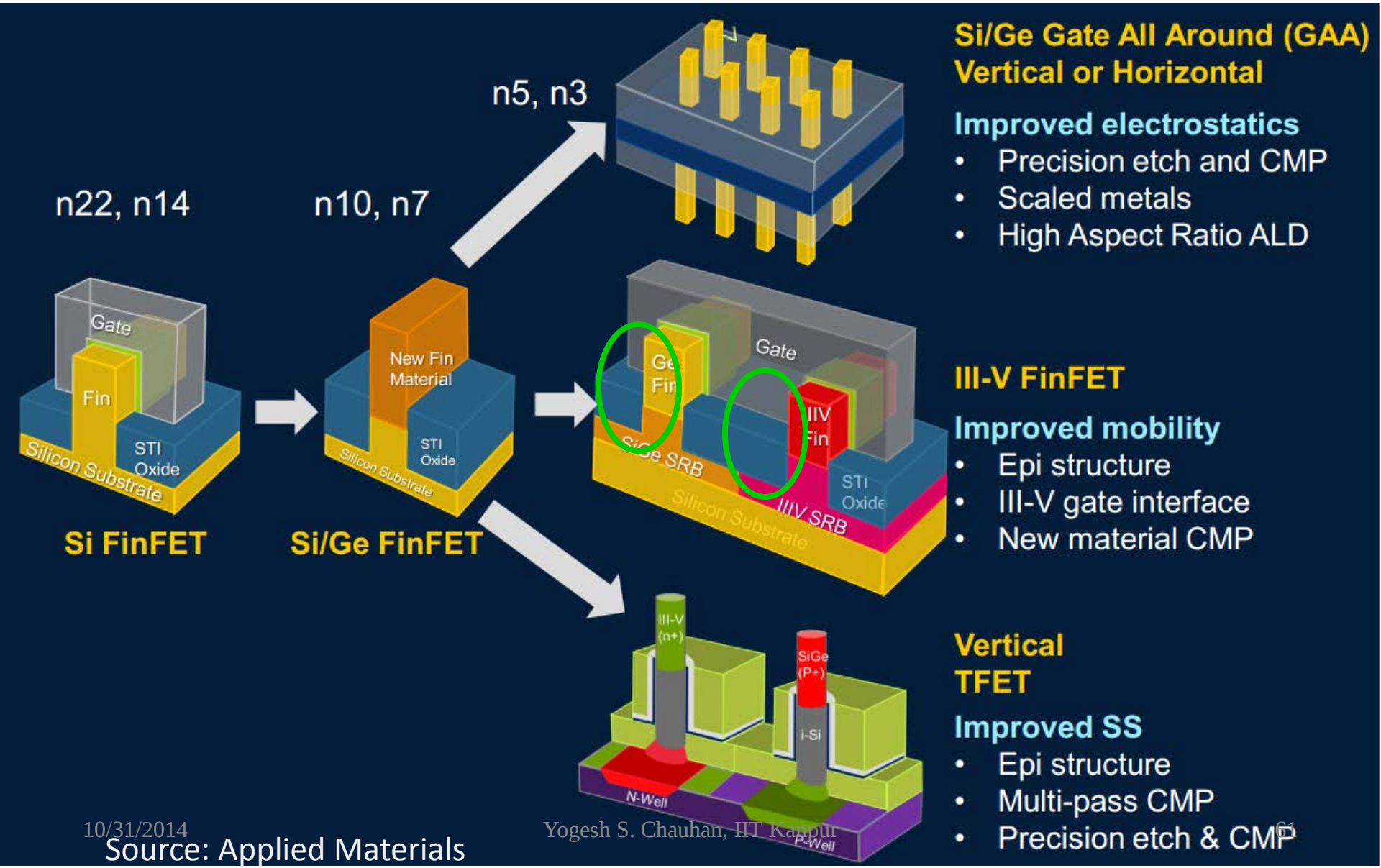
Data from: J. J. Gu et al. IEDM 2012





S. Khandelwal et. al., "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Workshop on Compact Modeling, Washington D.C., USA, June 2014.

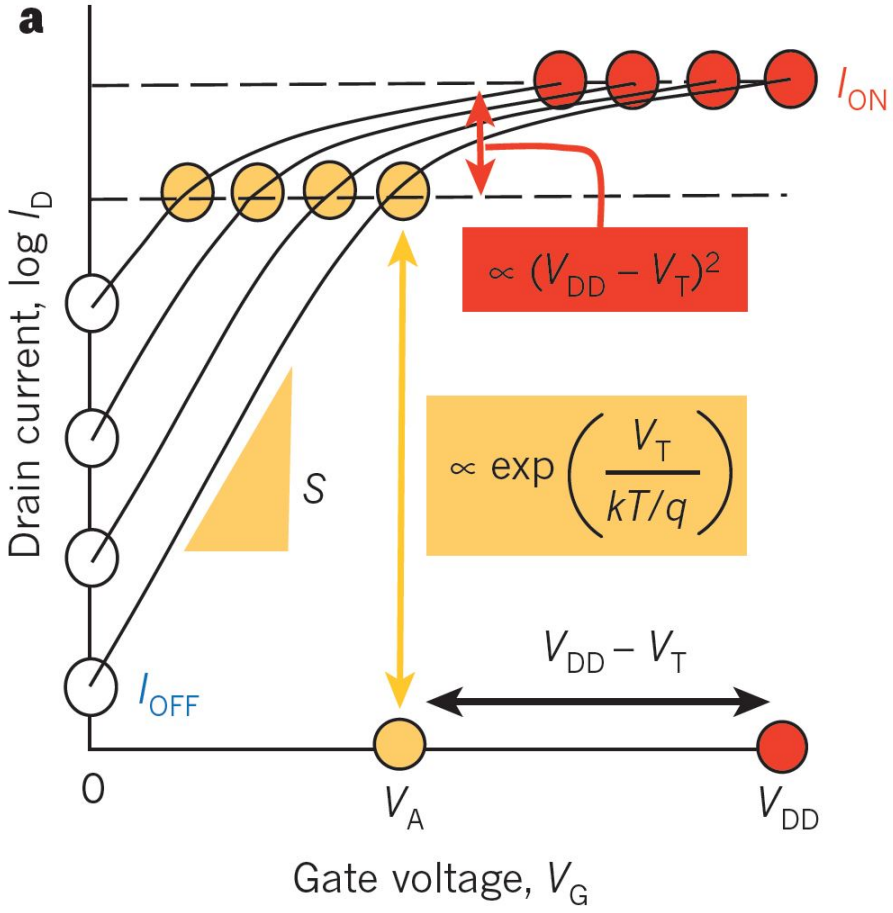
Transistor Pathway

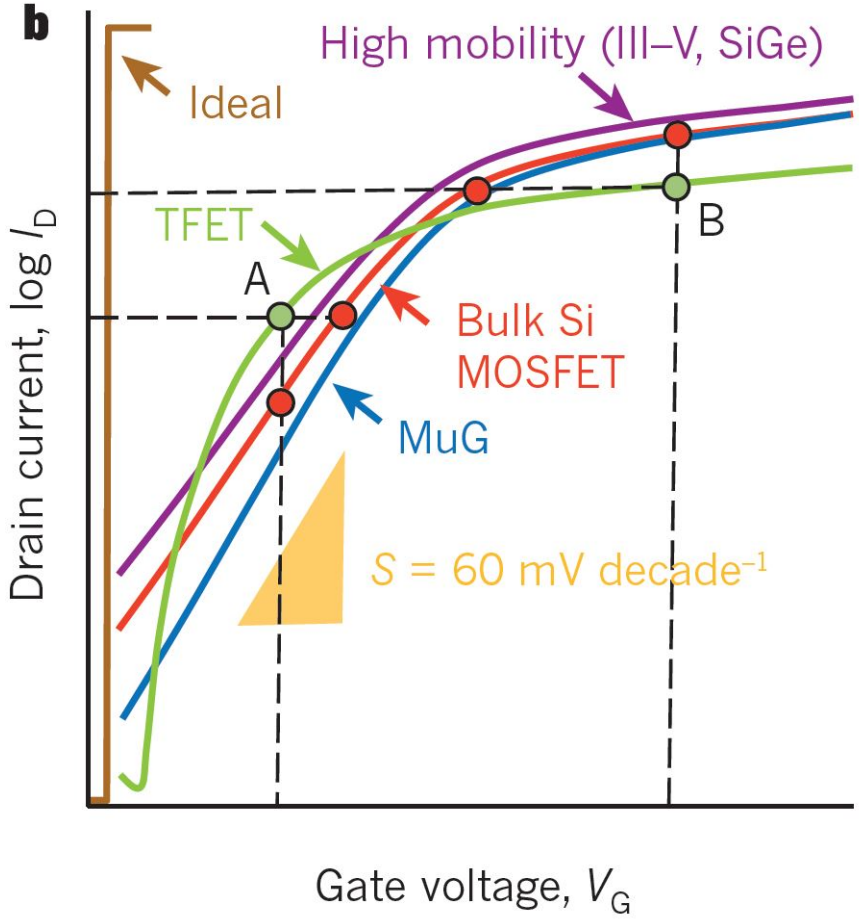


Source: Applied Materials

Future devices – Beyond CMOS

Power challenge





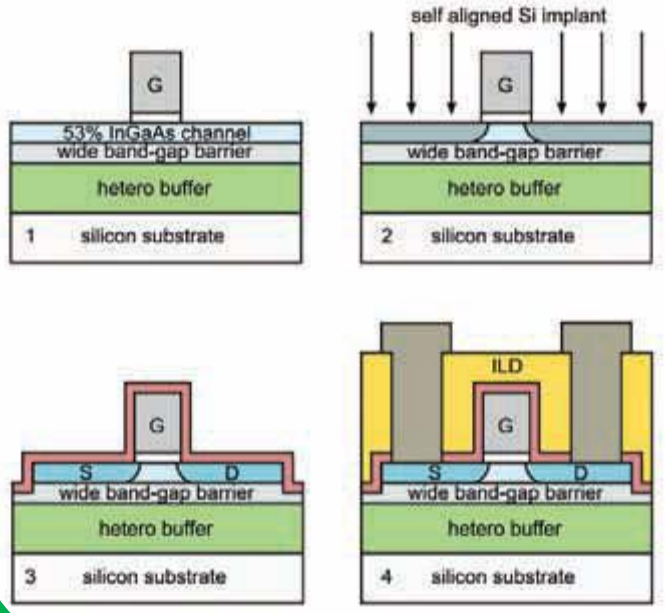
Scaling down of both the V_{DD} and V_T maintains same performance (I_{ON}) by keeping the overdrive (VDD - VT) constant.

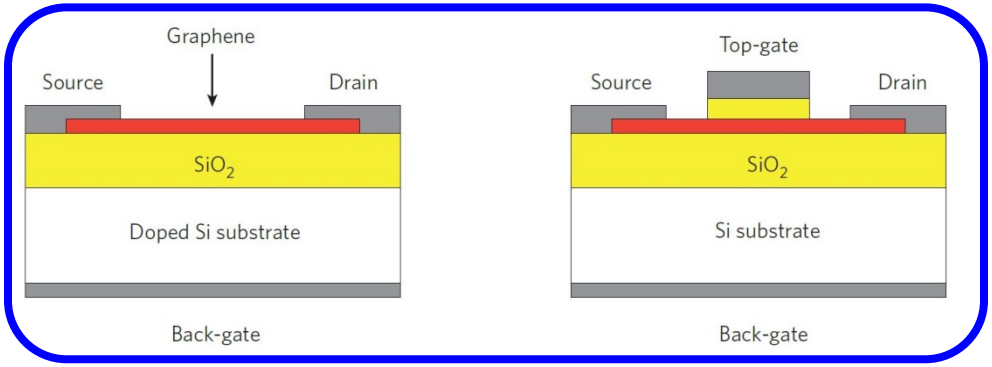
Adrian Ionescu et al., Nature 2011

Future devices – Beyond CMOS

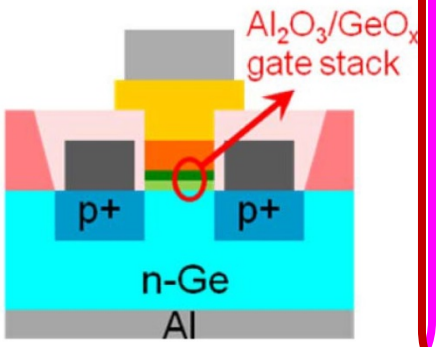
- Alternate channel material

III-V Transistor (InGaAs)

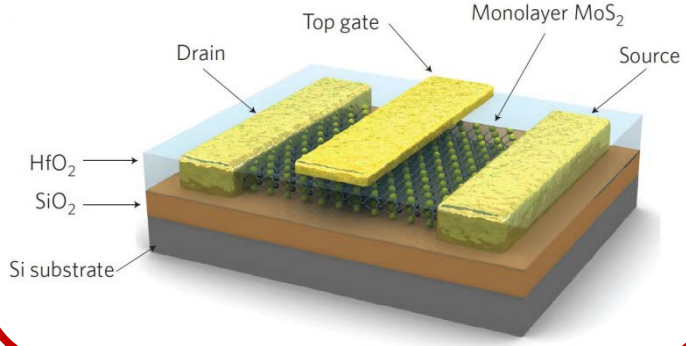




Ge PMOSFET



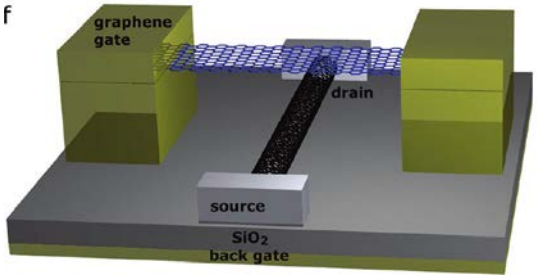
MoS_2 Transistor

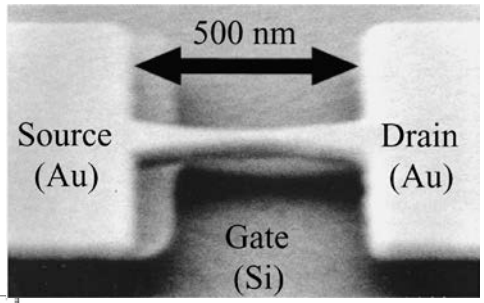


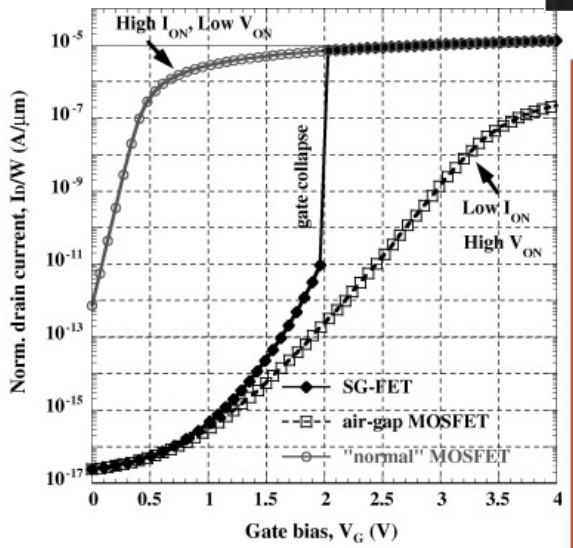
Source:
Sematech
NATURE NANOTECHNOLOGY | VOL 6 | MARCH 2011

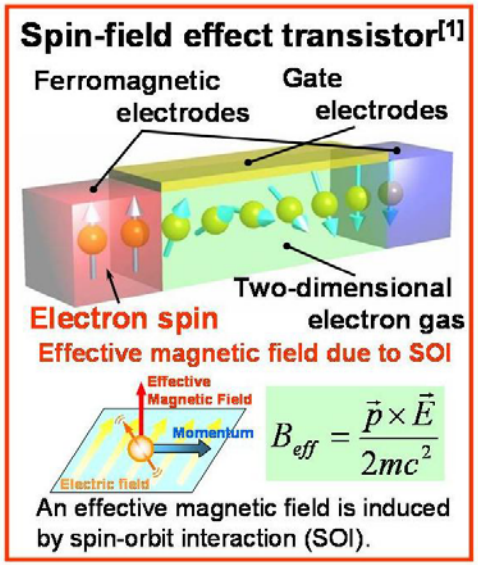
Future devices – Beyond CMOS

Suspended Gate/body FET

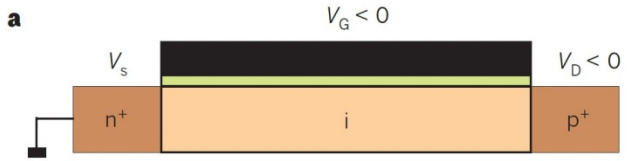




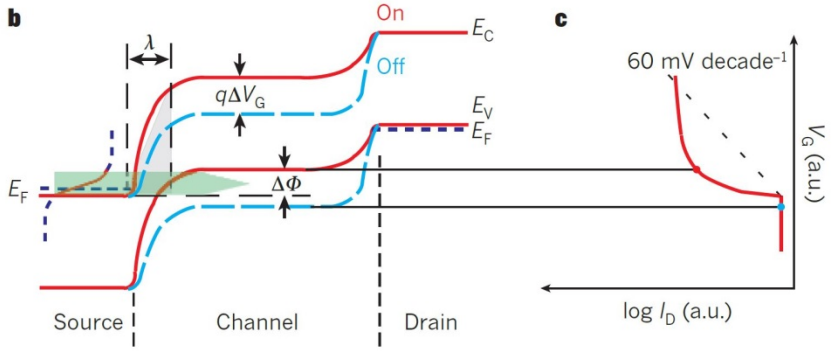


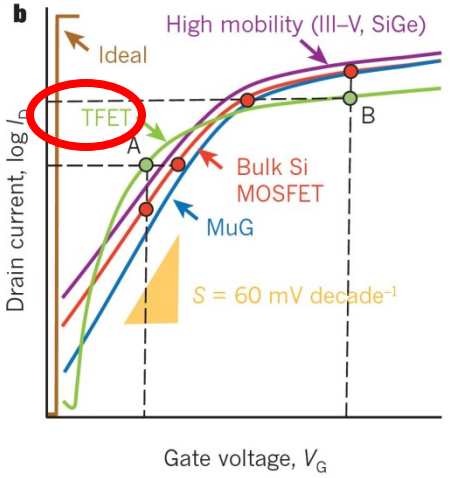


Magnetic devices



Tunnel FET





My Two years at IIT Kanpur

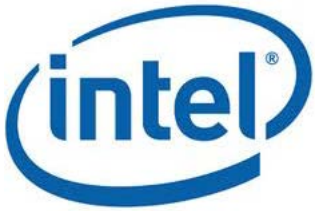
- Received IBM Faculty Award (2013)
- Awarded Ramanujan Fellowship (2012)
- Group: Postdoc–1, Ph.D.–7, M.Tech–6, R.A.–4
- Funding > Rs. 3crore
  - Device Characterization Lab (1.75crore)
  - Upgraded computational infra. (50Lac)
- Collaboration: >20 companies/labs

Publications:

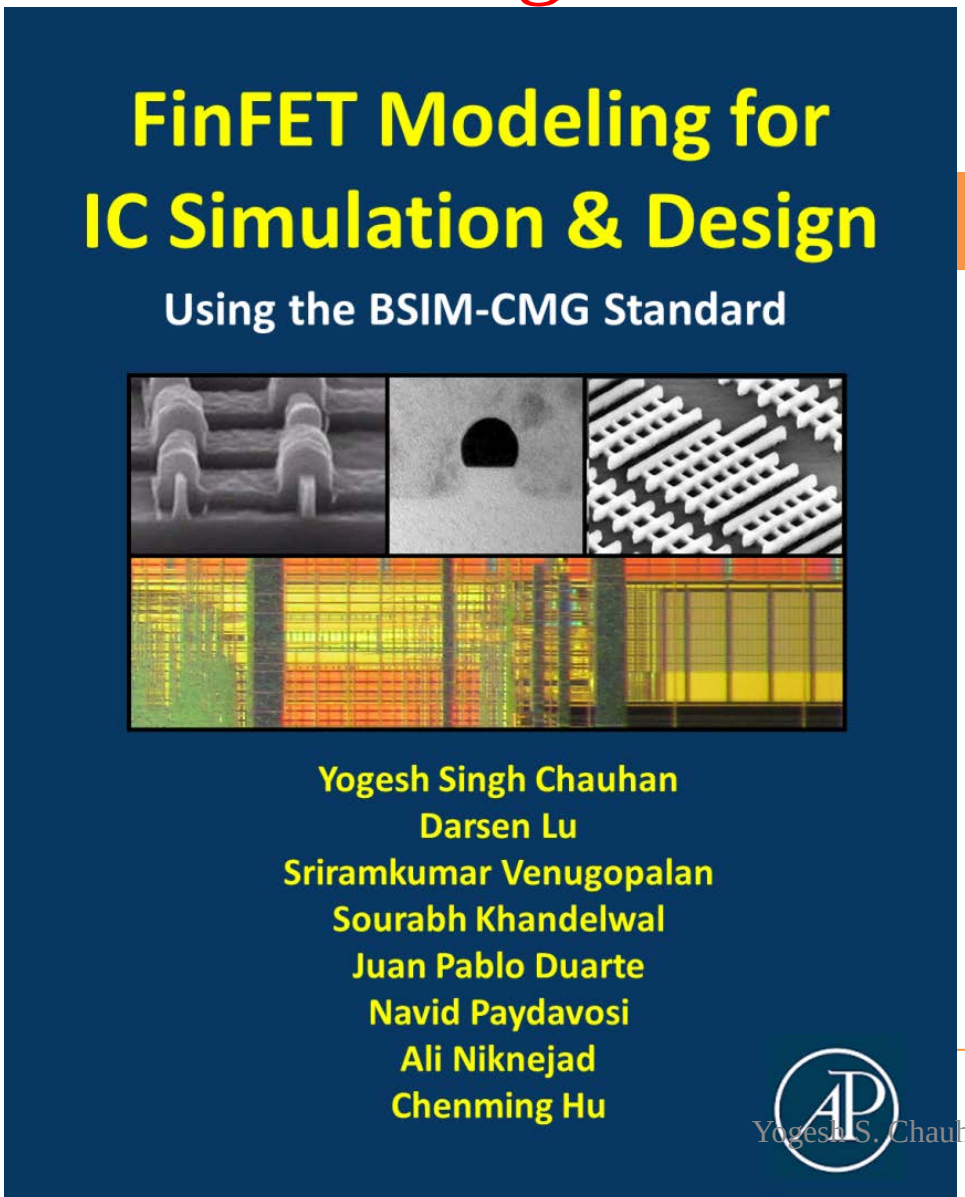
10 journal papers, 13 conference papers,
10 invited talks

Joint Development & Collaboration

- Working closely with universities/companies on model development and support



FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



Chapters

Summary

- Future is beyond your imagination.
- Challenges
  - Technology – Hardware and Software
  - Need Innovation
- Opportunities
  - Entrepreneurship
  - Research
  - Jobs (private/public)
- Knowledge economy

Check my homepage!

- Recent publications
- "Modeling of GaN based Normally-off FinFET", accepted in IEEE Electron Device Letters, 2014.
- "BSIM6: Analog and RF Compact Model for Bulk MOSFET", IEEE Trans. on Elec. Devices, Feb. 2014.
- "A Robust Surface-Potential-Based Compact Model for GaN HEMT IC Design", IEEE Trans. on Elec. Devices, Oct. 2013.
- "Extraction of Isothermal Condition and Thermal Network in UTBB SOI MOSFETs", IEEE Electron Device Letters, Sept. 2012.
- "BSIM-IMG: A Compact Model for Ultra-Thin Body SOI MOSFETs with Back-Gate Control", IEEE Trans. on Elec. Devices, Aug. 2012.
- "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Nanotech, Washington D.C., USA, June 2014.
- "High Voltage LDMOSFET Modeling using BSIM6 as Intrinsic-MOS Model", IEEE PrimeAsia, Visakhapatnam, Dec. 2013.