FinFET Modeling for 10nm and beyond - Si, Ge and III-V channel

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Acknowledgements

- BSIM Team
  - Chenming Hu
  - Juan Pablo Duarte
  - Darsen Lu
  - Sourabh Khandelwal
- My students
  - Chandan Yadav
  - Avirup Dasgupta
  - Tapas Dutta

About me

- Joined IIT Kanpur in 2012
- Awarded Ramanujan Fellowship (2012)
- Received IBM Faculty Award (2013)
- Funding
  - Device characterization laboratory (1.75crore)
  - Upgraded computational infra.
- Group: Postdoc–3, Ph.D.–9, MTech–8, R.A.–3
- Collaboration: >25 companies/universities

Publications in last 3 years:

- 17 journal papers
- 18 conference papers

Lab website – http://www.iitk.ac.in/nanolab

Joint Development & Collaboration

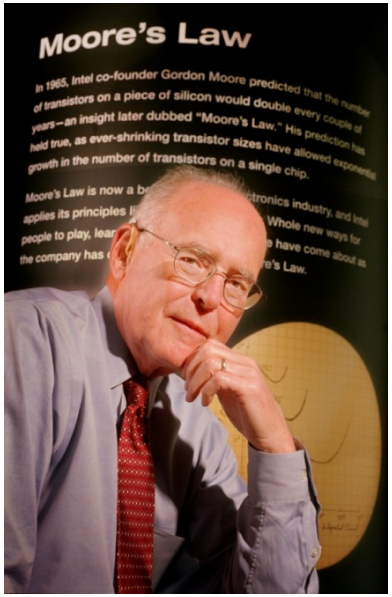
- Working closely with universities/companies on model development and support

Outline

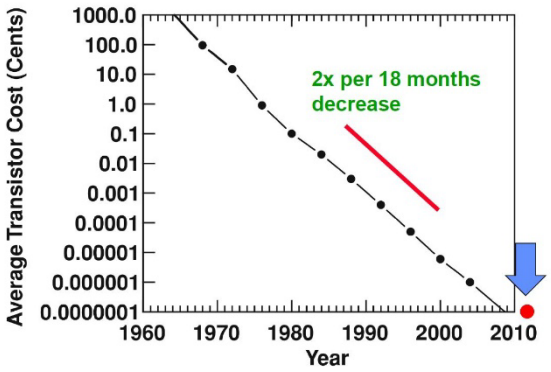
- Bulk MOSFET and Scaling
- FinFET and Compact Modeling
- Unified Compact Model for arbitrary geometry
- What next?

IC industry for >40 years

- Closer distance between elements – *Pitch*
  - *Faster* signal transfer and processing rate
- For the same Chip size (or cost), *more functionality*
- *Mass production* – Wafer size doubled every 10years.
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - *Price* of memory/logic gates has dropped 100 million times.
- The primary engine that powered the proliferation of electronics is "*miniaturization*".
- More circuits on each wafer → cheaper circuits.
- Miniaturization is key to the improvements in *speed and power consumption* of ICs.

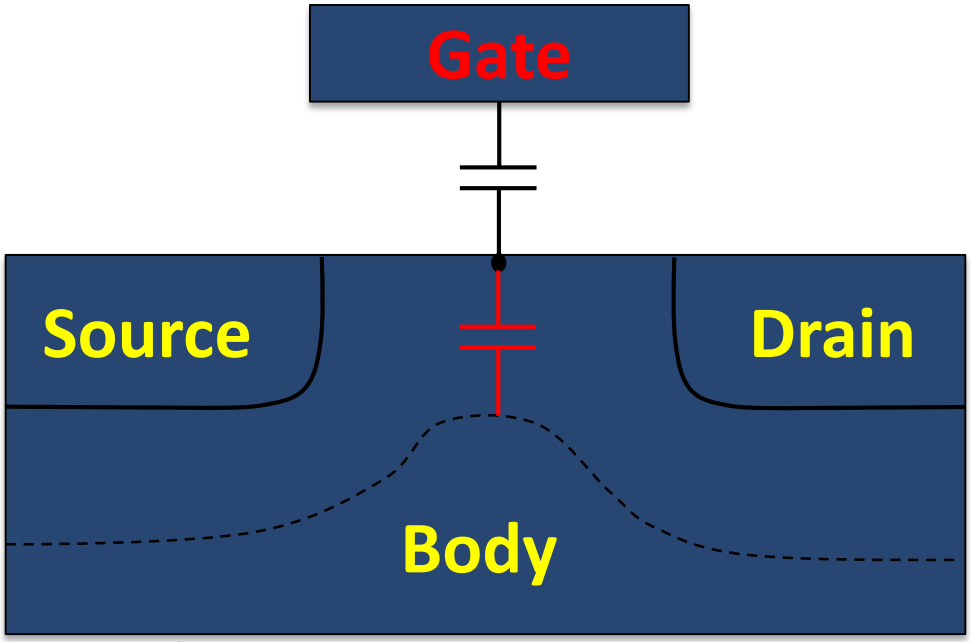


1 Nano-$ / Transistor!

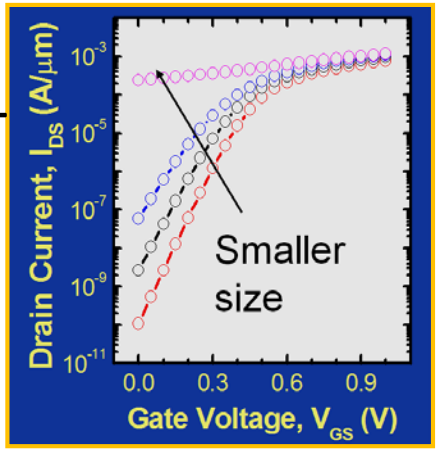


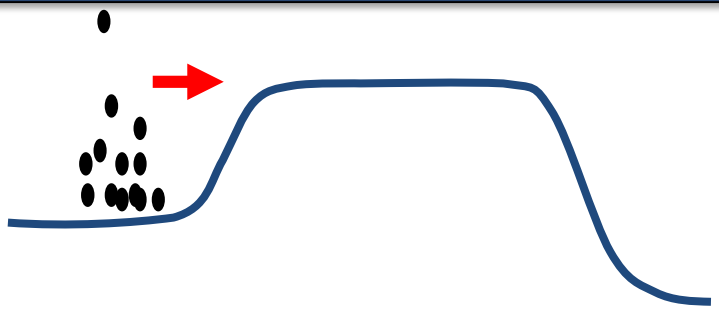
It's not technology! → It's economy.

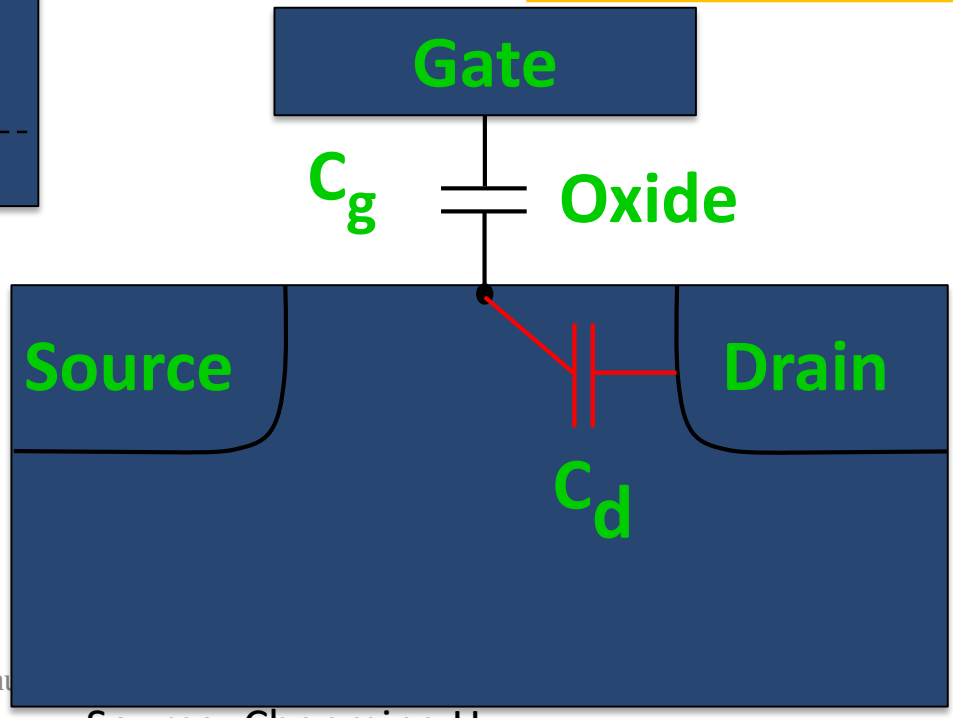
Why divorce after 40 years?



Short Channel –
Big Problem



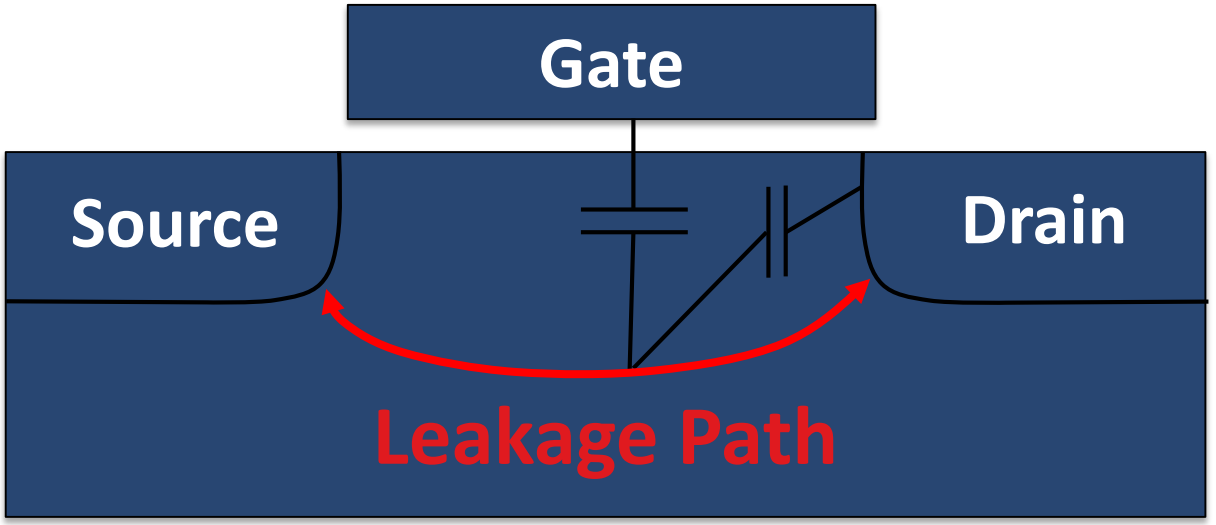




- $Q_G = Q_i + Q_b$
- Charge sharing

Source: Chenming Hu

Making Oxide Thin is Not Enough



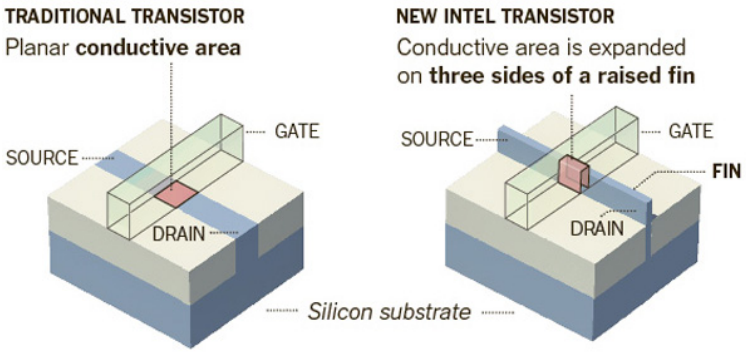
Gate cannot control the leakage current paths that are far from the gate.

MOSFET in sub-22nm era

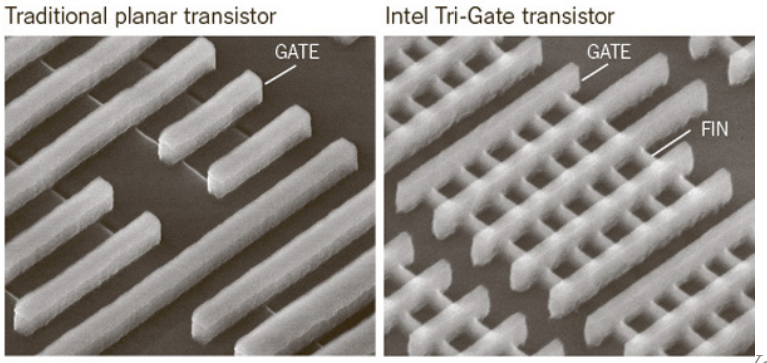
FinFET

New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.



The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.



Source: Intel

THE NEW YORK TIMES

NY Times

FDSOI

Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices

New platform enables planar FD technology, the only planar solution to sustain Moore's law

From the Semicon West trade show, San Francisco, July 12, 2010 – The Soitec Group (Euronext Paris), the world's leading supplier of engineered substrates for the microelectronics industry, announced today that the company is ready with the Ultra-Thin Buried Oxide (UTBOX) extension to its Ultra-Thin (UT) silicon-on-insulator (SOI) platform, thereby providing a robust substrate solution for chip designers tackling the performance, power and density challenges of mobile consumer devices. Fully Depleted (FD) planar body transistors are now recognized as the right path on the CMOS roadmap for the 22nm generation and beyond. With FD planar transistor technology on UTBOX wafers, chip designers can enhance their usual design flows and techniques. High-volume capacity is available for the 22nm node at Soitec's manufacturing sites in France and Singapore.

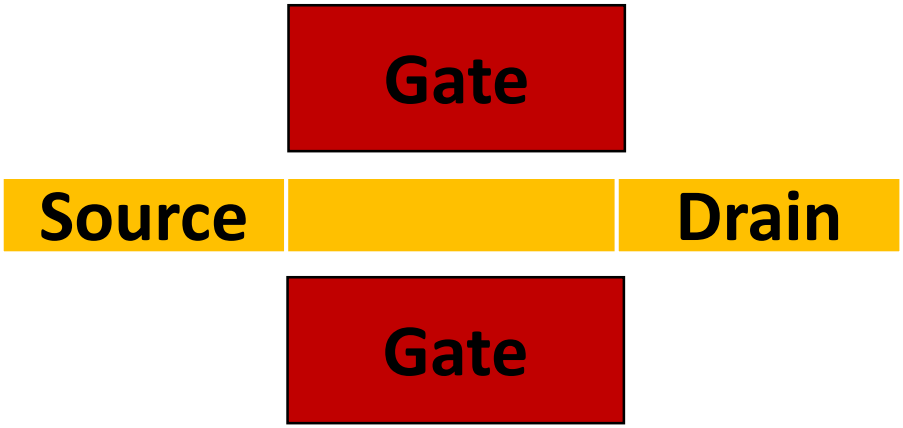
"Soitec is ready with the UTBOX wafers for planar FD architectures: the infrastructure, the process maturity, yield and the capacity are all in place to support demand," said Soitec president and chairman, André-Jacques Auberton-Hervé. "Industry leaders confirm that FD planar technology is the right choice for mobile consumer products, which need higher performance without compromising power. Our UTBOX offering shows the critical role our materials play as the starting point for energy-efficient, state-of-the-art electronics."

SOITEC

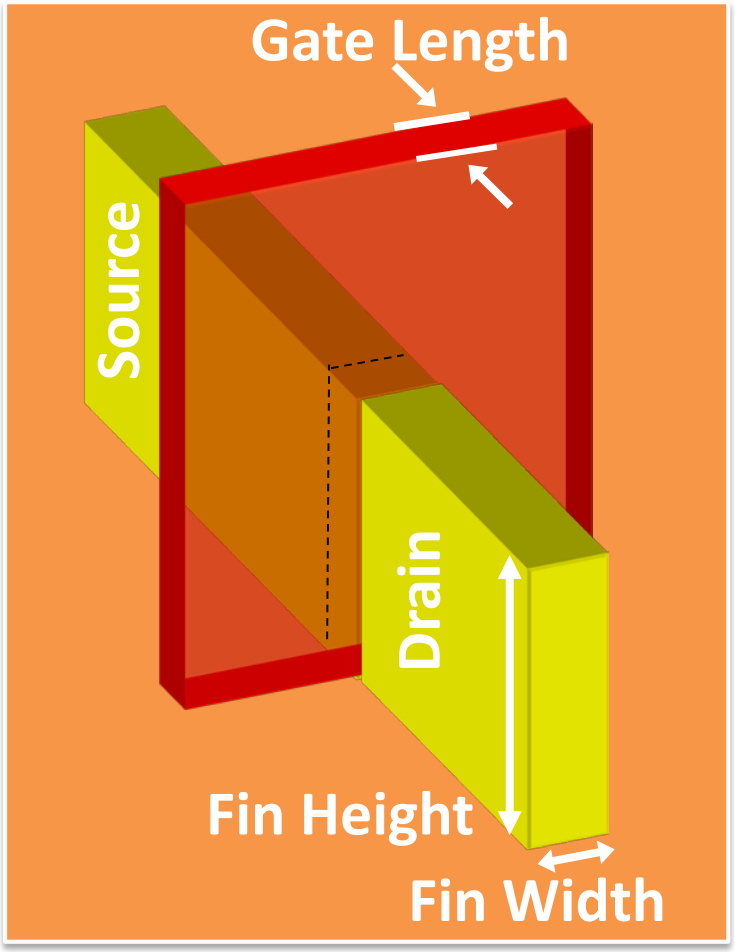
One Way to Eliminate Si Far from Gate

Thin body controlled

By multiple gates.

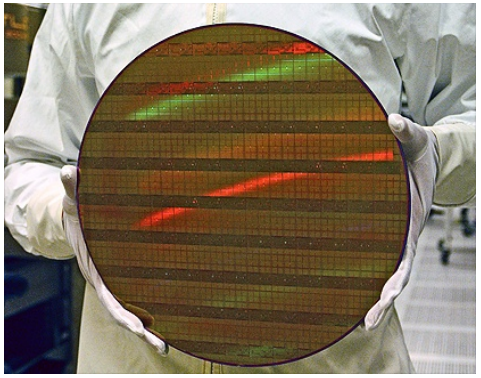


FinFET body is a thin Fin.

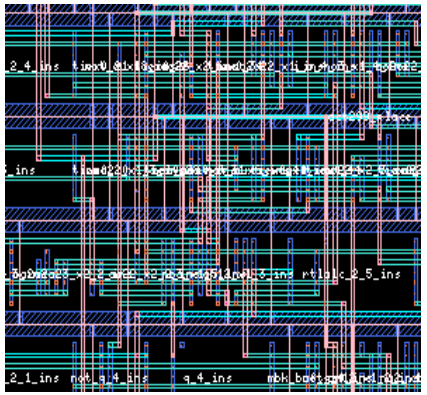


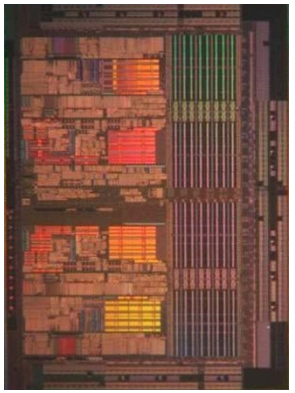
N. Lindert et al., DRC paper II.A.6, 2001

Transistor Compact Model



Is the vehicle of information transfer





Technology → **EDA / Design**

- **Fast**

  ~ 10µs / bias point

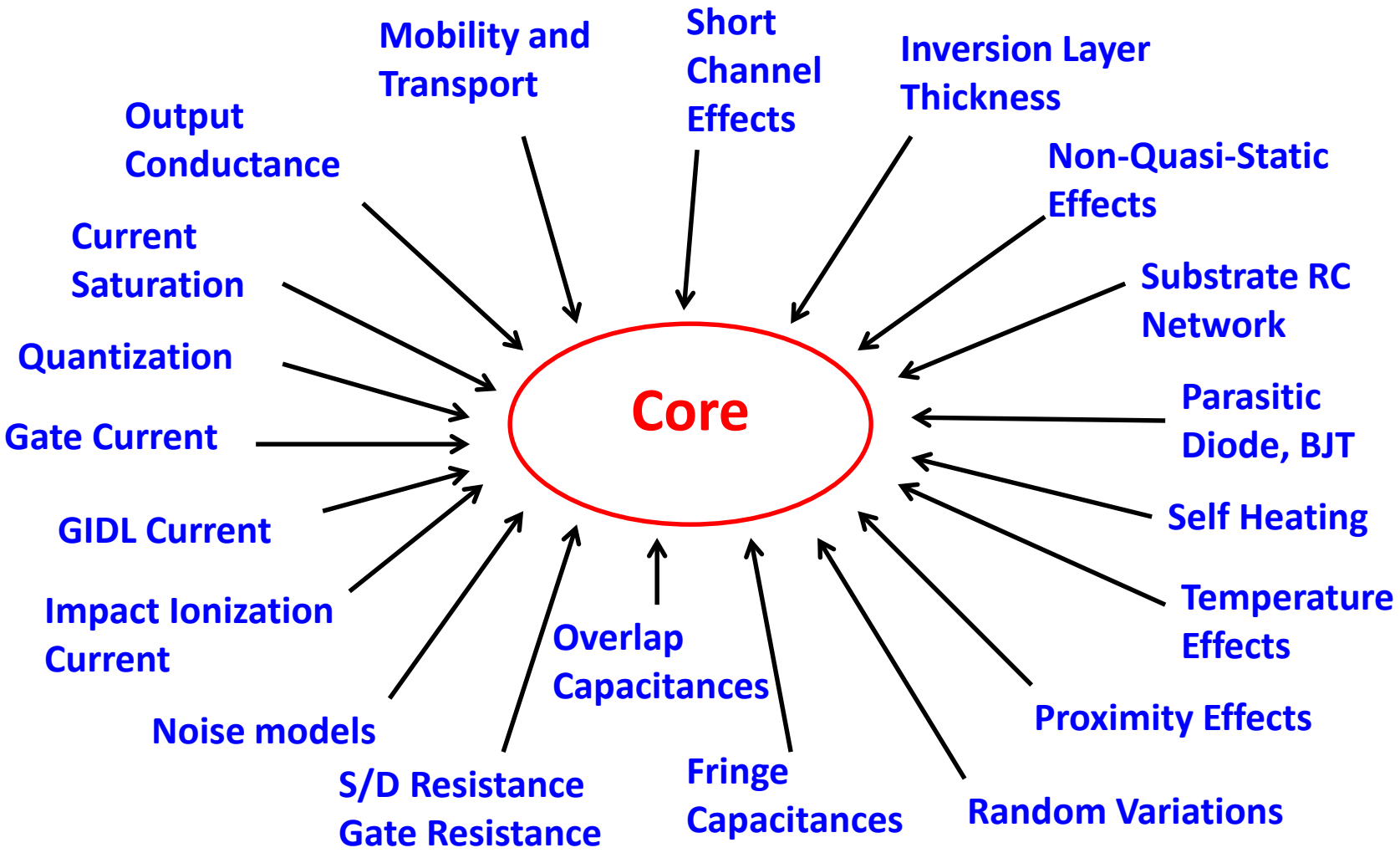
- **Accurate**

  ~ 1% error

- **Robust**

  Crash free for all circuits.

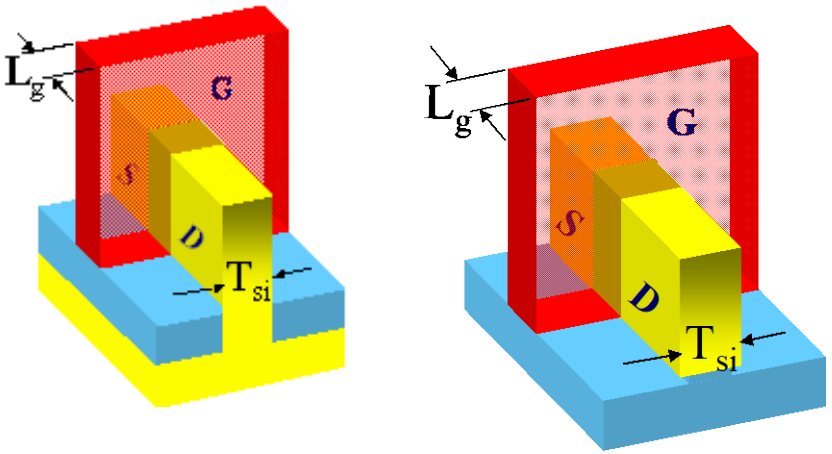
Compact Model is Art Based on Science



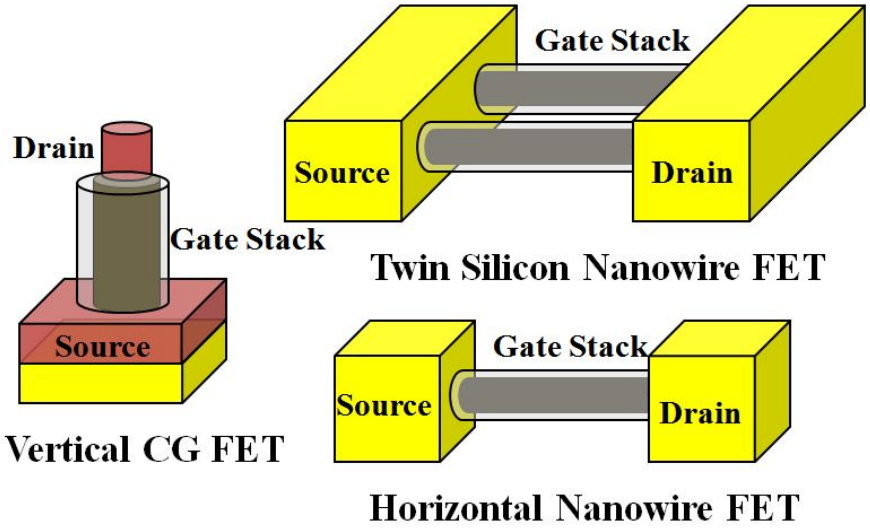
Y. S. Chauhan et.al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET," IEEE TED, 2014.

BSIM-CMG: Industry standard FinFET model

- Selected as Industry standard 2012

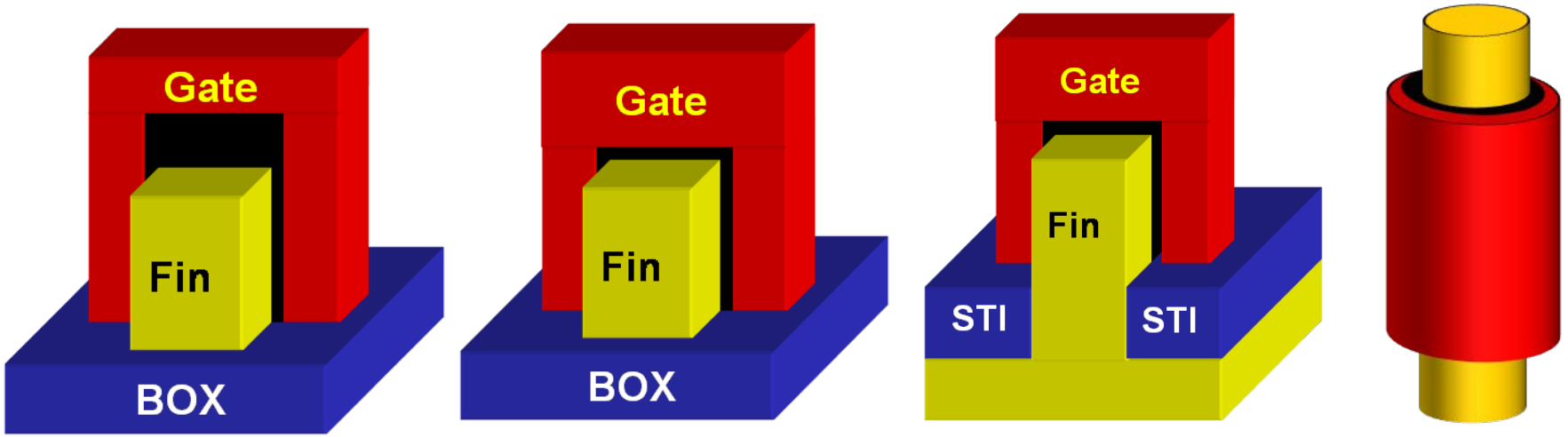


FinFETs on Bulk and SOI Substrates



BSIM-CMG

- Common Multi-gate (BSIM-CMG):
- All gates tied together



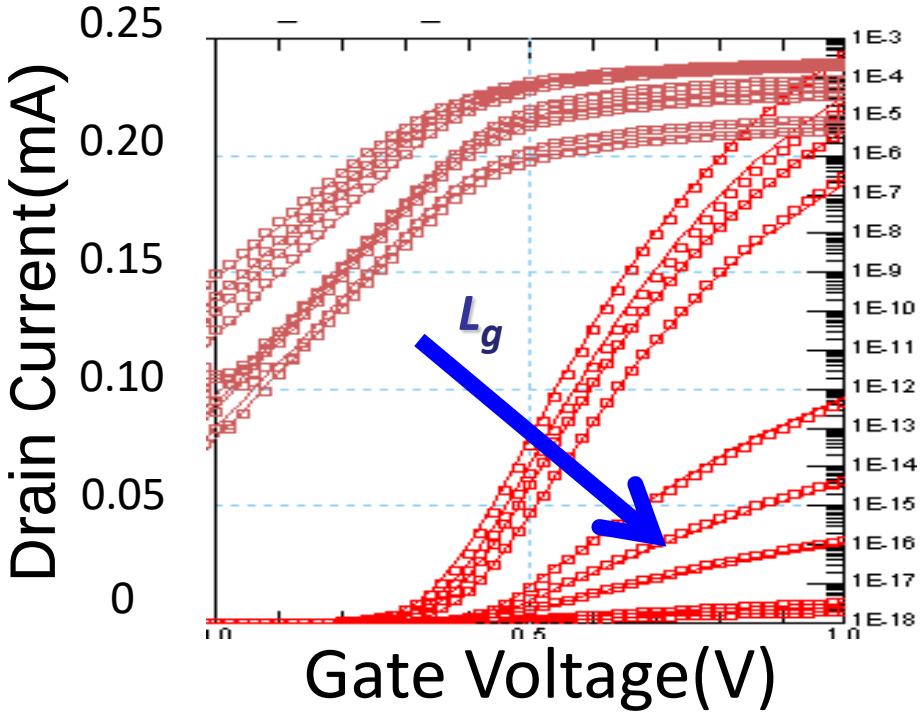
- Surface-potential-based core I-V and C-V model
- Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates

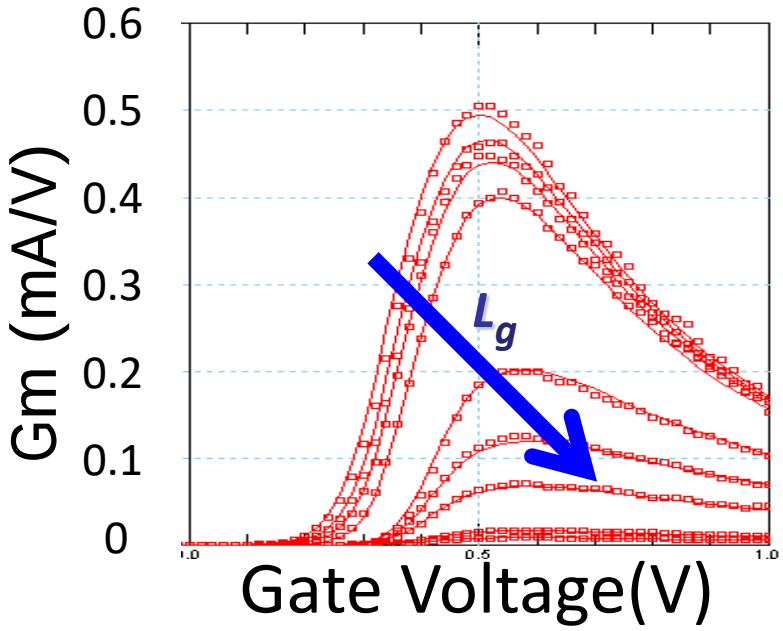
Y. S. Chauhan et. al., Workshop on Compact Modeling, 2011, Boston.

Verification: 30nm to 10µm FinFETs

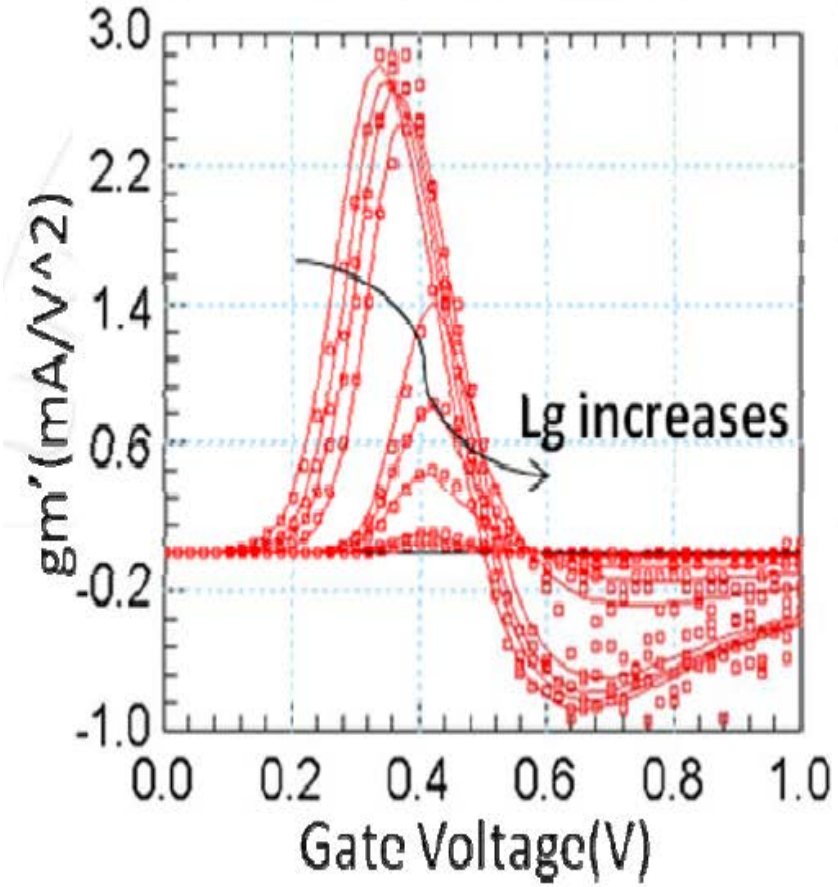
Each curve is for one Lg

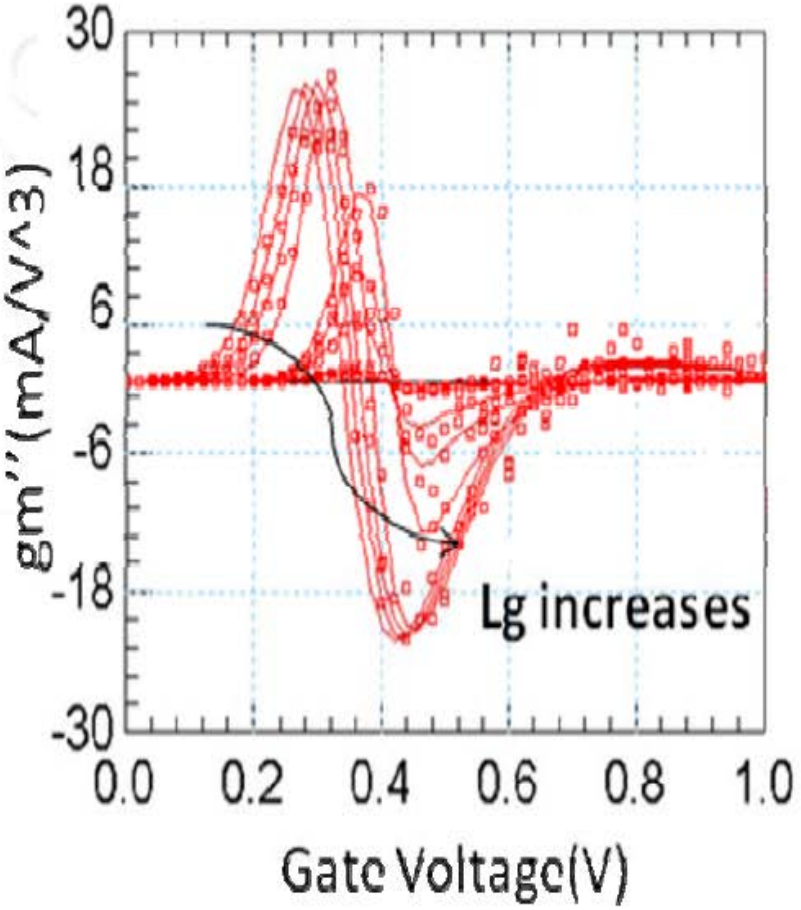
Symbols: Data; Lines: BSIM-CMG Model



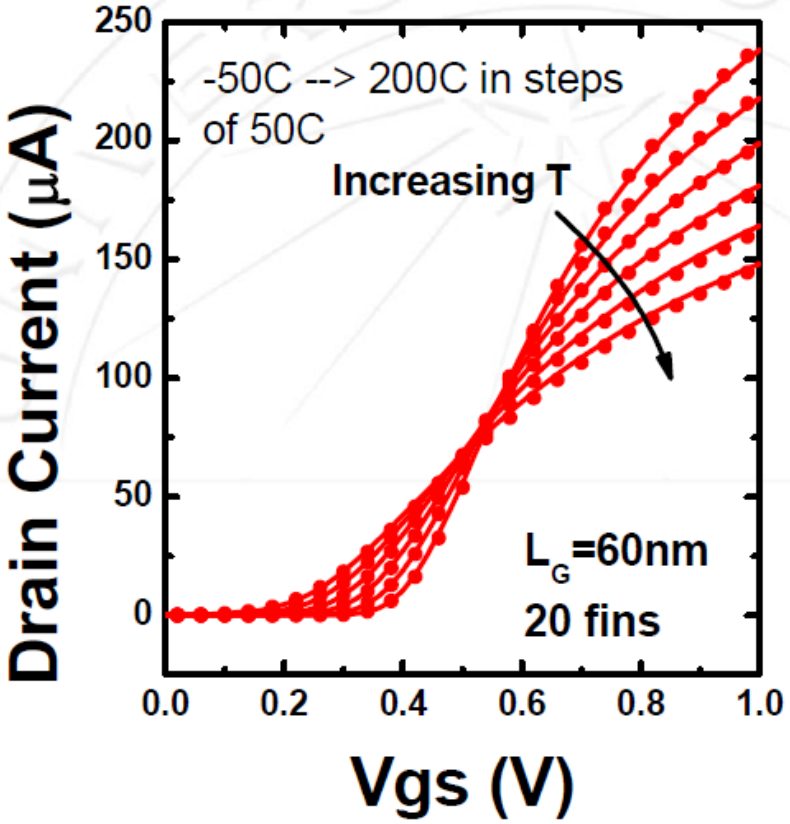


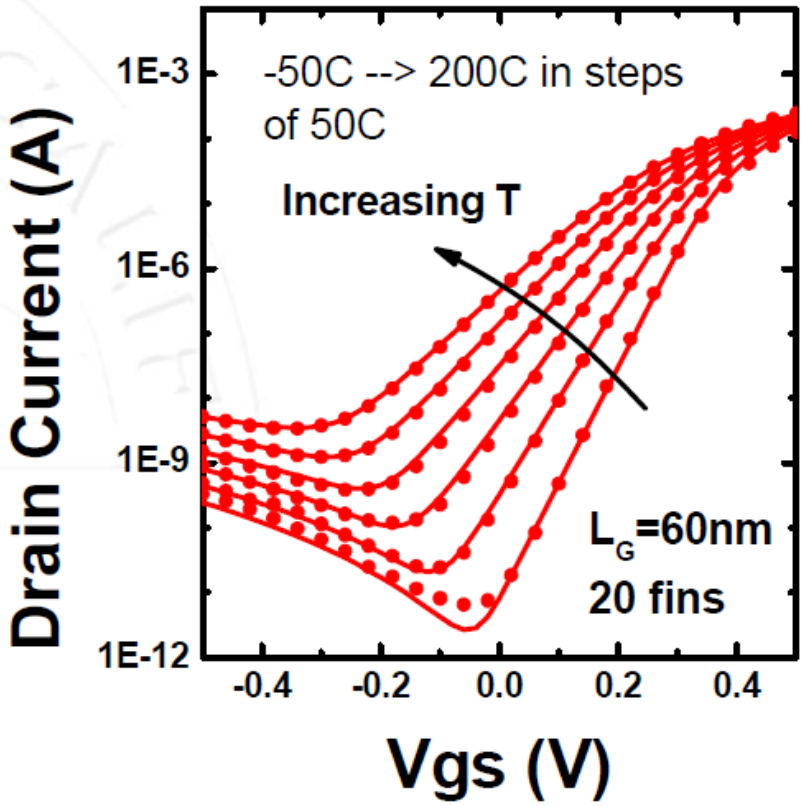
g_m` & g_m`` of 30nm to 10µm FinFETs





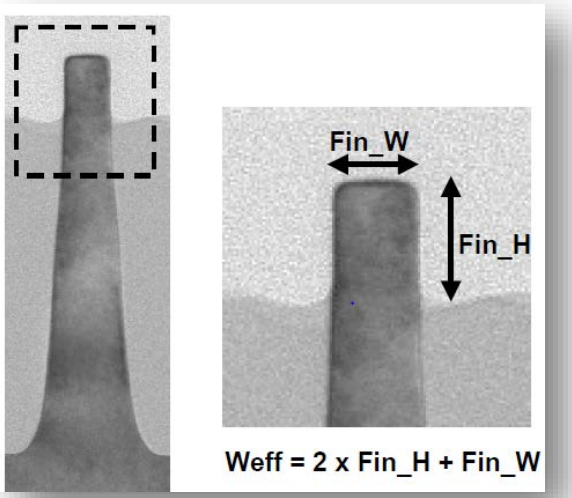
Temperature Model verified for FinFET

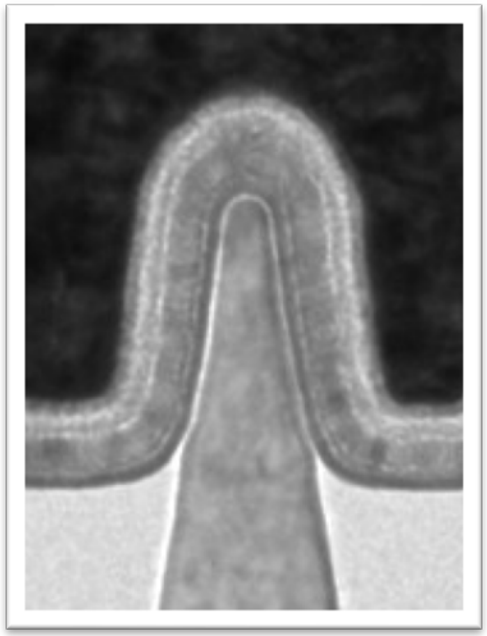




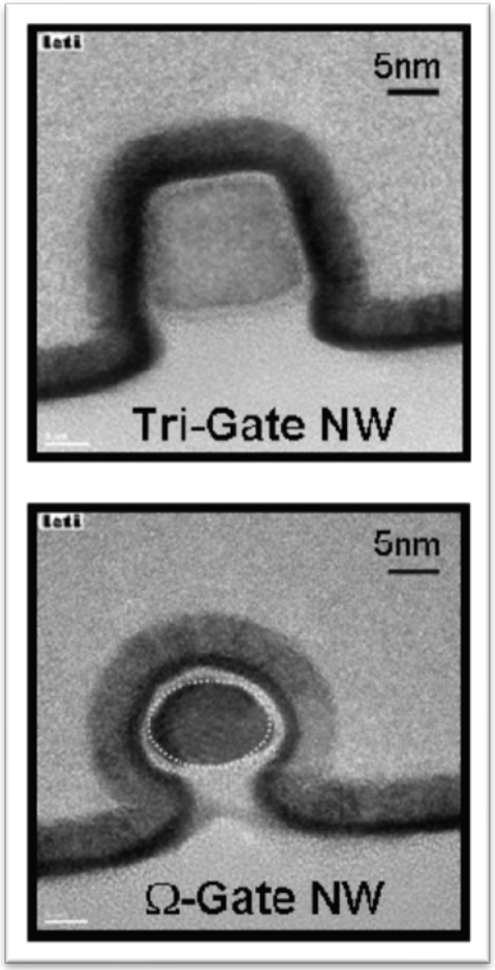
FinFET's Various Complex Cross-Sections

TSMC, IEDM 2010

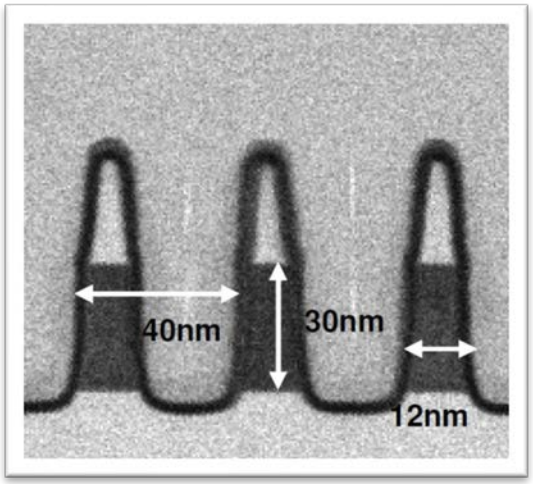




Leti, VLSI 2012



IBM, VLSI 2012



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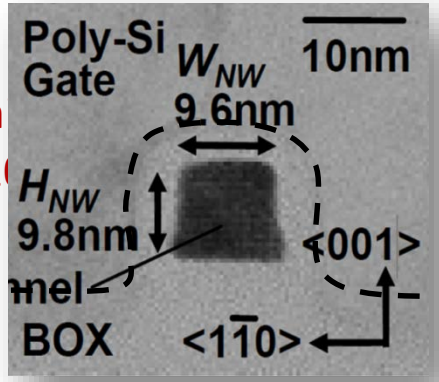
VLSI 2(

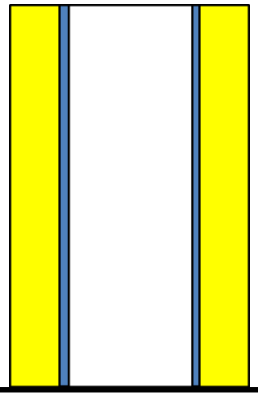


Prior Models Available for Two Simple Cross-Sections Only – Deductive model

1. Double-Gate FinFET:

Charge Equation :

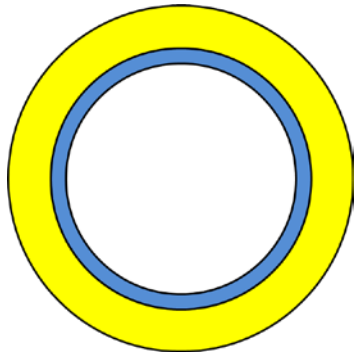
$$V_G - V_{\rm FB} + \frac{t_{\rm ox}}{2\varepsilon_{\rm ox}} Q_d - V = -\frac{t_{\rm ox}}{2\varepsilon_{\rm ox}} Q_e + v_T \ln \frac{Q_e(Q_e+Q_d)/(4v_T\varepsilon_{\rm si}/W_{\rm si})}{q\frac{n_i^2}{N_{\rm si}} W_{\rm si}\left[1-\exp\frac{W_{\rm si}}{4v_T\varepsilon_{\rm si}}(Q_e+Q_d)\right]}$$



2. Cylindrical FinFET:

Charge Equation:

$$V_G - V_{FB} + \frac{\ln(1+t_{ox}/R)}{2\pi\varepsilon_{ox}} Q_{d,Cy} - V = -\frac{\ln(1+t_{ox}/R)}{2\pi\varepsilon_{ox}} Q_{e,Cy} + v_T \ln \frac{-Q_{e,Cy}}{q\frac{n_i^2}{N_{si}}\pi v_T R^2} + v_T \ln \frac{-(Q_{d,Cy}+Q_{e,Cy})/4\varepsilon_{si}\pi}{1-\exp\frac{Q_{d,Cy}+Q_{e,Cy}}{4\varepsilon_{si}\pi v_T}}$$



New Unified Model for Complex FinFET Cross-Sections – Inductive model

$$v_G - v_O - v_{CH} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{-q_t} - q_t - 1}\right)$$

$$v_O = v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_T C_{ins} N_{ch}}\right)$$

$$q_t = (q_m + q_{dep})\frac{A_{ch} C_{ins}}{\varepsilon_{ch} W^2}$$

Model Parameters:

Fin Area: A_{ch}

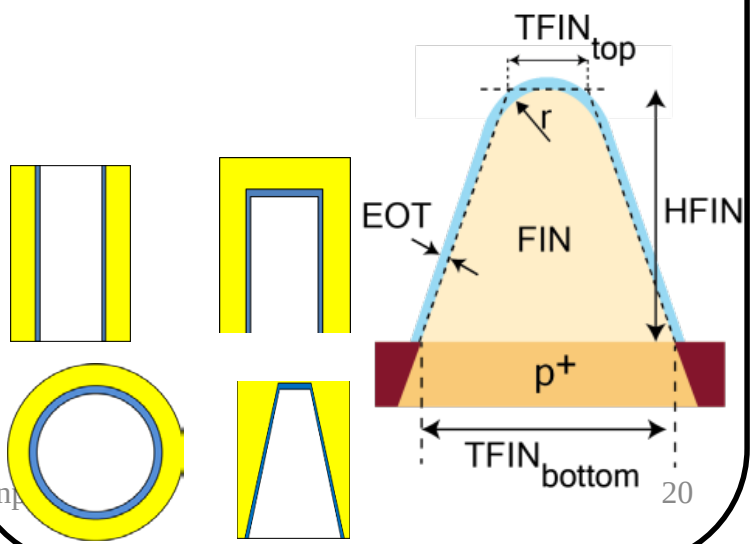
Channel Doping: N_{ch}

Channel Width: W

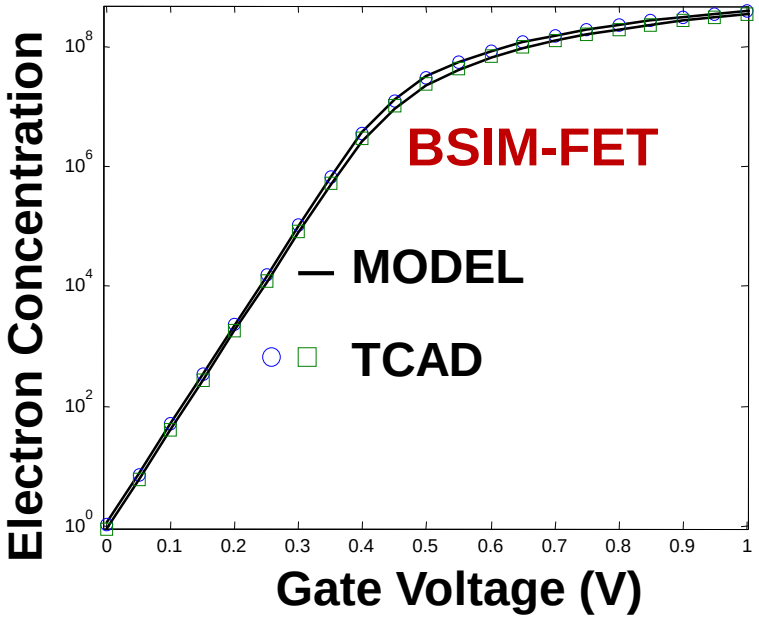
Insulator Cap: C_{ins}

Unified Model for

various Fin shapes



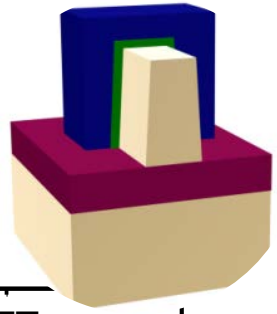
Even FinFET with this “fin” shape

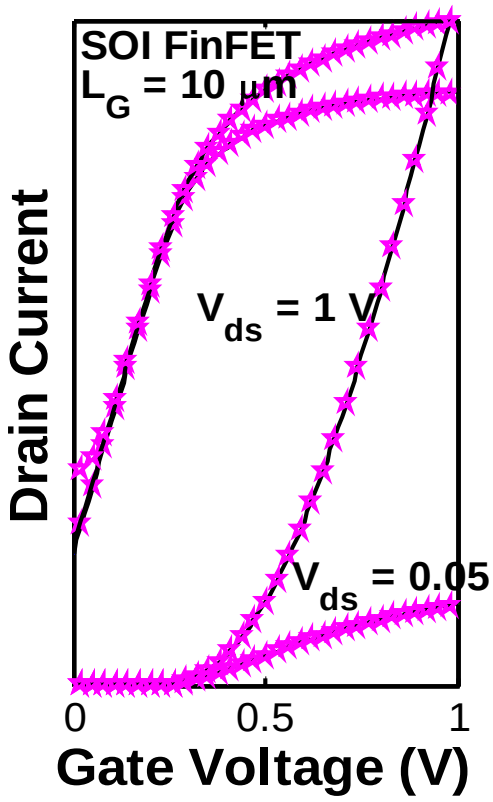


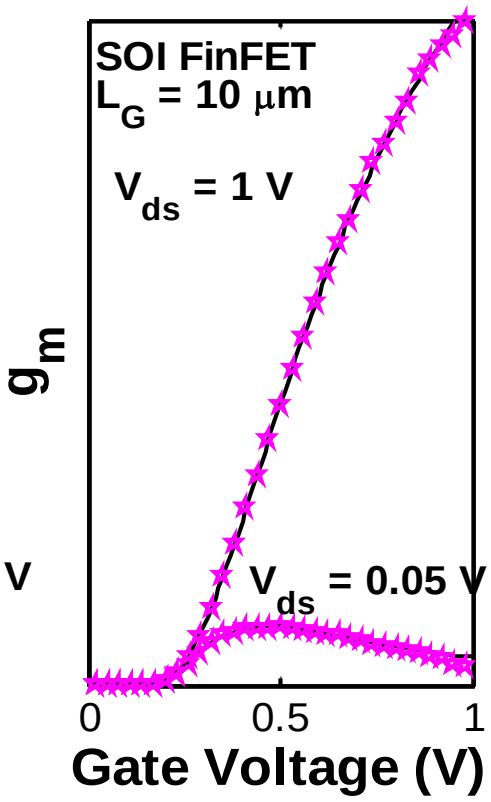
J. P. Duarte et. al., SRC TECHCON 2014.

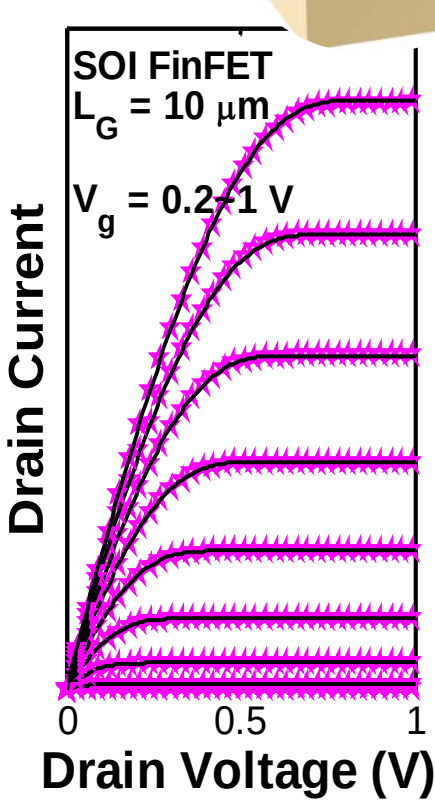
Experimental FinFET Example: I-V

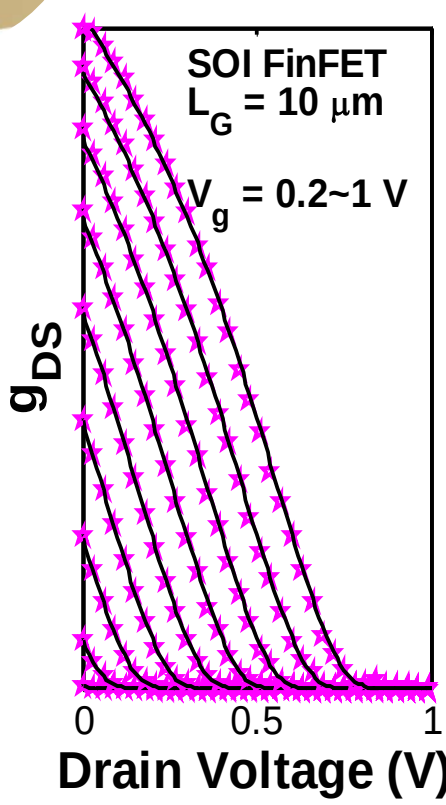
SOI FinFET











*FinFET fabricated by SEMATECH

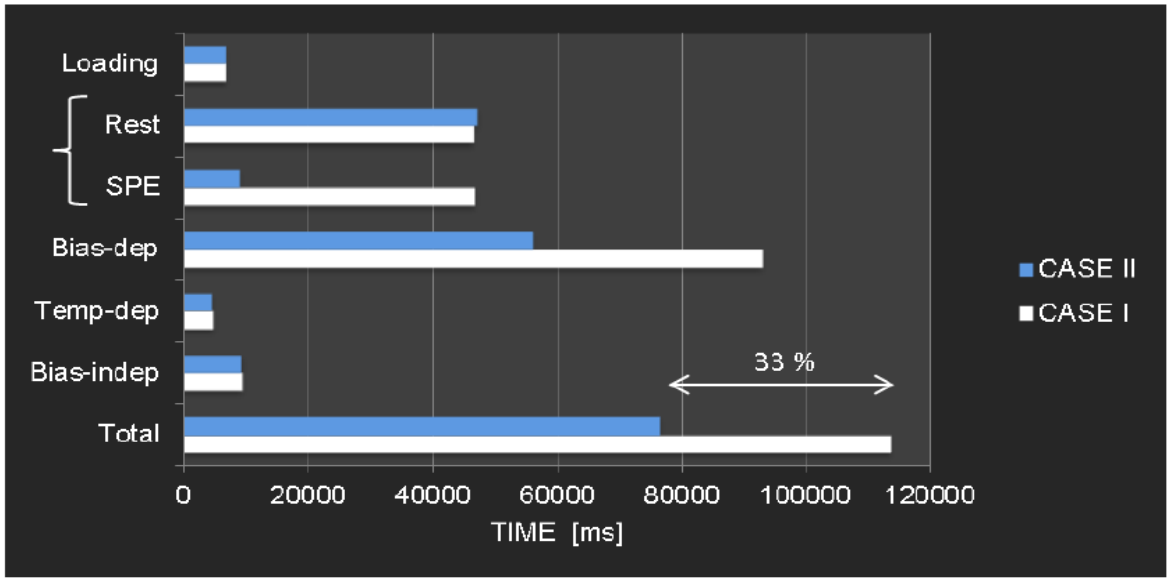
BSIM-CMG Model Speed Improvement

- Model Speed Improvement ~ 30%
- New core model used in BSIM-CMG109

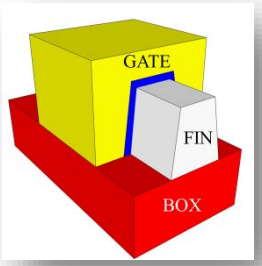
	Calls	Total*	Bias-indep	Temp-dep	Bias-dep*	SPE	Rest of Bias-dep	Loading
CASE I	1555029	113629.42	9298.9	4665.3	92895.17	46627.9379	46267.2321	6770.05
%		100	8.18	4.11	81.75	41.04	40.72	5.96
CASE II	1555029	76360.47	9252.45	4463.74	55910	8878.4928	47031.5072	6734.28
%		100	12.12	5.85	73.22	11.63	61.59	8.82

*Total = Bias-indep + Temp-dep + Bias-dep + Loading

*Bias-indep = SPE + Rest



3D Model for Short Channel Effects



- SCEs are 3-D effects
  - Need to solve the 3-D Poisson's equation.

$$\nabla^2\psi(x,y,x) = -\frac{qN_{ch}}{\varepsilon_{ch}}$$

- **DIBL Equations:** $\Delta V_{TH} = f(\vec{V},\lambda) \quad SS = g(\vec{V},\lambda)$

λ: characteristic field penetration length

$$\lambda_{DG} \approx \sqrt{\frac{\varepsilon_{ch} T_{ch} t_{ins}}{\varepsilon_{ins}}}$$

K. Suzuki, EDL 1996

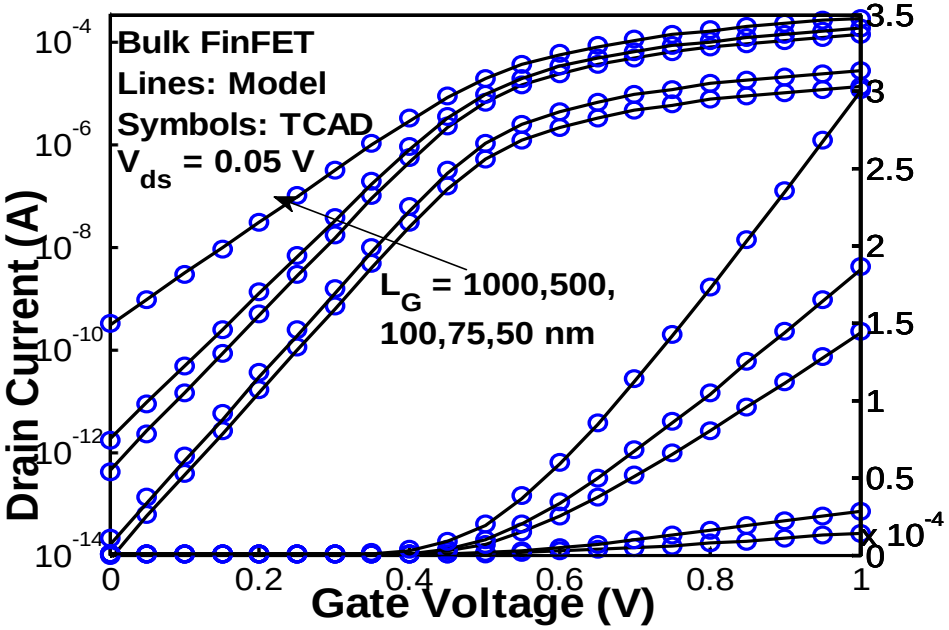
$$\lambda_{CyG} \approx \sqrt{\frac{2\varepsilon_{ch} R^2 ln\left(1+\frac{t_{ins}}{R}\right)}{\varepsilon_{ins}}}$$

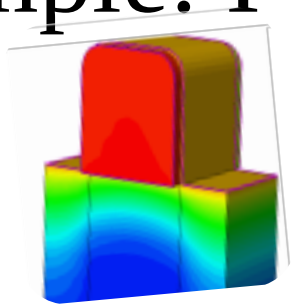
C. P. Auth, EDL 1997

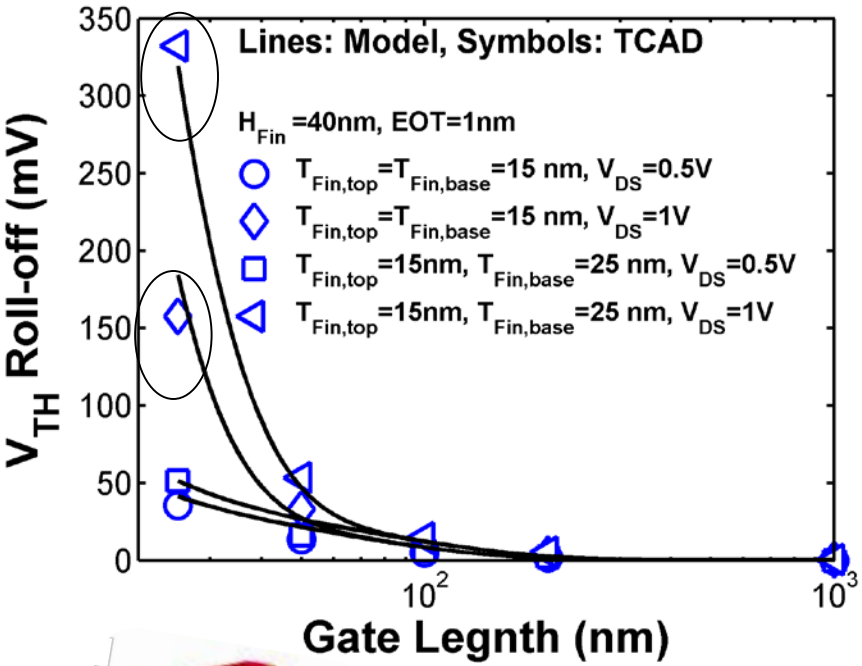
Unified λ

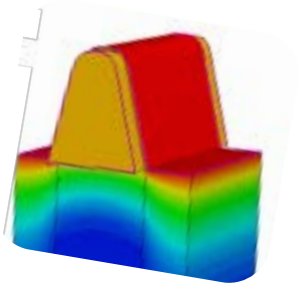
$$\lambda \approx \sqrt{\frac{\varepsilon_{ch} A_{ch}}{C_{ins}}}$$

TCAD FinFET Example: I-V: Scaling

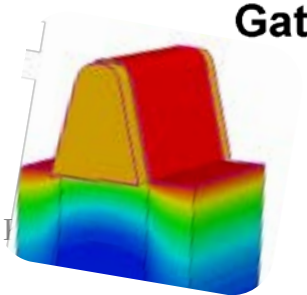








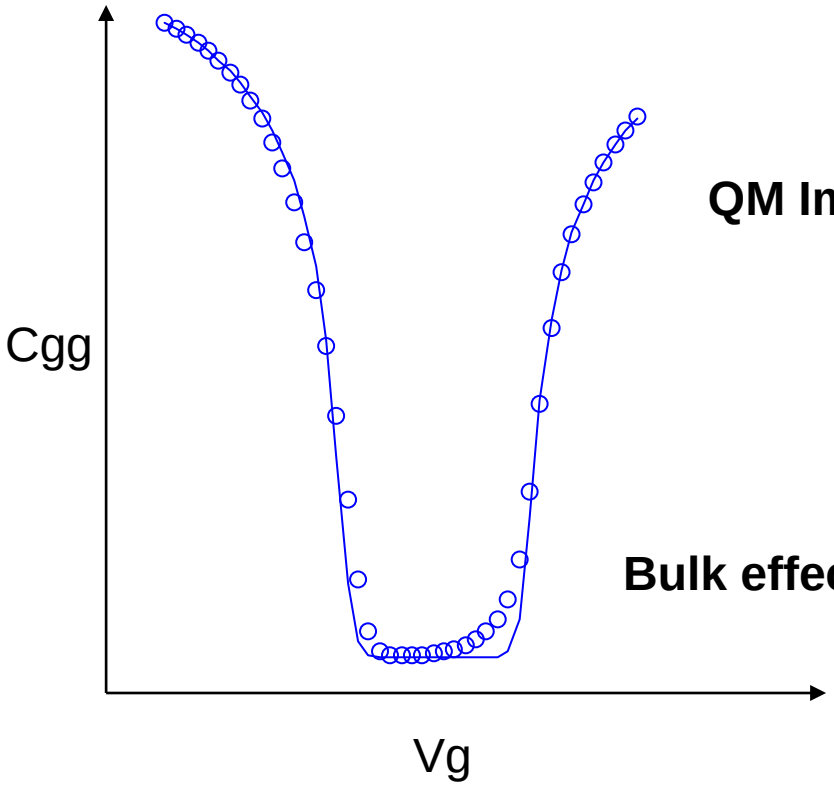
$$\lambda \approx \sqrt{\frac{\varepsilon_{ch} A_{ch}}{C_{ins}}}$$



Experimental FinFET on Bulk Example:

New QM Effects + Body Bias model

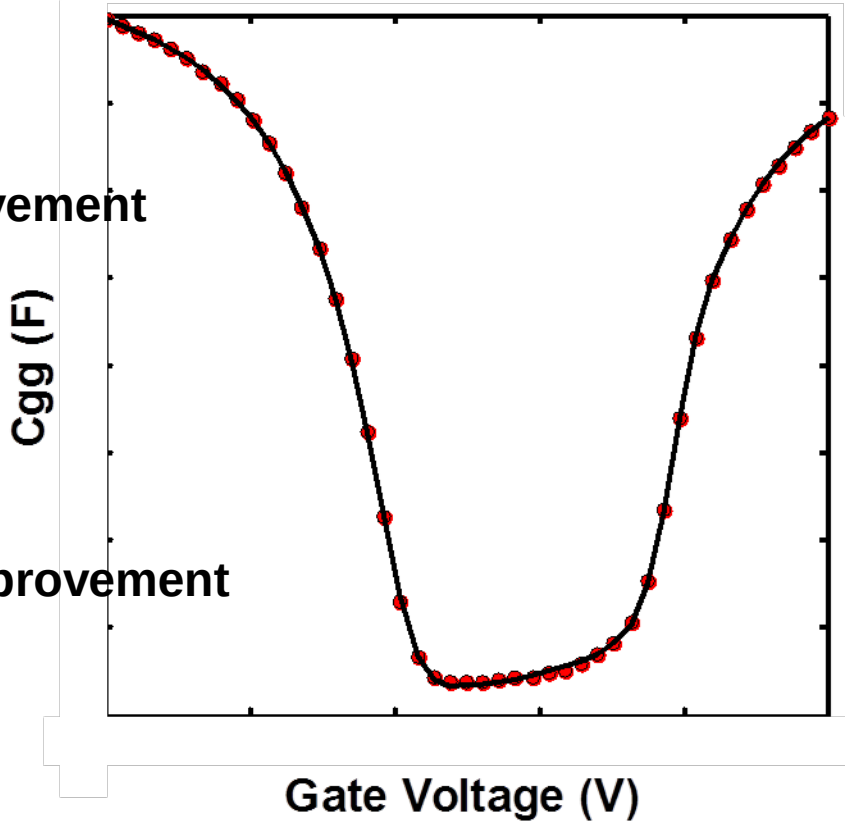
Lines: Old BSIM-CMG



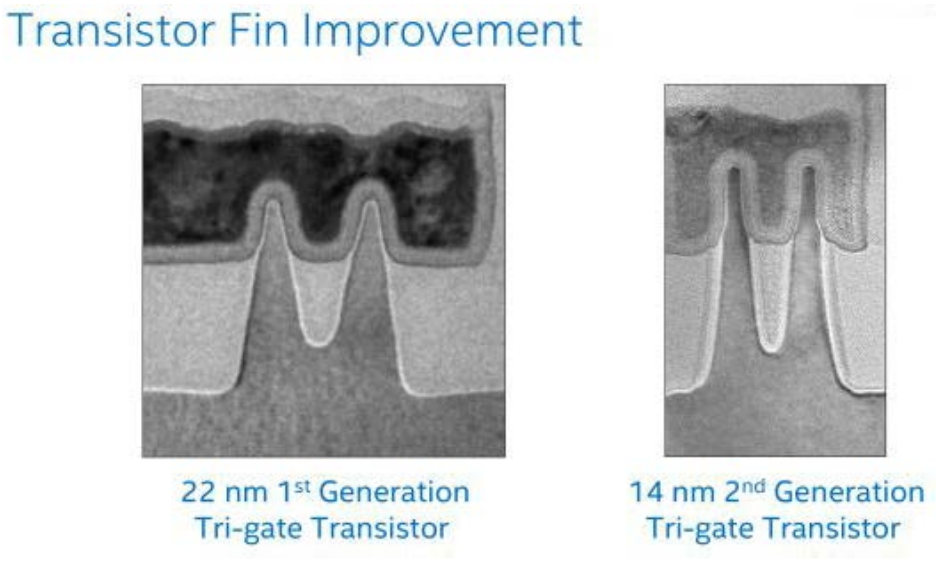
QM Improvement

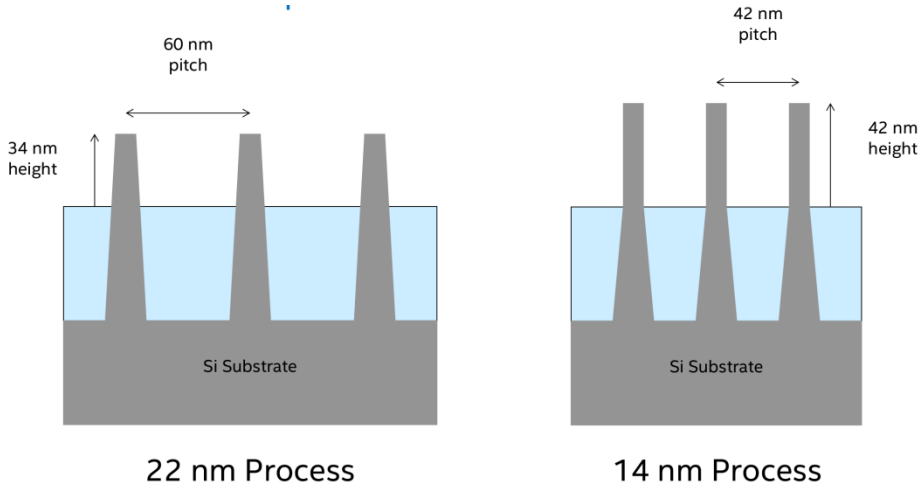
Bulk effect Improvement

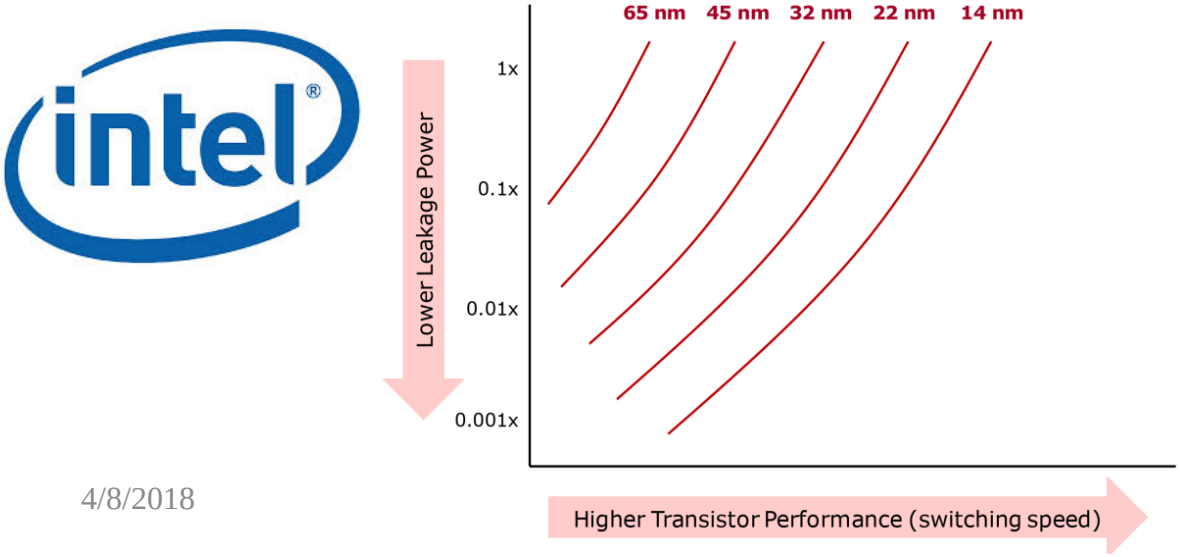
Lines: New BSIM-CMG



State-of-the-Art **14nm** FinFET



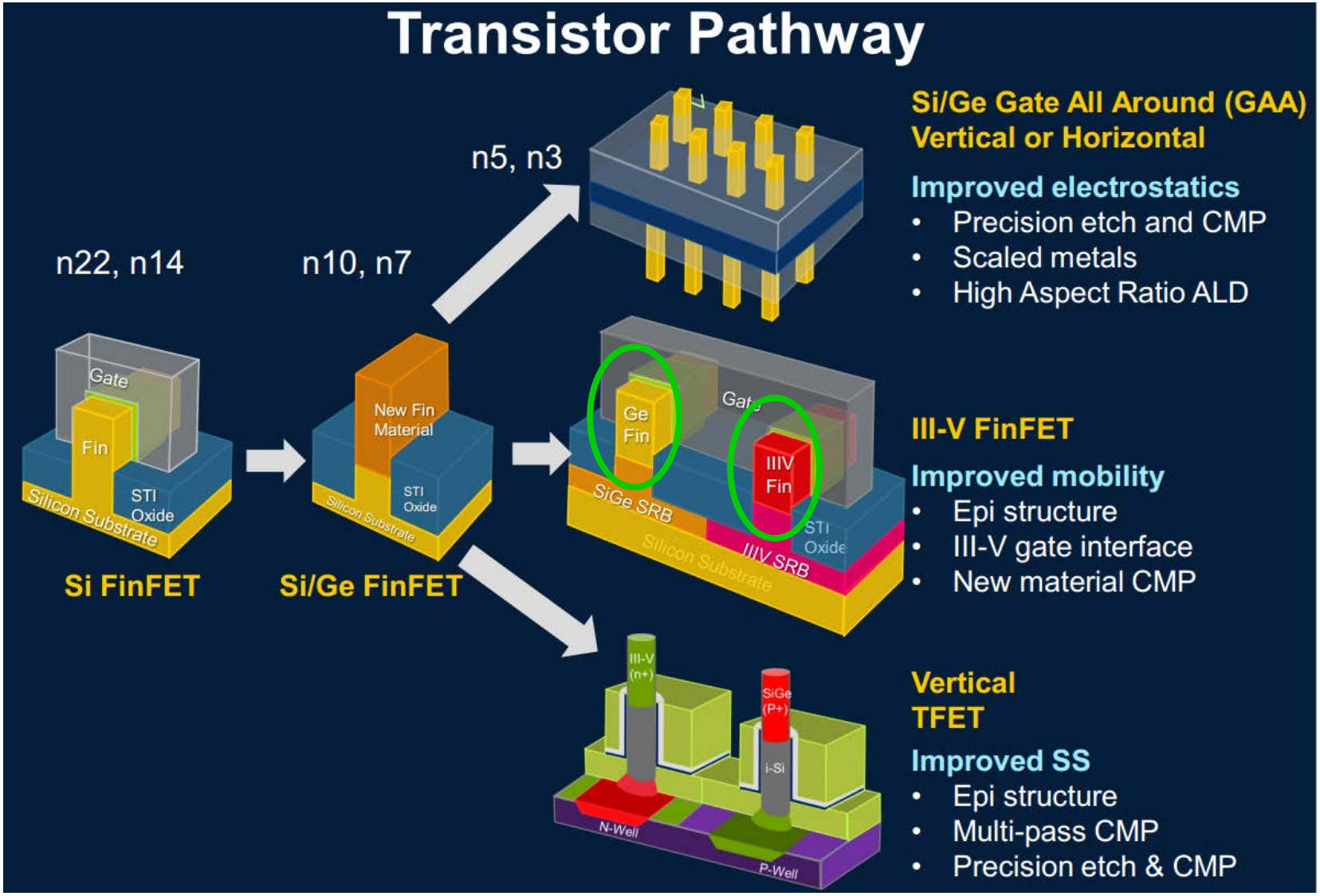




Taller and Thinner Fins for increased drive current and performance

Source: Anandtech

Future – 10nm and beyond



Source: Applied Materials

Key points for 10nm and beyond

- Reduced leakage – Better sub-threshold slope
  - Ultra-thin channel
  - Electrostatic control → Nanowire transistor
- Higher mobility channel
  - Si NMOS and PMOS
  - Ge PMOS
  - SiGe
  - III-V materials NMOS – InAs, InGaAs etc.

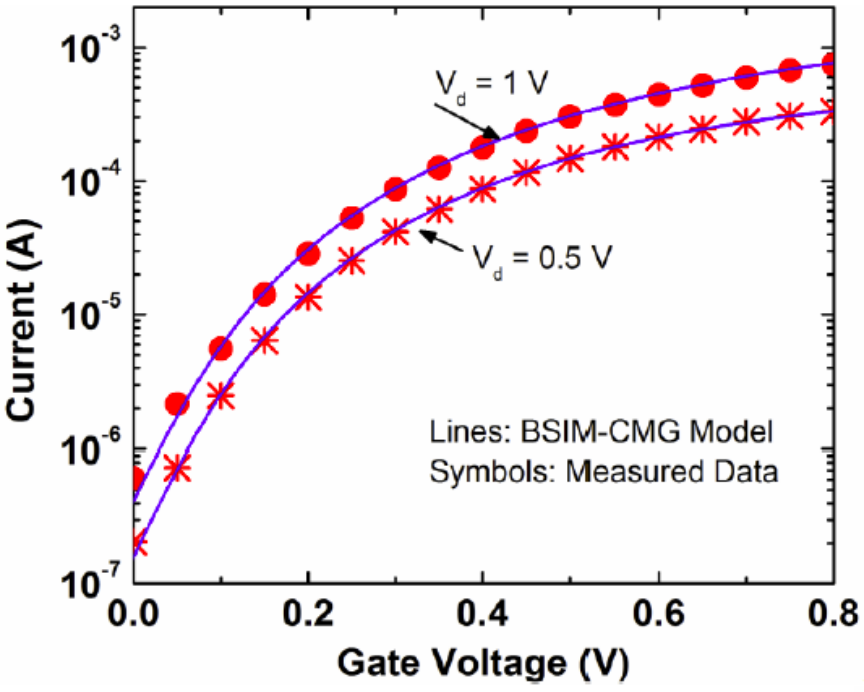
$$I_{off}(nA) = 100\frac{W}{L}10^{-\frac{V_{TH}}{S}}$$

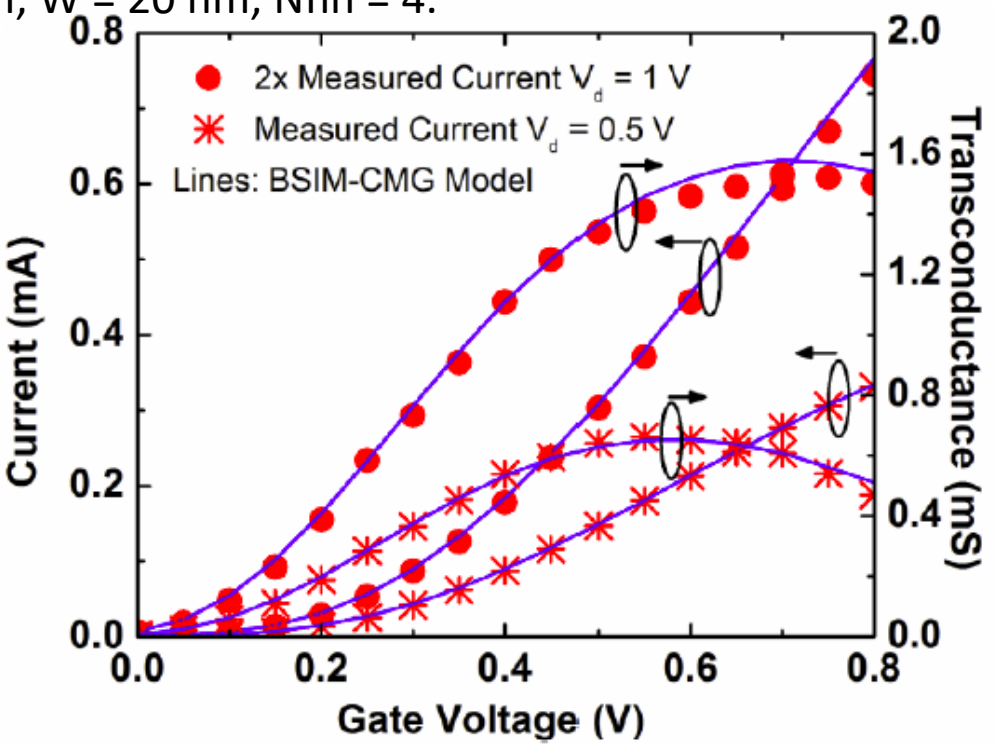
$$I_{dsat} = \frac{W}{2L}C_{ox}\mu_{eff}(V_{gs} - V_t)^2$$

InGaAs FinFET Modeling

- BSIM-CMG with the **new Quantum Effects model** used to model InGaAs FinFETs

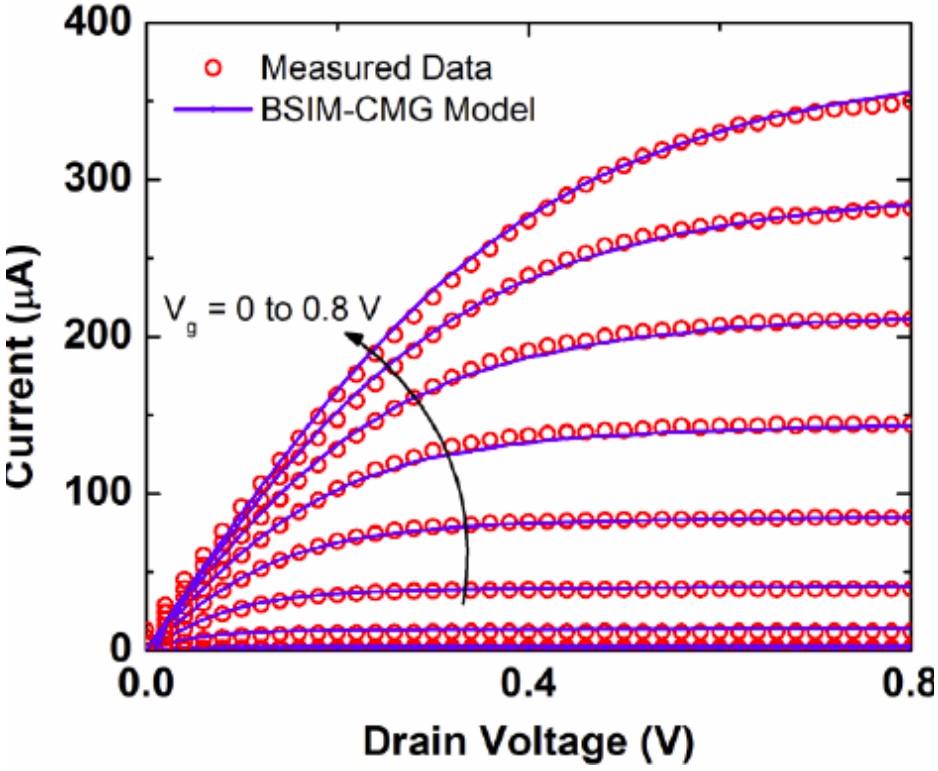
L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.

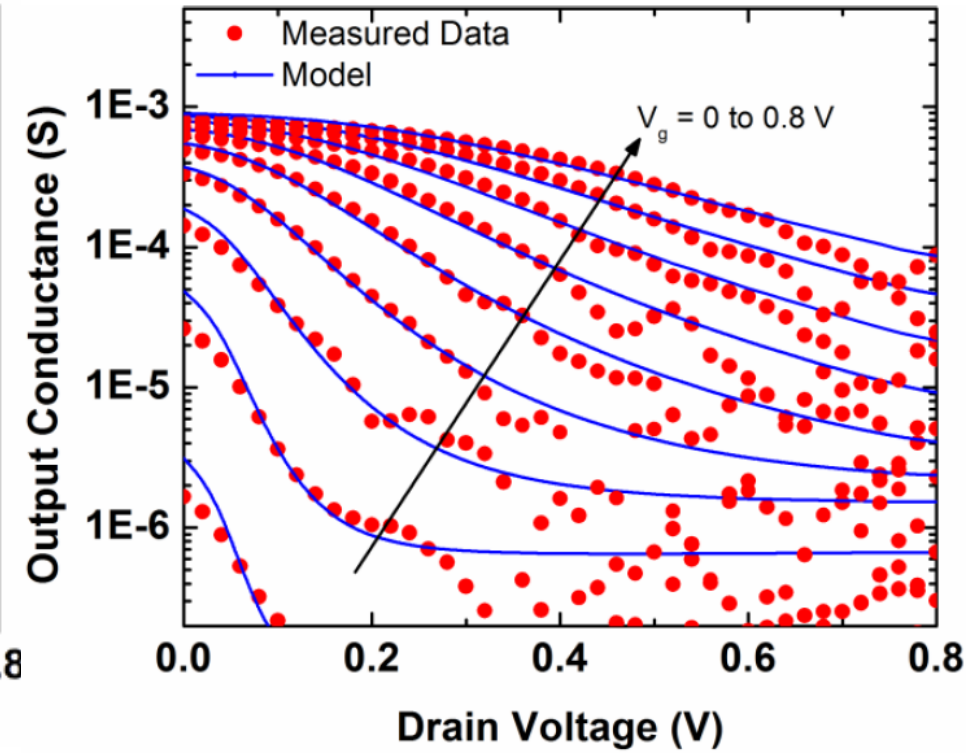




S. Khandelwal, J. P. Duarte, N. Paydavosi, Y. S. Chauhan, J. J. Gu, M. Si, P. D. Ye, and C. Hu, "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Workshop on Compact Modeling, 2014.

InGaAs FinFET Modeling

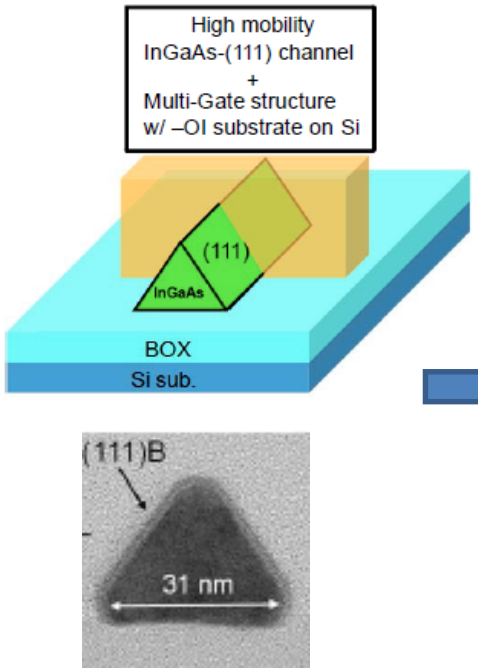




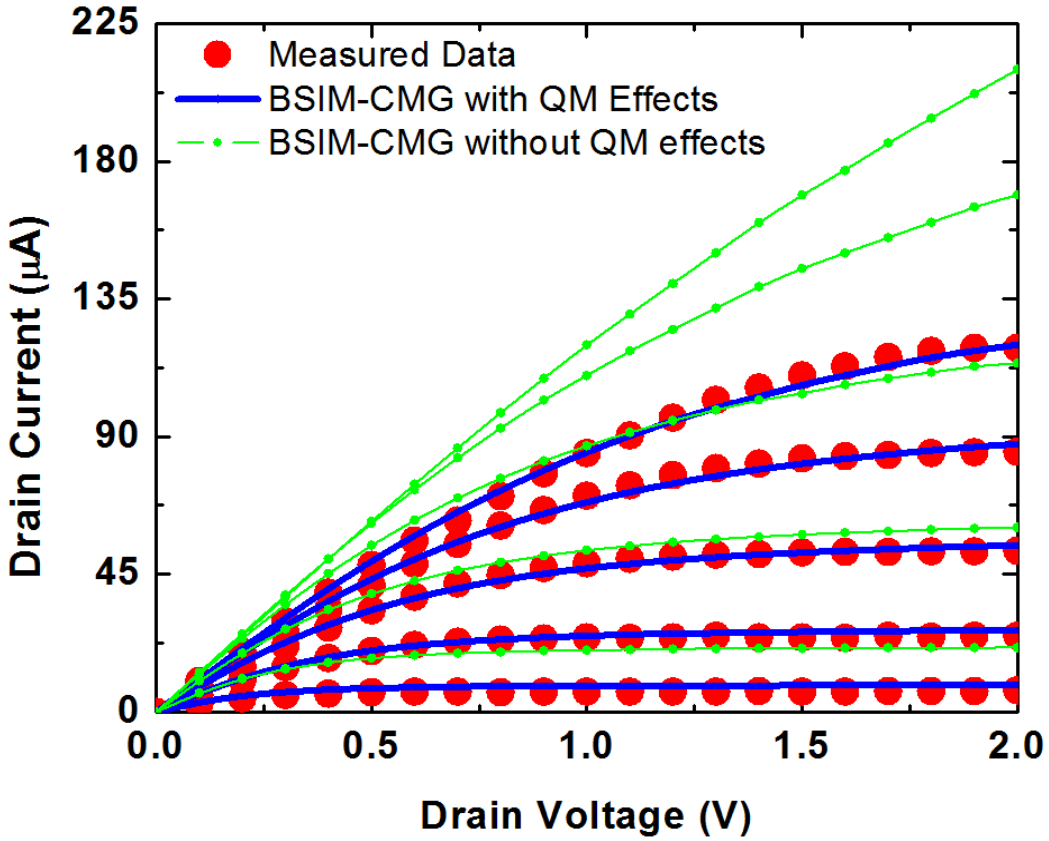
L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.

Data from: J. J. Gu et al. IEDM 2012

InGaAs FinFETs with Triangular Cross-section



T. Irisawa et al. IEDM 2013



Importance of accurate modeling of Quantum Effects

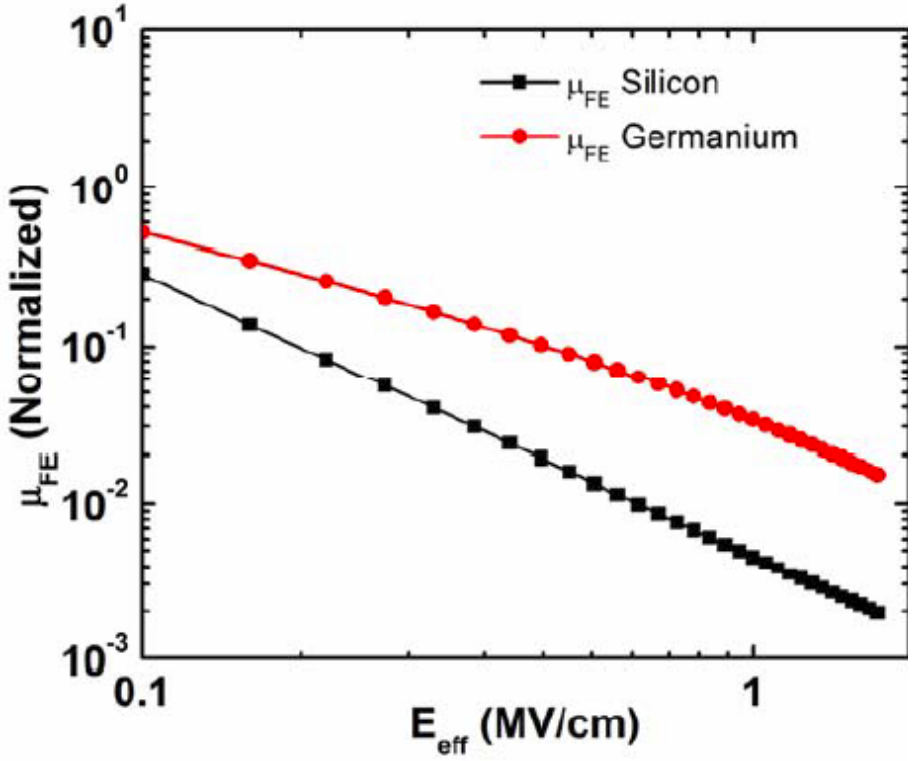
Modeling of Germanium FinFETs @10nm

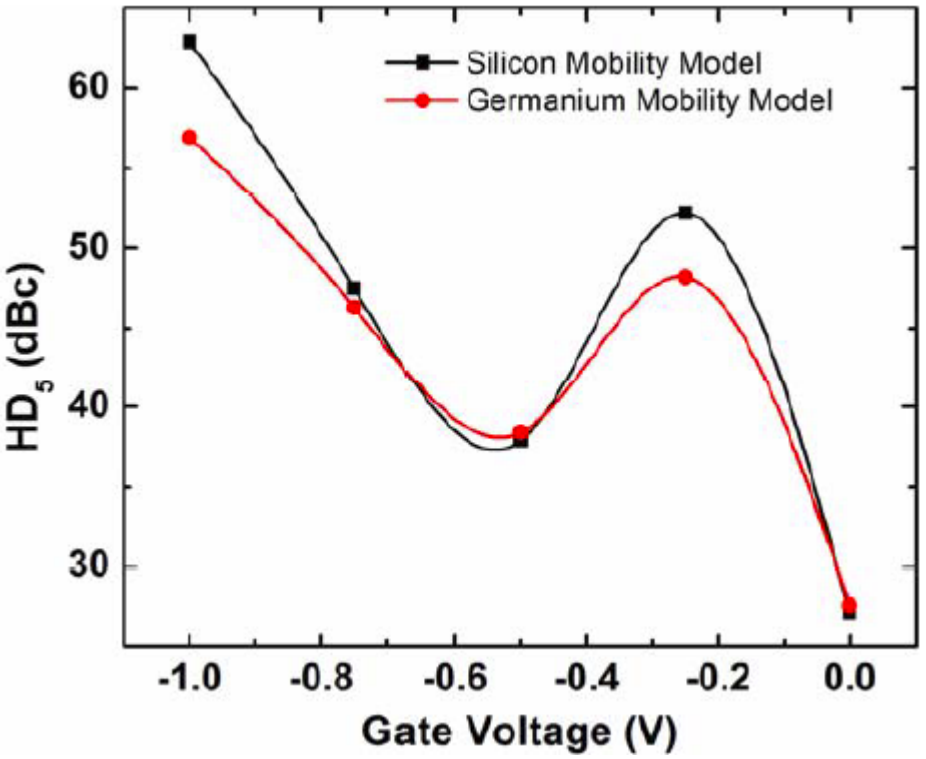
- Ge FinFET may be used in 10nm node for better P-FinFET.
- Industry standard BSIM FinFET model can now model Ge FinFET.
- Early availability of a unified Si/Ge FinFET model facilitates technology-circuits co-development.

Modeling Germanium FinFETs

- User selectable MOD to model Ge FinFETs
  - Material Mode “MTRLMOD” = Si (Default) or Ge
- “MTRLMOD”=Ge invokes new mobility model for Ge
- MTRLMOD = Ge sets key parameters for Ge
  - Band-Gap, Mobility …
- MTRLMOD=Ge model verified with experimental data
  - Excellent Model Calibration Results
  - Scalable Ge FinFET Model

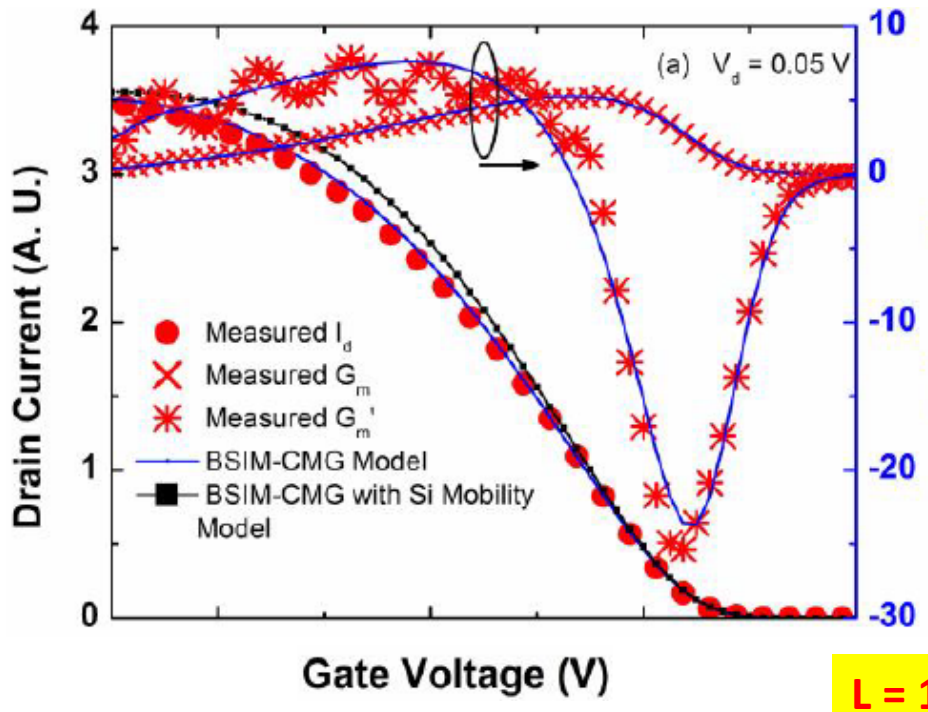
Germanium Mobility Model

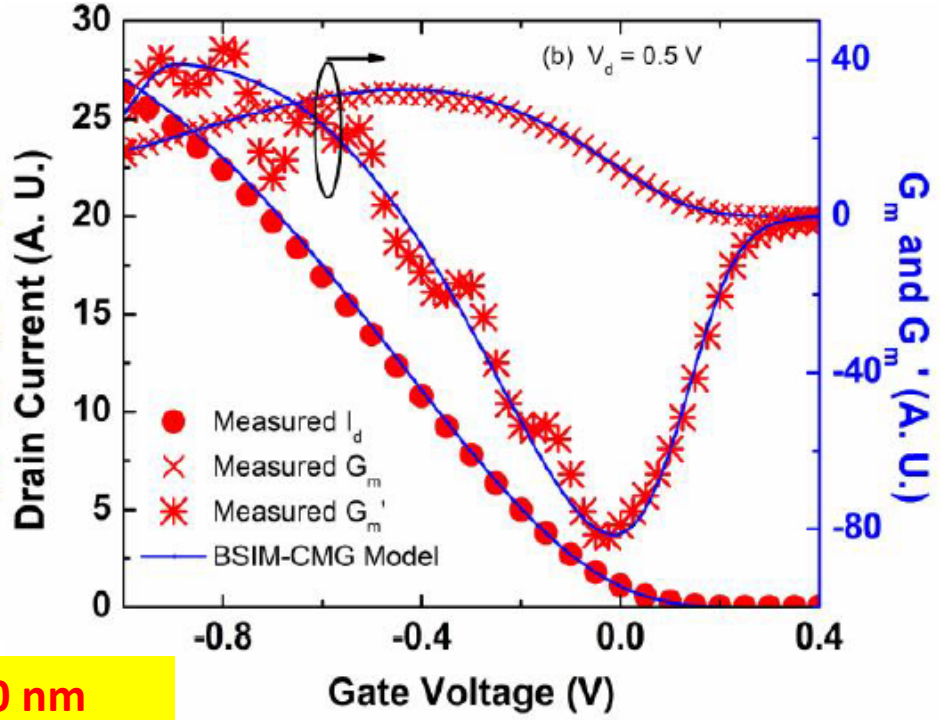




- Due to the lower *m** of holes in Ge the charge-centroid is farther away from the oxide interface resulting in a weaker SR scattering.
- Ge mobility has a weaker dependence on E_{eff} up-to ~0.5 MV/cm as the impact of SR scattering is only seen at much higher E_{eff} in Ge as compared to Si.

BSIM-CMG Model Results for Ge pFinFETs

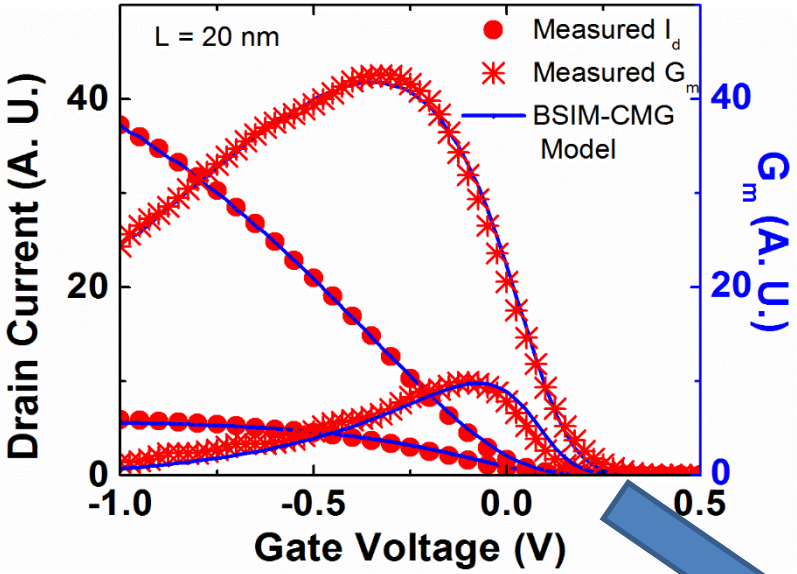


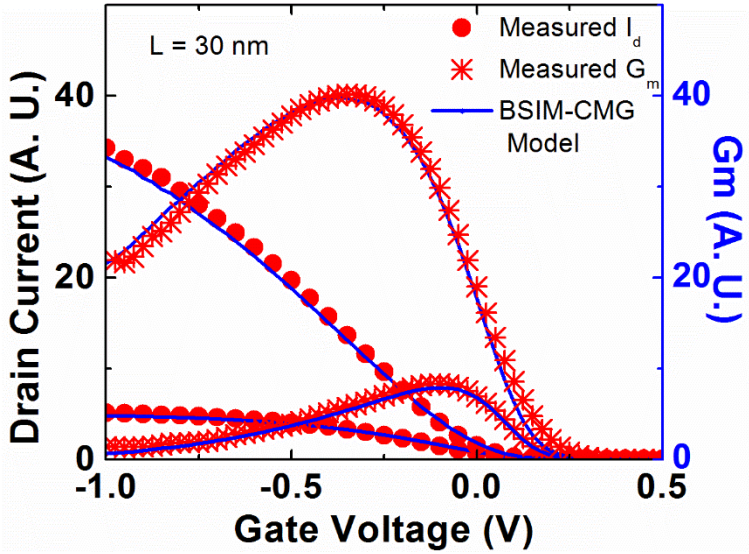


L = 130 nm

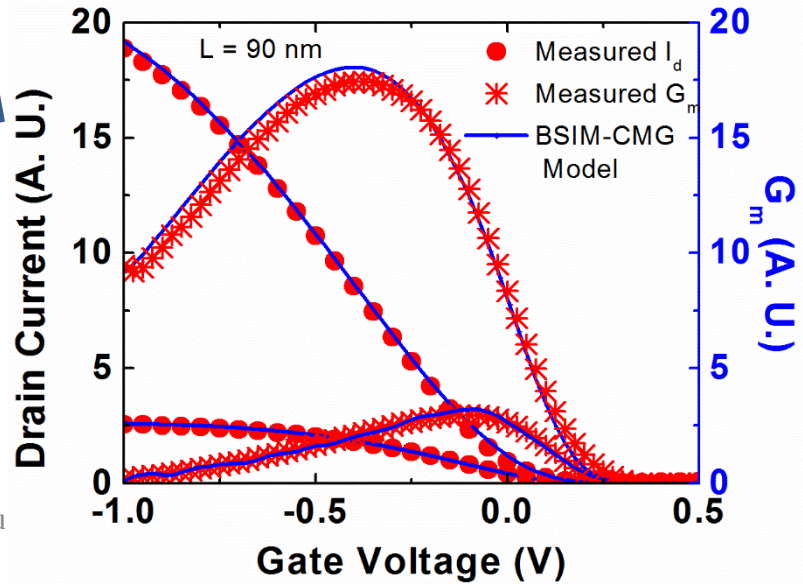
S. Khandelwal et. al., "Modeling 20nm Germanium FinFET with the Industry Standard FinFET Model", IEEE Electron Device Letters, Vol. 35, Issue 7, July 2014.

BSIM-CMG Model Scalability for Ge pFinFETs



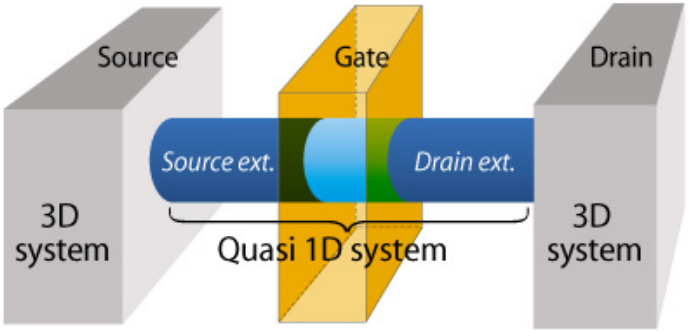


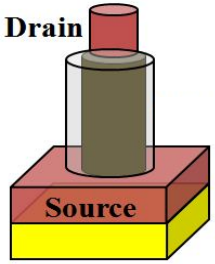
L increasing



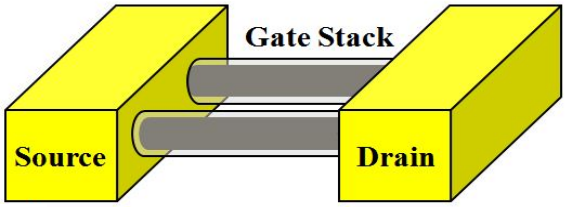
L varying from 20 nm to 90 nm Scalable Model

Forward Looking Modeling of Pillar/Nanowire FET

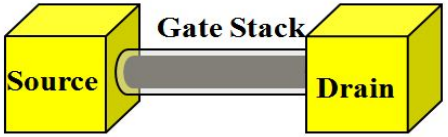




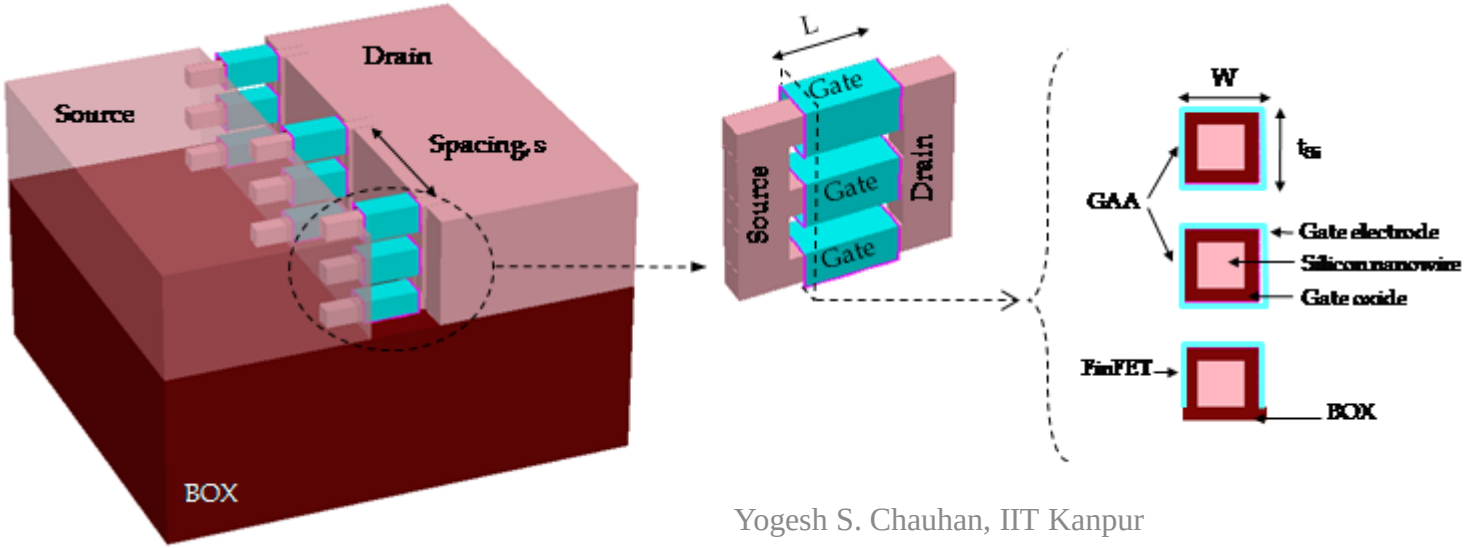
Vertical Pillar FET



Twin Silicon Nanowire FET

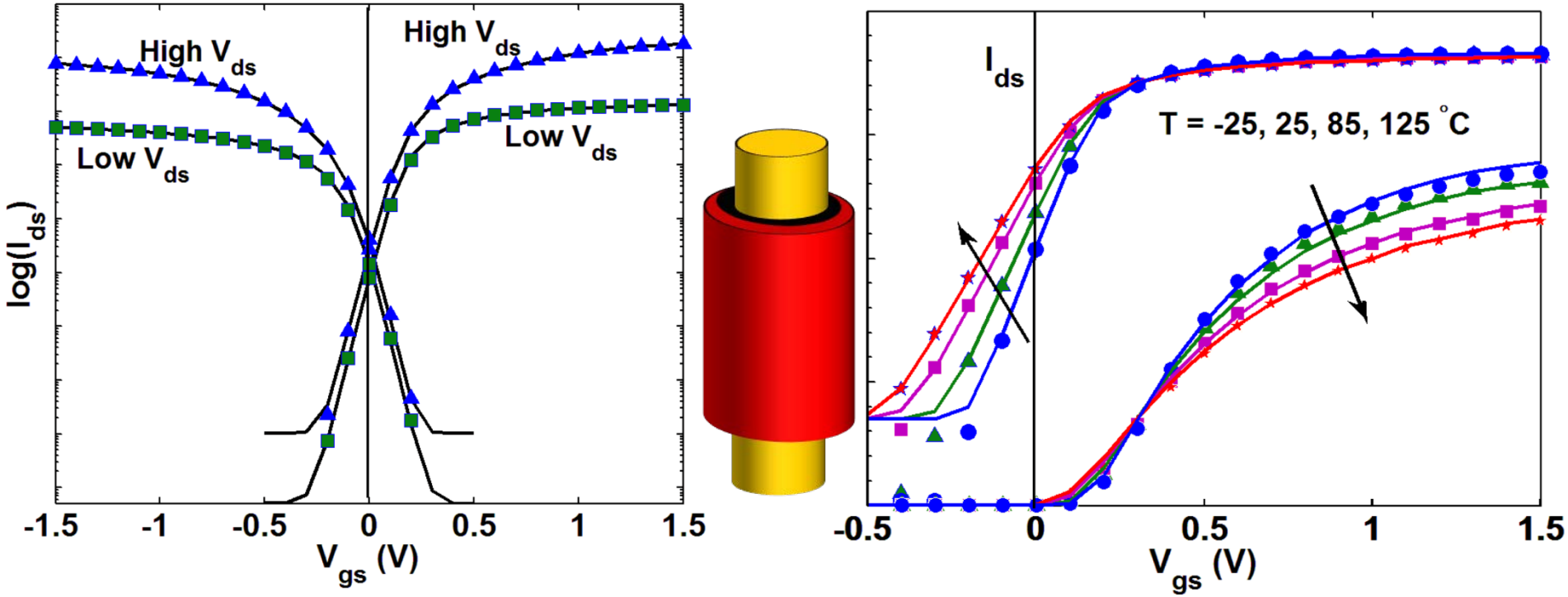


Horizontal Nanowire FET



Validation on Asymmetric Nanowire FET

Symbols – experimental data



Ids-Vgs for N-type Nanowire for different temperatures

S. Venugopalan et. al., "Modeling Intrinsic and Extrinsic Asymmetry of 3D Cylindrical Gate/ Gate-All-Around FETs for Circuit Simulations", IEEE Non-Volatile Memory Technology Symposium, Shanghai, China, Nov. 2011.

Modeling of III-V FinFET

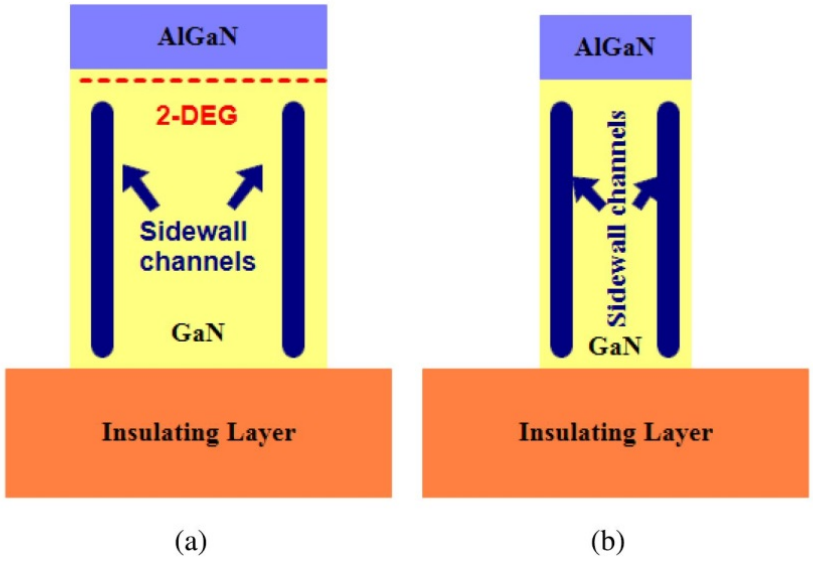


Fig. 1. Schematic showing sidewall channels and 2-DEG channel in AlGaN/GaN based FinFET devices; (a) Wide fin-width device, (b) Narrow fin-width device [12].

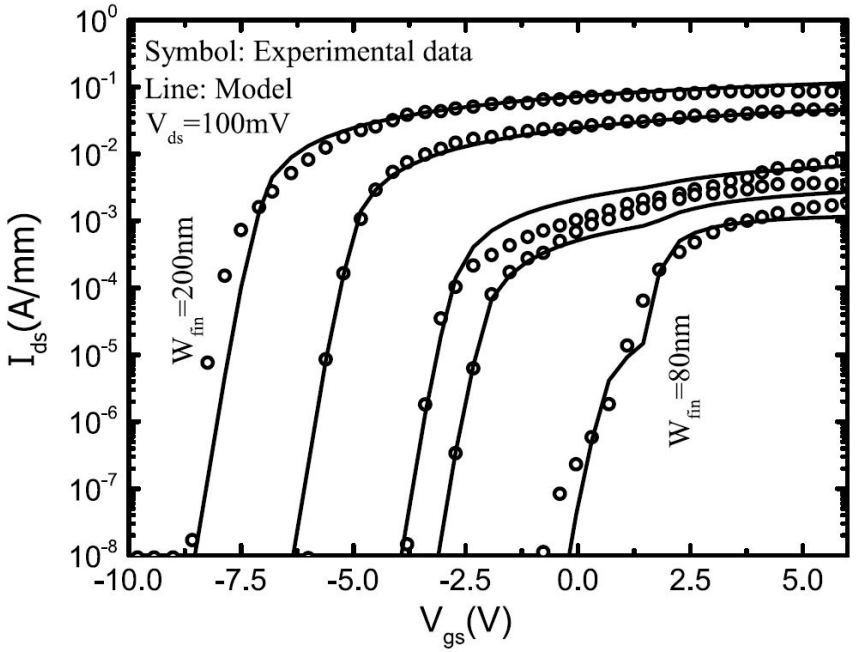


Fig. 3. Subthreshold behaviour of model with experimental data [12], for W_{fin}=80nm, 120nm, 140nm, 180nm and 200nm and $Lg = 1.0\mu m$. Drain current is normalized with total gate width $(W_{fin} + 2H_{fin})$, where $H_{fin} = 120nm$.

Chandan Yadav et. al., "Modeling of GaN-Based Normally-Off FinFET", IEEE Electron Device Letters, June 2014.

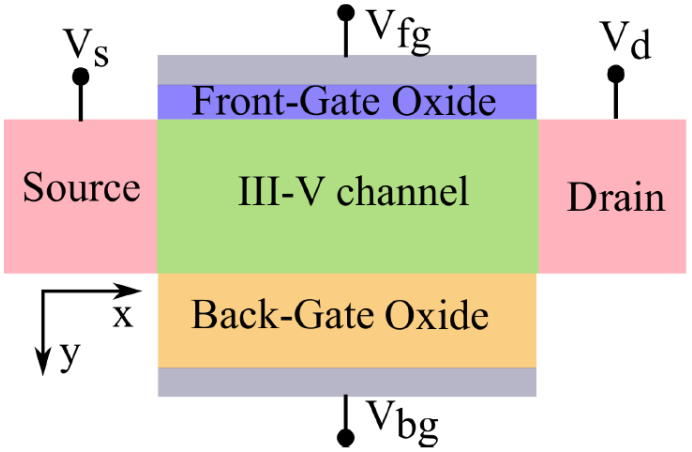
7nm & beyond – Would it be a smooth ride?

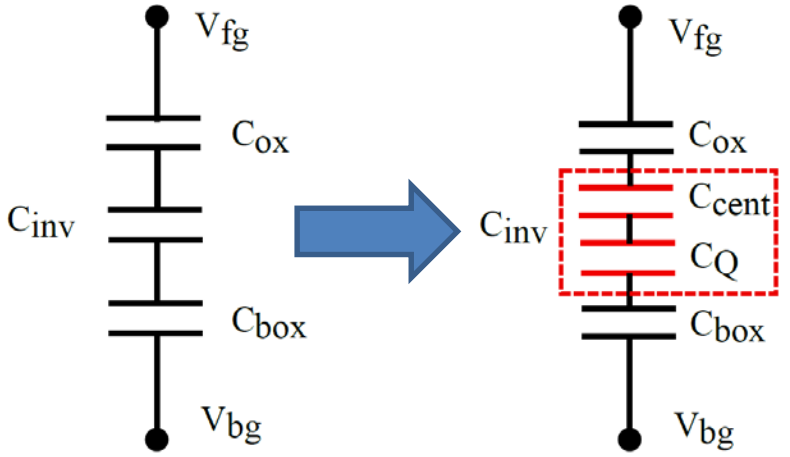
- Effects in ultra-thin Si/Ge/III-V Transistors
  - Quantum Capacitance
  - Charge centroid
  - Source to Drain Tunneling
  - Bandgap variation with thickness
  - Effective mass variation with thickness

Quantum Capacitance

- Concept of the quantum capacitance was given by S. Luryi, which originates when vertical electric field partially penetrates the inversion charge in channel.
- The quantum capacitance depends on 2-D density of states $\rho_{2D} = \frac{m_{||}^*}{\pi\hbar^2}$ and valley degeneracy factor ($g_{v.}$)
- Quantum Capacitance

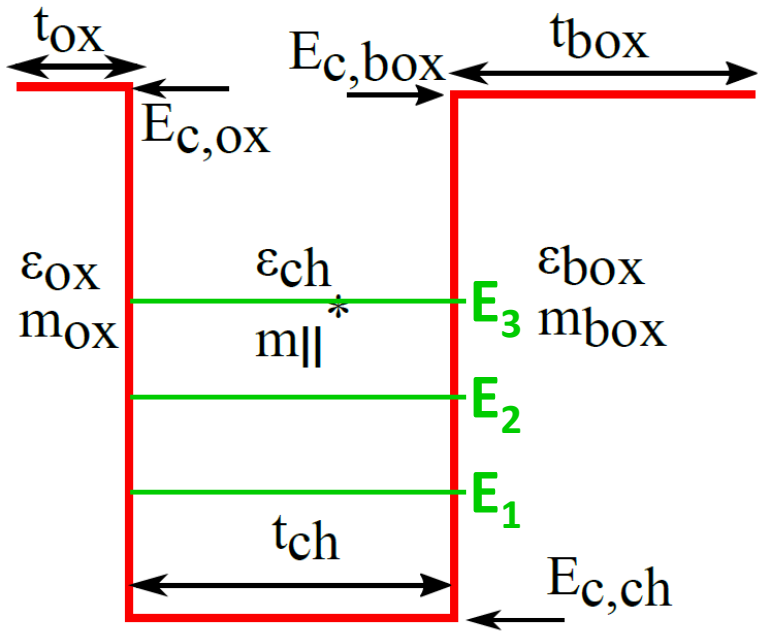
$$C_Q = \frac{q^2 g_v m_{||}^*}{\pi\hbar^2}$$

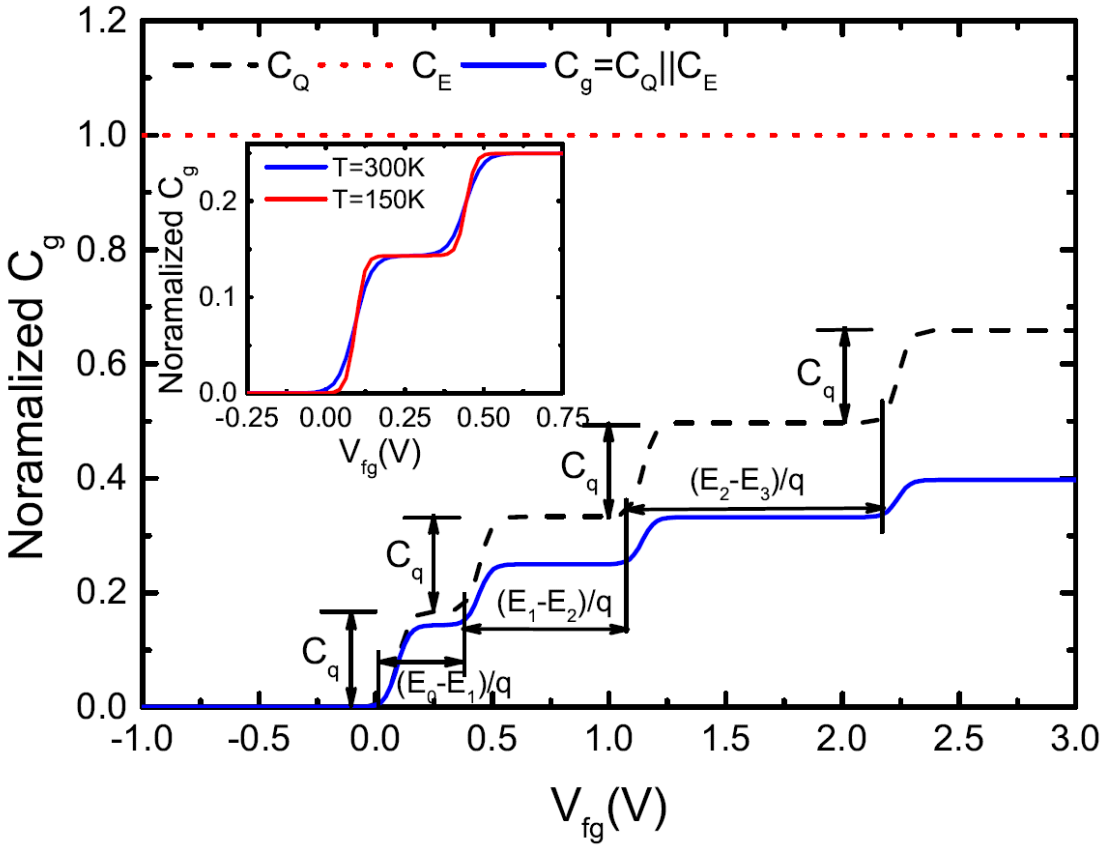




Quantum Capacitance

Thin body device is a 2D system.

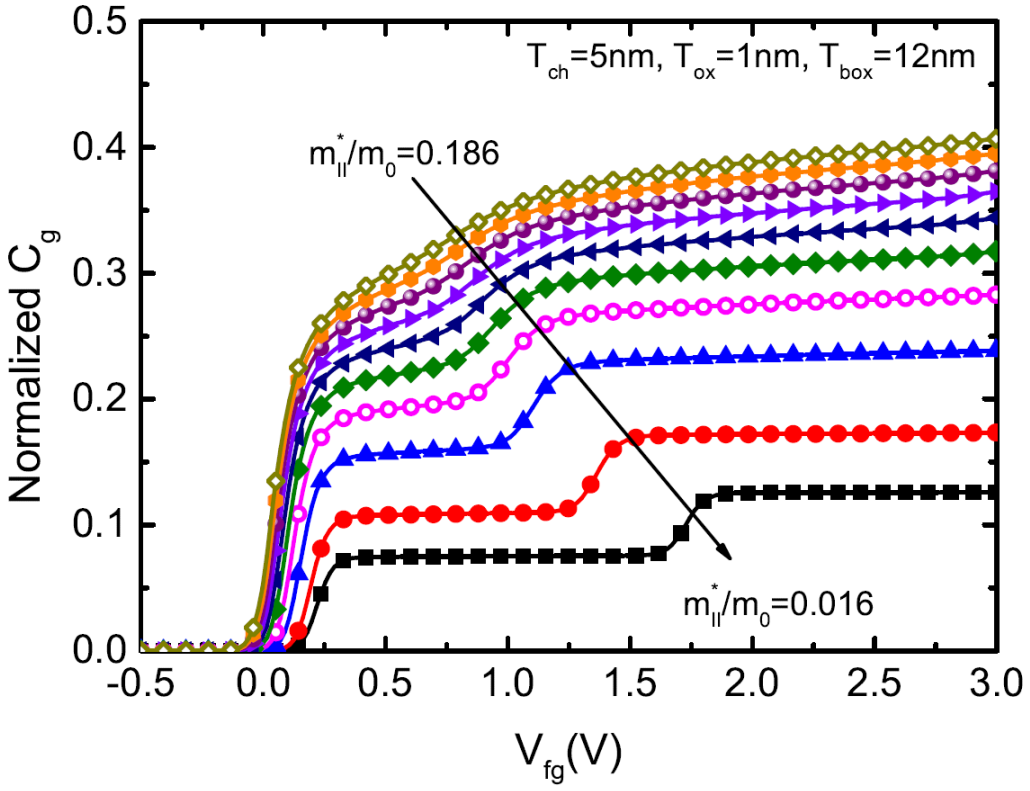




C. Yadav et. al., submitted in Solid State Electronics.

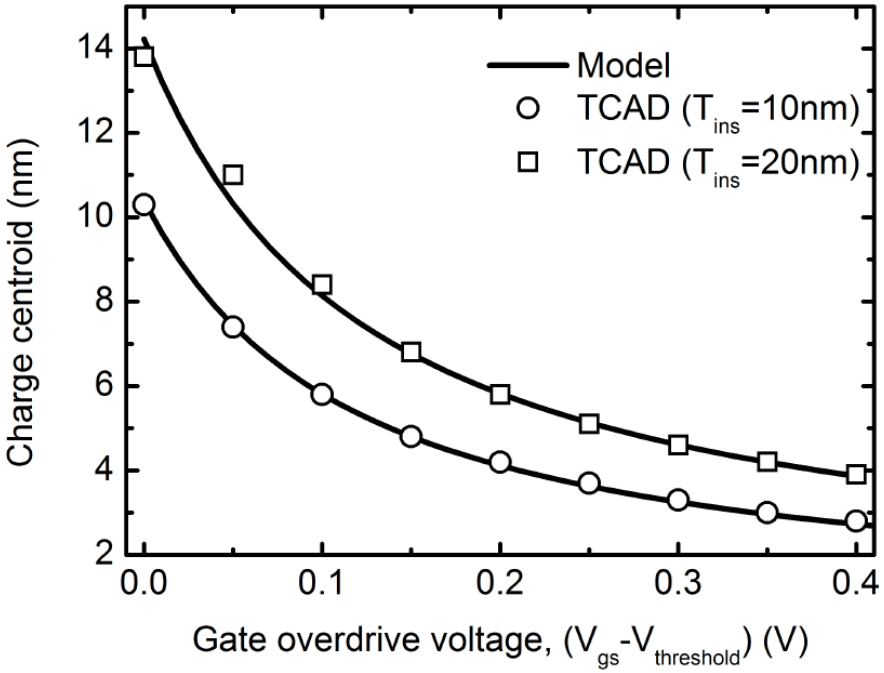
Quantum Capacitance & III-V

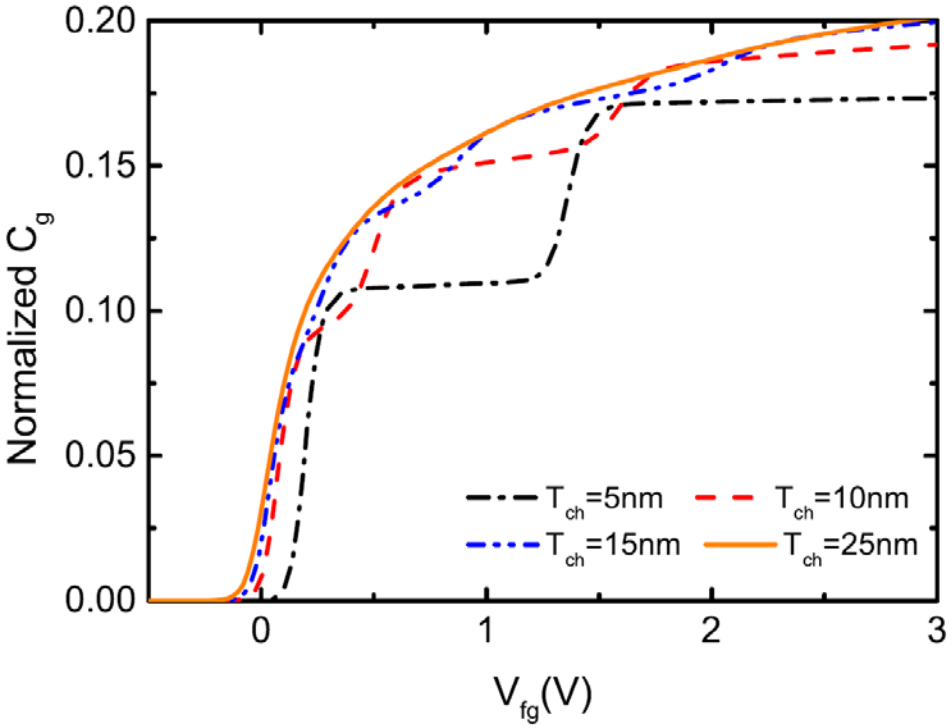
- Very strong impact on gate capacitance with low effective mass channel



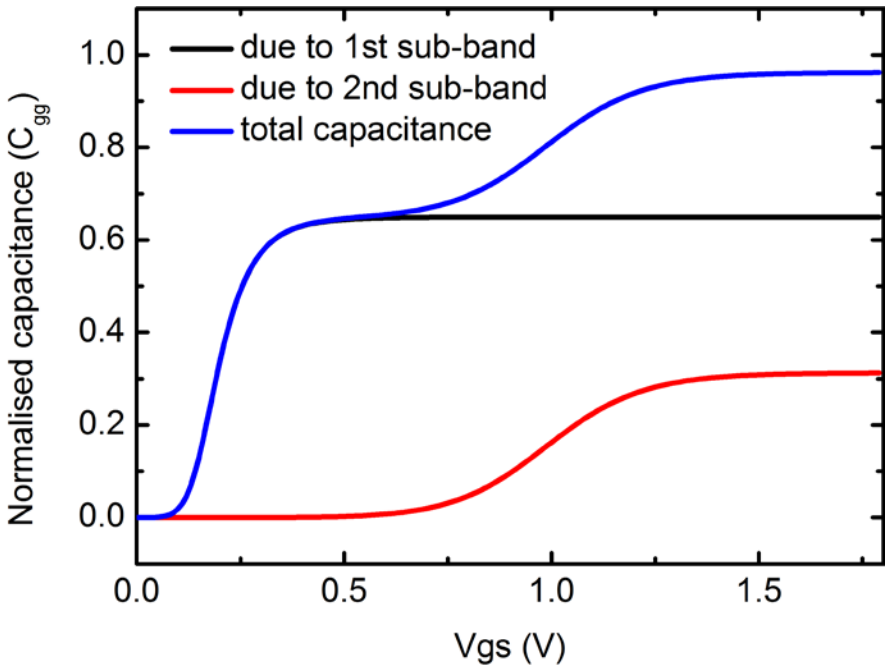
Charge centroid

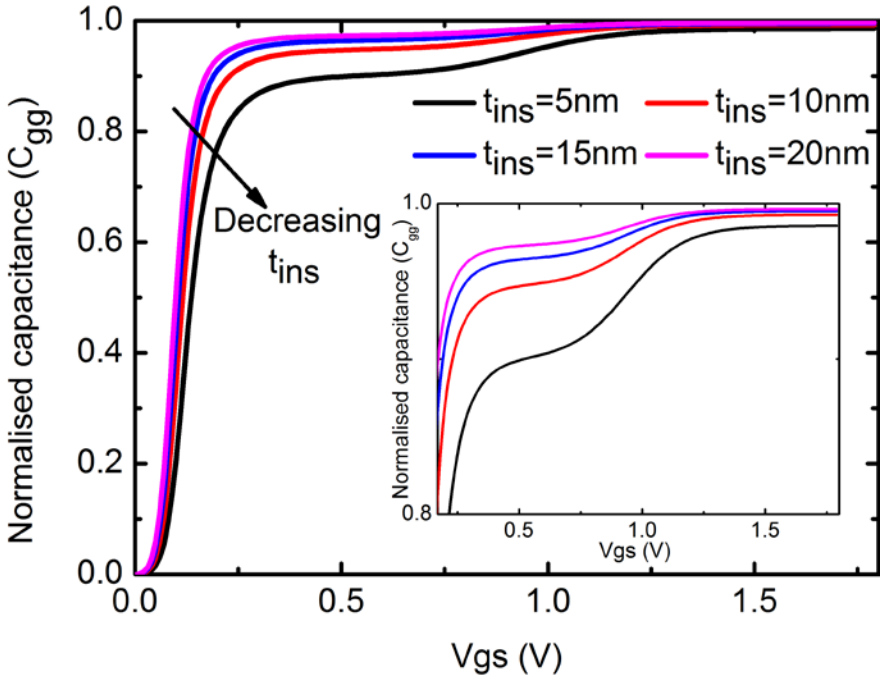
- Charge centroid in conjunction with Quantum capacitance can deteriorate C-V further.





Modeling of Quantum Capacitance in III-V FinFET



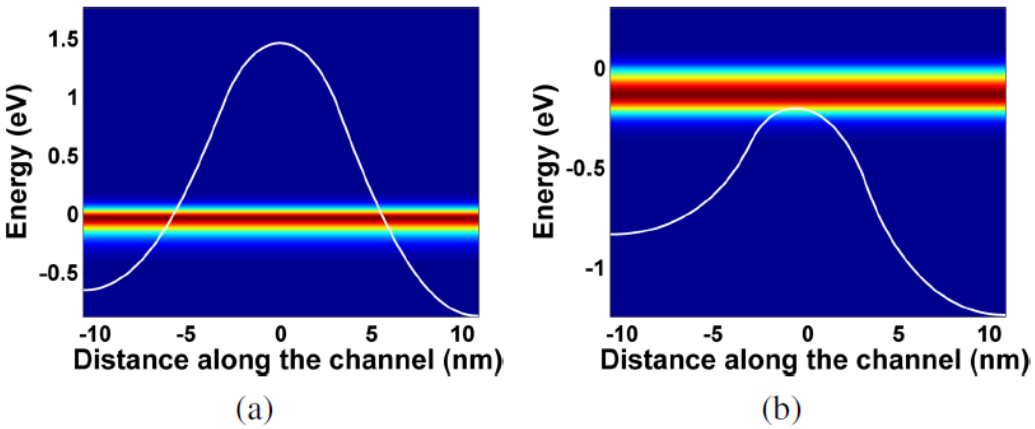


Avirup Dasgupta et. al., "Modeling of Quantum Capacitance in III-V Transistors", being submitted in IEEE EDL.

Source to Drain Tunneling in III-V FETs

- Under the barrier transport

$$T(E) = exp\left(\frac{-2}{\hbar}\int\sqrt{2m_e^*(E_{barrier}(x)-E)}\,dx\right)$$



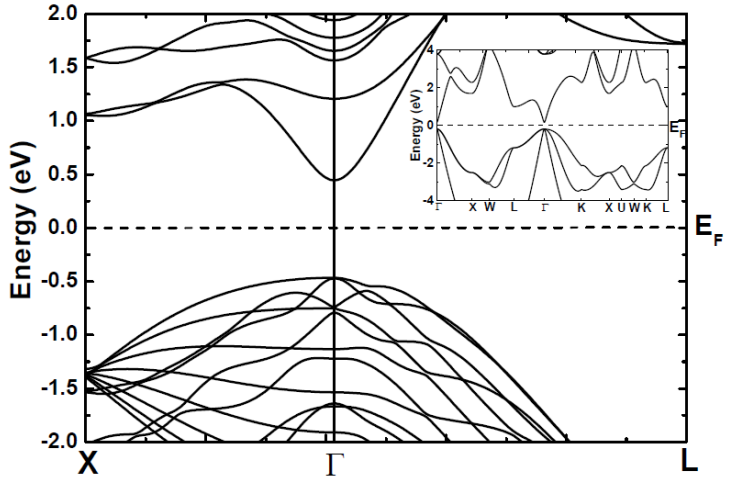
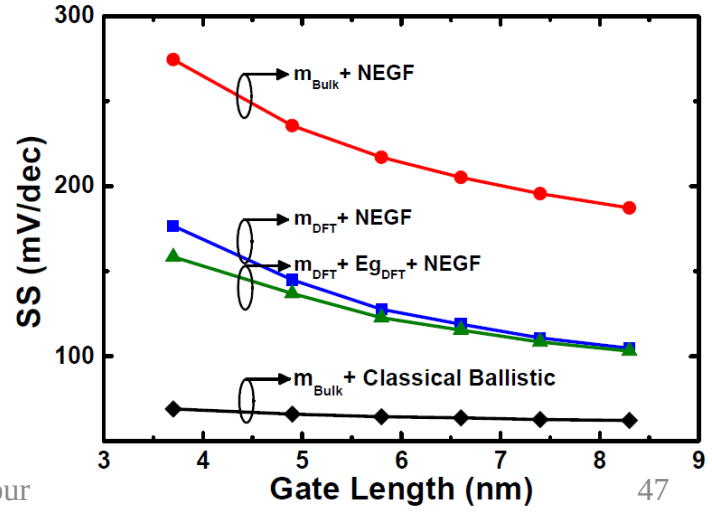


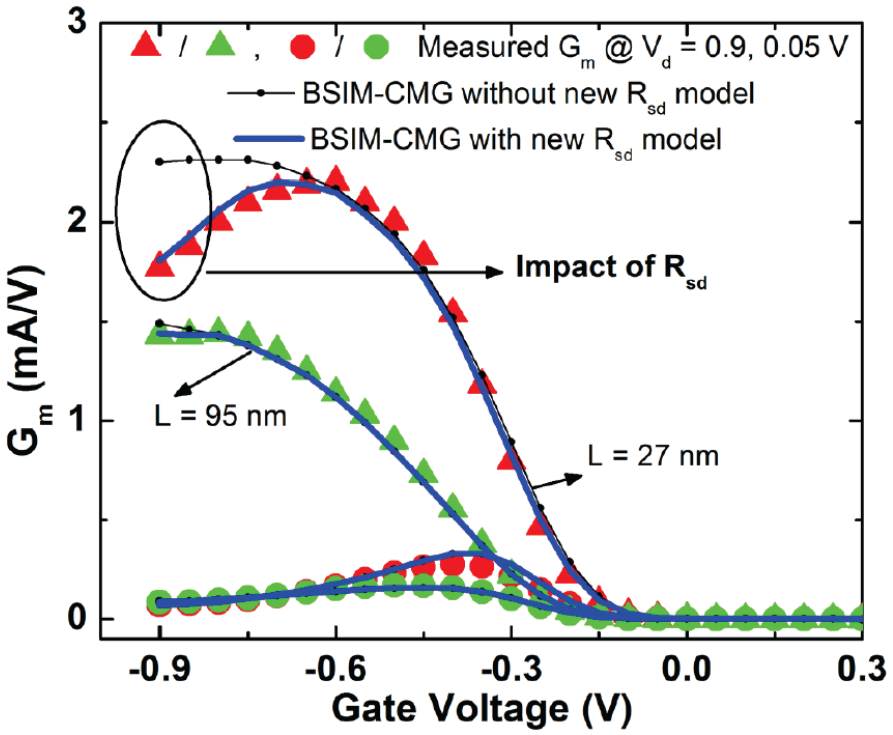
Fig. 2. Bandstructure of 2.43 nm thick InAs slab (16 atomic layers) calculated using DFT ($m_e^* = m_{DFT} = 0.0944\,\mathrm{m_0}$, $E_g = 0.91$ eV). *Inset:* InAs Bulk Bandstructure ($m_e^* = m_{Bulk} = 0.023\,\mathrm{m_0}$, $E_g = 0.35$ eV)

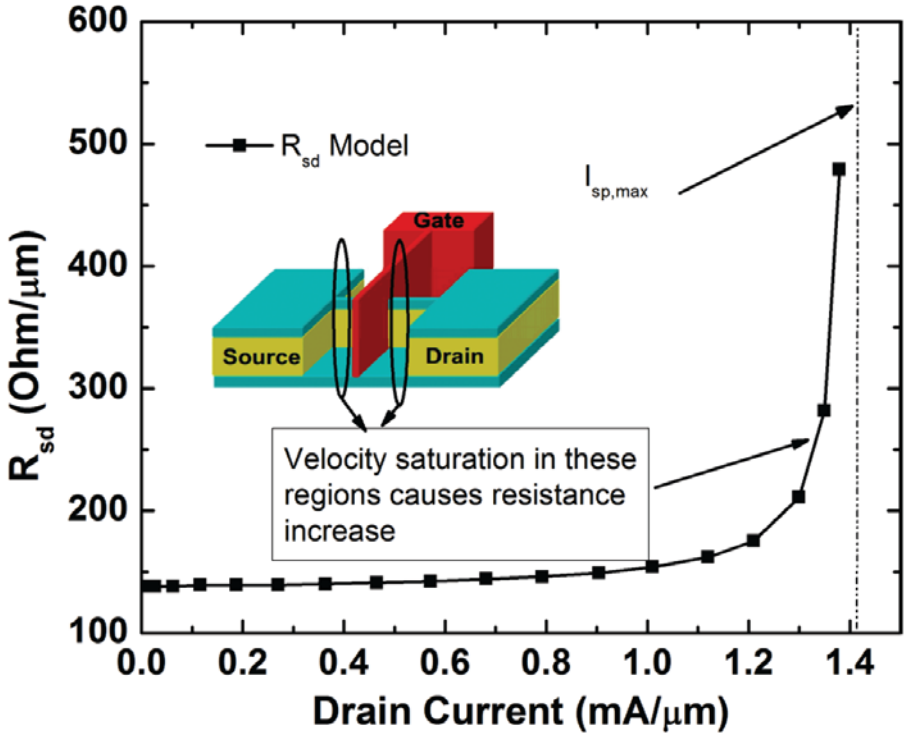


T. Dutta et. al., "Source to Drain Tunneling in III-V MOSFETs", submitted in IEEE Electron Device Letters.

Modeling SiGe FinFETs with Thin Fin

- Current Dependent Source/Drain Resistance





S. Khandelwal et. al., submitted in IEEE Electron Device Letters.

High Mobility channel

- Different materials for NMOS and PMOS
  - Complex integration
- NMOS
  - III-V materials NMOS – InAs, InGaAs etc.
- PMOS
  - Ge PMOS
  - SiGe
- Bulk mobility of Ge = 4000 > Si 1450 cm^2/V-s
- How about using Ge based CMOS?

First Experimental Demonstration of Ge CMOS Circuits from Purdue (IEDM 2014)

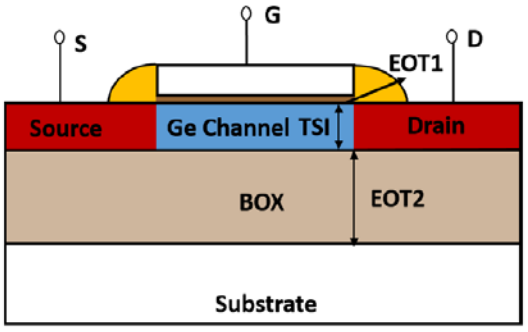
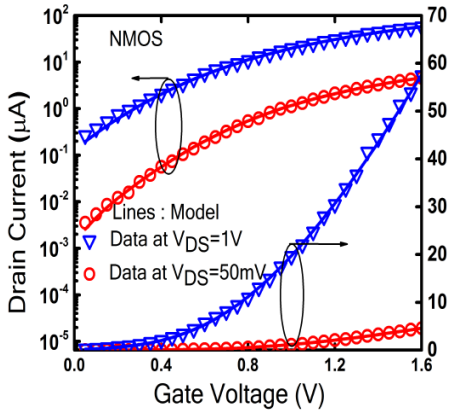
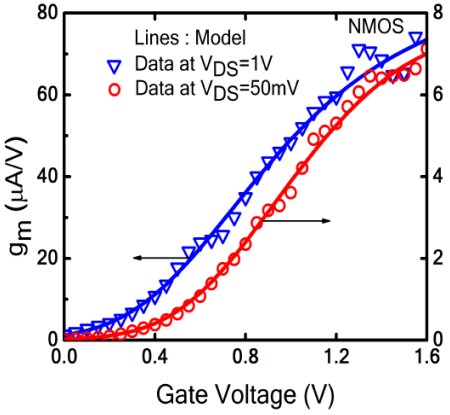
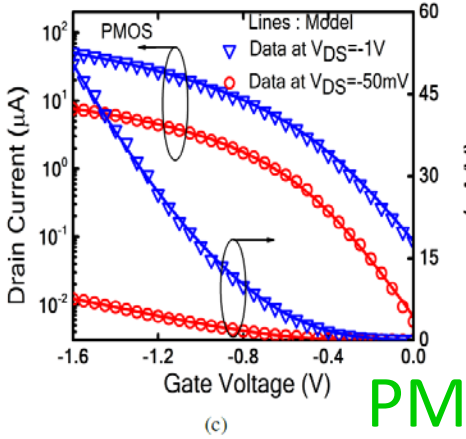


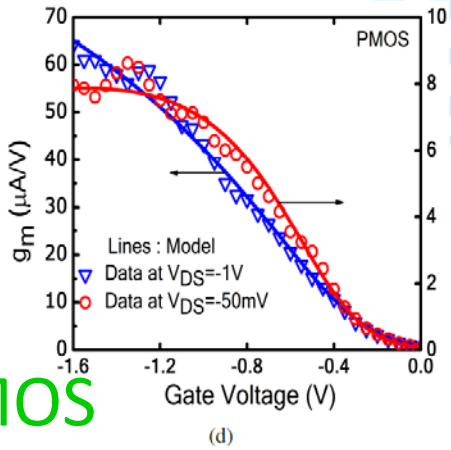
Fig. 1. Illustration of GeOI device under discussion. The device has channel length L=50nm, thickness TSI=15nm, EOT1=4.5nm, EOT2=400nm. In this letter, we are modeling the GeOI devices with industry standard BSIM-IMG model, which is a surface potential based model.



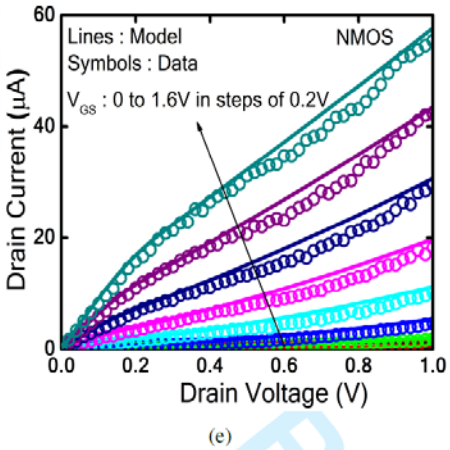


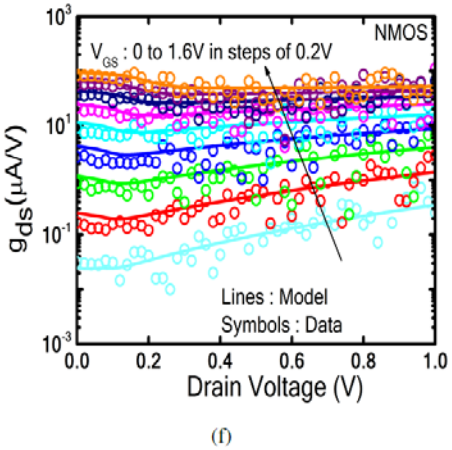
NMOS





PMOS





H. Agarwal et. al., "Modeling of Ge MOSFETs Using Industry Standard Model and Experimental CMOS Circuit Validation", submitted in IEEE Electron Device Letters.

BSIM-IMG vs. Experimental Ge circuit

Ge CMOS Inverter VTC

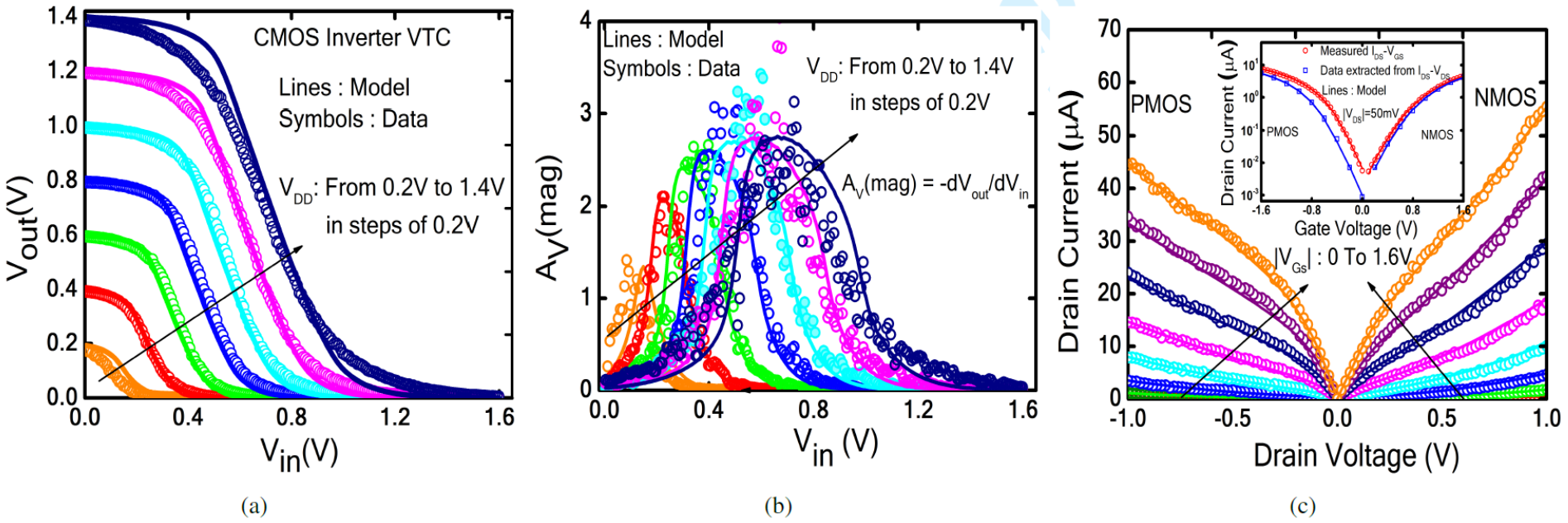
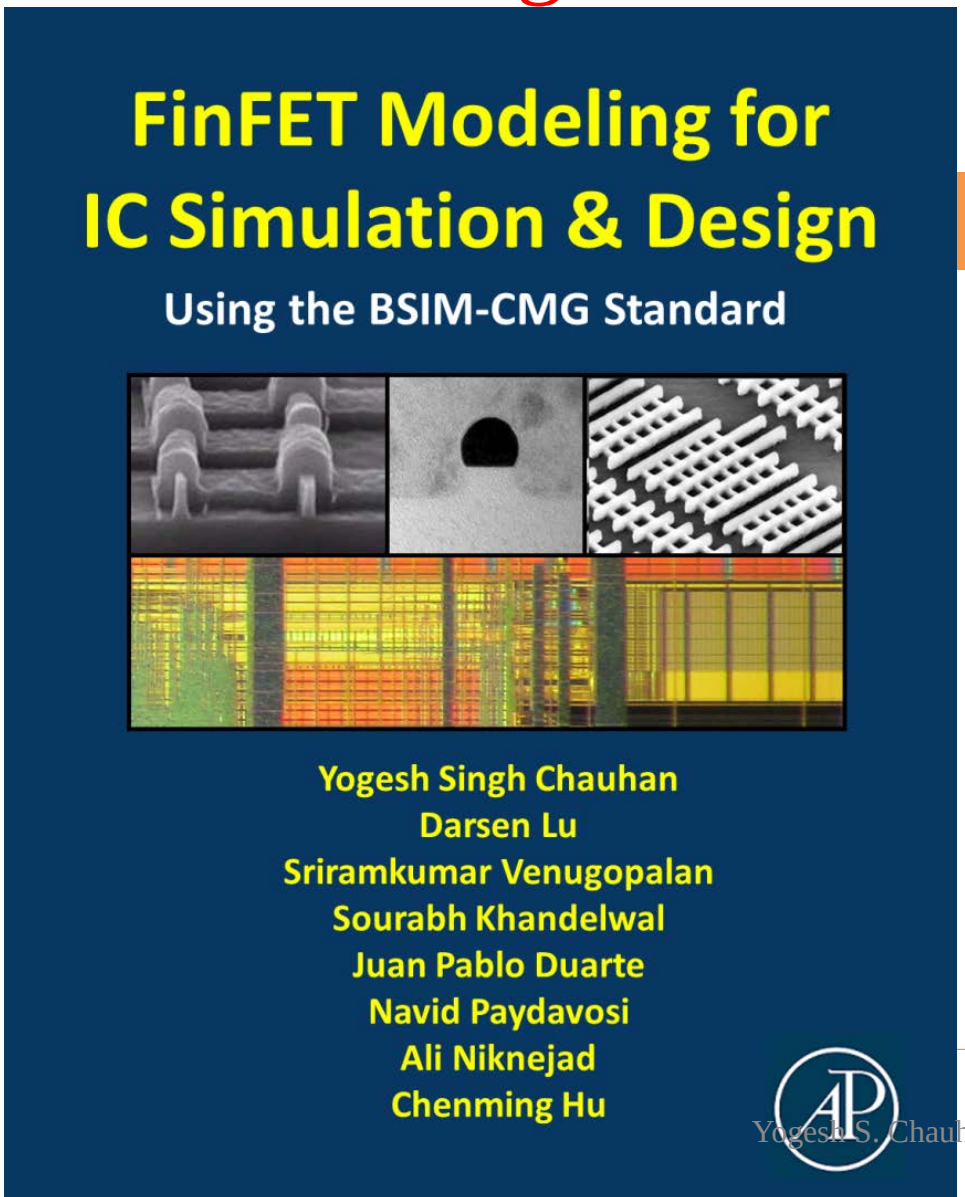


Fig. 3. BSIM-IMG model validation with GeOI CMOS inverter for V_{DD} ranging from 0.2V to 1.4V: (a) Voltage transfer characteristics (b) CMOS inverter gain vs input voltage (c) device characteristics simulated with parameter set optimized for I_{DS}-V_{DS}. The BSIM-IMG accurately models the inverter behaviour, especially for V_{DD} up to 1V. It is important to note that the static characteristics are available up to $V_{DD} = 1V$, and the model is optimized till that bias range. Inverter gain is an important parameter as it determines noise margin, and is a function of g_m and g_{ds} which are accurately modeled. Inset figure in (c) compares I_{DS} obtained from I_{DS}-V_{GS} measurement and extracted from I_{DS}-V_{DS}, highlighting the device degradation. It is observed that the threshold voltage shift is more prominent in PMOS as compared to NMOS.

H. Agarwal et. al., "Modeling of Ge MOSFETs Using Industry Standard Model and Experimental CMOS Circuit Validation", submitted in IEEE Electron Device Letters.

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

Available online on Elsevier.

Relevant Publications

- H. Agarwal, P. Kushwaha, S. Khandelwal, J. P. Duarte, Y.-K. Lin, H.-L. Chang, C. Hu, H. Wu, P. D. Ye and Y. S. Chauhan, "Modeling of GeOI and Validation with Ge-CMOS Inverter Circuit using BSIM-IMG Industry Standard Model", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
- C. Yadav, A. Agarwal, and Y. S. Chauhan, "Analysis of Quantum Capacitance Effect in Ultra-Thin-Body III-V Transistor", IEEE International Conference on VLSI Design, Kolkata, India, Jan. 2016.
- C. Yadav, J. P. Duarte, S. Khandelwal, A. Agarwal, C. Hu, and Y. S. Chauhan, "Capacitance Modeling in III-V FinFETs", IEEE Transactions on Electron Devices, Vol. 62, Issue 11, Nov. 2015.
- S. Khandelwal, J. P. Duarte, A. Medury, Y. S. Chauhan, S. Salahuddin, and C. Hu, "Modeling SiGe FinFETs with Thin Fin and Current Dependent Source/Drain Resistance", IEEE Electron Device Letters, Vol. 36, Issue 7, July 2015.
- C. Yadav, A. Agarwal, and Y. S. Chauhan, "Compact Modeling of Charge Density and Capacitance in III-V channel Double Gate FETs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- A. Dasgupta, A. Agarwal, and Y. S. Chauhan, "Compact Model for charge centroid in III-V FETs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- A. Dasgupta, A. Agarwal, and Y. S. Chauhan, "Compact Modeling of Quasi-Ballistic transport in FETs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- T. Dutta, M. Agrawal, A. Agarwal and Y. S. Chauhan, "Wavefunction Penetration Effects in Extremely Scaled III-V MOSFETs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- J. P. Duarte, S. Khandelwal, A. Medury, C. Hu, P. Kushwaha, H. Agarwal, A. Dasgupta, and Y. S. Chauhan "BSIM-CMG: Standard FinFET Compact Model for Advanced Circuit Design", IEEE European Solid-State Circuit Conference (ESSCIRC), Graz, Austria, Sept. 2015. (Invited)
- C. Yadav, A. Agarwal, Y. S. Chauhan, "Simulation study of gate capacitance with back bias effects in III-V UTB devices", SRC TECHCON, Austin, USA, September 2015.
- S. Khandelwal, J. P. Duarte, A. Medury, Y. S. Chauhan, and C. Hu, "New Industry Standard FinFET Compact Model for Future Technology Nodes", IEEE VLSI Technology symposium, Kyoto, June 2015.
- C. Yadav, P. Kushwaha, S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling of GaN based Normally-off FinFET", IEEE Electron Device Letters, Vol. 35, Issue 6, June 2014.
- S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling 20nm Germanium FinFET with the Industry Standard FinFET Model", IEEE Electron Device Letters, Vol. 35, Issue 7, July 2014.
- C. Yadav, P. Kushwaha, H. Agarwal, and Y. S. Chauhan, "Threshold Voltage Modeling of GaN Based Normally-Off Tri-gate Transistor", IEEE India Conference (INDICON), Pune, India, Dec. 2014.
- A. Dasgupta, C. Yadav, P. Rastogi, A. Agarwal, and Y. S. Chauhan, "Analysis and Modeling of Quantum Capacitance in III-V Transistors", IEEE International Conference on Emerging Electronics (ICEE), Bangalore, India, Dec. 2014. (Best Poster Award)
- S. Khandelwal, J. P. Duarte, N. Paydavosi, Y. S. Chauhan, J. J. Gu, M. Si, P. D. Ye, and C. Hu, "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Workshop on Compact Modeling (WCM), Washington D.C., USA, June 2014.
- N. Paydavosi, S. Venugopalan, Y. S. Chauhan, J. P. Duarte, S. Jandhyala, A. M. Niknejad, and C. Hu, "BSIM - SPICE Models Enable FinFET and UTB IC Designs", IEEE Access, May 2013.
- Y. S. Chauhan, S. Venugopalan, N. Paydavosi, P. Kushwaha, S. Jandhyala, J. P. Duarte, S. Agnihotri, C. Yadav, H. Agarwal, A. Niknejad, and C. Hu, "BSIM Compact MOSFET Models for SPICE Simulation", IEEE International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Gdynia, Poland, June 2013. (Invited)
- Y. S. Chauhan, S. Venugopalan, M. A. Karim, S. Khandelwal, N. Paydavosi, P. Thakur, A. M. Niknejad, and C. C. Hu, "BSIM - Industry Standard Compact MOSFET Models", IEEE European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, Sept. 2012. (Invited)