Physics and Modeling of Negative Capacitance Transistors

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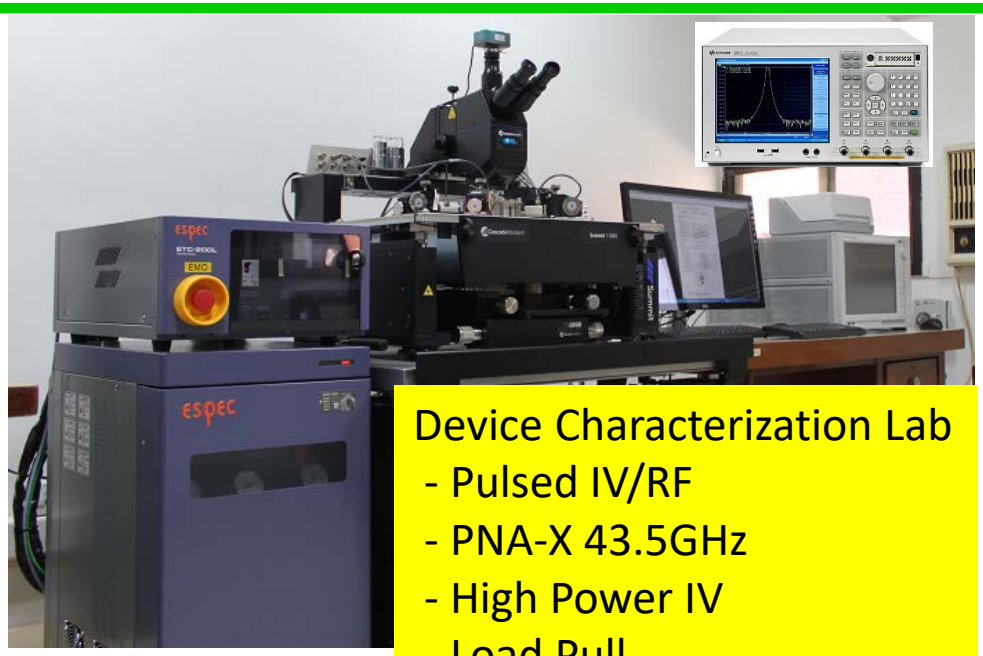
My Group and Nanolab

Current members – 30

- Postdoc – 3
- Ph.D. – 18
- Seven PhD graduated

	2018	2017	2016	2015	2014
Books	1*			1	
Journal	20	19	18	9	5
Conference	10	11	30	30	8



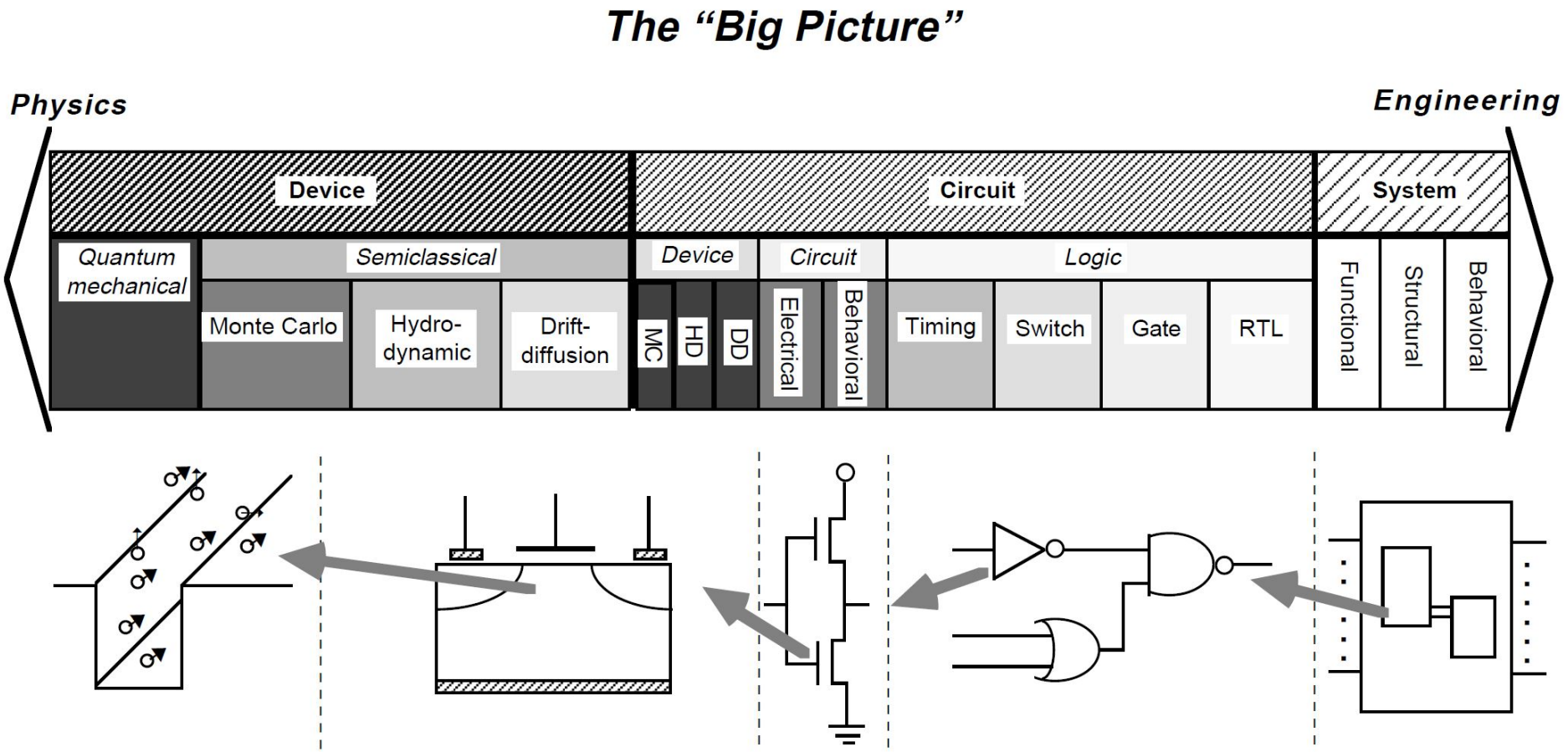
Device Characterization Lab
- Pulsed IV/RF
- PNA-X 43.5GHz
- High Power IV
- Load Pull

Joint Development & Collaboration

Outline

- Negative Capacitance and Transistor
- Modeling of NC-FinFET
- Impact of Material Parameters
- Switching Delay and Energy
- Conclusion

Spectrum of Approaches to Analyzing Electronic System



SPICE and Device Models

that the diagonal elements of the nodal admittance matrix would be

sequent spread of circuit sit tion and its negative side effec

Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.

adequate as pivot choices in effecting its factorization into lower and

the engineering intuition of ci designers.

Ron Rohrer

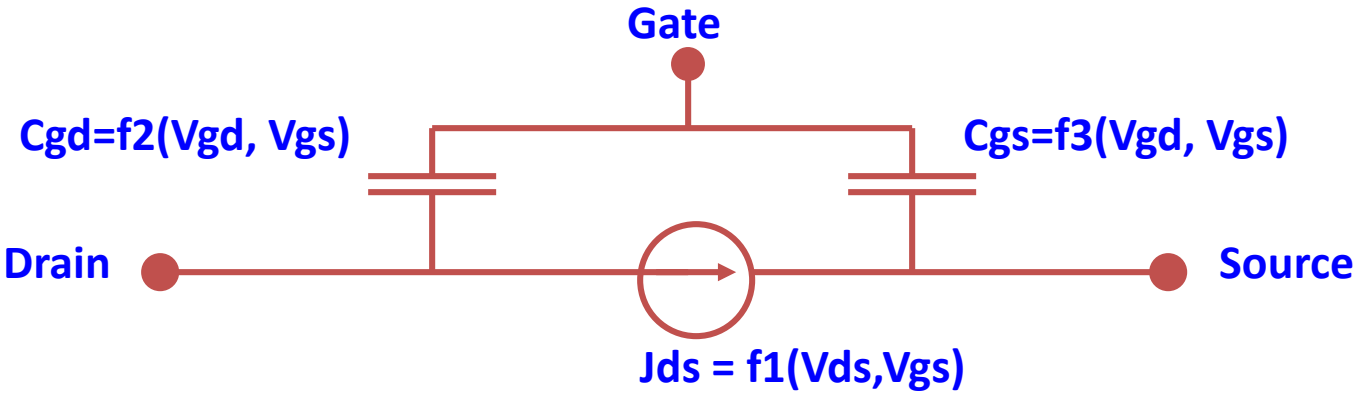
Special Issue on 40th Anniversary of SPICE

SPRING 2011 IEEE SOLID-STATE CIRCUITS MAGAZINE

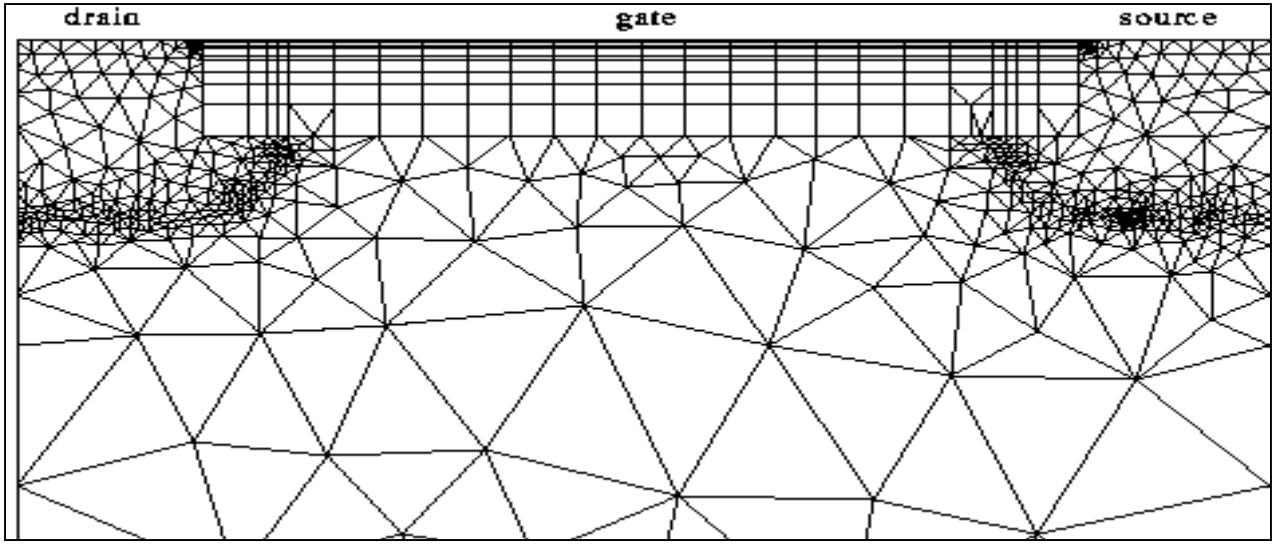
What is a Compact Model?

Compact MOSFET Model

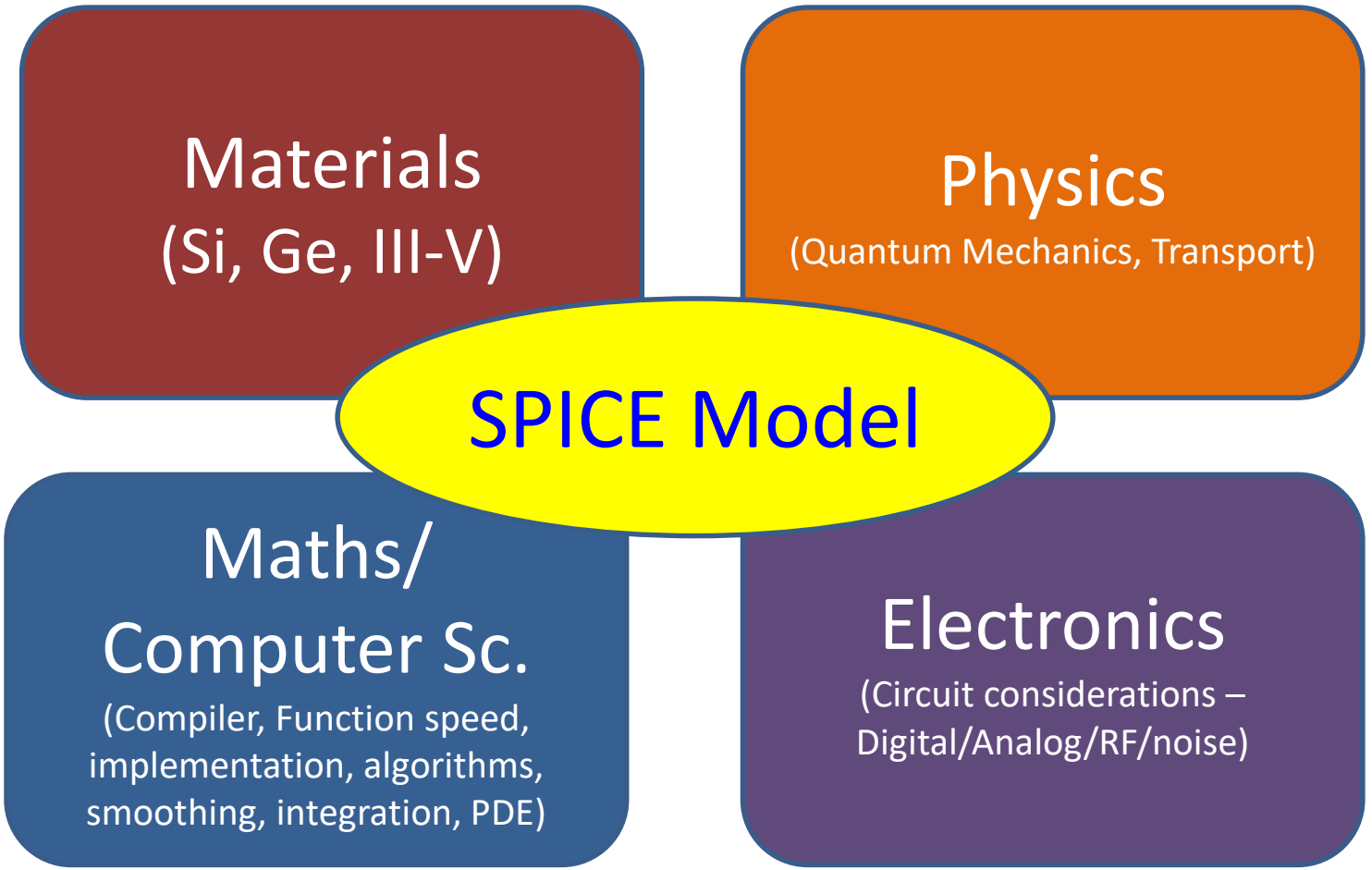
Compact Model



TCAD Model



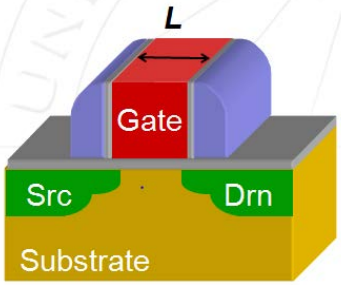
Challenges in Compact Modeling



BSIM Family of Compact Device Models

1990 1995 2000 2005 2010

BSIM1,2 BSIM3

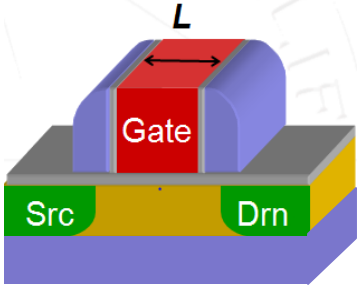


BSIM4

Conventional MOSFET

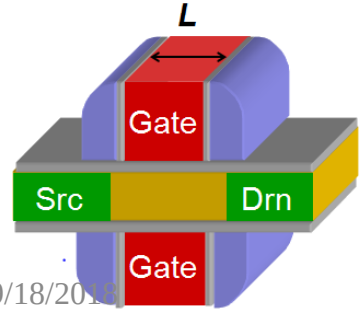
New

BSIM5 BSIM6



Silicon on Insulator MOSFET

BSIMSOI



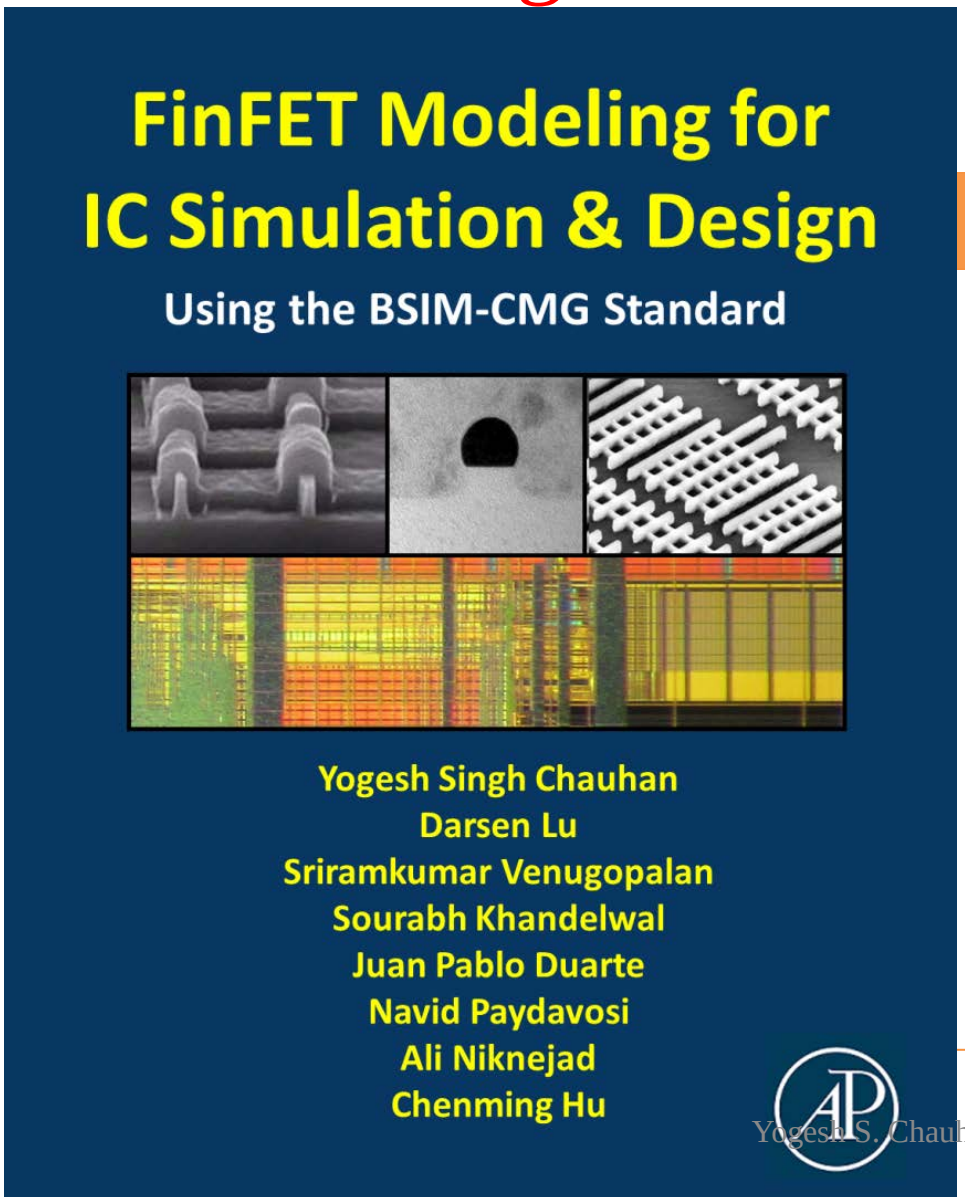
BSIM-CMG

BSIM-IMG

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



Chapters

Some Snapshots from recent work

Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

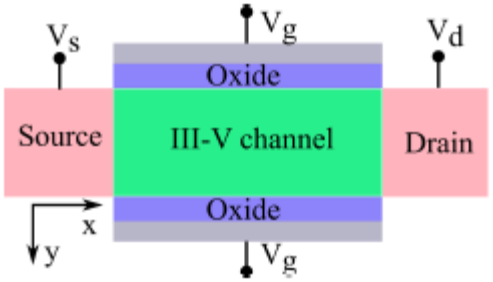
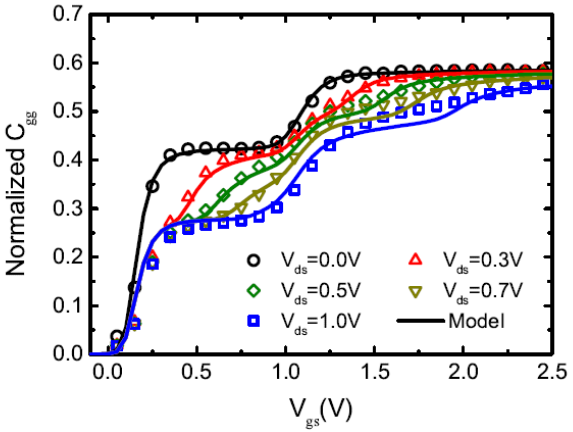
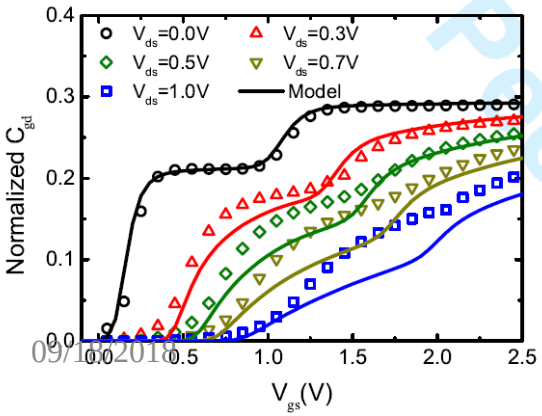
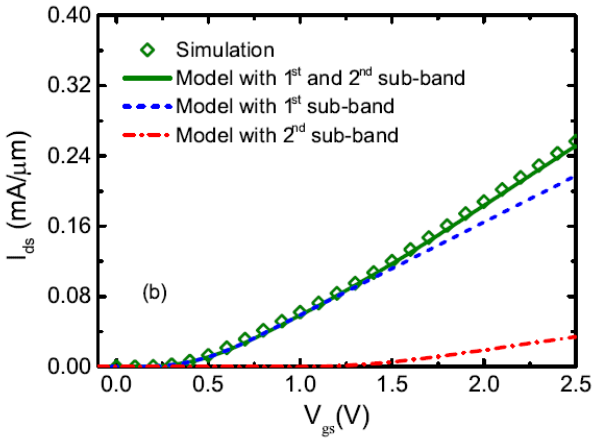
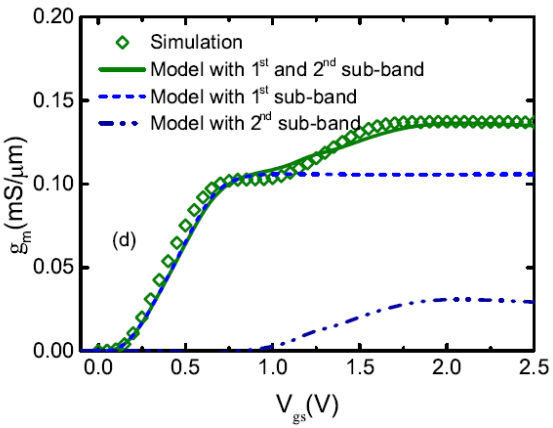


Fig. 1. Schematic of III-V channel double-gate field effect transistor (DGFET) used in the study where V_g, V_d and V_s denotes the applied voltage at gate, drain and source terminals, respectively.



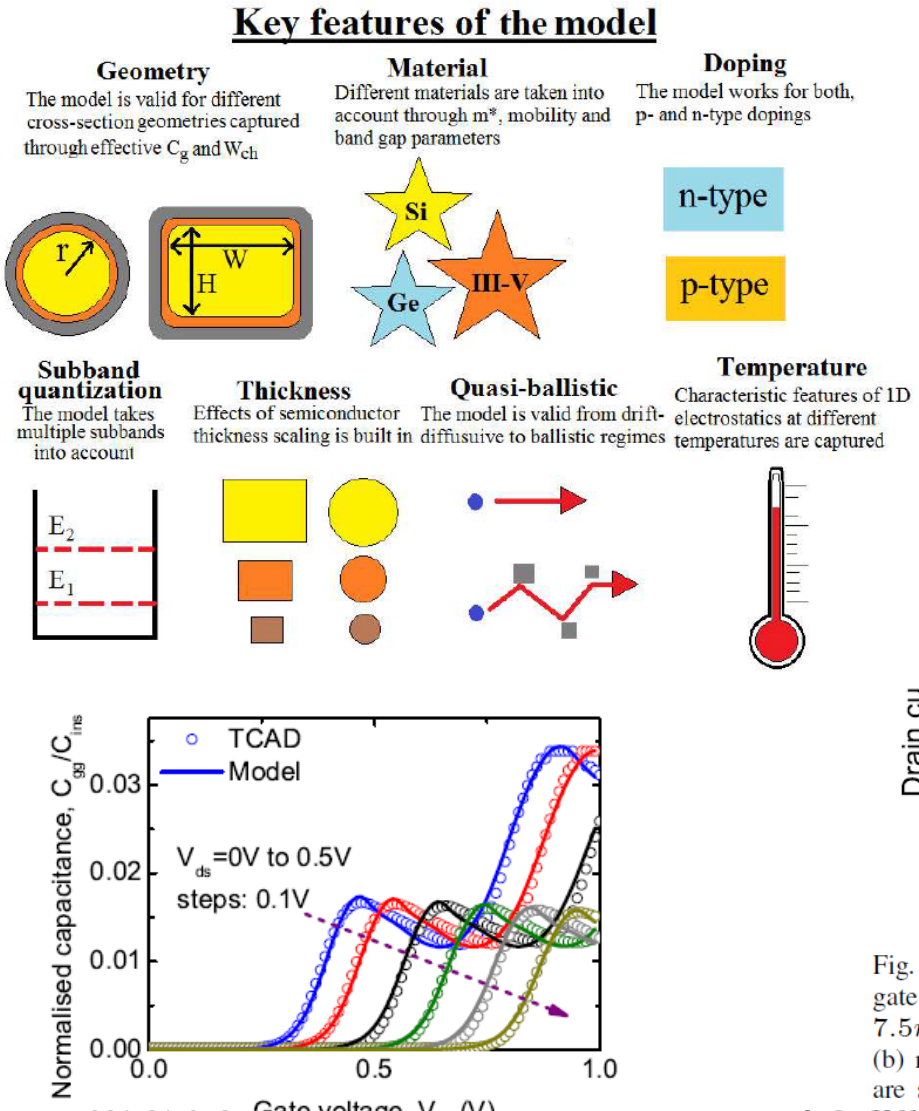


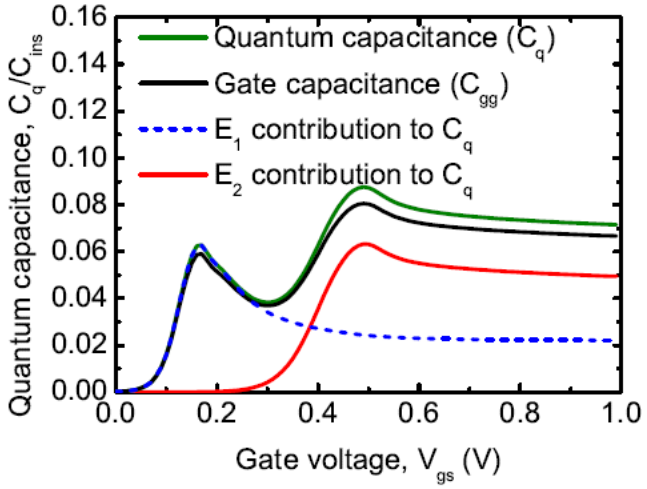


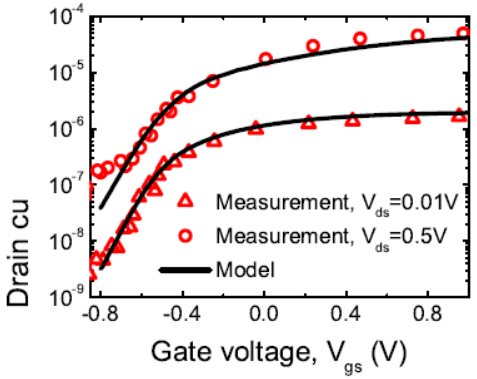


C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.

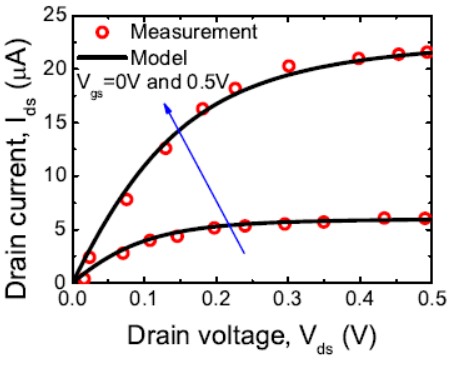
Modeling of Quasi-ballistic Nanowire FETs







(a)

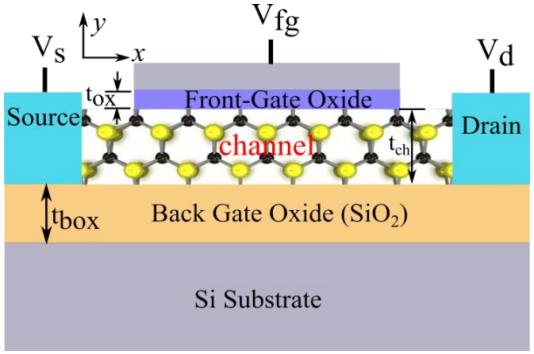


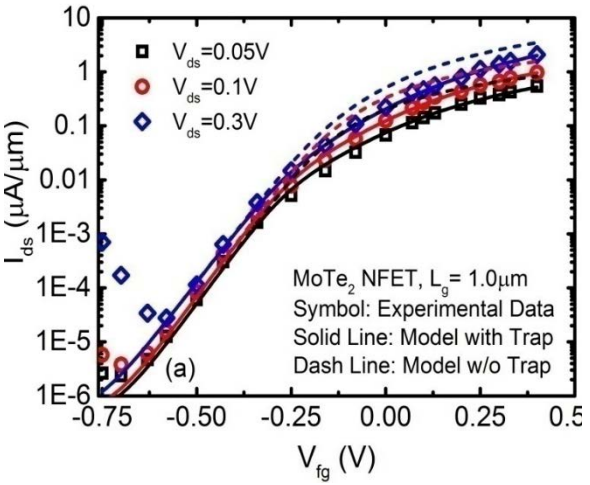
(b)

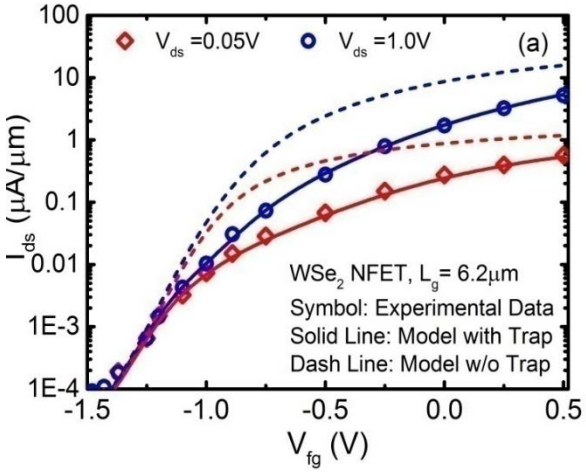
Fig. 12: **Circular quasi-ballistic InAs nanowire:** Drain current as a function of the gate and drain voltages for n-type $InAs$ nanowires, with a circular cross-section ($r = 7.5nm$), $L_g = 100nm$ and $EOT = 0.92nm$ (Device 5)[44], are shown in (a) and (b) respectively. Device works in the quasi-ballistic regime. Relevant parameter values are specified in Table II. Short channel effect related parameters have been used as in [19], [20].

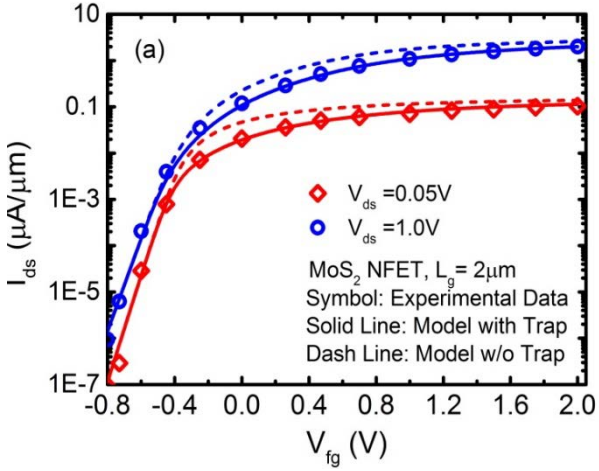
Modeling of TMD transistor

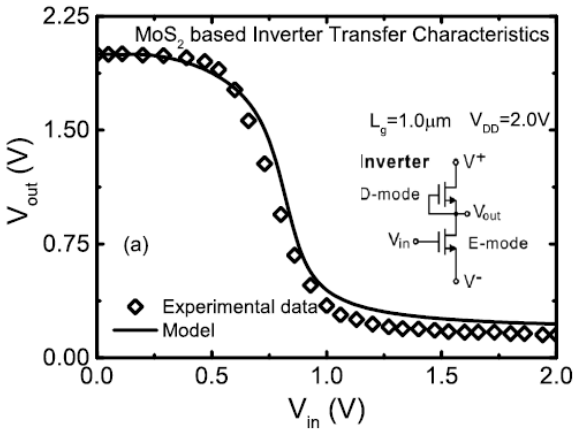
- 2D density of state
- Fermi–Dirac statistics
- Trapping effects











C. Yadav et. al. "*Compact Modeling of Transition Metal Dichalcogenide based Thin body Transistors and Circuit Validation*", IEEE TED, March 2017.

News (March 14, 2018)

- Our ASM-GaN-HEMT Model is industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

Si Compact Models

Si2 Approves IC Design Simulation Standards for Gallium Nitride Devices

March 14, 2018 / 0 Comments / in Compact Model, Frontpage /

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

http://www.si2.org/cmc/

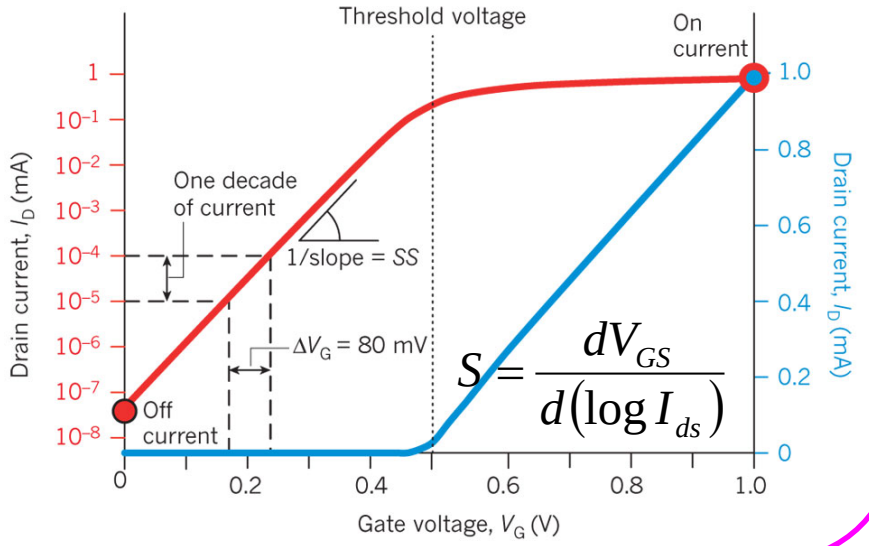
http://www.si2.org/2018/03/14/gallium-nitride-models/

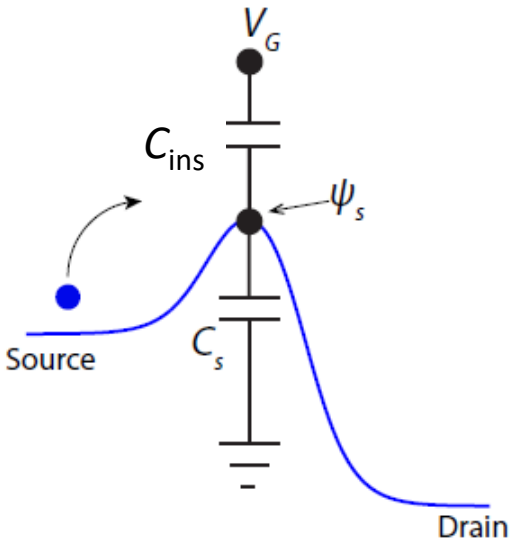
Outline

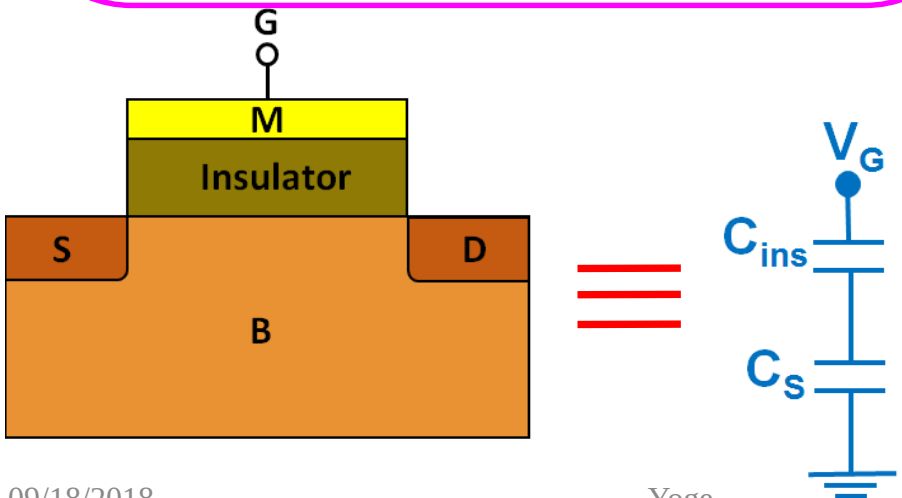
- Negative Capacitance and Transistor
- Modeling of NC-FinFET
- Impact of Material Parameters
- Switching Delay and Energy
- Conclusion

Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.







$$S = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial \psi_S} \frac{\partial \psi_S}{\partial \log_{10} I_D}$$

$$= \left(1 + \frac{C_S}{C_{ins}}\right).60\text{mV/decade}$$

As $1 + \frac{C_S}{C_{ins}} \geq 1$, $S \geq 60mV/decade$

Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as

- Definition 1: $C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1}$ = inverse curvature of free energy density
- Definition 2: $C_{ins} = \frac{\partial P}{\partial E}$ = slope of the polarization vs electric field curve

where P = Polarization in dielectric, G = Free energy density and E = Externally applied electric field

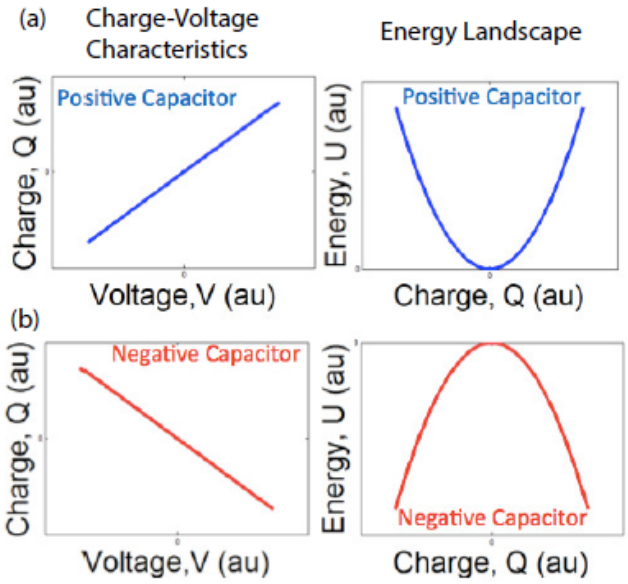
- Two types of non-linear dielectrics:
  - Paraelectric : No polarization when electric field is removed.
  - Ferroelectric : Two possible states of polarization when electric field is removed.

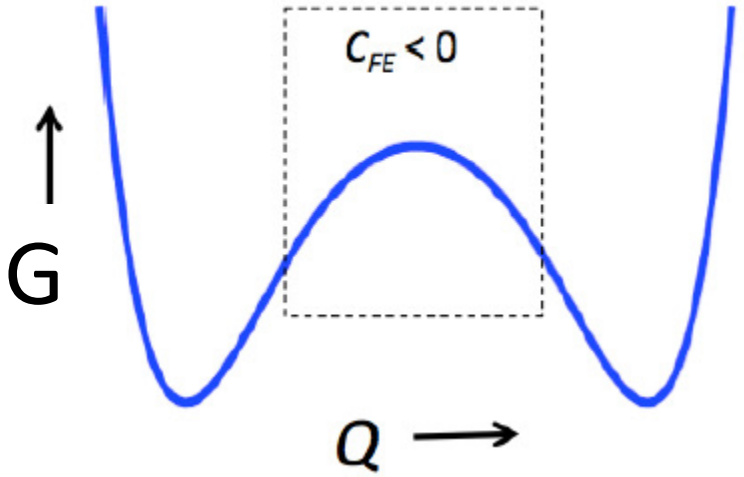
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!

  $C_{ins} < 0$ and $\frac{C_S}{C_{ins}} < 0$, then $\left(1 + \frac{C_S}{C_{ins}}\right) < 1$ → $S < 60\text{mV/decade}$

- For a capacitor
  - Energy $G = \frac{Q^2}{2C}$ → Capacitance $C = {}^{1}\Big/_{\frac{d^2G}{dQ^2}} = 1/Curvature$





Energy landscape of ferroelectric materials.

$Q = \epsilon E + P \cong P$

Ref. – S. Salahuddin et. al., *Nano Letters,* 2008.

Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- In general, α and β can be +ve or –ve but γ is always +ve for stability reasons.
- Dynamics of G is given by $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$

δ = Polarization damping factor

- In the steady state, $\frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

For $\alpha > 0$ and at $E = 0$, there exit only one real root

$P = 0$

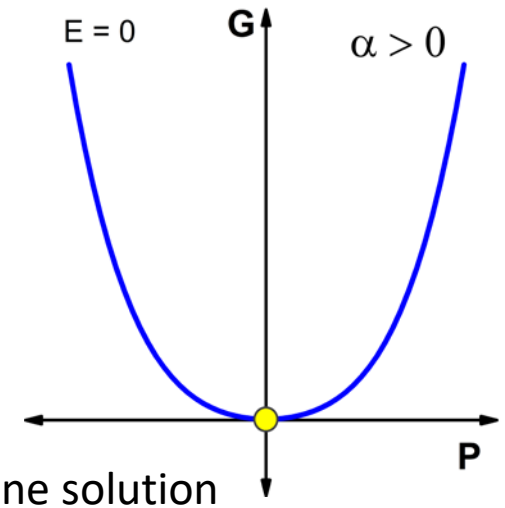
A Paraelectric Material

For $\alpha < 0$ and at $E = 0$, there exit three real roots

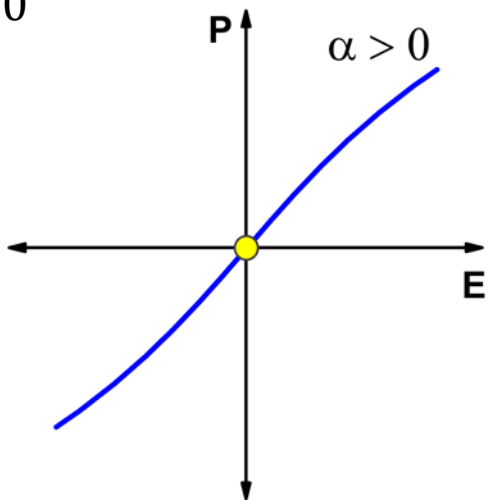
$P = 0, \pm P_r$ where $P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$

A Ferroelectric Material has a non-zero P at zero E.

Positive and Negative Capacitances

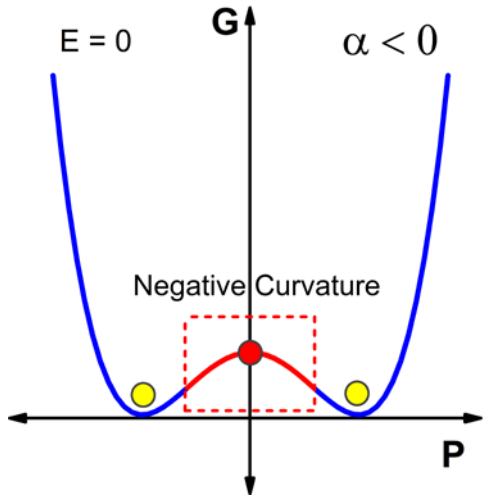


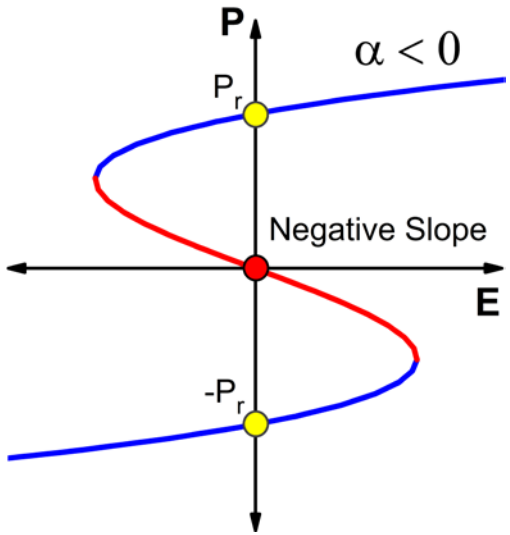
Only one solution at $E = 0$



Paraelectric

A Positive Capacitor





Ferroelectric

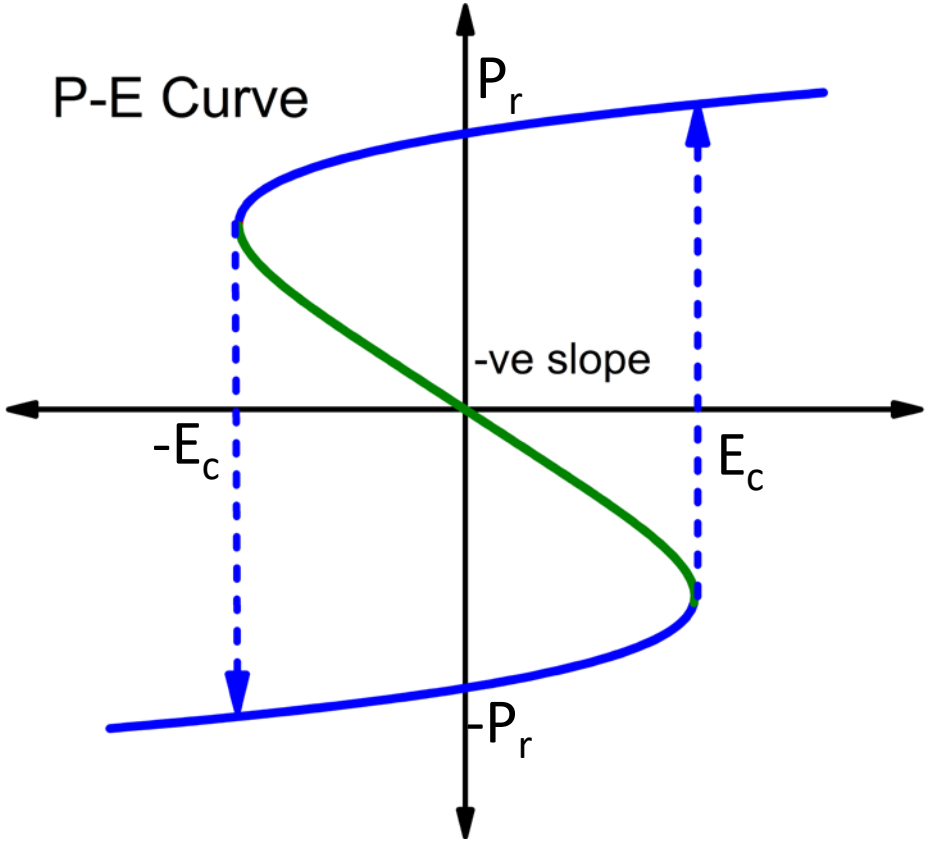
A Conditionally Negative Capacitor

Three possible solutions at $E = 0$

$P = 0$ is not possible in a isolated Ferroelectric due to maxima of energy or a negative capacitance

$$C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1} = \frac{\partial P}{\partial E} < 0$$

Negative Capacitance in Ferroelectric



$$C_{ins} = C_{fe}$$

-ve slope region can be stabilized if

$$C_{GG} = \left(\frac{1}{-|C_{fe}|} + \frac{1}{C_S}\right)^{-1} > 0$$

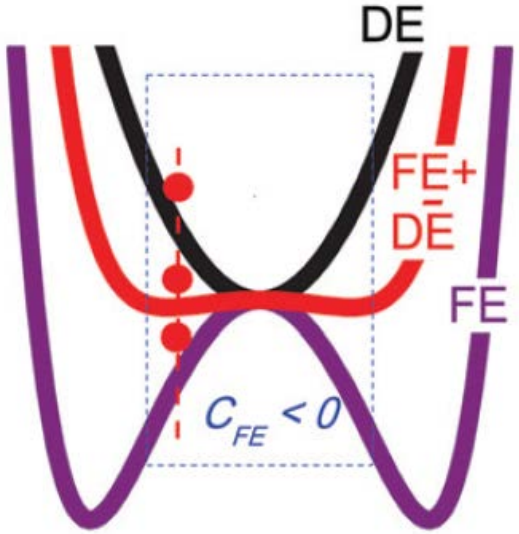
or,

$$|C_{fe}| > C_S$$

S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008.

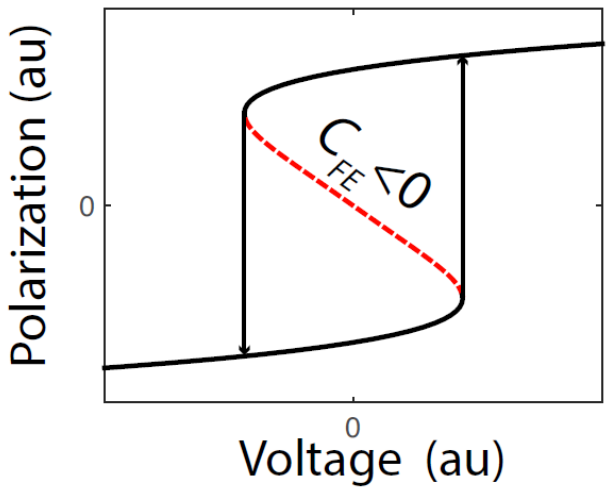
How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

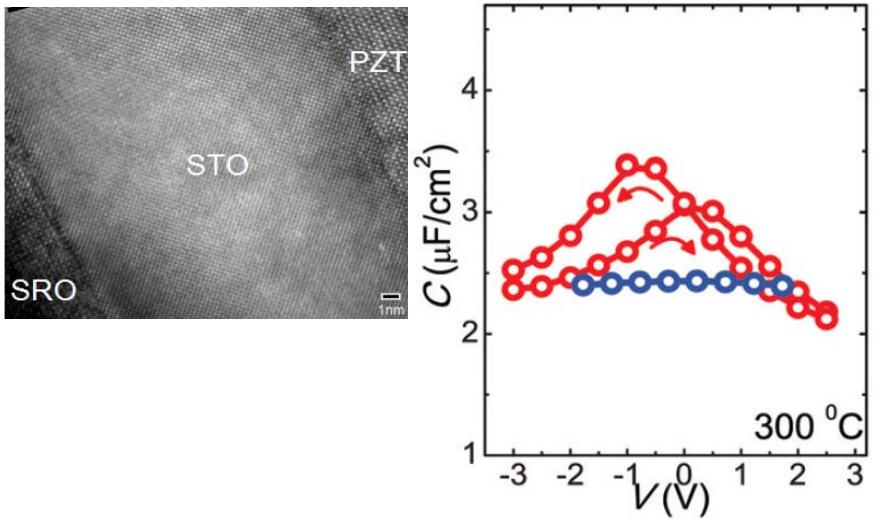


A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011

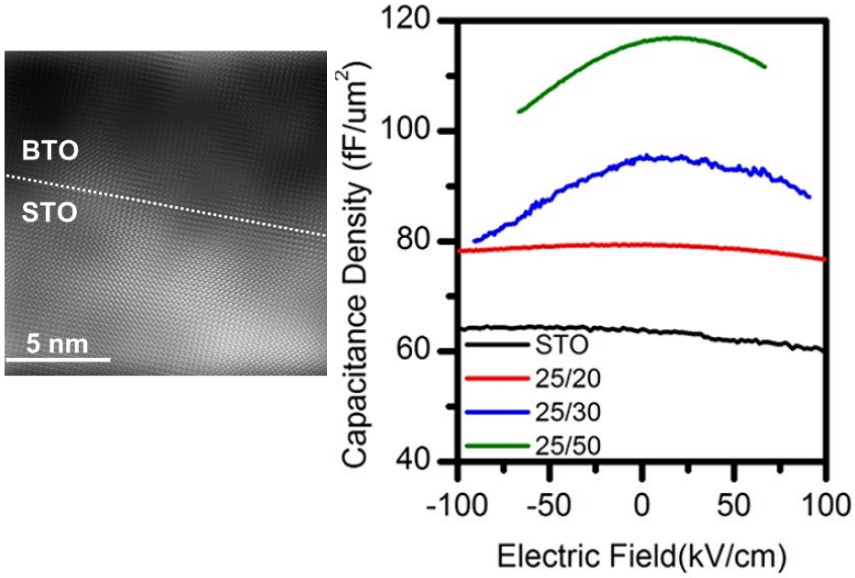
- $\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0$
- $C_{DE} < |C_{FE}|$ and $C_{FE} < 0$
- $C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0$



Ferroelectric-Dielectric Systems



A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011.



D. J. Appleby et al., Nano Letters, vol. 14, no.7, pp. 3864–3868, 2014.

Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.

$$C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$$

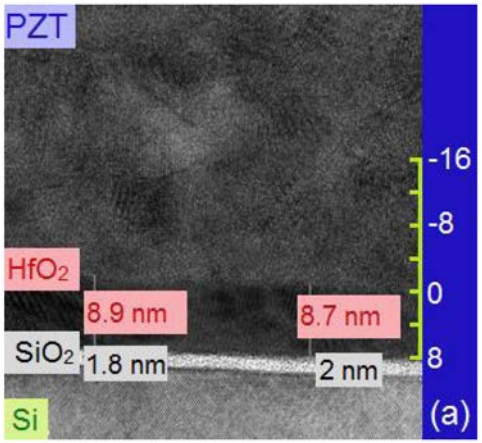
Negative Capacitance FETs

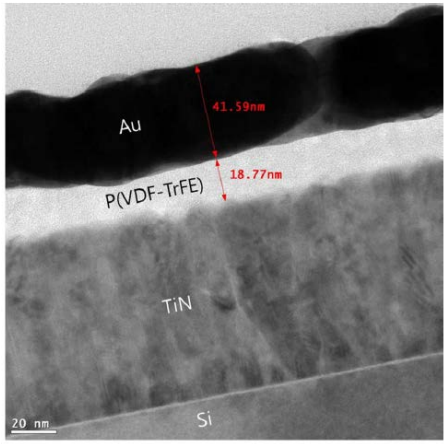
$PbZr_{0.52}Ti_{0.48}O3$ FE with HfO_2 buffer interlayer

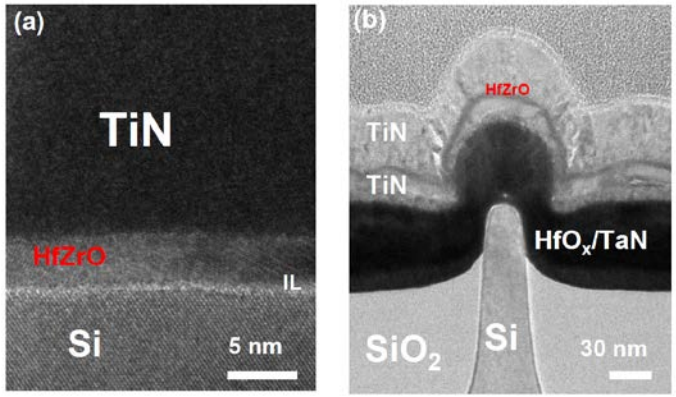
$P(VDF_{0.75}\text{-}TrFE_{0.25})$ Organic Polymer FE

HfZrO FE

CMOS compatible FE







S. Dasgupta et al., IEEE JESCDC, 2015.

J. Jo et al., Nano Letters, 2015

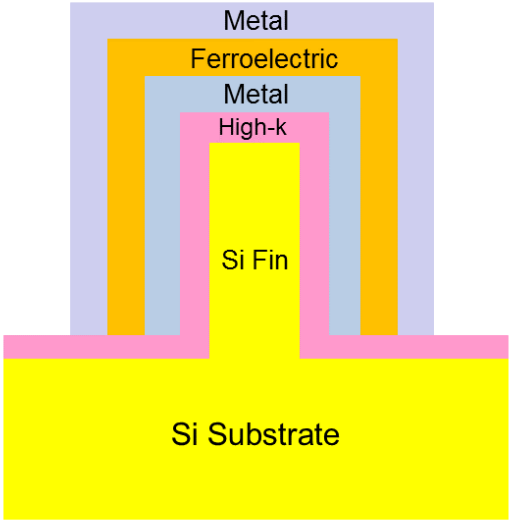
K.-S. Li et al., in IEEE IEDM, 2015.

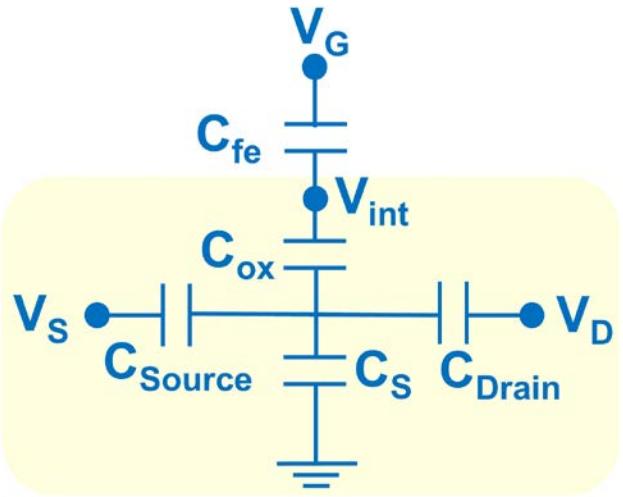
Outline

- Negative Capacitance and Transistor
- Modeling of NC-FinFET
- Impact of Material Parameters
- Switching Delay and Energy
- Conclusion

Device Structure

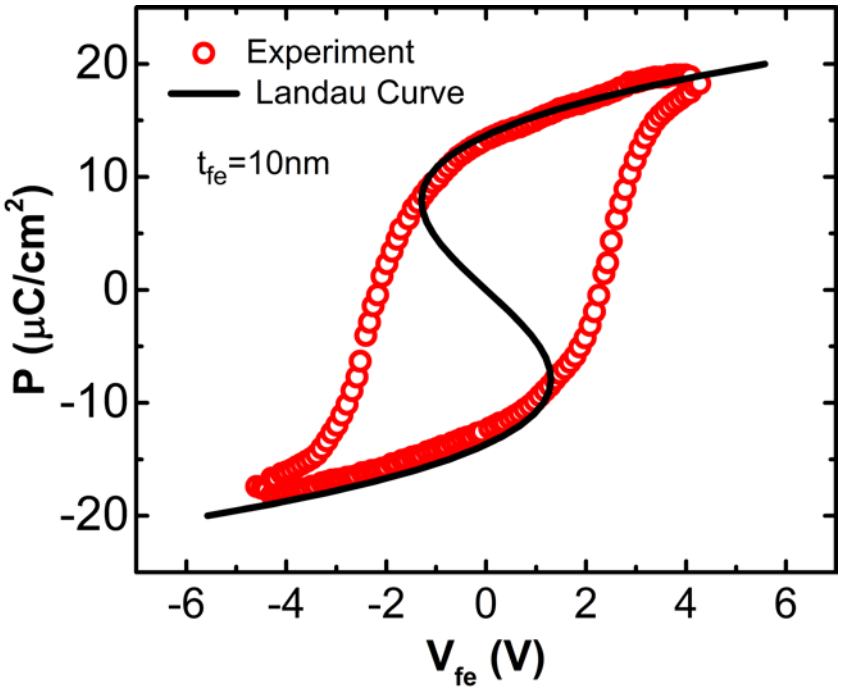
Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)





- Metal internal gate provides an equipotential surface with a spatially constant V_{int}.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.

Experimental Calibration of L-K Model



Calibration of L-K with P-V_{fe} curve for Y-HfO2 with 3.6 mol% content of $YO_{1.5}$[3]

$\alpha = -1.23 \times 10^9$ m/F

$\beta = 3.28 \times 10^{10}$ m/F

$\gamma = 0$ (2nd order phase transition)

Gibb's Energy,

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

Dynamics of G is given by

$$\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$$

In the steady state, $\frac{dP}{dt} = 0$

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$

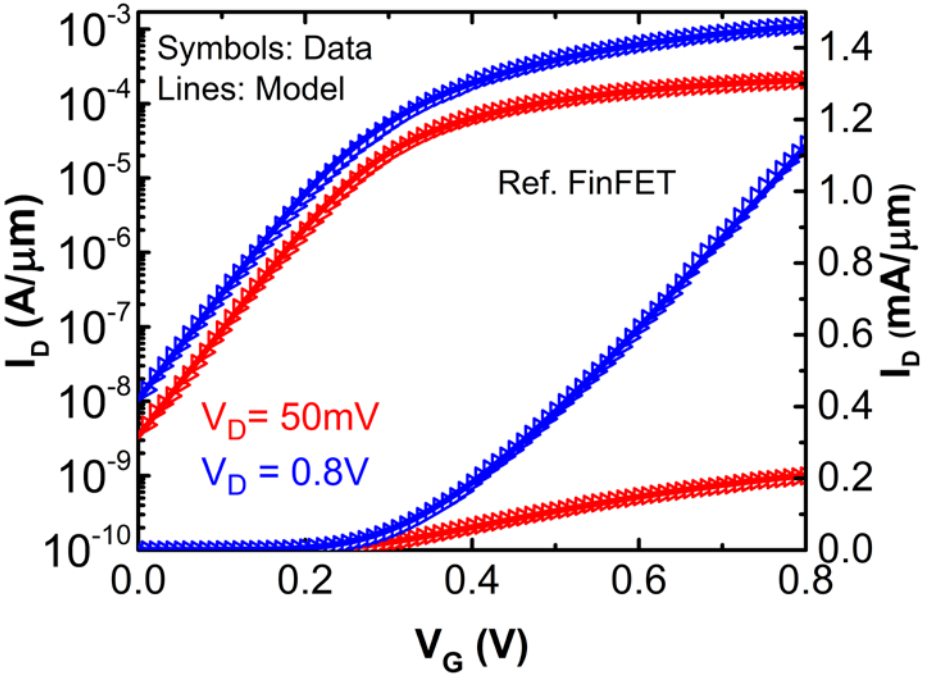
[1] Devonshire et al., The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 40, no. 309, pp. 1040–1063, 1949.

*[2] Landau, L. D. & Khalatnikov, I. M. On the anomalous absorption of sound near a second order phase transition point. Dokl. Akad. Nauk **96,** 469472 (1954).*

[3] J. M¨uller et al., JAP, vol. 110, no. 11, pp. 114113, 2011.

Calibration of Baseline FinFET

Calibration of baseline FinFET with
22 nm node FinFET.



BSIM-CMG model is used to model baseline FinFET.

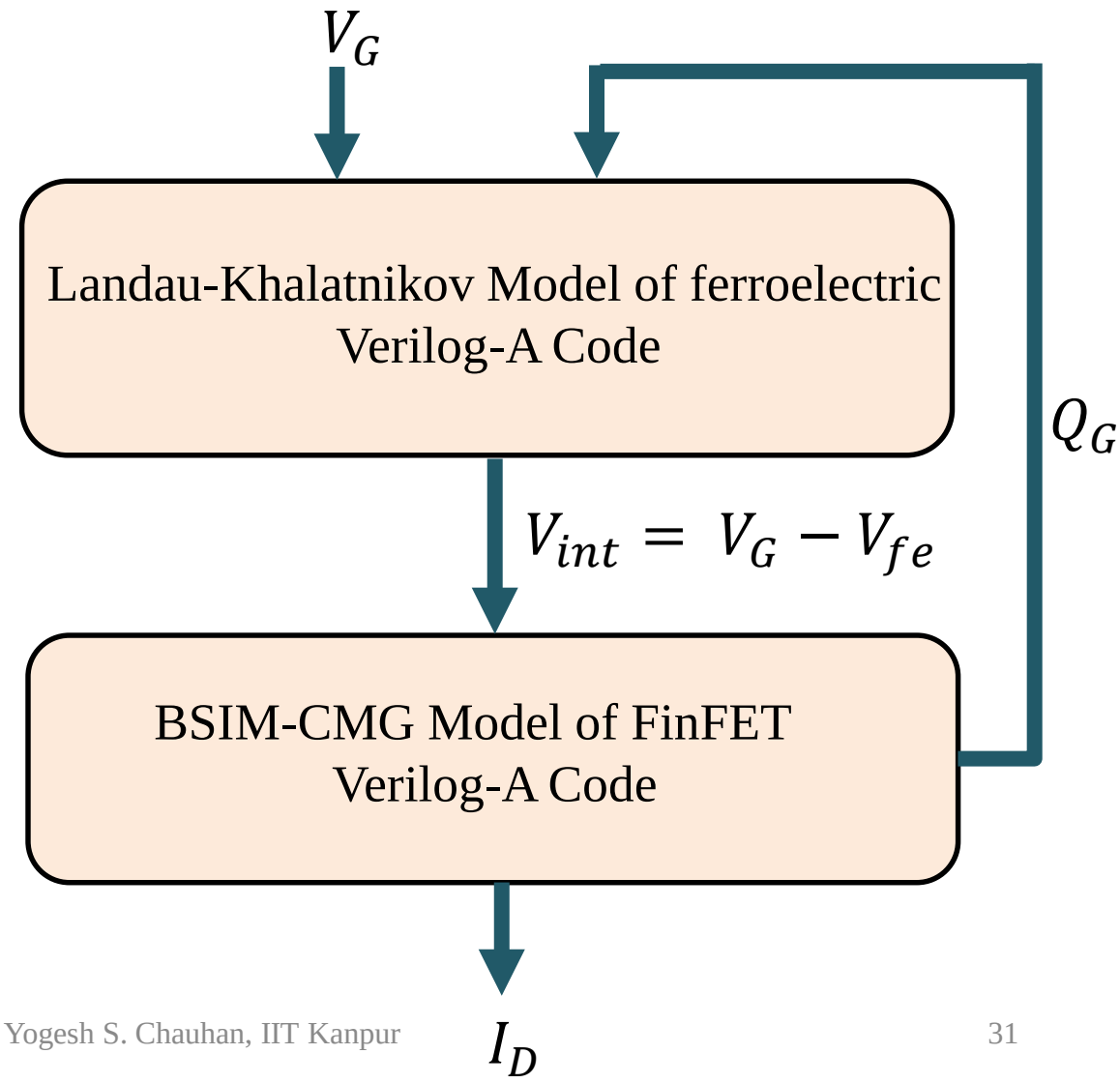
Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

C. Auth et al., in VLSIT, 2012, pp. 131–132.

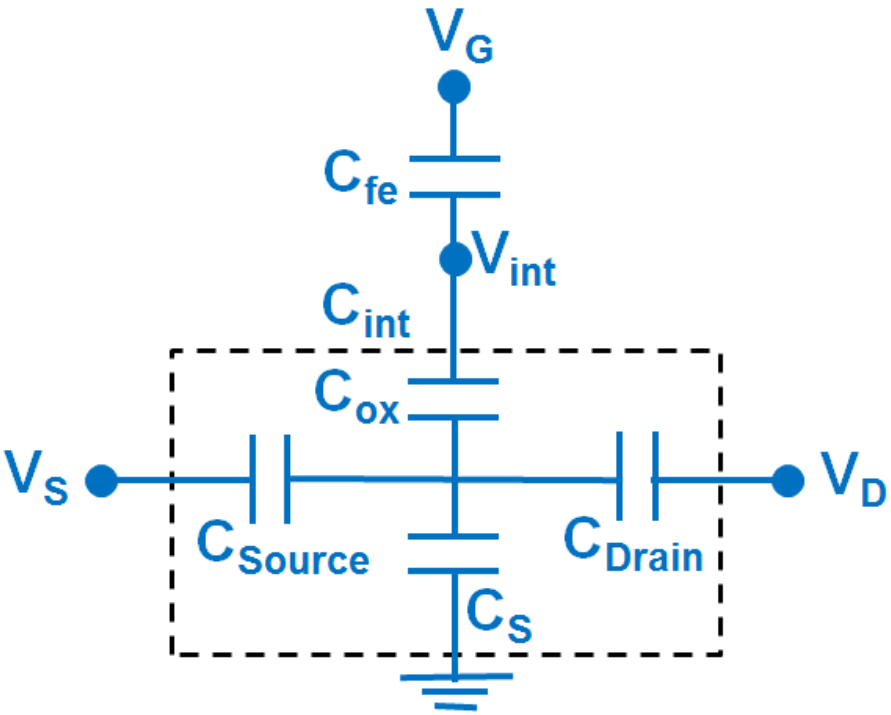
Complete Modeling Flowchart

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$



Capacitances and Voltage Amplification



$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

$$C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)}$$

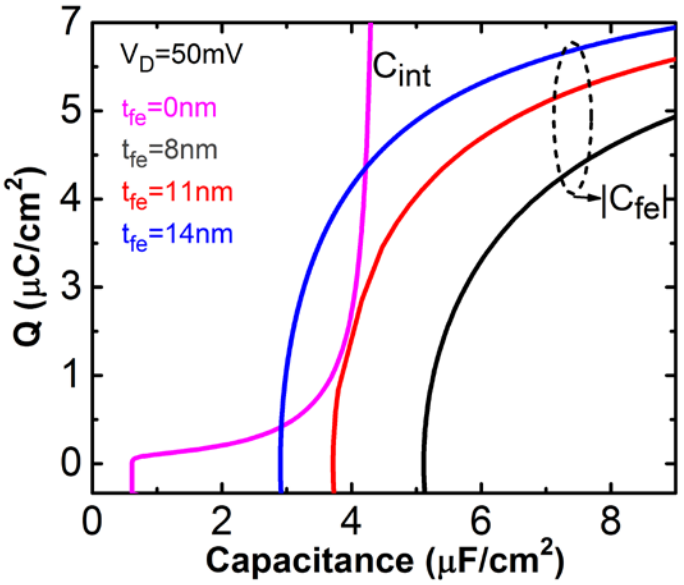
$$\frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}}$$

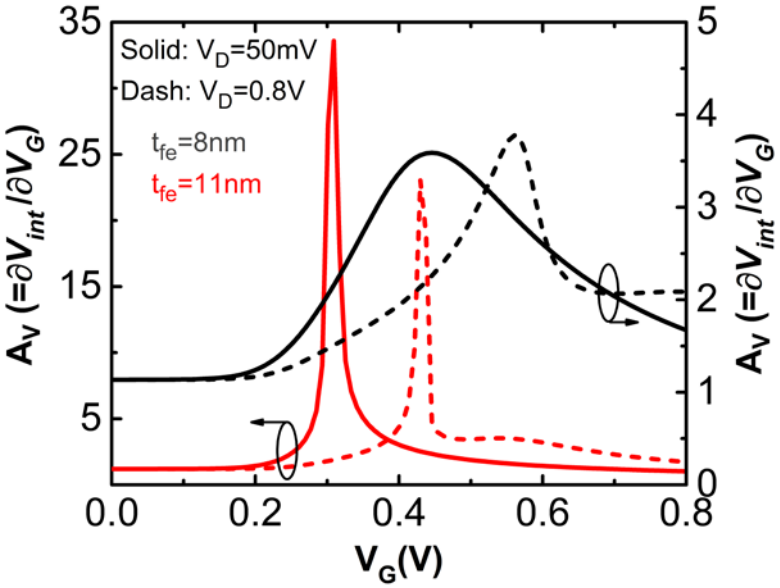
Capacitance matching between $|C_{fe}|$ and C_{int} increases the gain.

Internal Voltage Gain,

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

Capacitance Matching





- Capacitance matching increases with t_{fe} which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.

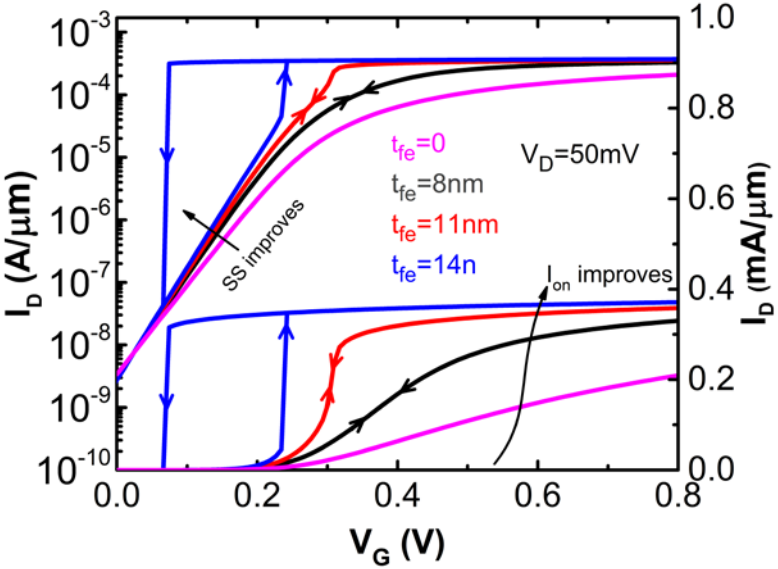
- Increase in V_D reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.

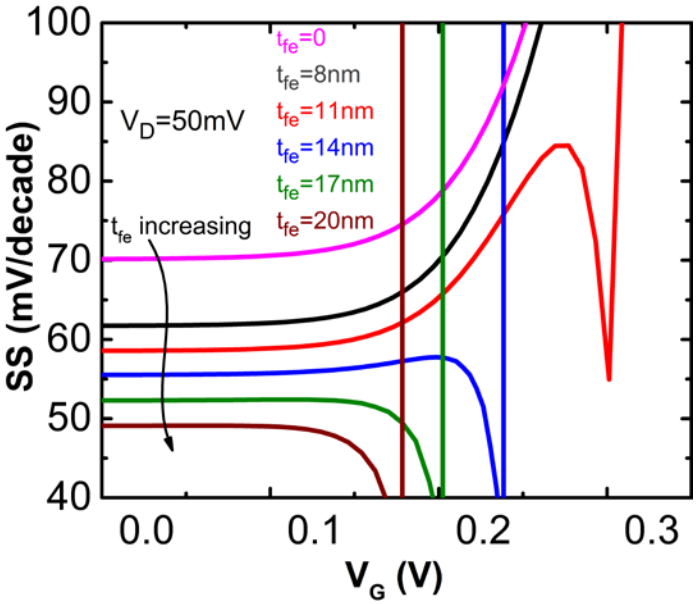
I_D-V_G Characteristics – SS region

- As t_{fe} increases
  - Capacitance matching is better
  - C_S and C_{ins} are better matched

$$S = \left(1 - \frac{C_S}{|C_{ins}|}\right).60\text{mV/dec}$$

- As $t_{fe}\uparrow \rightarrow SS\downarrow$



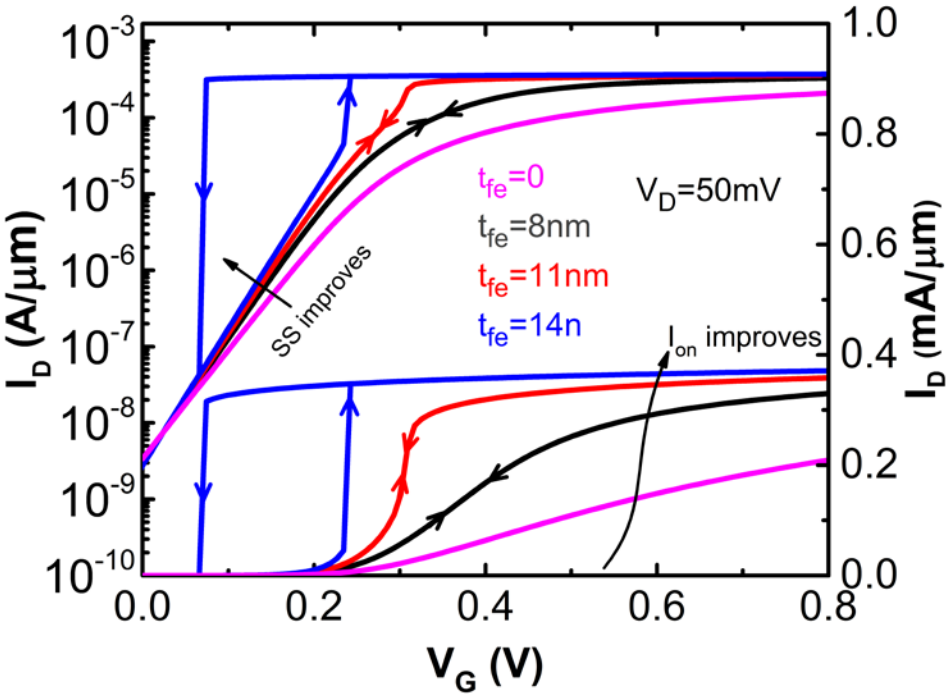


I_D-V_G Characteristics – ON region

- As t_{fe} increases
  - Capacitance matching is better

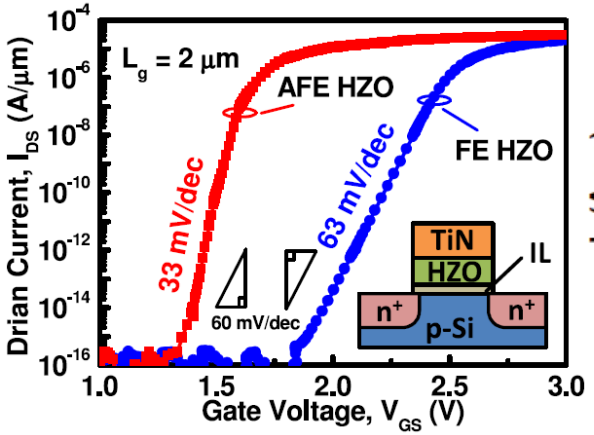
$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, I_{ON} increases.

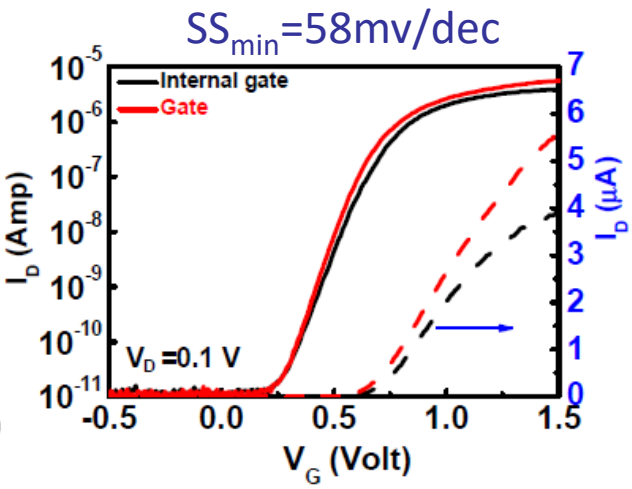


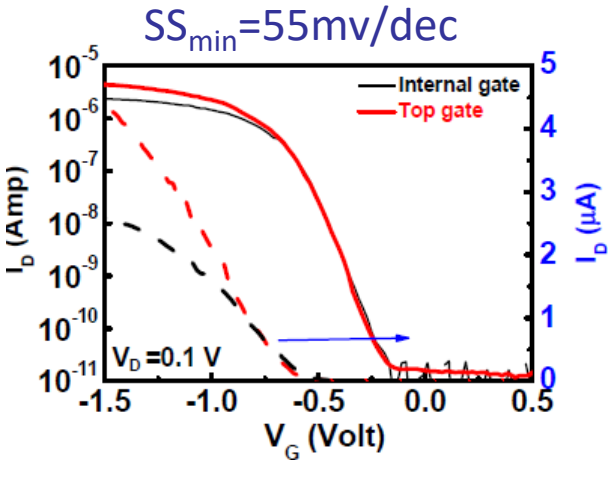
Note the significant improvement in I_{ON} compared to SS.

I_D-V_G Experimental Demonstration

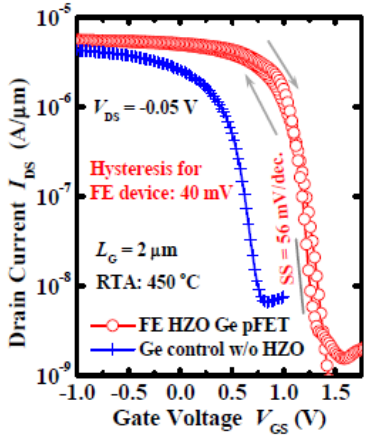


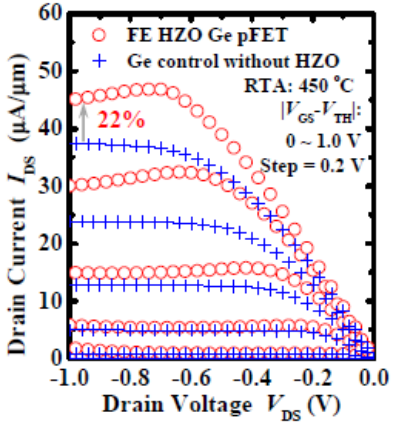
M. H. Lee *et al*., in *IEEE JEDS*, July 2015.



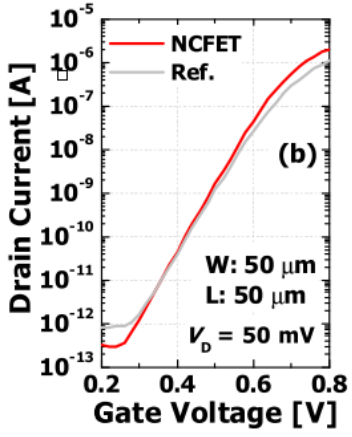


K. S. Li *et al*., in *IEEE IEDM* , 2015

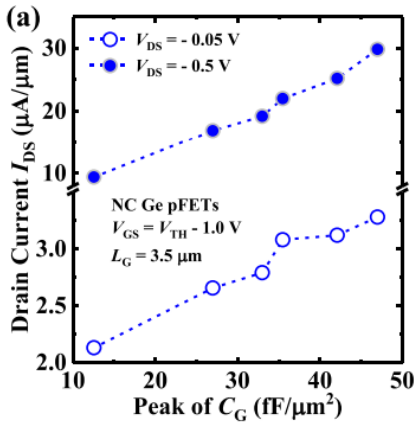




J. Zhou et al., in IEEE IEDM, 2016.



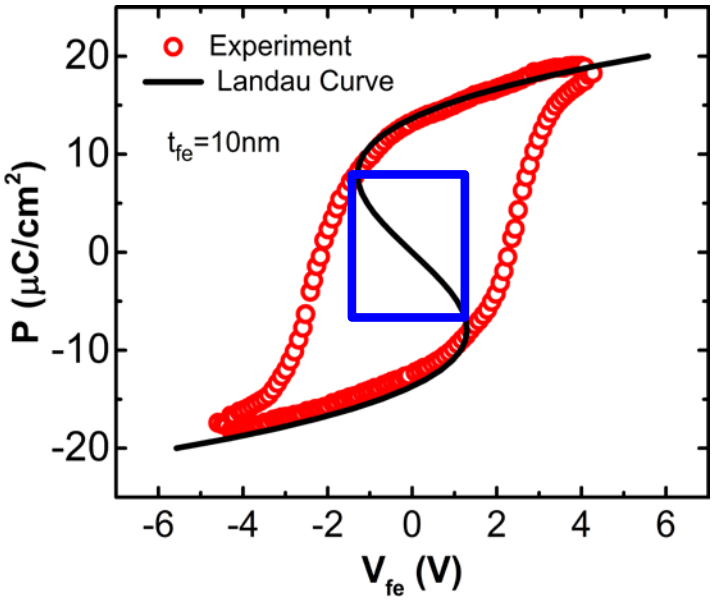
D. Kwon et al., in IEEE EDL, 2018

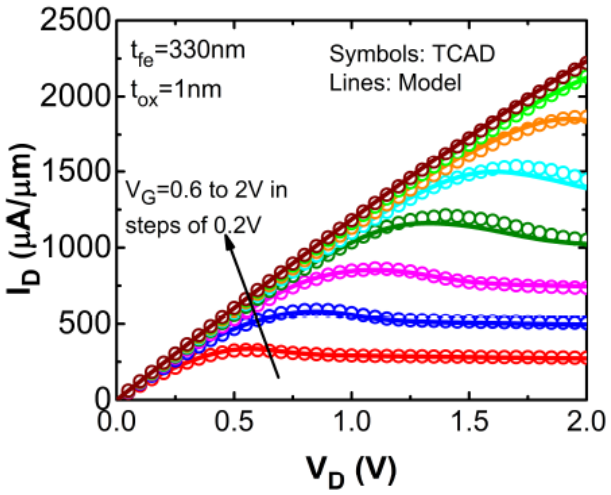


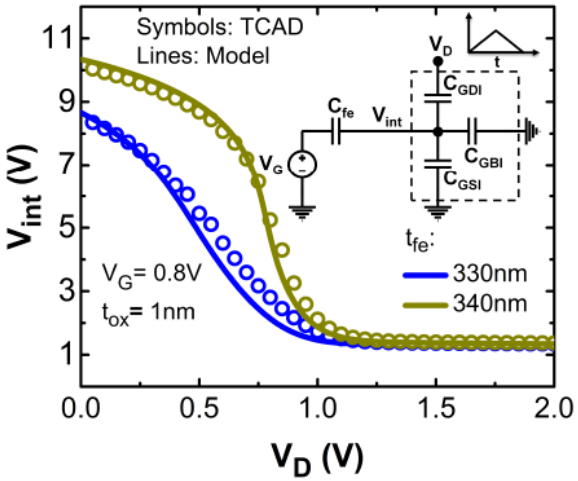
Jing Li et al., in IEEE EDL, 2018

I_D-V_D Characteristics

FE material is different.





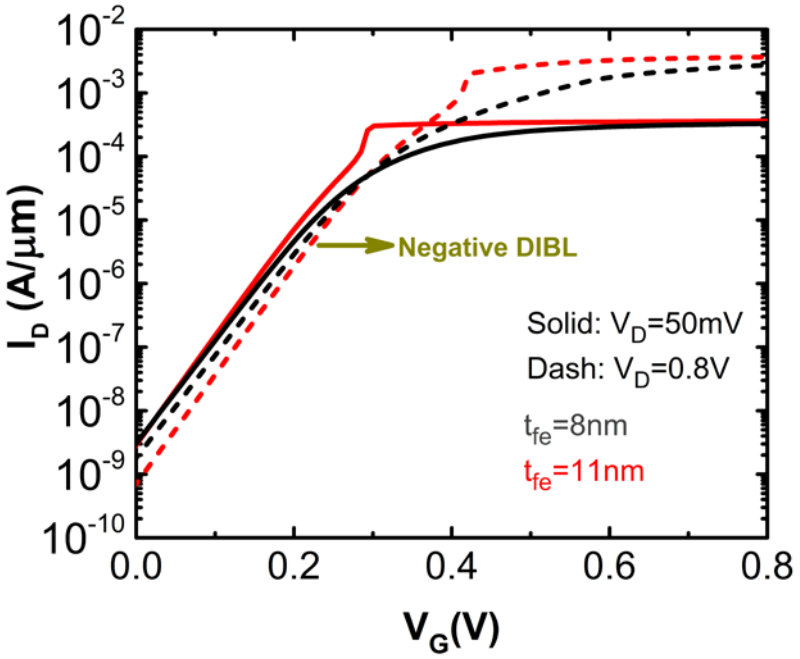


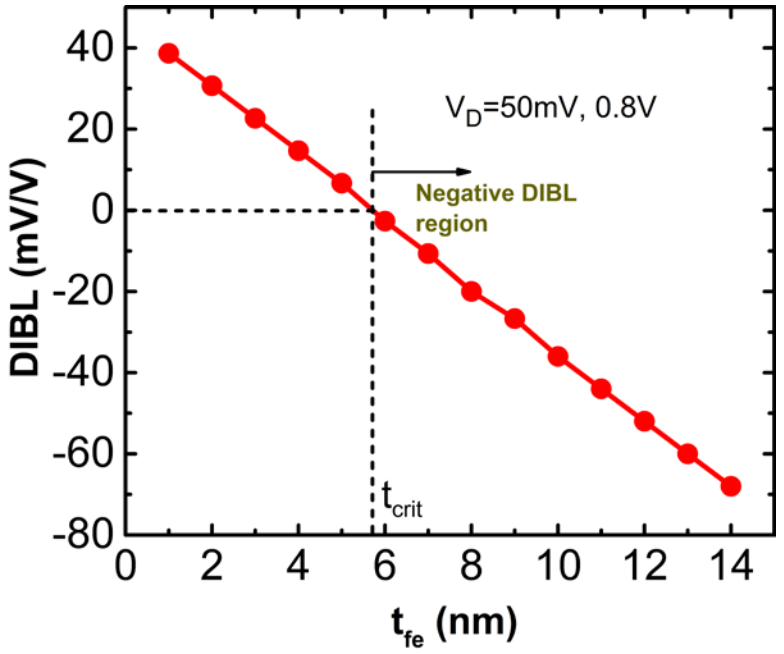
- NCFET is biased in negative capacitance region.
  - Q_G or P is positive → V_{fe} is negative.

- V_{DS}↑ → Q_G or P↓ → $|V_{fe}|$ ↓ → $V_{int}=V_G+|V_{fe}|$ ↓ → A_V ↓ → Current reduces

G. Pahwa, …, Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance", IEEE TED, Dec. 2016.

Negative DIBL





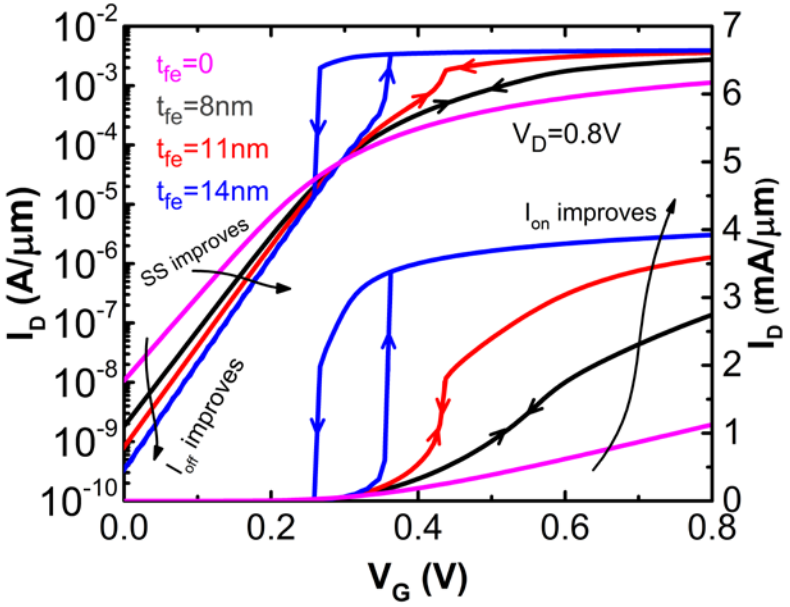
- V_D reduces Q_G which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with t_{fe} due to increased V_{fe} drop.
- V_{th} increases with V_D instead of decreasing.
  - Higher I_{ON} still lower I_{OFF}!

I_D-V_G Characteristics – High V_{DS}

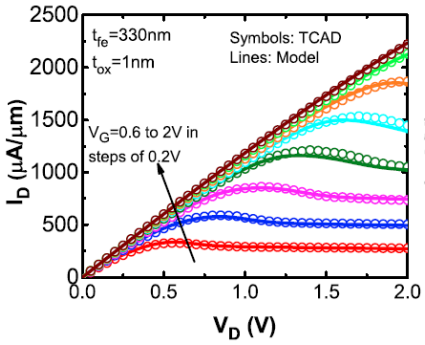
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is the region of instability.

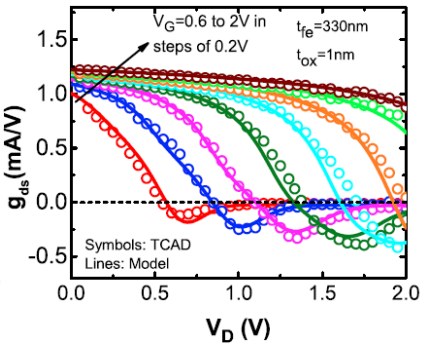
- As t_{fe} increases
  - SS reduces, I_{ON} increases.
  - I_{OFF} reduces for high V_D.

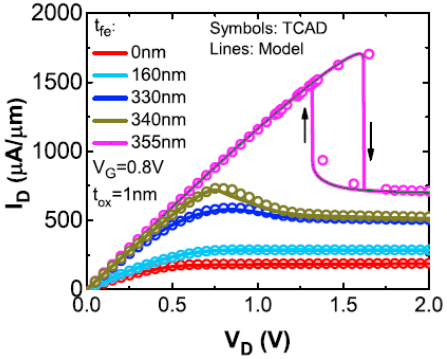
- Width of hysteresis at larger thicknesses can be controlled with V_D.

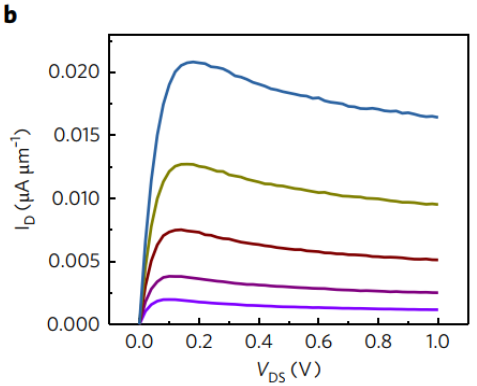


Negative Output Differential Resistance



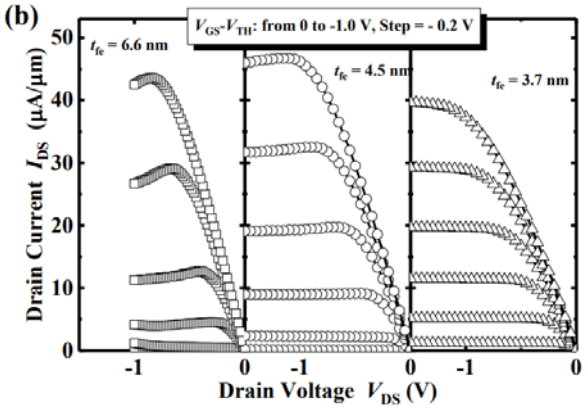


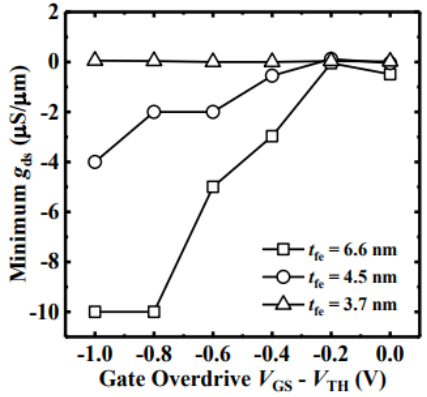


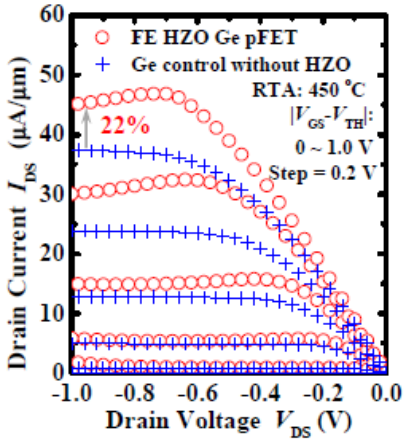


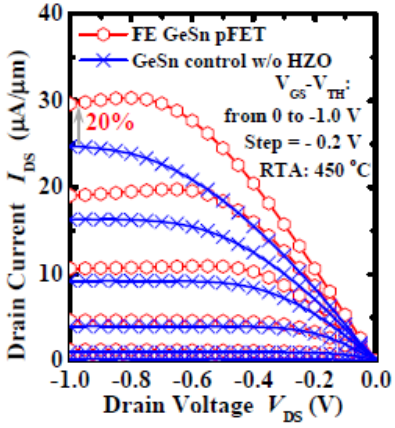
G. Pahwa *et al.*," *IEEE TED*, Dec. 2016

Mengwei Si *et al.*, *Nature Nanotechnology, 2018*





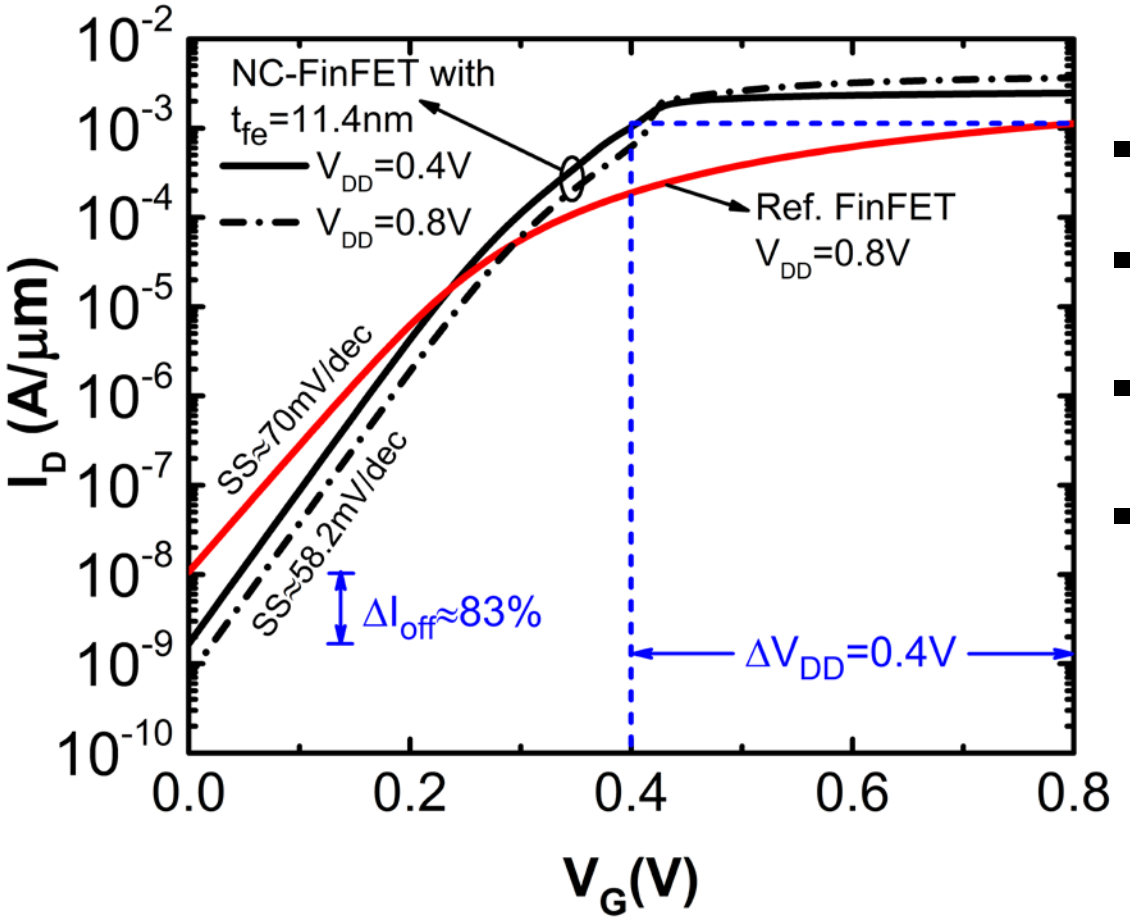




J. Zhou *et al.*, *IEEE, JEDS, 2018*

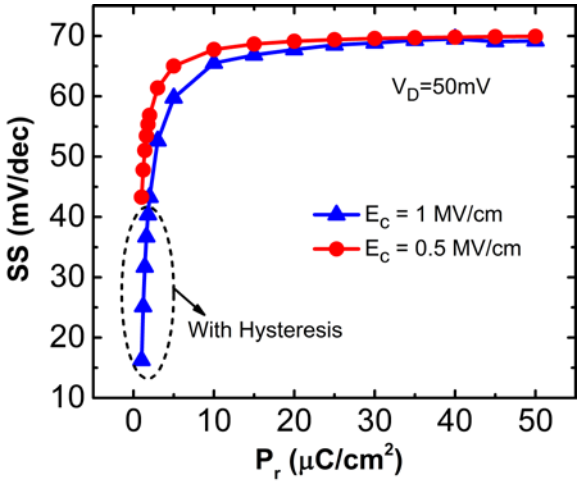
J. Zhou *et al.*, *IEDM 2016*

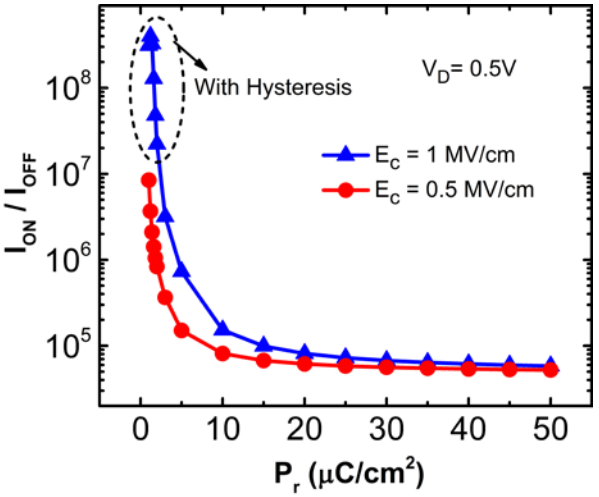
Optimum NC-FinFET

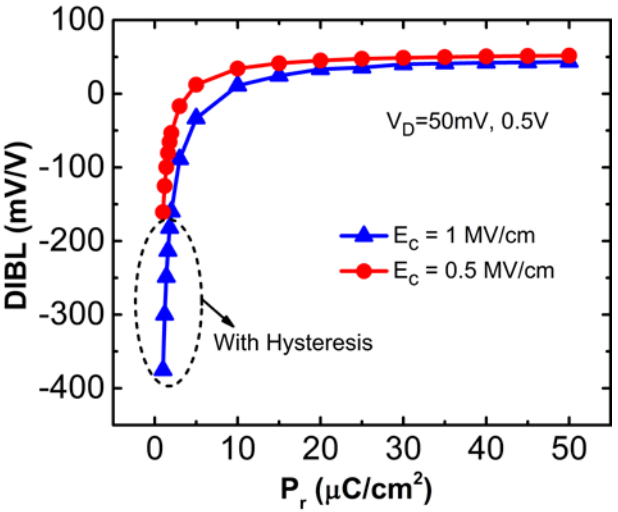


- Same I_{ON} as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- V_{DD} reduction by 0.4 V.
- I_{OFF} reduction by 83 %.

Ferroelectric Parameters Variation







If $\gamma = 0$,

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{{P_r}^3}$$

P_r = Remnant Polarization

E_c = Coercive Field

$$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$$

- Low P_r and high E_c
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I_{ON} but reduce I_{OFF} due to a more negative DIBL ⇒ high I_{ON}/I_{OFF}.

D. Ricinschi et al., JPCM, vol. 10, no. 2, p. 477, 1998.

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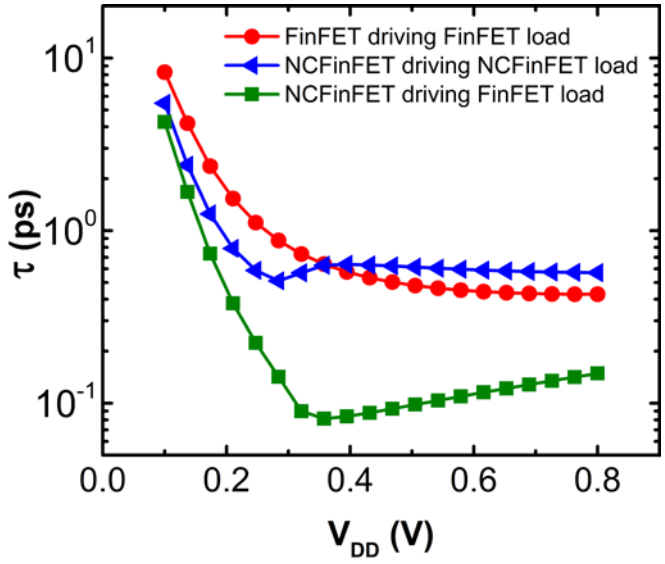
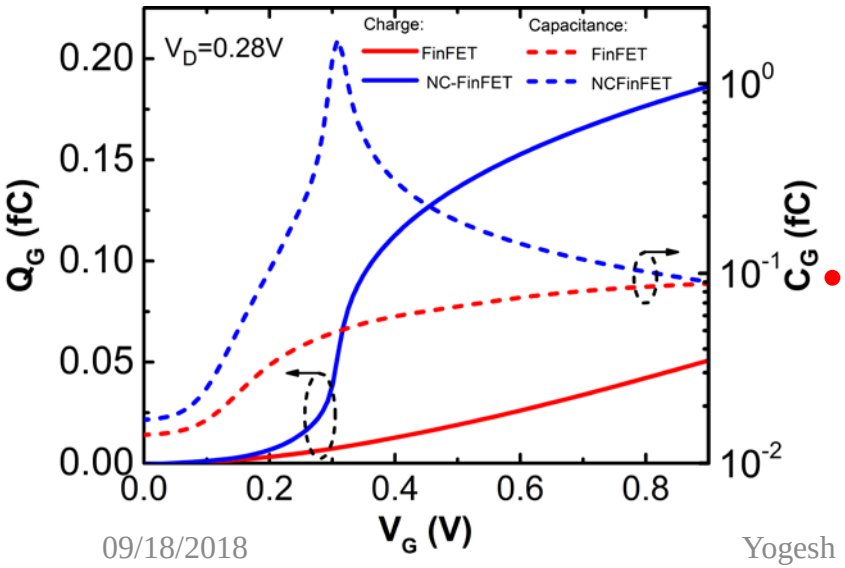
Intrinsic Delay



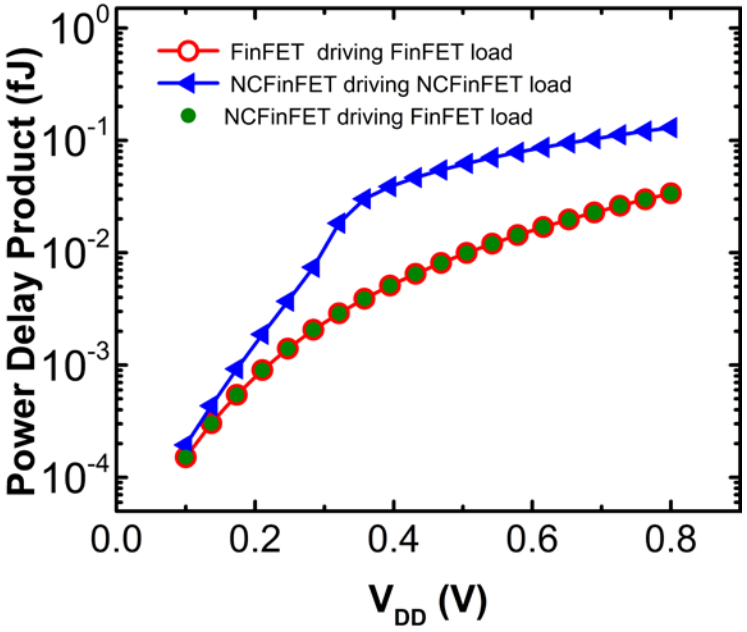


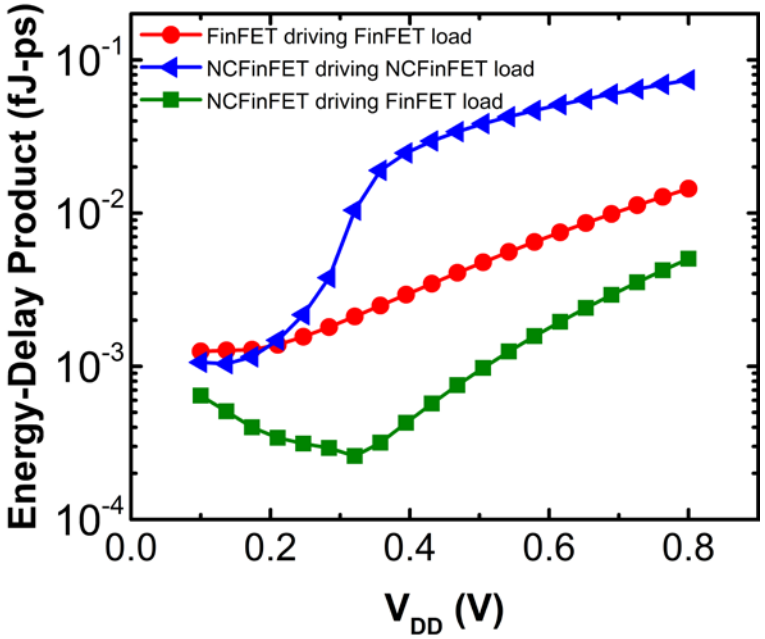
$$\text{Delay, } \tau = \frac{\Delta Q_G}{I_{ON}}$$

$$\Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD})$$

- NC-FinFET driving NC-FinFET
  - For high V_{DD}, high I_{ON} advantage is limited by large amount of ΔQ_G to be driven.
  - Outperforms FinFET at low V_{DD}.
  - Minimum at $V_{DD} \approx 0.28$ V corresponds to a sharp transition in Q_G.
- NC-FinFET driving FinFET load provides full advantage of NC-FinFET.

Power and Energy Delay Products



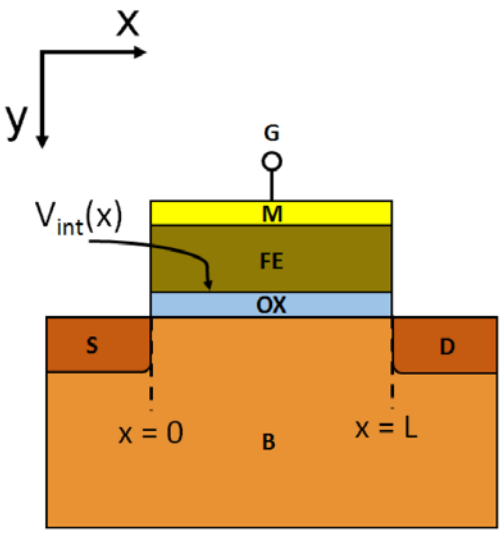


$$PDP = \Delta Q_G . V_{DD}$$

$$EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}}$$

- NC-FinFET driving NC-FinFET shows advantage only for low V_{DD}.
- NC-FinFET driving FinFET load is the optimum choice.

Modeling of MFIS NCFET



Contrast with MFIMS structure:

- P and V_{int} vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models[1,2]:

Implicit equations – tedious iterative numerical solutions

[1] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.

[2] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct. 2010.

Explicit Modeling of Charge

$$V_{fe} = Et_{fe} = aQ_G + bQ_G^3$$

Voltage Balance:

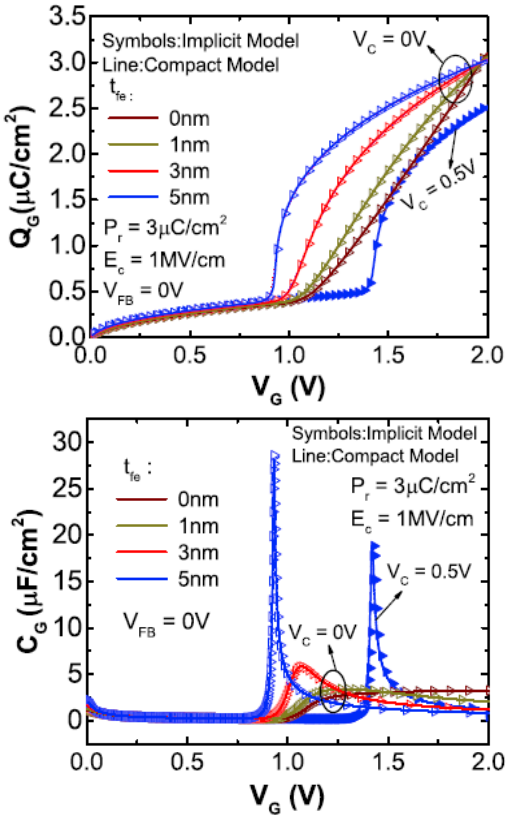
$$V_G - V_{FB} = V_{fe} + \frac{Q_G}{C_{ox}} + \psi_S = a_{eff} Q_G + bQ_G^3 + \psi_S$$

$Q_G - \psi_S$ relation[1]

$$Q_G = \text{sign}(\psi_S)\gamma C_{ox}\left[\psi_S + V_t(e^{-\psi_S/V_t} - 1) + e^{-(2\phi_F + V_C)/V_t}(V_t e^{\psi_S/V_t} - \psi_S - V_t)\right]^{1/2}$$

→ Implicit equation in Q_G

→ **Goal:** Explicit Model with good initial guesses for each region of NCFET operation

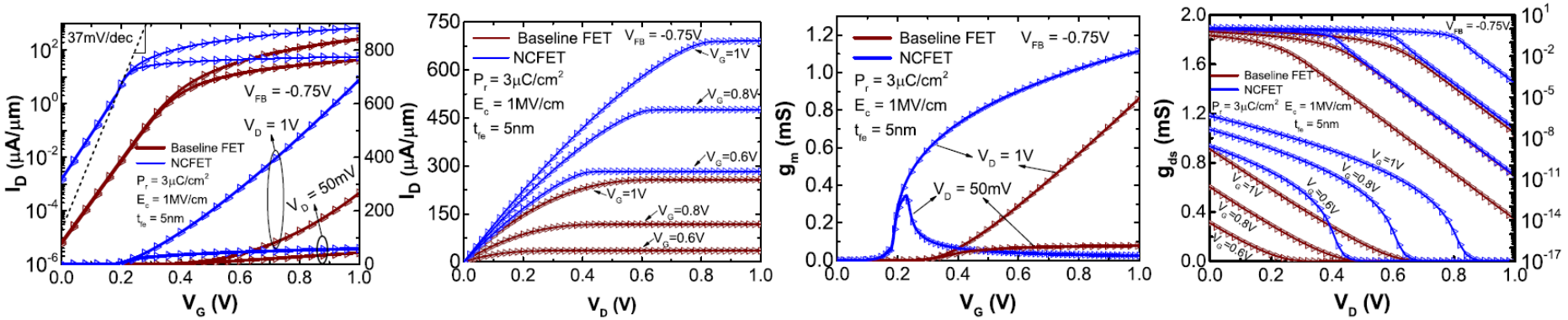


Both the Q_G and its derivatives match well with implicit model

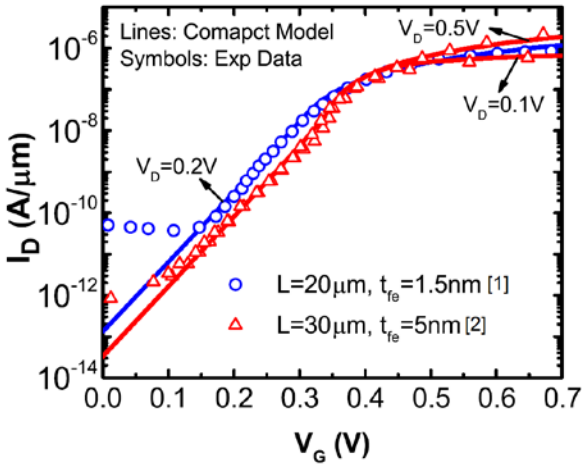
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," in *IEEE Transactions on Electron Devices*, March 2017.

Drain Current Model Validation

Against Full Implicit Calculations



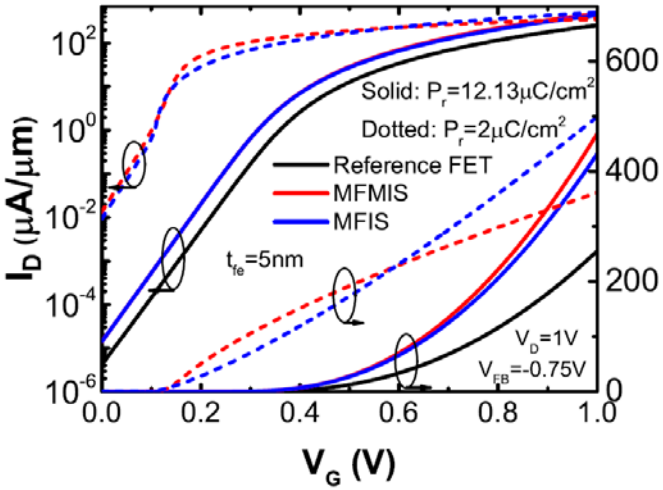
Against Experimental Data

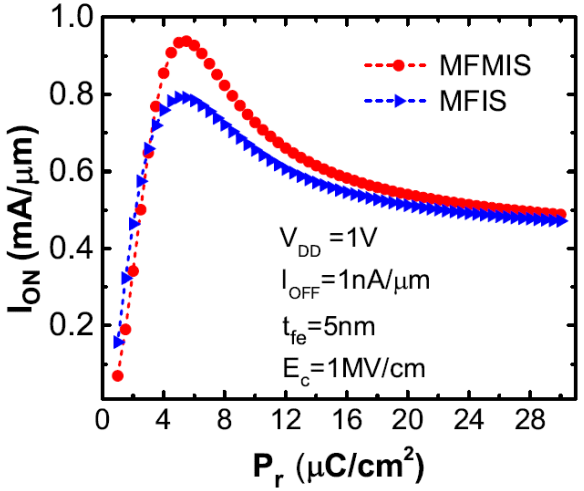


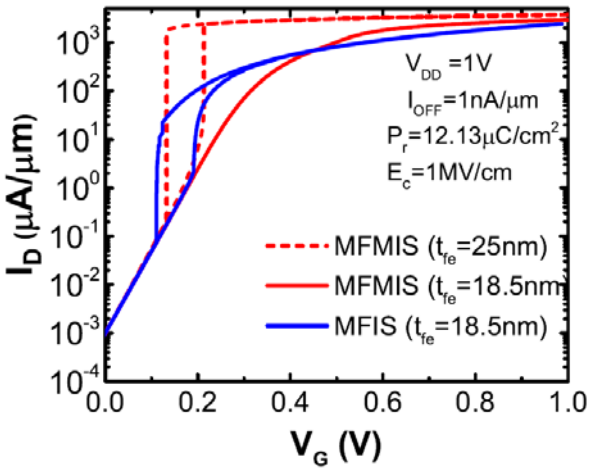
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," *IEEE Transactions on Electron Devices*, March 2017.

[1] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.1.1–12.1.4. [2] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.5.1–22.5.4.

MFIS Vs MFIS





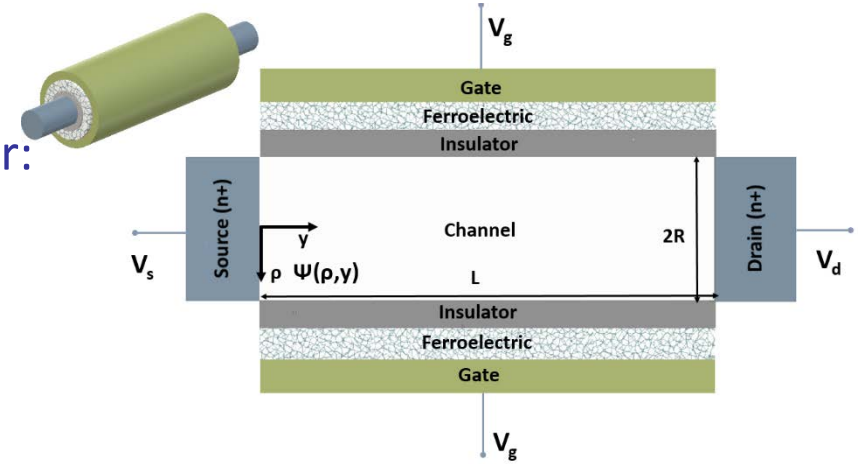


- MFIS excels MFMIS for low P_r ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", accepted in *IEEE Transactions on Electron Devices*, 2018.

Compact Modeling of MFIS GAA-NCFET

$$V_{fe} = a_0 Q + b_0 Q^3$$



Radial Dependence in Ferroelectric Parameter:
(Ignored in others work)

$$a_0 = 2aR\ln[1 + t_{fe}/(R + t_{ins})]$$

$$b_0 = 2bR^3[1/(R + t_{ins})^2 - 1/(R + t_{ins} + t_{fe})^2]$$

Mobile Charge Density:

$$Q = \varepsilon_{si}\left(\frac{d\psi}{d\rho}\right)\Big|_{\rho=R} = \left(\frac{2\varepsilon_{si}}{R}\right)\left(\frac{2kT}{q}\right)\left(\frac{\beta^2}{1-\beta^2}\right)$$

Voltage Balance:

$$V_g - \Delta\phi - \psi_s = (a_0 + 1/C_{ins})Q + b_0 Q^3$$

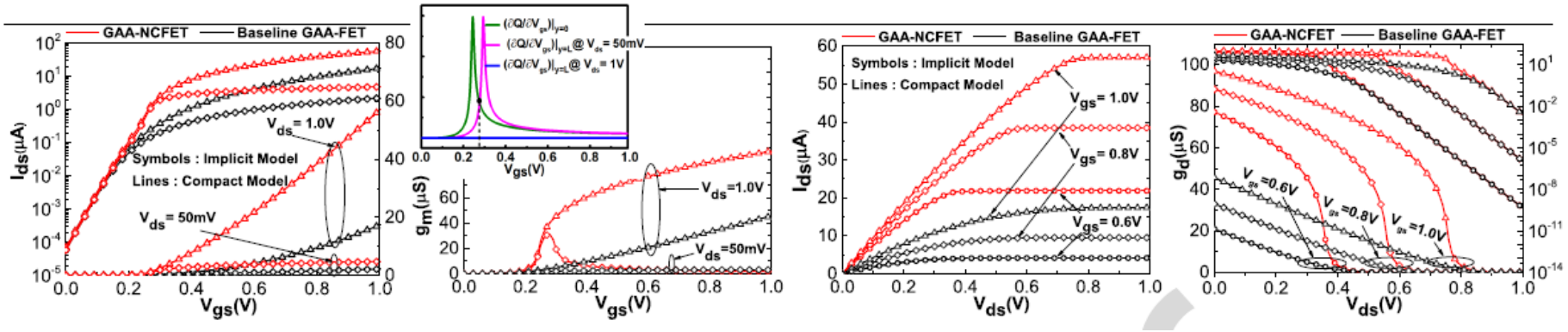
Implicit Equation in β:

$$\ln(\beta) - \ln(1-\beta^2) + m\left(\frac{\beta^2}{1-\beta^2}\right) + n\left(\frac{\beta^2}{1-\beta^2}\right)^3 - G = 0$$

→ **Goal:** Explicit Model for β with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.

Drain Current Model Validation

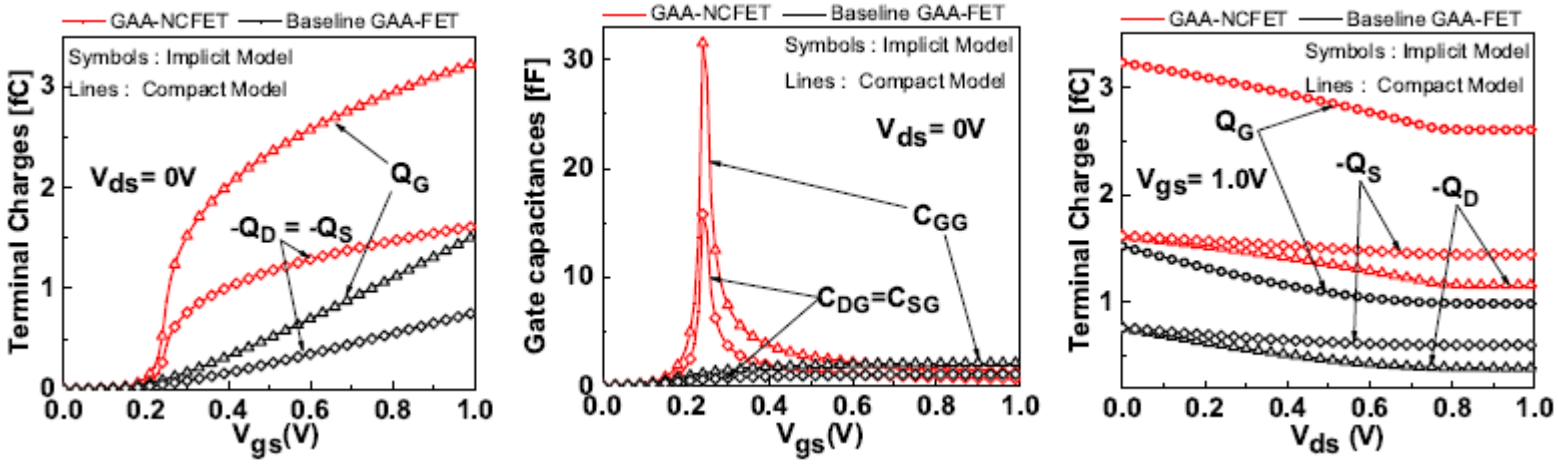
Against Full Implicit Calculations



- In contrast to bulk-NCFETs
  - Multi-gate NCFETs with an undoped body exhibit same I_{OFF} and V_{th} due to absence of bulk charges.
  - GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.

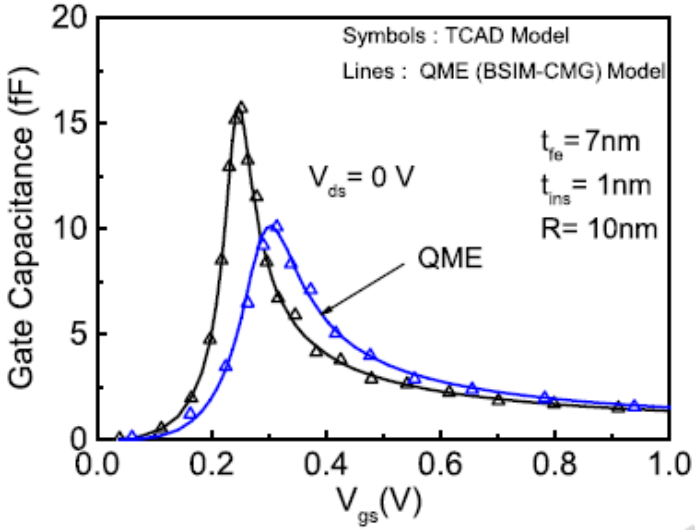
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.

Terminal Charges in GAA-NCFET



- Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
- For high V_{DS}, the Q_G for GAA-NCFET is saturates to $(4/5)^{th}$ of the maximum value (at Vds = 0) in contrast to conventional devices for which it saturates to $(2/3)^{rd}$ of the maximum value.

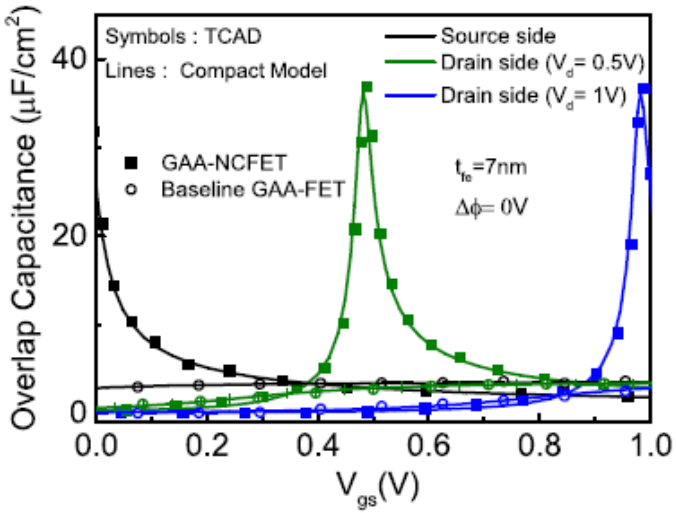
Quantum Mechanical Effect in GAA-NCFET



- The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.

A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.

Modeling of overlap capacitance in GAA-NCFET



- Overlap region can be modeled as MFMIS capacitor

$$Q_{\text{dep}} = (qN_D V)/A$$

$$Q_{\text{acc}} = -C_{\text{ins}}[(V_{\text{int}})_{s/d} - V_{s/d}]$$

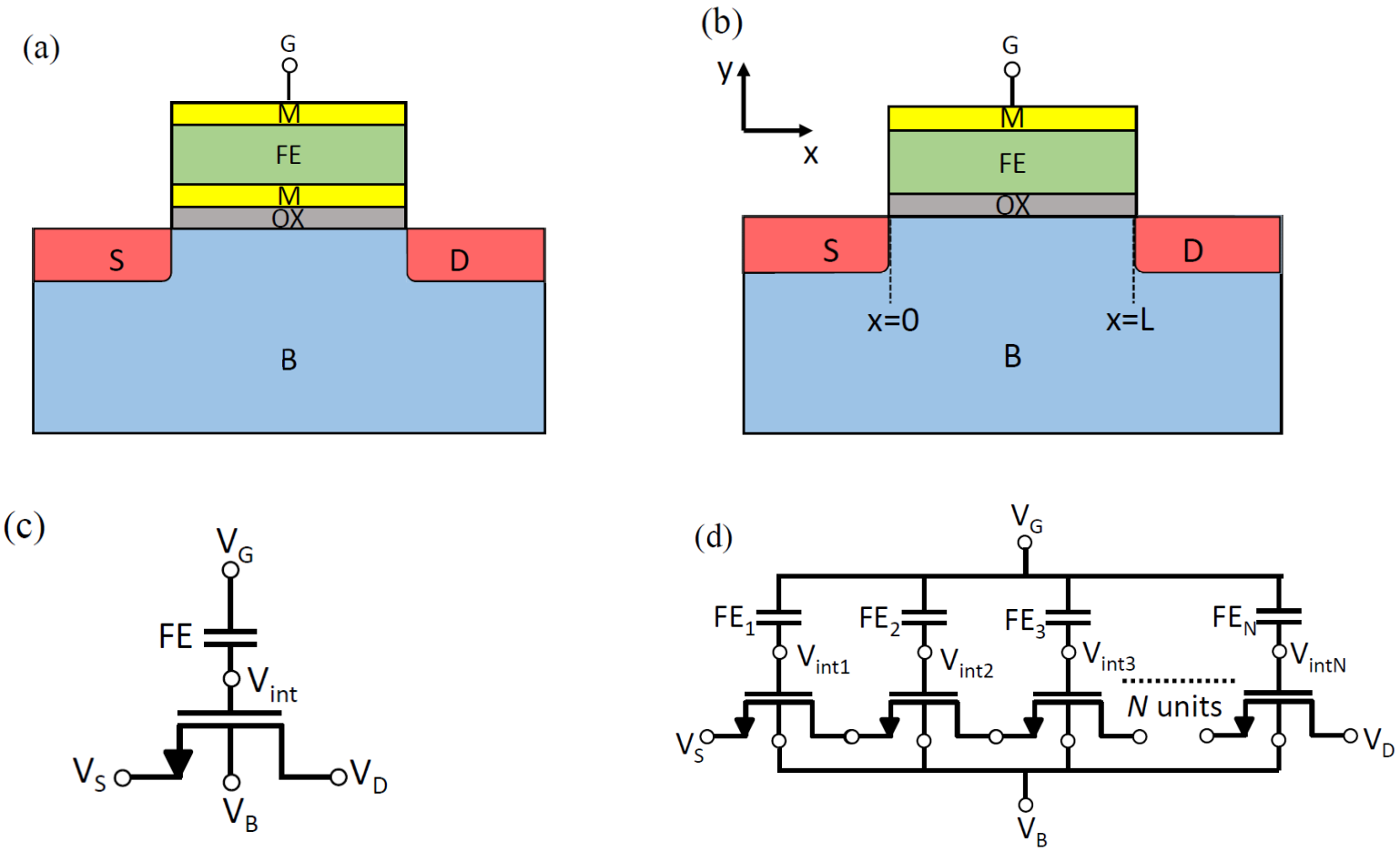
- Total overlap capacitance

$$Q_{\text{ov}} = -0.5\left[Q_{\text{acc}} + Q_{\text{dep}} - \sqrt{(Q_{\text{acc}} - Q_{\text{dep}})^2 + 4\delta}\right]$$

- In MFMIS structure, due to the presence of internal metal gate the parasitic capacitances directly add up to the internal FET capacitance which strongly affects capacitance matching between the internal FET and the ferroelectric layer along the channel.

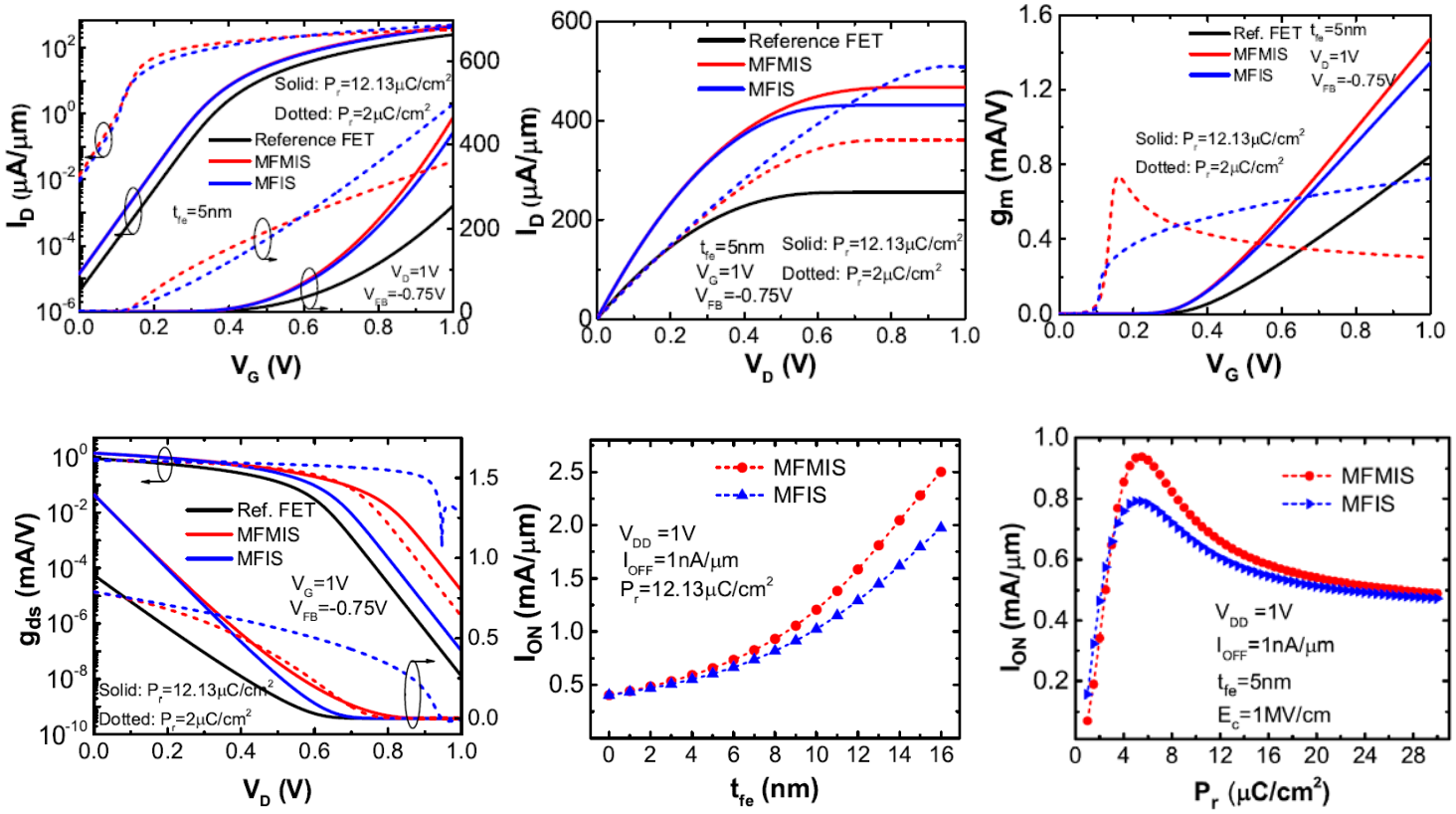
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.

MFMIS Vs MFIS



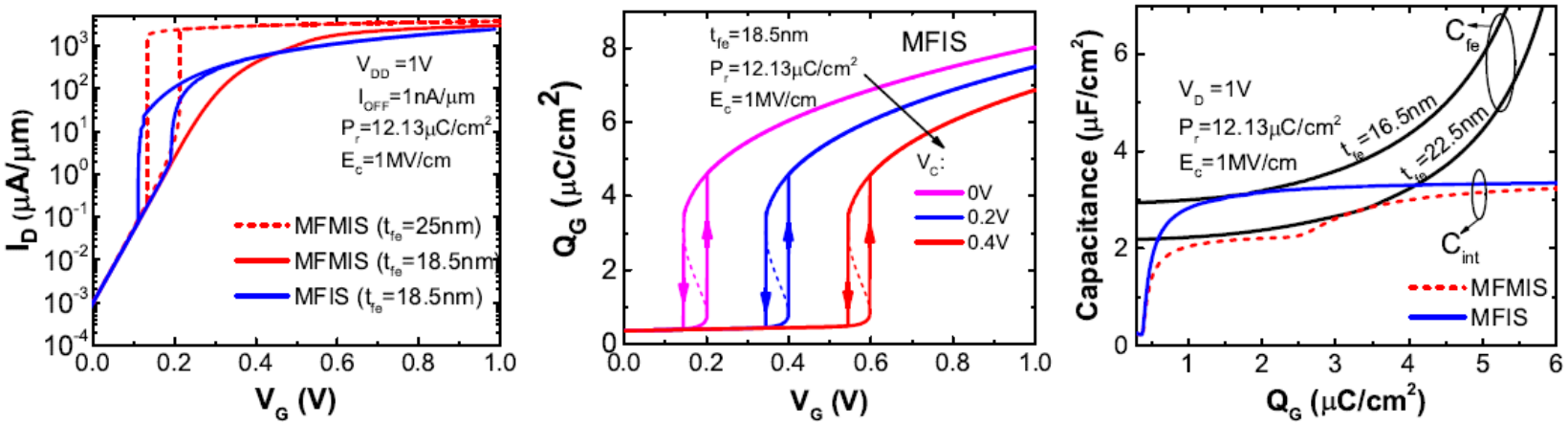
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

Comparing I_D-V_G and I_D-V_D Characteristics (long channel)



- MFIS excels MFMIS for low P_r ferroelectrics only, in long channel NCFETs.

Hysteresis Behavior



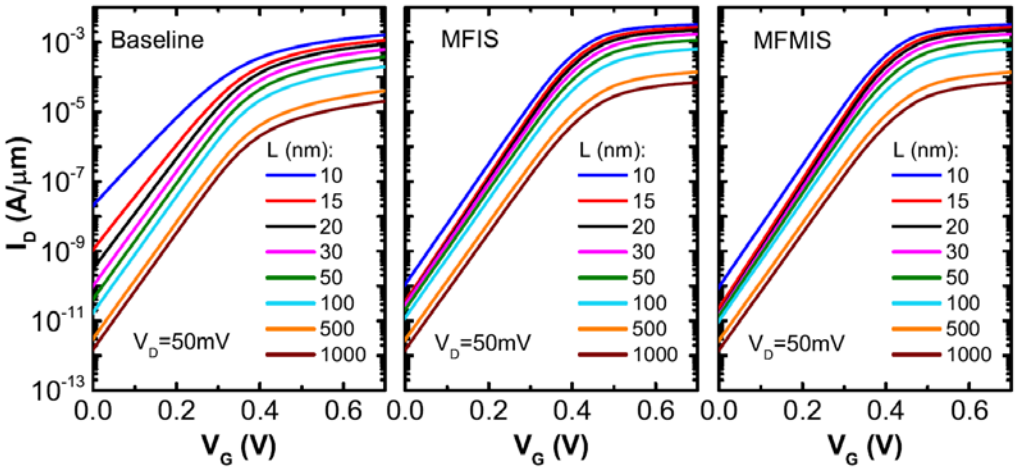
- Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
- Source end dipole switches, first, owing to its least hysteresis threshold.
- Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

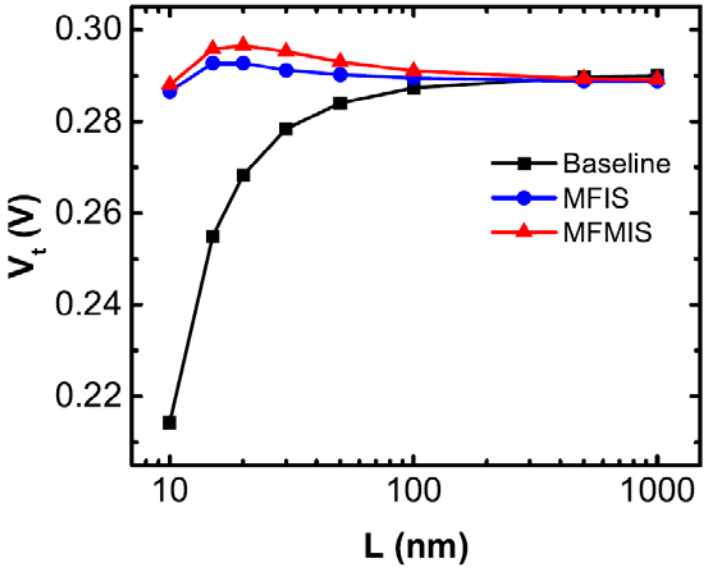
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

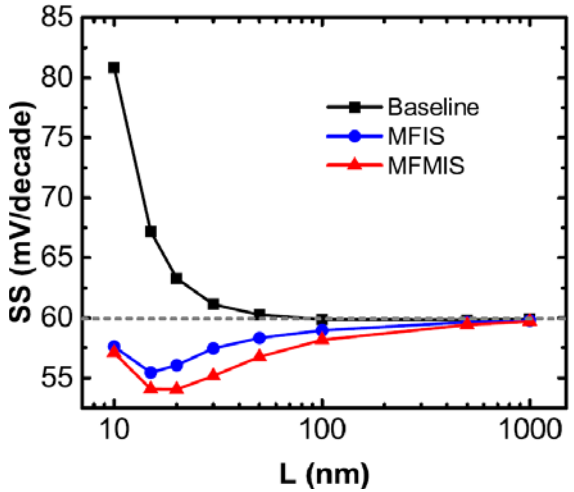
MFMIS vs MFIS: Short Channel Effects

OFF Regime (low V_D)

2D Numerical Simulation Results





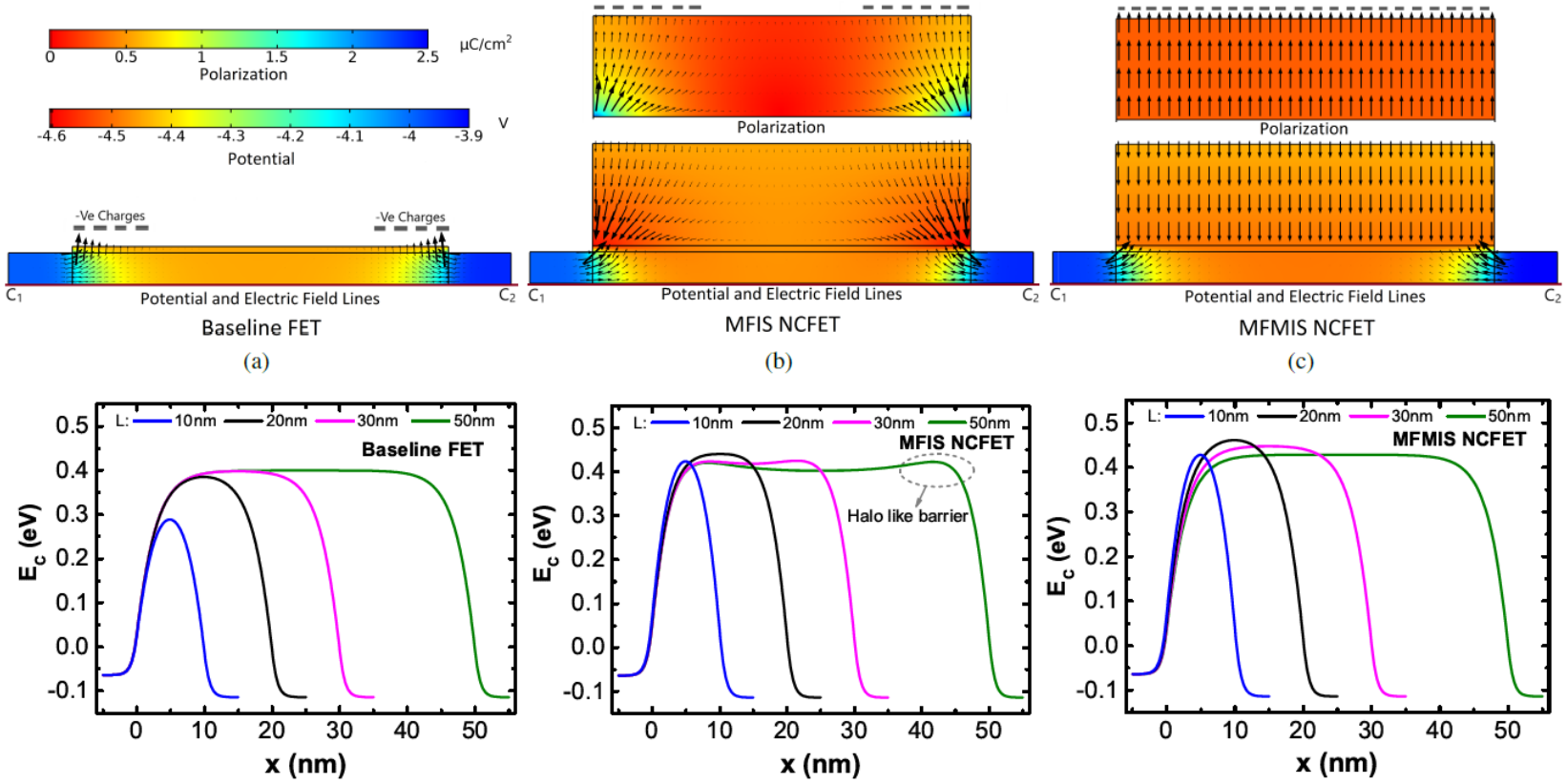


P_r=0.1213 μC/cm^2 E_C=1MV/cm t_{fe}=8nm

NCFETs exhibit reverse trends in V_t and SS with scaling except for very small lengths.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures*", submitted to IEEE Transactions on Electron Devices.

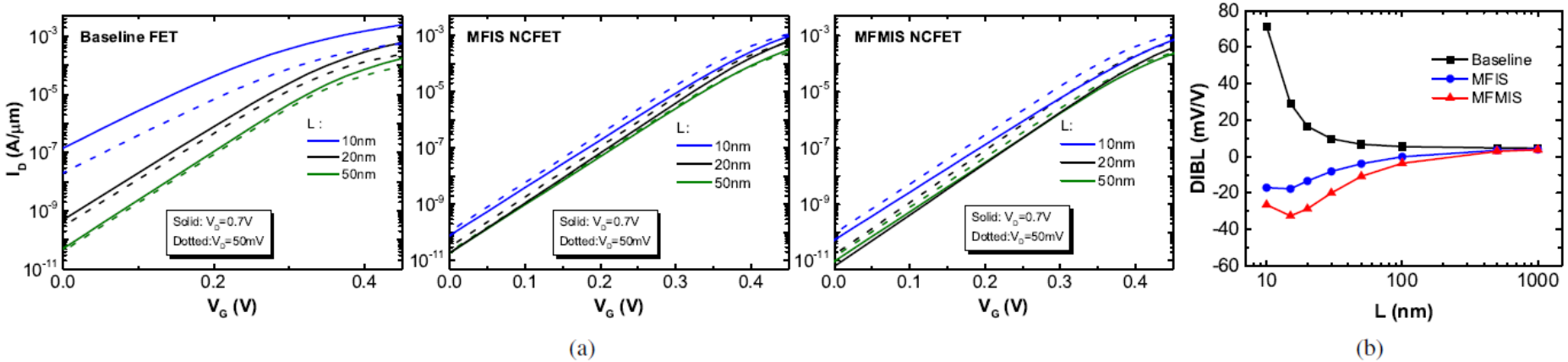
Reverse V_t Shift with Scaling

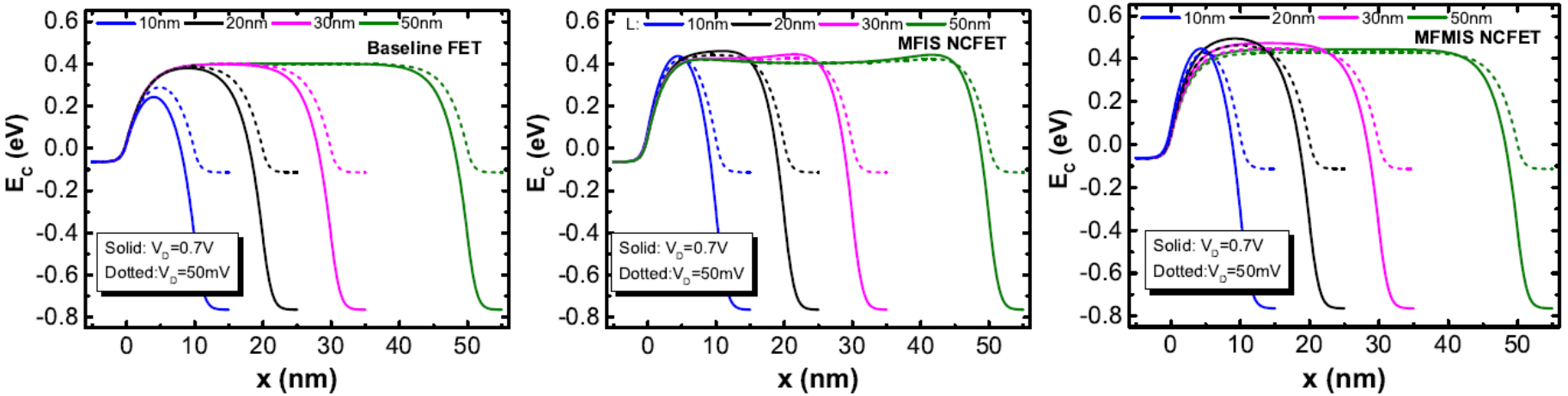


- Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.
- In MFIS, fringing effect remains localized to channel edges only → Halo Like barriers.
- In MFMIS, internal metal extends this effect to the entire channel → larger V_t than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures*", accepted in IEEE Transactions on Electron Devices.

OFF Regime (high V_{DS}): Negative DIBL



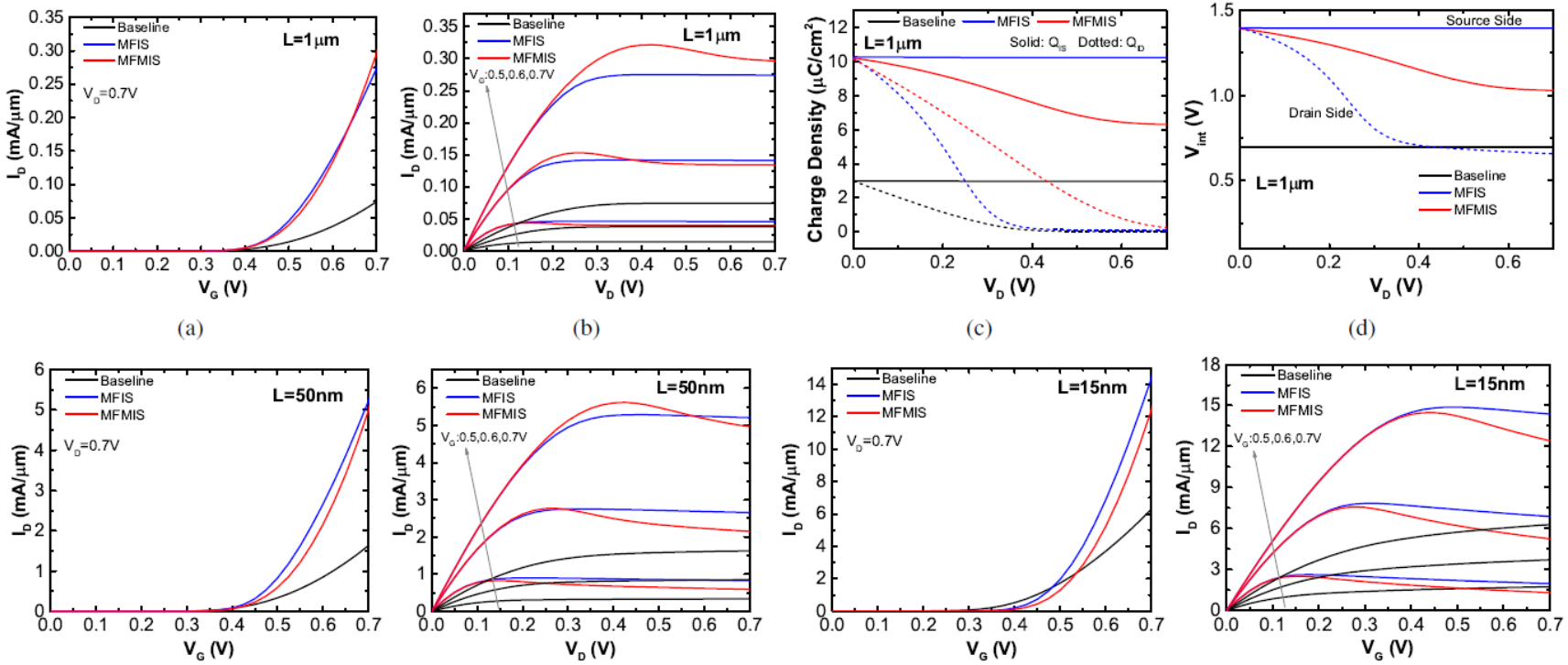


- Negative DIBL effect increases with Scaling.
- More pronounced in MFMIS than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures*", submitted to IEEE Transactions on Electron Devices.

ON Regime

High P_r=0.1213 μC/cm^2



- Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling → lower V_{DSat} of MFIS results in lower I_{DS}.
- However, internal metal in MFMIS helps V_{DS} impact to easily reach source side→ Q_{IS} ↓ → Larger NDR effect in MFMIS than MFIS.
- In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former.

Does polarization damping really limit operating frequency of NC-FinFET based circuits?

Recent Demonstration by Global Foundries on 14nm NC-FinFET

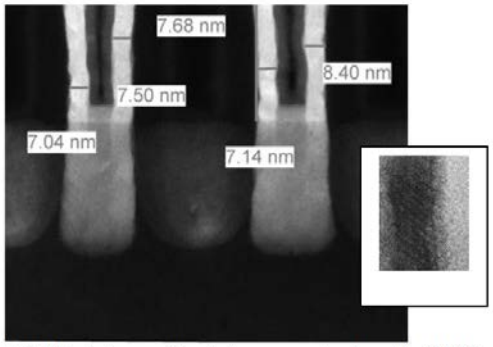


Fig. 3: TEM picture of minimum gate length RMG with 8nm FE. The inset shows the crystallinity of the FE film.

[1] Krivokapic, Z. et al., IEDM 2017

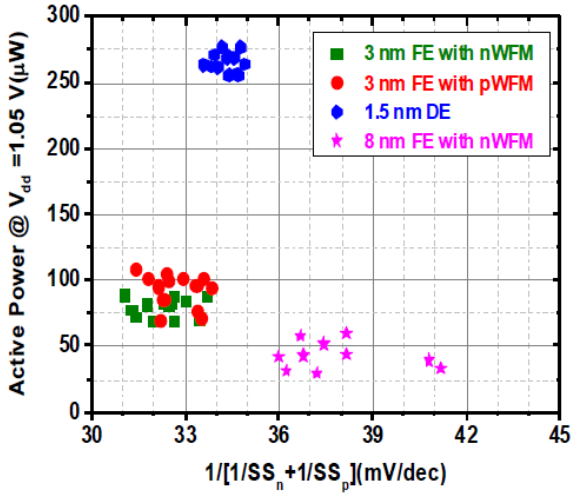


Fig. 13: Active power of FO3 inverter RO vs. effective SS for V_{dd}=1.05V.

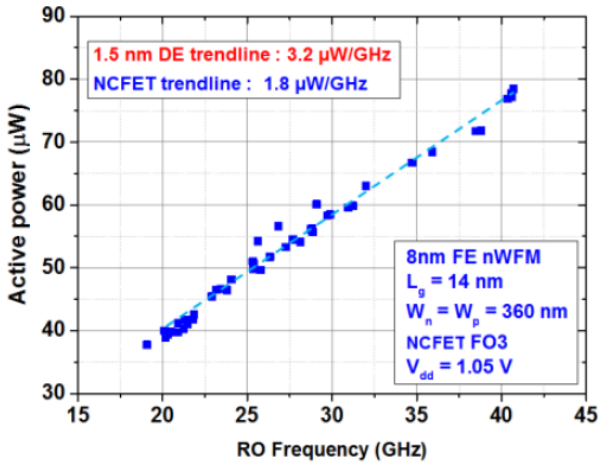
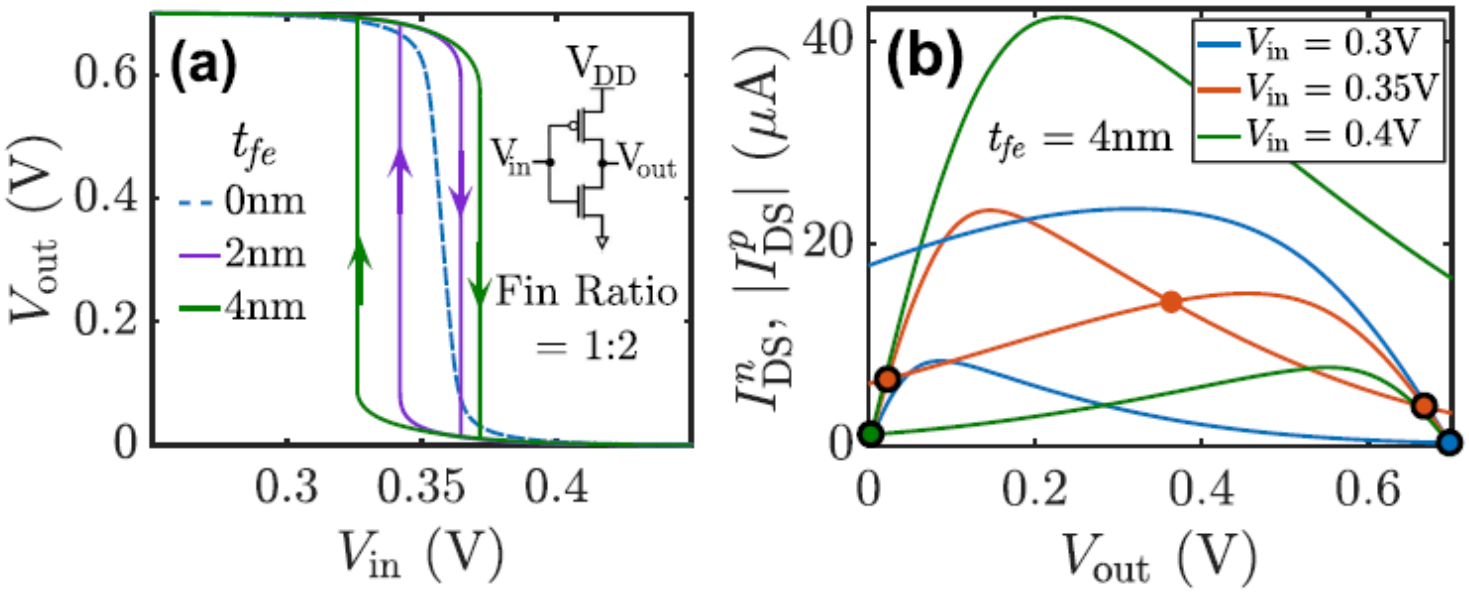


Fig. 14: Active power of NCFET FO3 inverter RO with W_n=W_p=360nm, L=14nm.

- Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power[1].
- Another theoretical study predicted intrinsic delay due to polarization damping in NCFET to be very small (270 fs)[2].

[2] Chatterjee, K., Rosner, A. J. & Salahuddin, IEEE Electron Device Letters 38, 1328–1330 (2017).

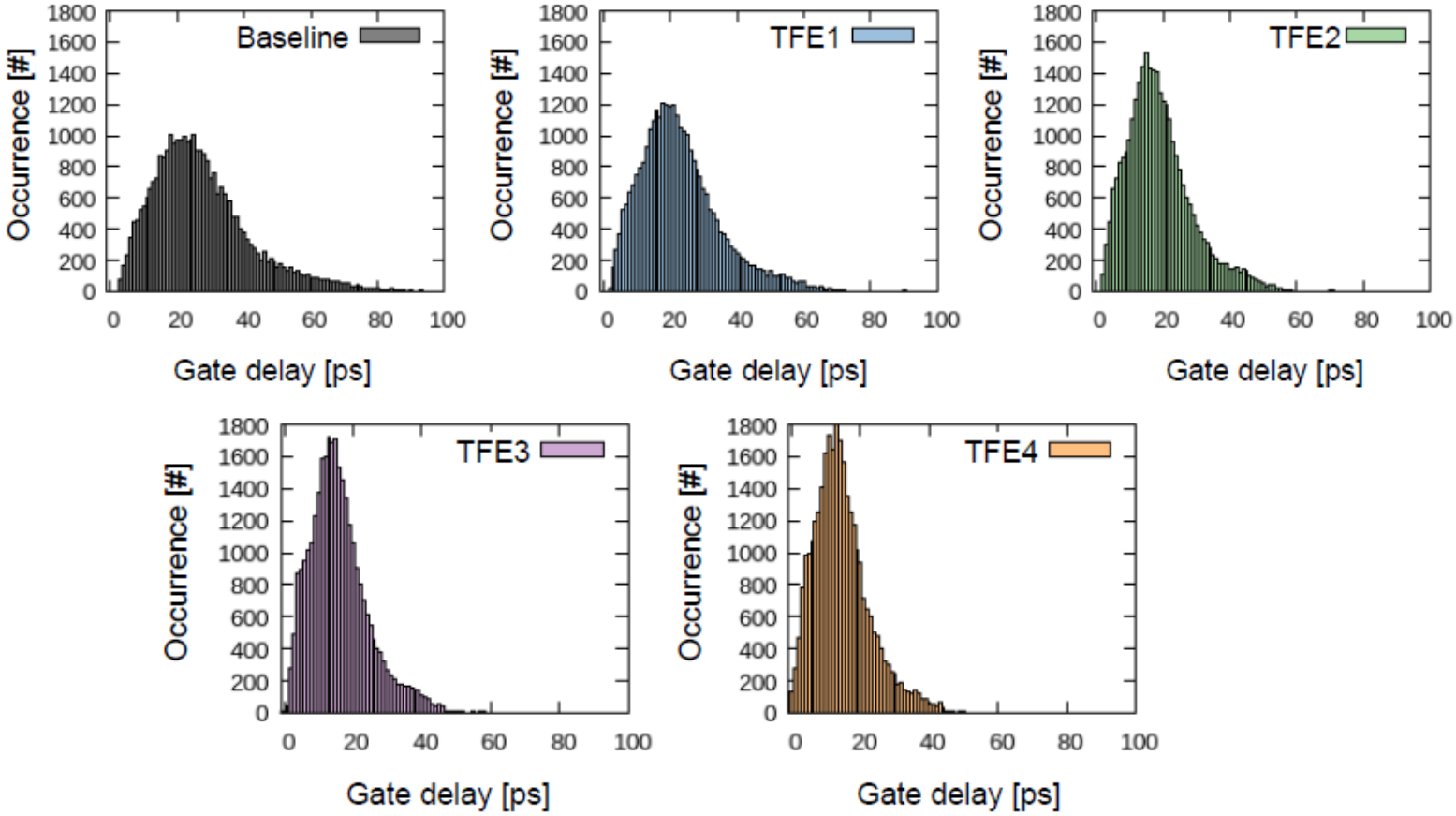
NC-FinFET based inverters



- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

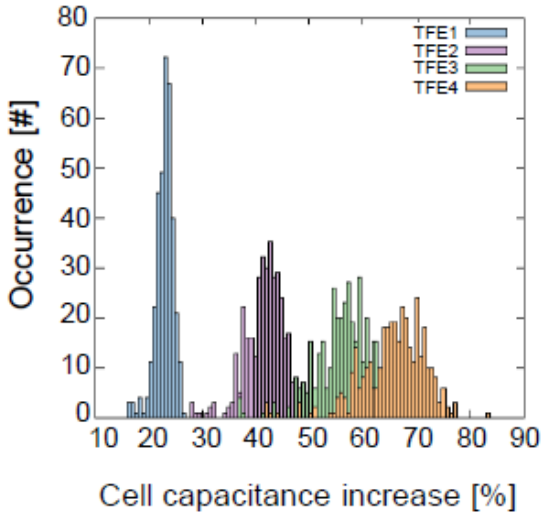
Effects of NCFET on standard cells: 7nm FinFET standard cell library

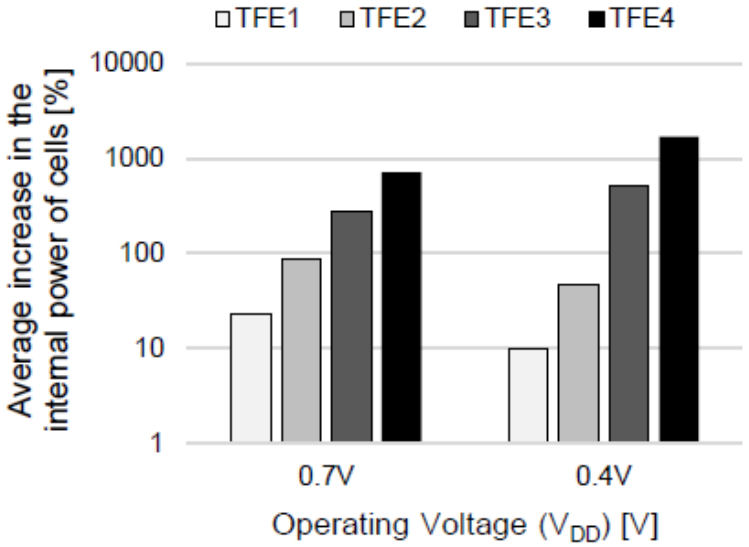


- Increasing t_{fe} – larger A_v in transistors (i.e., steeper slope and higher ON current) → Delay of cells become smaller.

Accepted in IEEE Access

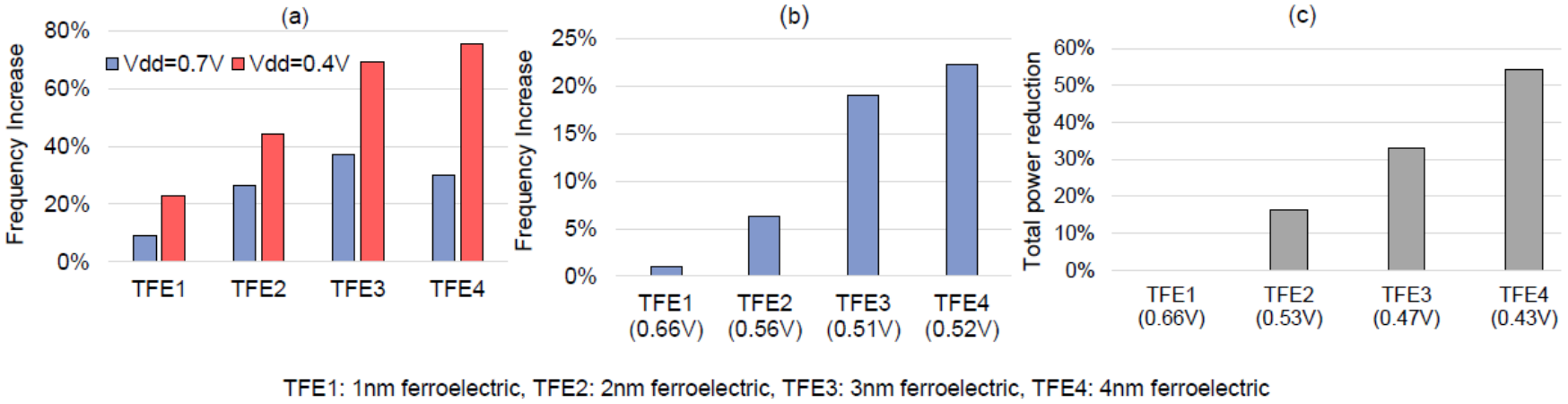
Effects of NCFET on standard cells: 7nm FinFET standard cell library





- Increase in t_{fe} leads to an increase in the total cells' capacitance which further increases internal power of the cells.
- Same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.

Effects of NCFET on future processor design



TFE1: 1nm ferroelectric, TFE2: 2nm ferroelectric, TFE3: 3nm ferroelectric, TFE4: 4nm ferroelectric

(a) What is the frequency increase due to NCFET under the same voltage constraint?

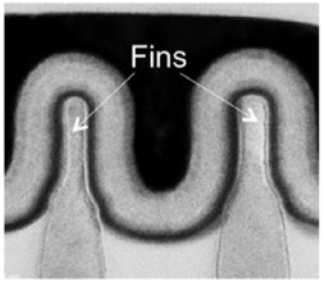
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?

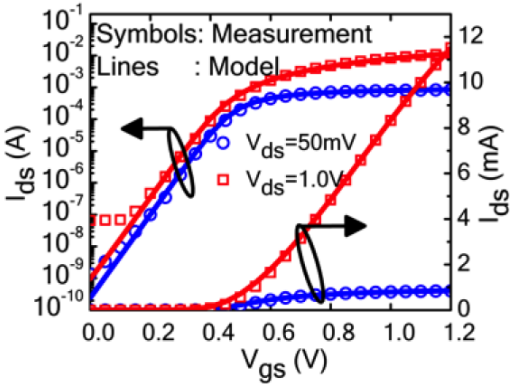
(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

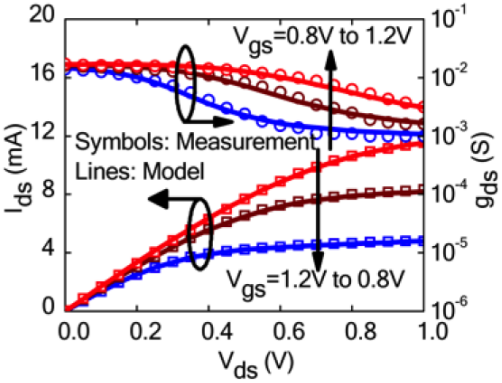
H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance", under revision in IEEE Access, 2018.

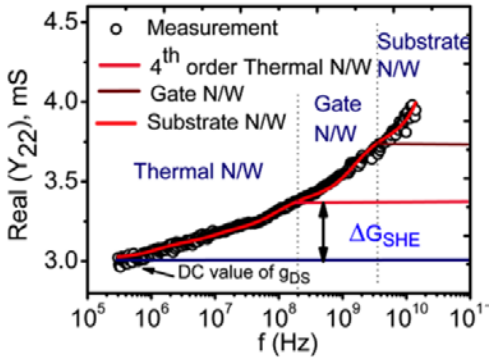
NC-FinFET RF Performance

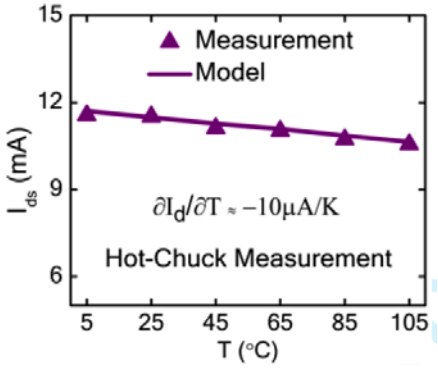
- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis

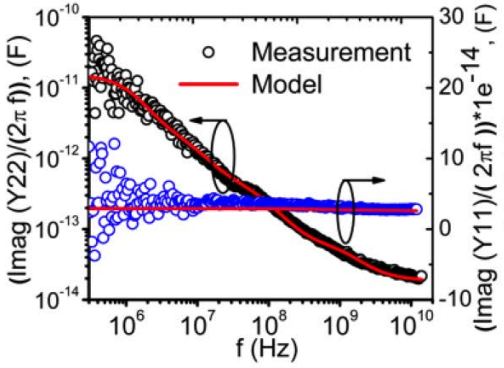


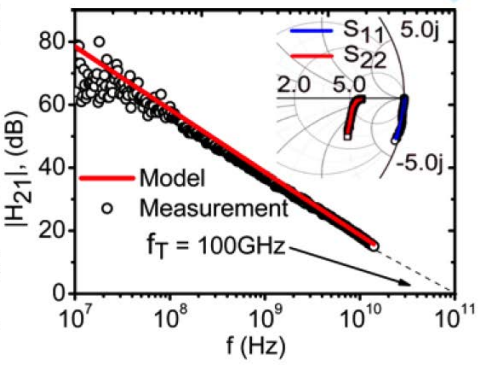






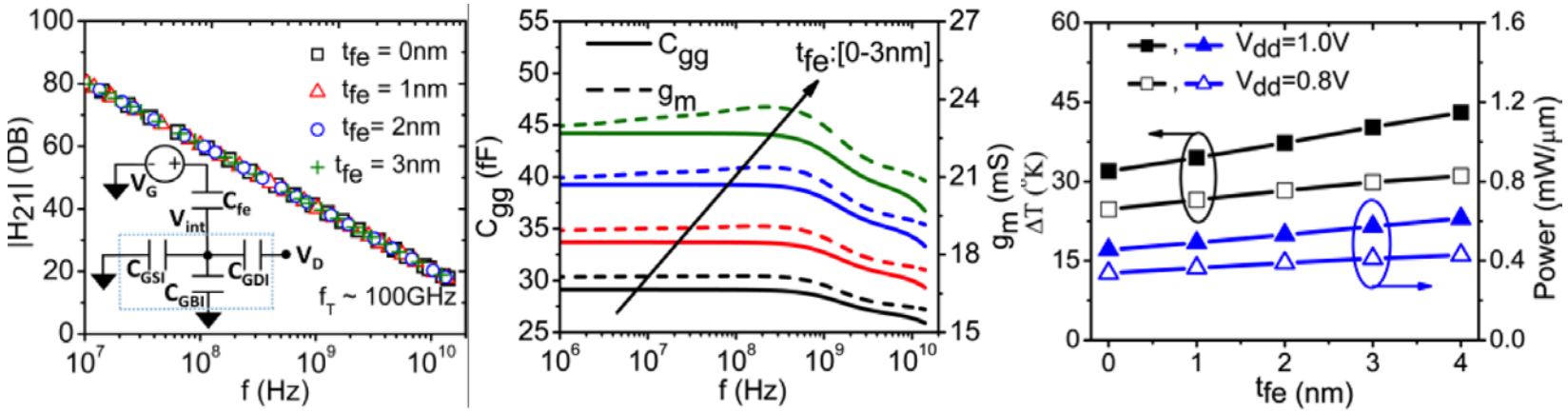






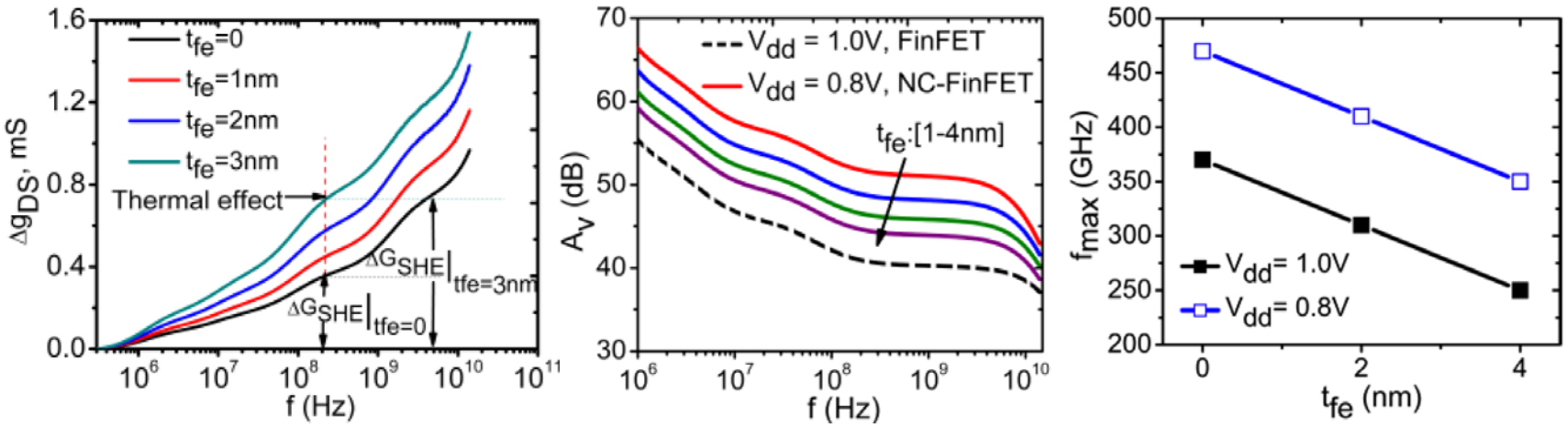
R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook, and A. Dixit, "Evaluation of 10nm Bulk FinFET RF Performance - Conventional vs. NC-FinFET", IEEE Electron Device Letters, Aug. 2018.

NC-FinFET RF Performance



- Current gain ($\propto {}^{g_m}/_{C_{gg}}$) is almost independent of t_{fe} as both the g_m and C_{gg} increase with t_{fe} almost at a constant rate.
  - Cut-off frequency (f_T) remains identical for both the Baseline and NC-FinFET.
- Temperature rise and Power consumption due to self-heating increase with t_{fe} as I_d increases. Reduce V_{dd} to achieve energy efficient performance.

NC-FinFET RF Performance

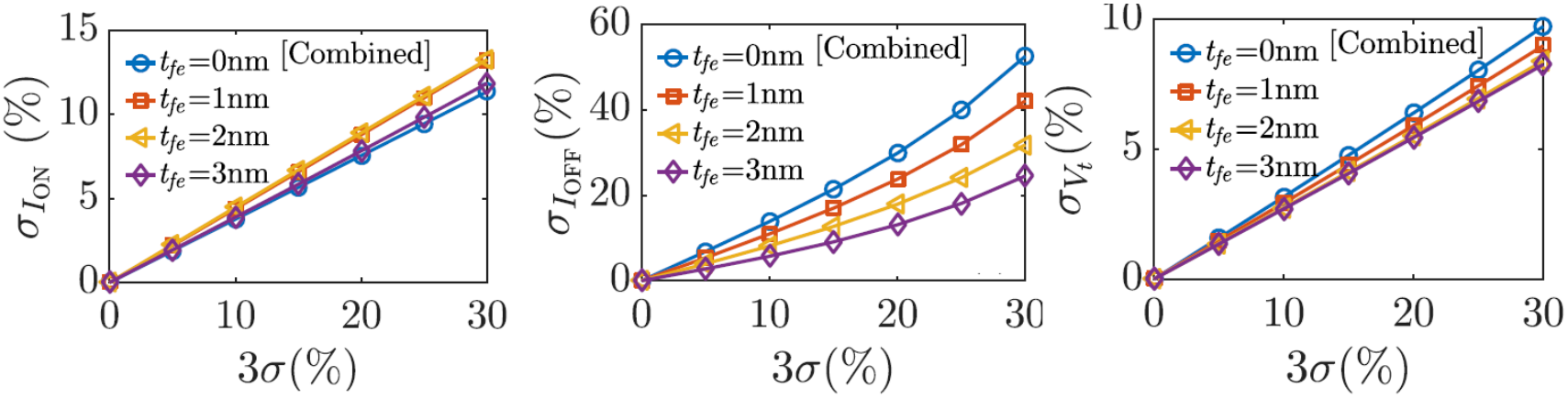


- g_{ds} and self heating ($\Delta G_{SHE} \propto g_{ds}(f) - g_{ds}(dc)$) both increase with t_{fe} due to increased capacitance matching between C_{fe} and C_{int}.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\partial I_{ds}}{\partial V_{int}} * \frac{\partial V_{int}}{\partial V_{ds}} = g_m^{int} * A_V^D \quad \text{where} \quad A_V^D = \frac{-C_{GDI}}{|C_{fe}| - C_{int}}$$

- Voltage gain ($A_V = g_m/g_{ds} = C_{fe}/C_{GDI}$) decreases with t_{fe} due to decrease in C_{fe}.
- Maximum oscillation frequency (f_{max}) also reduces with t_{fe} which can be compensated by reducing V_{dd}.

Impact of Process Variations



- Variability in I_{ON}, I_{OFF}, and V_t due to combined impact of variability in L_g, T_{fin}, H_{fin}, EOT, t_{fe}, E_c, and P_r
- I_{ON}: Improvement is non-monotonic with t_{fe}
- I_{OFF}: Decreases monotonically with t_{fe}
- V_t: Decreases monotonically with t_{fe}

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, 2018.

Conclusion

- Maintaining I_{ON}/I_{OFF} is the biggest challenge in new technology nodes
- Negative capacitance FET is one of the best choice
  - Need to find sweet material ($HfZrO_2$?)
  - Integration in conventional CMOS process remains a challenge (lot of progress)
- Compact (SPICE) Models are ready for circuit evaluation

Relevant Publications from Our group

- "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Part I - Subthreshold Behavior ", under revision in IEEE TED.
- "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Part II - Above-Threshold Behavior “, under revision in IEEE TED.
- "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", IEEE TED, May 2018.
- "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE TED, Mar. 2018.
- "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE EDL, Jan. 2018.
- "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE EDL, Aug. 2017.
- "Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS Structure", IEEE TED, Mar. 2017.
- "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part I, Model description", IEEE TED, Dec. 2016.
- "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part II, Model validation", IEEE TED, Dec. 2016.
- "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", IEEE ICEE, Dec. 2016. (Best Paper Award)
- "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE ESSDERC, Switzerland, Sept. 2016. (Invited)

Thank You