ASM-GaN:

Industry Standard GaN HEMT Compact Model for Power-Electronics and RF Applications

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Outline

- Overview of Compact Modeling
- GaN HEMT
- ASM-GaN-HEMT Model
- Model Validation

My Group and Nanolab

Current members – 30

- Postdoc – 5
- Ph.D. – 16
- Seven PhD graduated

Device Characterization Lab
- Keysight B1500 IV/CV Parameter Analyzer
- Keysight B1505 High Power IV/CV Analyzer
- Maury's Pulsed IV/RF for GaN HEMTs
- Keysight PNA-X 43.5GHz
- Load-Pull system

Compact Modeling – Industrial Research

- Bulk MOSFET Modeling (DC to RF) – BSIM4 and BSIM-BULK (BSIM6)
- Partially Depleted SOI MOSFET Modeling (DC to RF) – BSIM-SOI
- Multigate MOSFET Modeling
  - FinFET & Nanowire Transistor – BSIM-CMG
  - Fully Depleted SOI (FDSOI) Transistor– BSIM-IMG
- High Voltage LDMOS Modeling – BSIM-HV
- GaN HEMT Modeling – ASM-HEMT
- DC, CV and RF Characterization
  - All models are validated on measured data

Joint Development & Collaboration

Berkeley
University of California

MACQUARIE
University
SYDNEY·AUSTRALIA

IIT Gandhinagar
Indian Institute of Technology Gandhinagar

imec

ims
BORDEAUX

EPFL
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

iemn
Institut d'Electronique, de Microélectronique et de Nanotechnologie
UMR CNRS 8520

infineon

CREE®

qorvo™

Raytheon

TOSHIBA

Soitec

maxim integrated™

UMC

KEYSIGHT TECHNOLOGIES

IBM

intel®

TEXAS INSTRUMENTS

tsmc®

freescale™ semiconductor

GLOBALFOUNDRIES®

ON Semiconductor®

ON

Mentor Graphics®

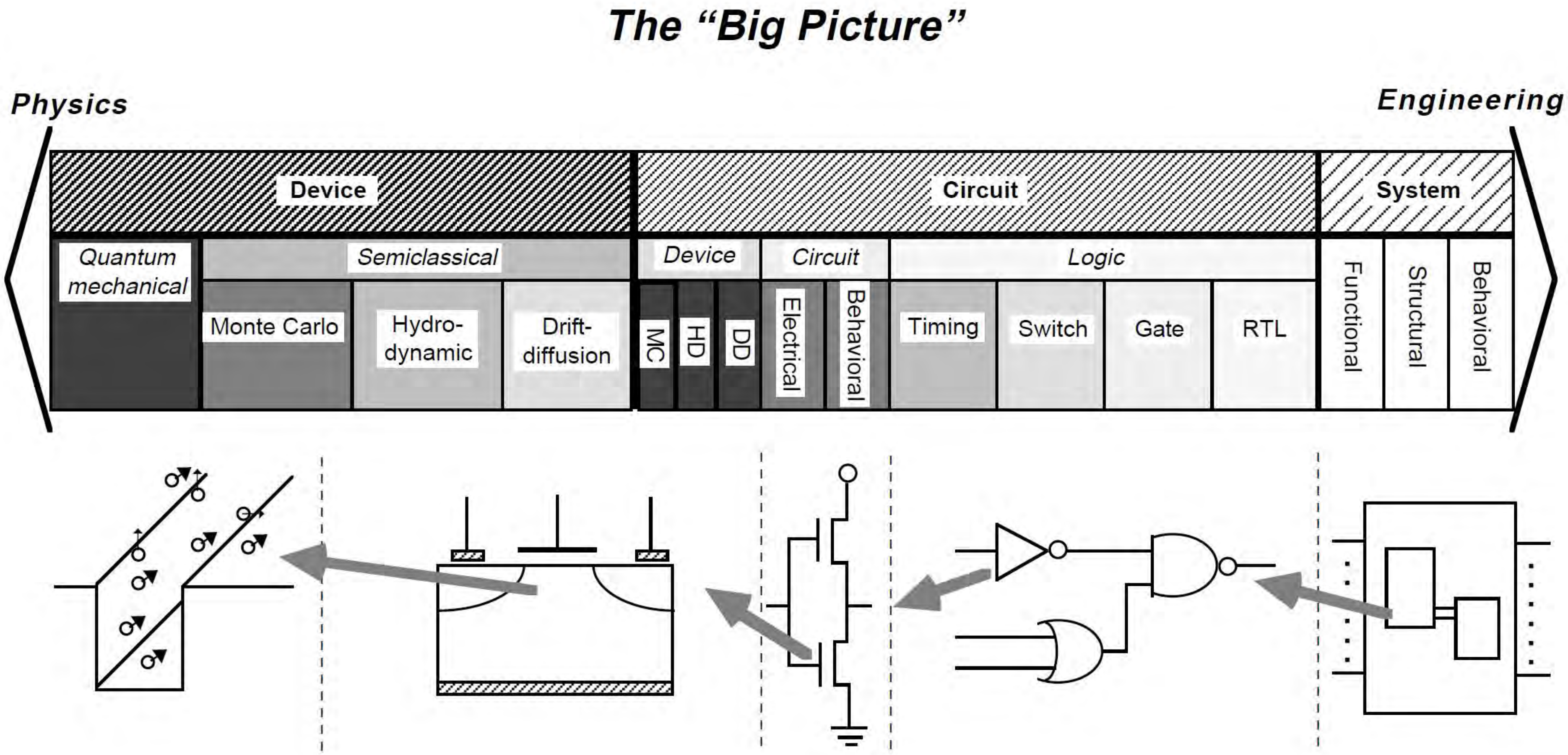
ST

cādence™

SYNOPSYS®

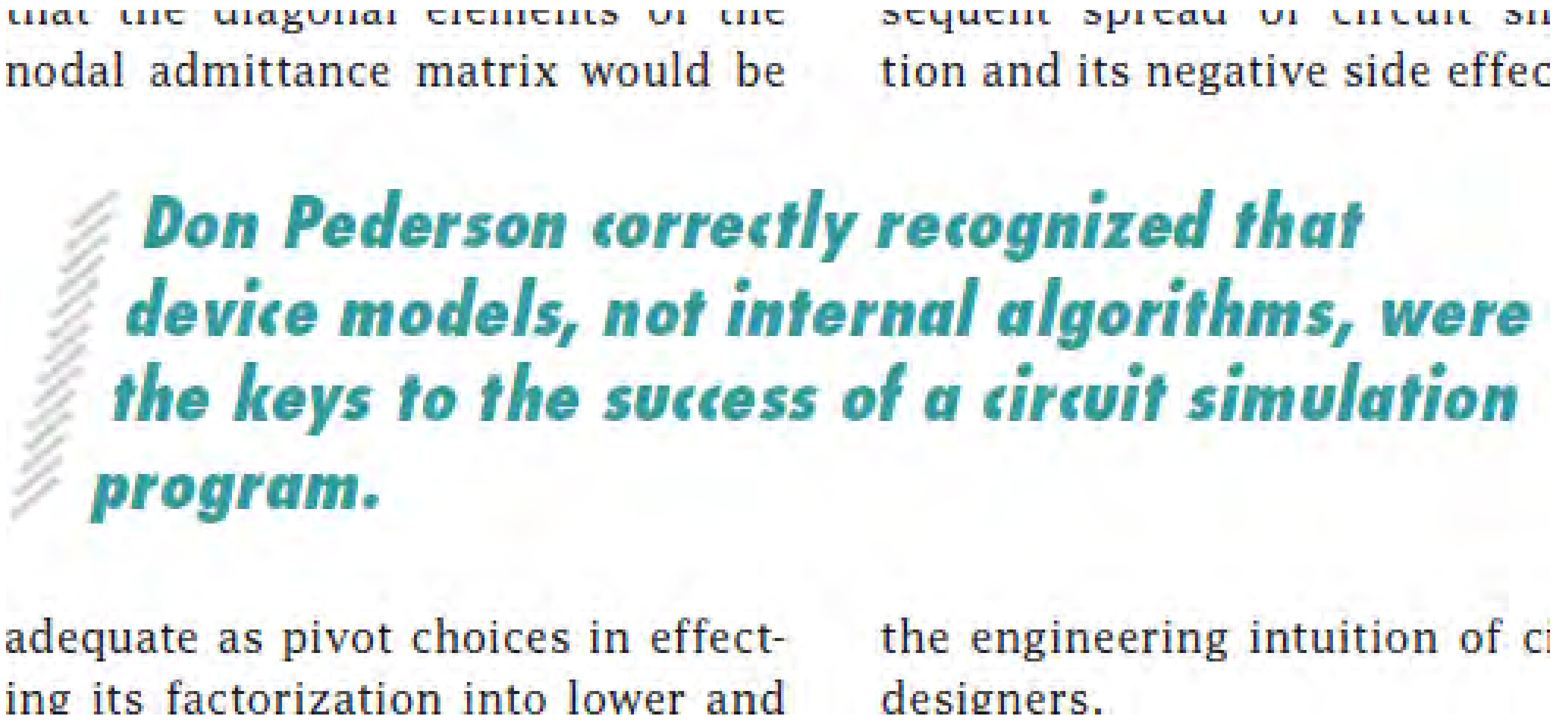
ANALOG DEVICES

Analyzing Electronic System



Source: Xing Zhou, NTU

SPICE and Device Models



> ***Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.***

nodal admittance matrix would be adequate as pivot choices in effecting its factorization into lower and

tion and its negative side effec

the engineering intuition of ci designers.

Ron Rohrer

Special Issue on 40th Anniversary of SPICE

SPRING 2011 *IEEE SOLID-STATE CIRCUITS MAGAZINE*

Device Model

- Good SPICE model should be
  - Accurate
    - Produce trustworthy simulations
  - Simple
    - Simulation time is minimum
    - Easy parameter extraction
- Balance between accuracy and simplicity depends on end application

Creating a model that is both accurate and simple is by no means a simple task.

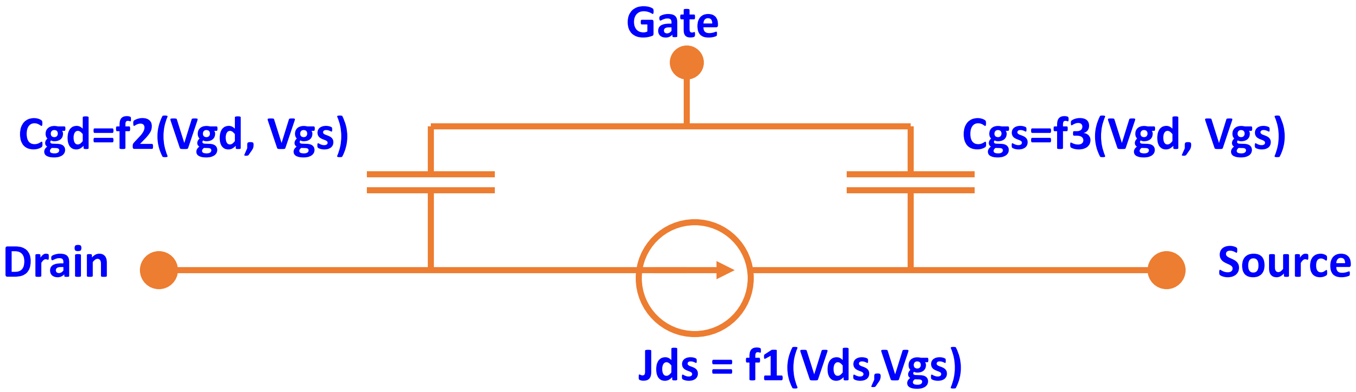
Model Types

- Look Up Table
- Physical model generally does not have parameters but does not fit with data accurately.
- Empirical models are mathematical models written to reflect measured characteristics
  - Angelov model for HEMT
- Compact SPICE models are the combination of physical and empirical methods.

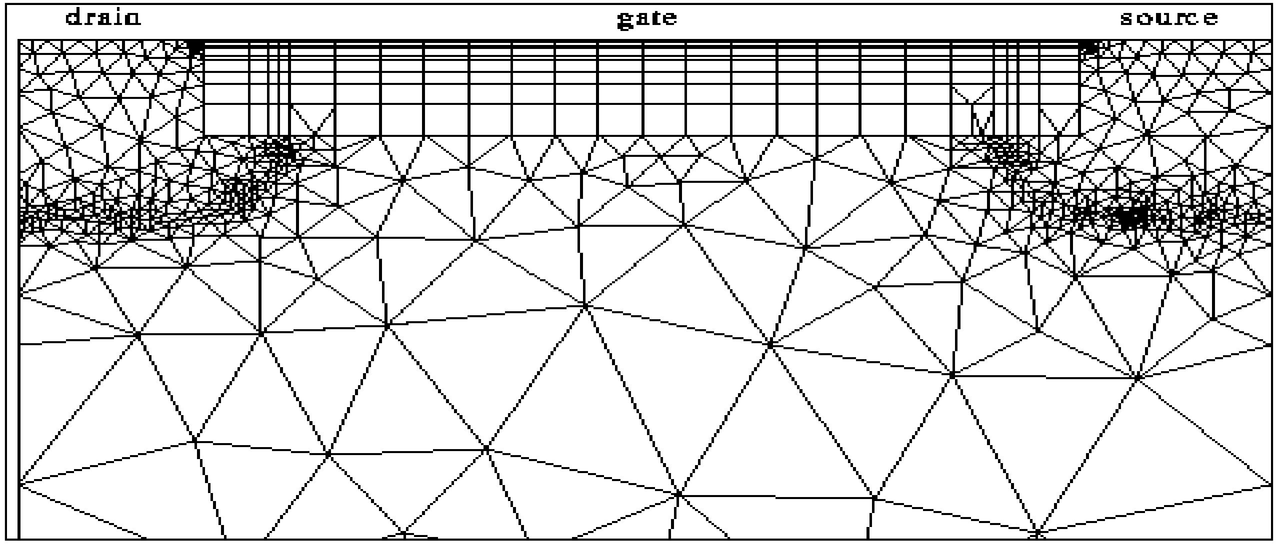
What is a Compact Model?

Compact MOSFET Model

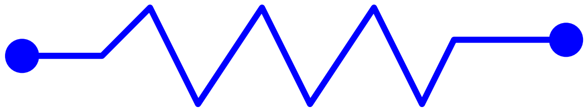
Compact Model



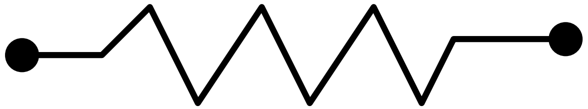
TCAD Model



Compact model complexity



I = V/R is a compact model for a resistor

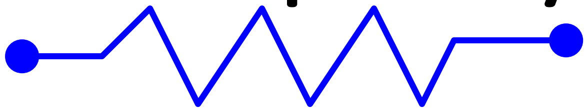


I = V/((q$_o$+TCR*(T-25))*(L-dL)/(W-dW))

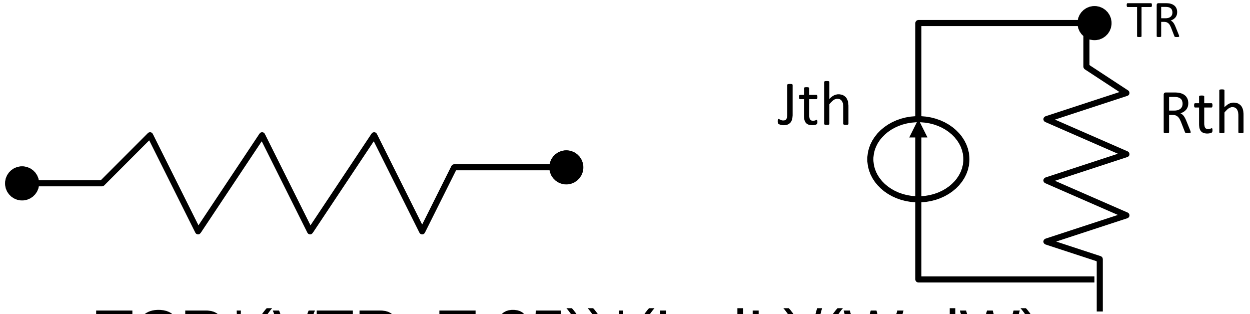
Add: Geometric Scaling

Temperature Scaling

Compact model complexity



I = V/R is a compact model for a resistor



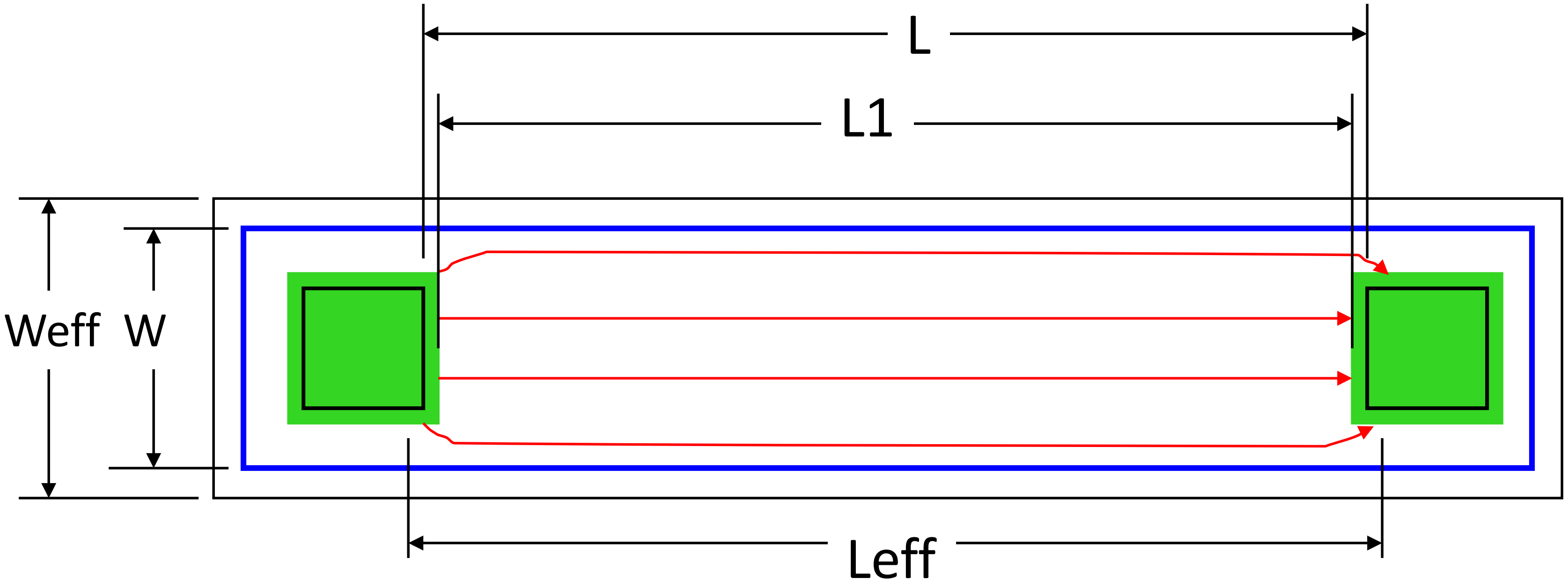
$I = V/((q_o+TCR*(VTR+T-25))*(L-dL)/(W-dW)$

Jth = V*I

Rth=Rth/(L*W)

Add: Geometric Scaling
Temperature Scaling
Self Heating

Effective Dimensions

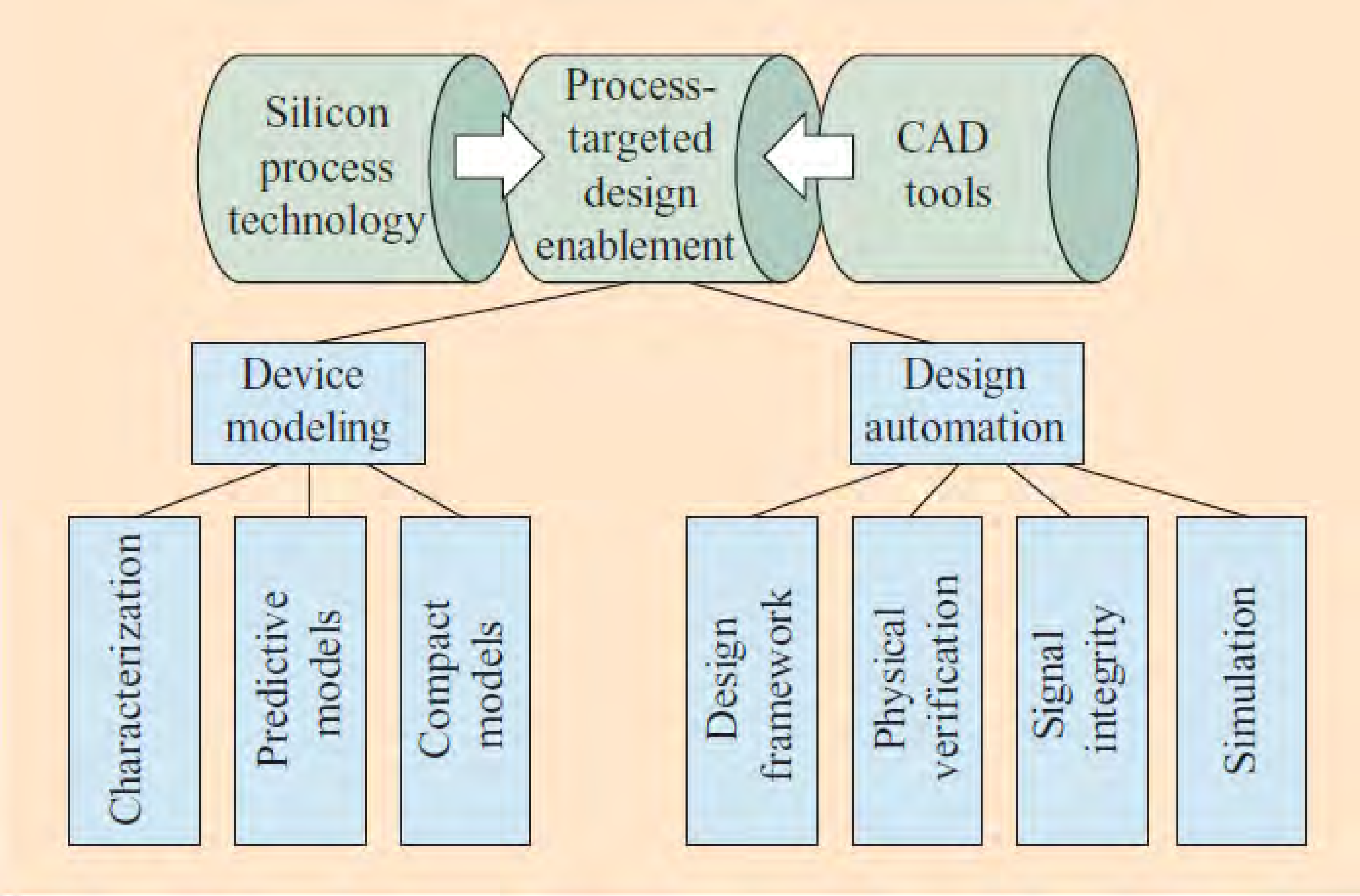


Drawn dimensions
Poly after etch
Contact after etch
Current Flow

L1 accounts for etch bias
Leff accounts for etch bias and spreading resistance

PDK and Compact Model

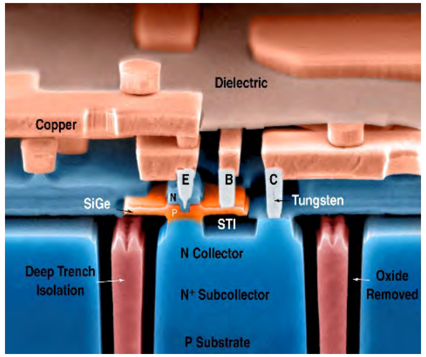
Enablers of a silicon chip design



Source: David HARAME at. al., IBM J. RES. & DEV. MARCH/MAY 2003

Goal of a PDK – The output of Enablement

Technology Innovation

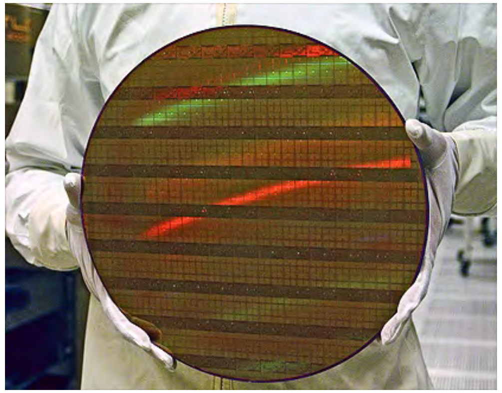


Enablement PDK
Key to Happy Designers!!

Circuit Designers

- Offer a circuit design environment that enables full exploitation of technology
  - Capture all device physics
  - Model impact of layout choices on device mean and variance
  - Include typical layout effects for simulation from schematic
  - Accurate modeling of layout effects for simulation from layout

Compact Modeling or SPICE Modeling



Medium of information exchange

- Good model should be
    - **Accurate:** Trustworthy simulations.
    - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~μsec
- Accuracy requirements
    - ~ 1% RMS error after fitting
- Example: BSIM-BULK, BSIM-CMG, BSIM-IMG

Industry Standard Compact Models

- Standardization Body – Compact Model Coalition
- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

http://www.si2.org/cmc/

Si2 Compact Models

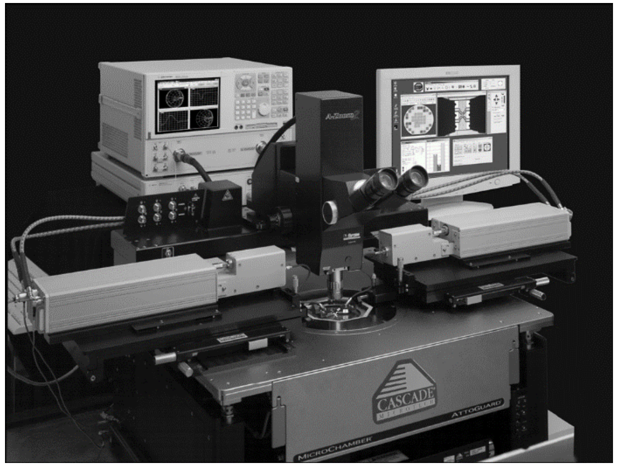
Compact Model Coalition (CMC) Members

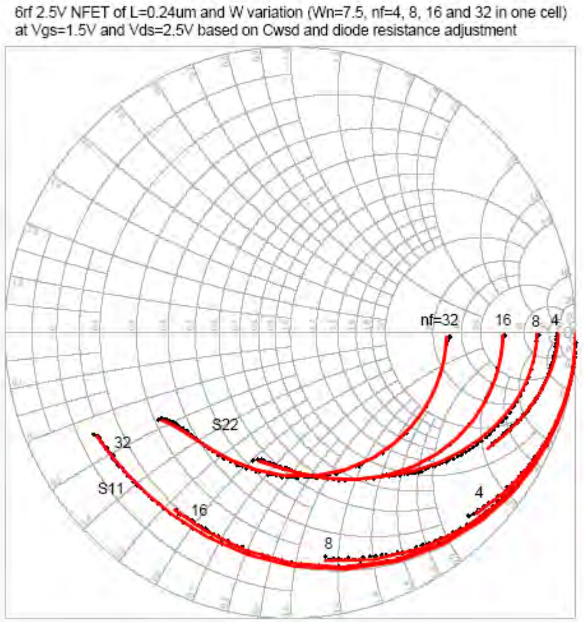
Currently, 32 companies are CMC members including the following:

- ams AG
- Analog Devices
- AWR/National Instruments Corporation
- Broadcom Corporation
- Cadence Design Systems
- Empyrean Software
- Fujitsu
- GLOBALFOUNDRIES
- IBM Corporation
- Infineon Technologies
- Intel Corporation
- Keysight Technologies
- Mentor Graphics Corporation
- Micron Technology, Inc.
- NXP
- ProPlus Design Solutions
- Qorvo
- Qualcomm
- Raytheon
- Renesas Electronics Corporation
- Ricoh
- Samsung Electronics Co., Ltd.
- Sandia National Laboratories
- Silvaco Inc.
- SK Hynix Inc.
- Sony
- STMicroelectronics
- Synopsys
- Taiwan Semiconductor Manufacturing Company Limited
- Texas Instruments
- Toshiba Corporation
- TowerJazz

Compact Model Build

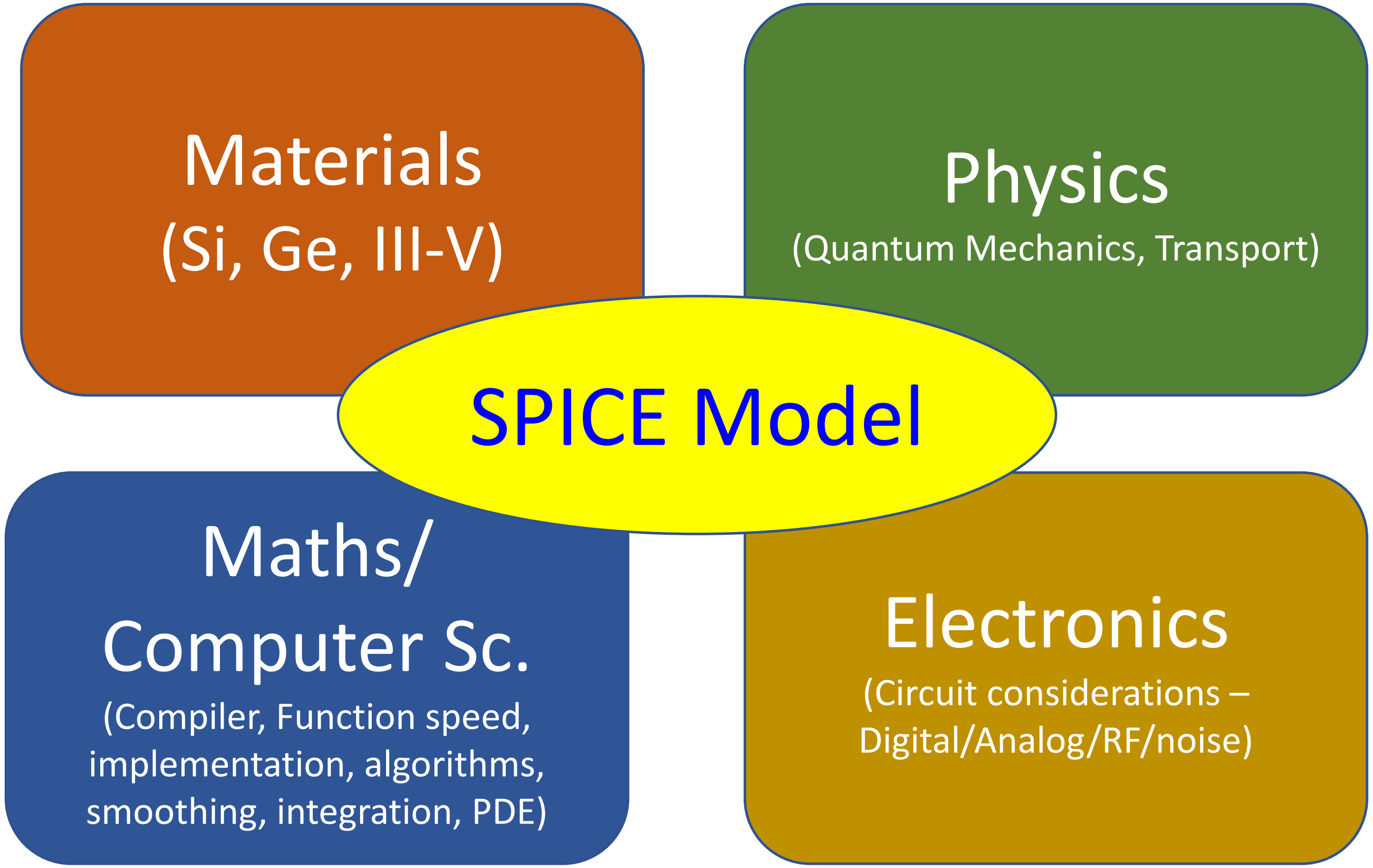
- Test site Specification
- Test site Layout
- Hardware build
- Measure data
- Fit to measured data
- Center model
- Test for convergence, physicality
- Model Process Variation
- Kit Integration
- Kit Test
- Release to customers





Curtesy: Josef Watts, IBM/GF

Challenges in Compact Modeling



Materials
(Si, Ge, III-V)

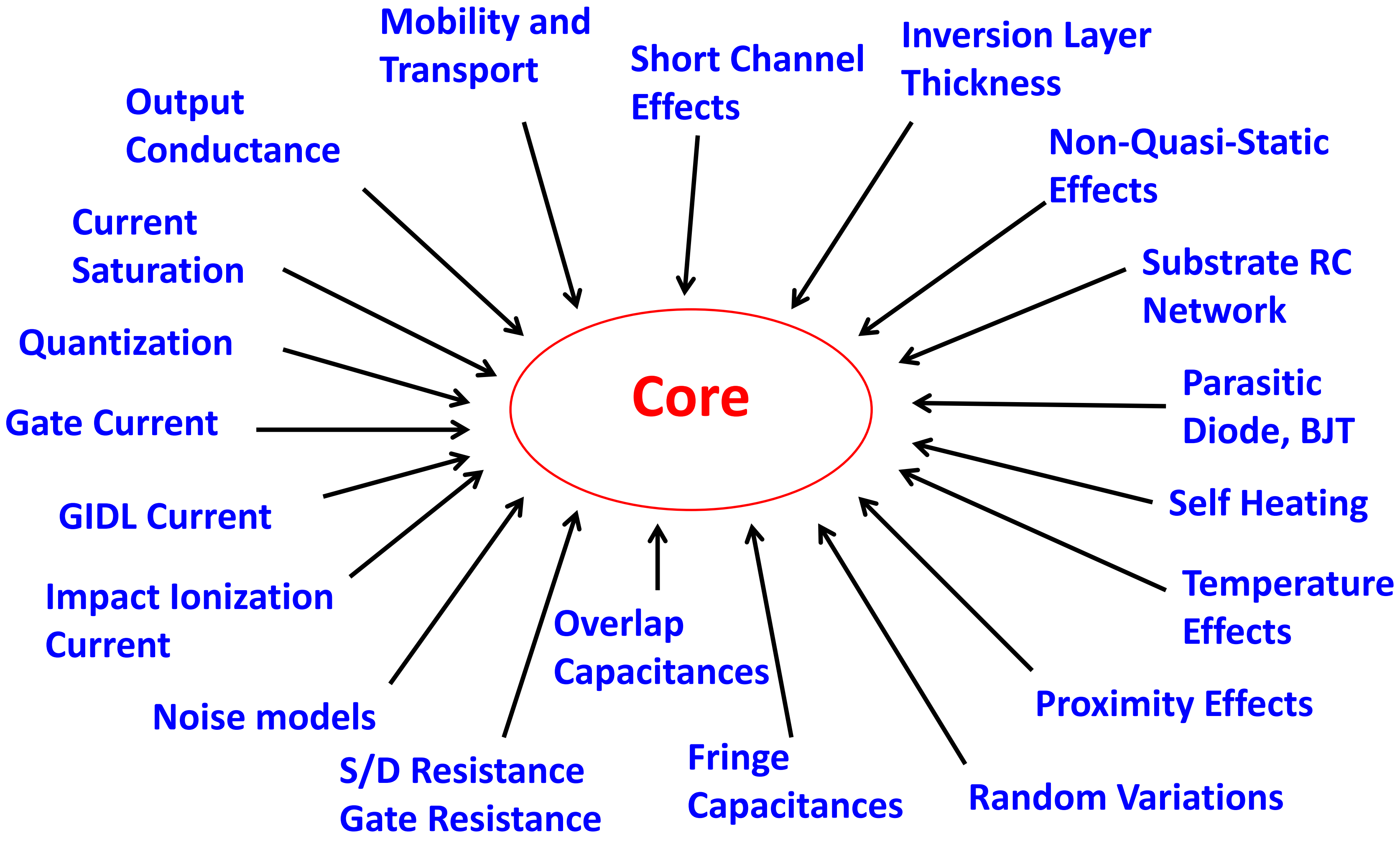
Physics
(Quantum Mechanics, Transport)

SPICE Model

Maths/
Computer Sc.
(Compiler, Function speed, implementation, algorithms, smoothing, integration, PDE)

Electronics
(Circuit considerations – Digital/Analog/RF/noise)

Compact Model is Art Based on Science



Core

Mobility and Transport

Short Channel Effects

Inversion Layer Thickness

Non-Quasi-Static Effects

Substrate RC Network

Parasitic Diode, BJT

Self Heating

Temperature Effects

Proximity Effects

Random Variations

Fringe Capacitances

Overlap Capacitances

S/D Resistance
Gate Resistance

Noise models

Impact Ionization Current

GIDL Current

Gate Current

Quantization

Current Saturation

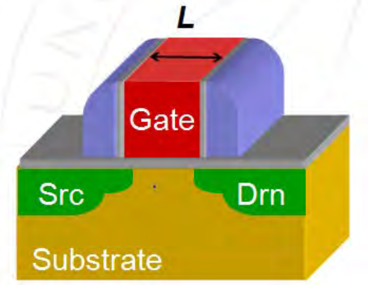
Output Conductance

Y. S. Chauhan et.al., “BSIM6: Analog and RF Compact Model for Bulk MOSFET,” IEEE TED, 2014.

BSIM Family of Compact Device Models

1990 **1995** **2000** **2005** **2010**

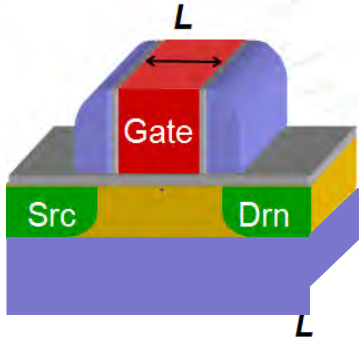
BSIM1,2 **BSIM3**



BSIM4

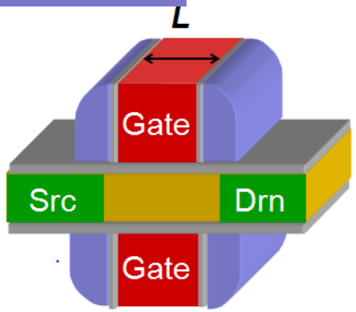
Conventional MOSFET

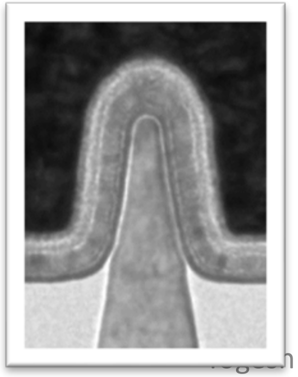
BSIM5 **BSIM-BULK (BSIM6)**



Silicon on Insulator MOSFET

BSIMSOI



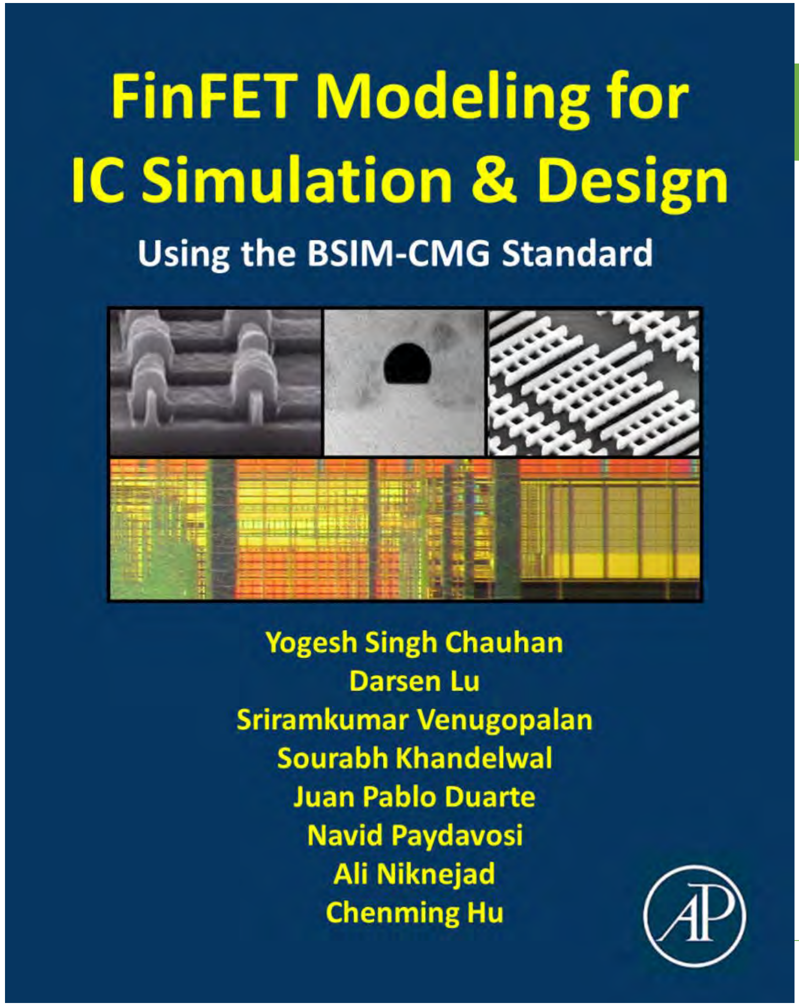


BSIM-CMG
BSIM-IMG

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



FinFET Modeling for IC Simulation & Design

Using the BSIM-CMG Standard

Yogesh Singh Chauhan
Darsen Lu
Sriramkumar Venugopalan
Sourabh Khandelwal
Juan Pablo Duarte
Navid Paydavosi
Ali Niknejad
Chenming Hu

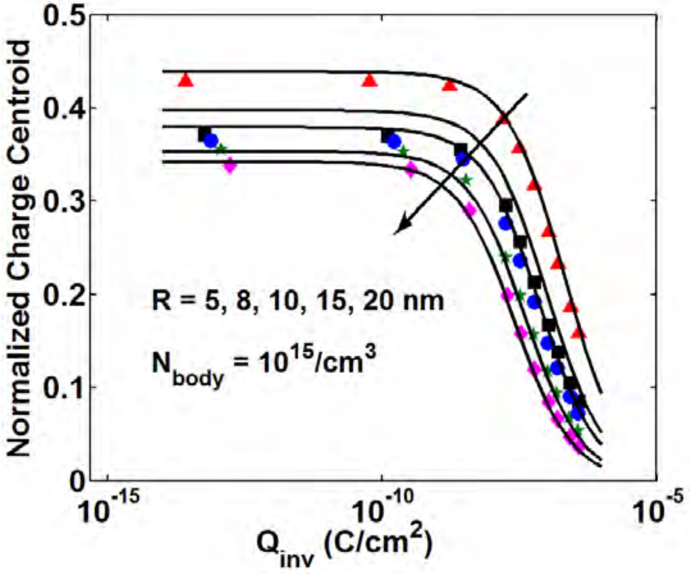
Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

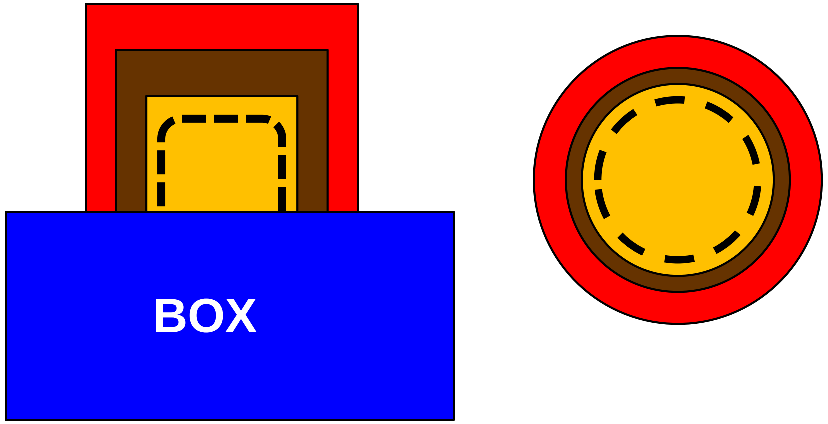
Some Snapshots from recent work

Quantum Mechanical Effects

- Predictive model for confinement induced V_{th} shift due to band splitting present in the model
- Effective Width model that accounts for reduction in width for a triple / quadruple / surround gate structure



S. Venugopalan et. al., IEEE TED, 2013



FinFET/Nanosheet Transistor

Width reduction due to structural confinement of inversion charge. (Dotted lines represent the effective width perimeter)

Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

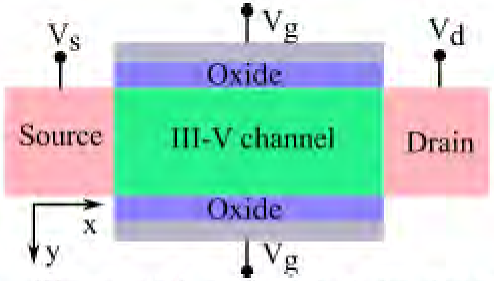
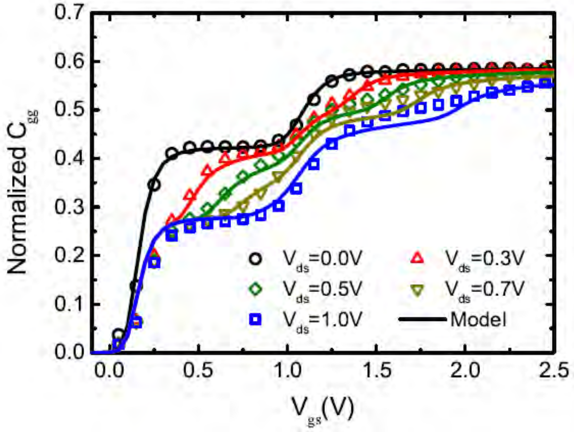
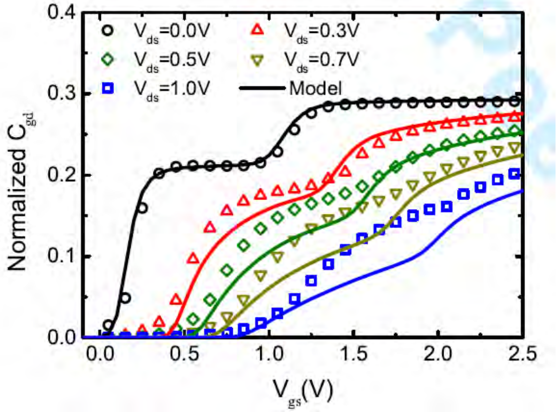
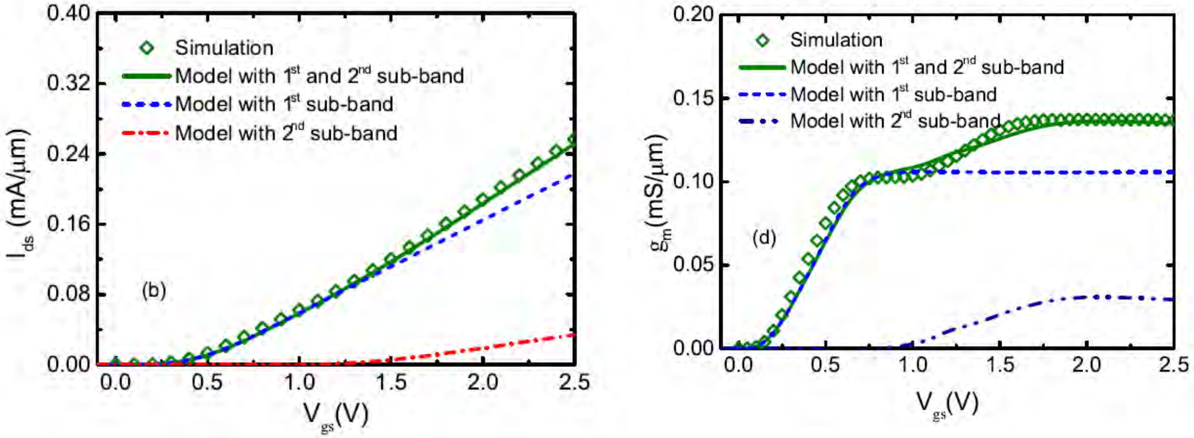


Fig. 1. Schematic of III-V channel double-gate field effect transistor (DGFET) used in the study where V_g, V_d and V_s denotes the applied voltage at gate, drain and source terminals, respectively.

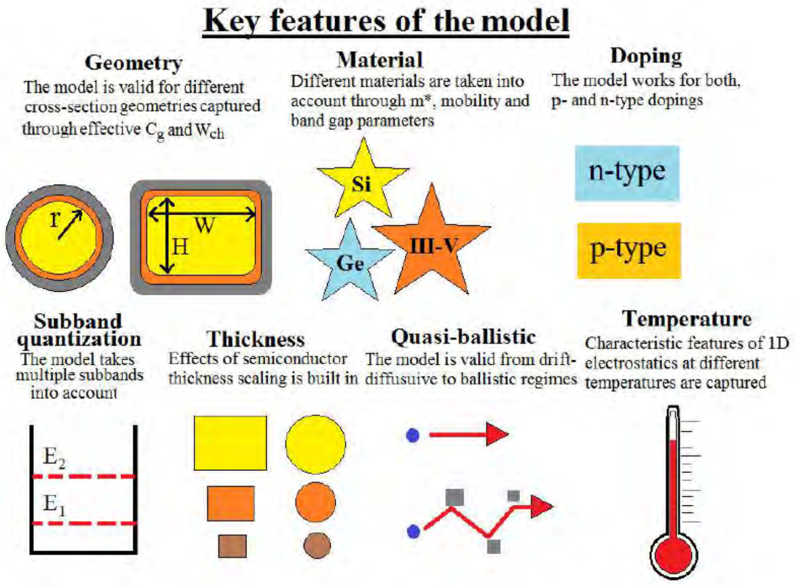






C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.

Modeling of Quasi-ballistic Nanowire FETs



Key features of the model

Geometry
The model is valid for different cross-section geometries captured through effective C_g and W_{ch}

Material
Different materials are taken into account through m*, mobility and band gap parameters

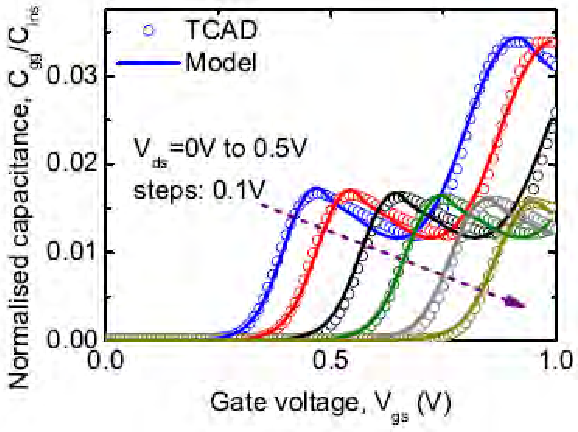
Doping
The model works for both, p- and n-type dopings

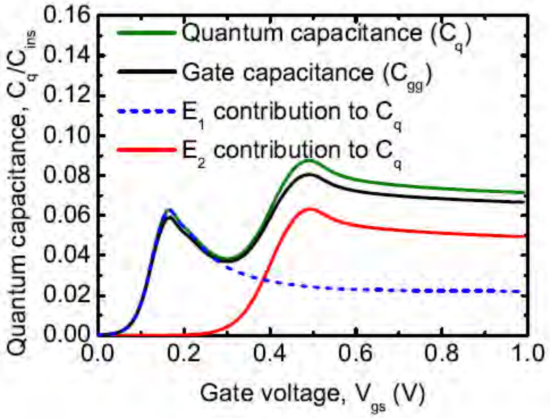
Subband quantization
The model takes multiple subbands into account

Thickness
Effects of semiconductor thickness scaling is built in

Quasi-ballistic
The model is valid from drift-diffusive to ballistic regimes

Temperature
Characteristic features of 1D electrostatics at different temperatures are captured





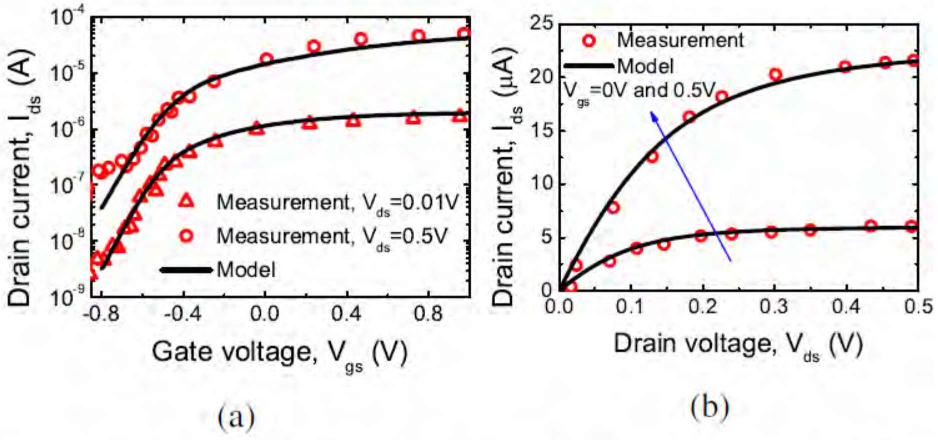
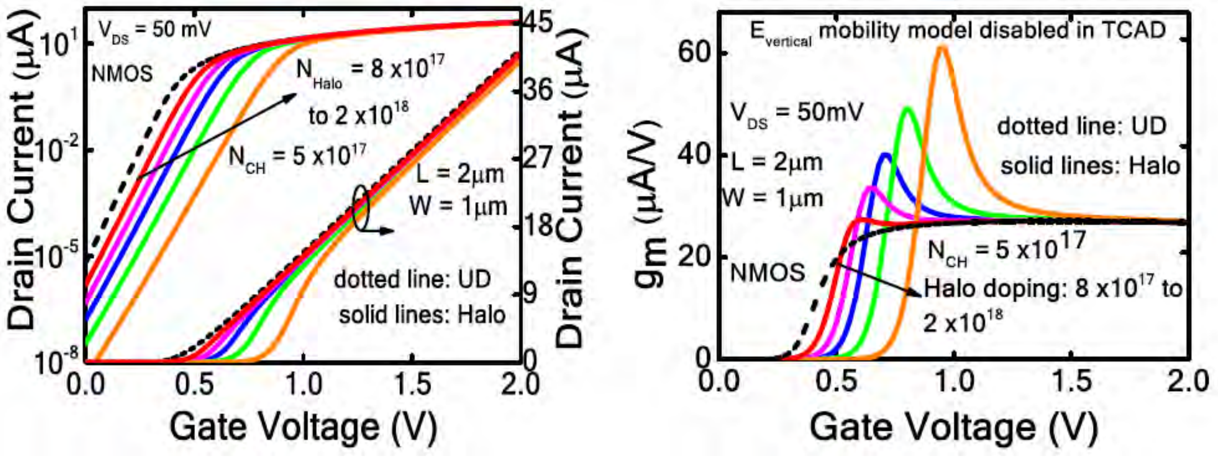
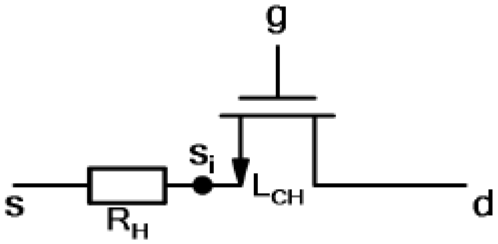


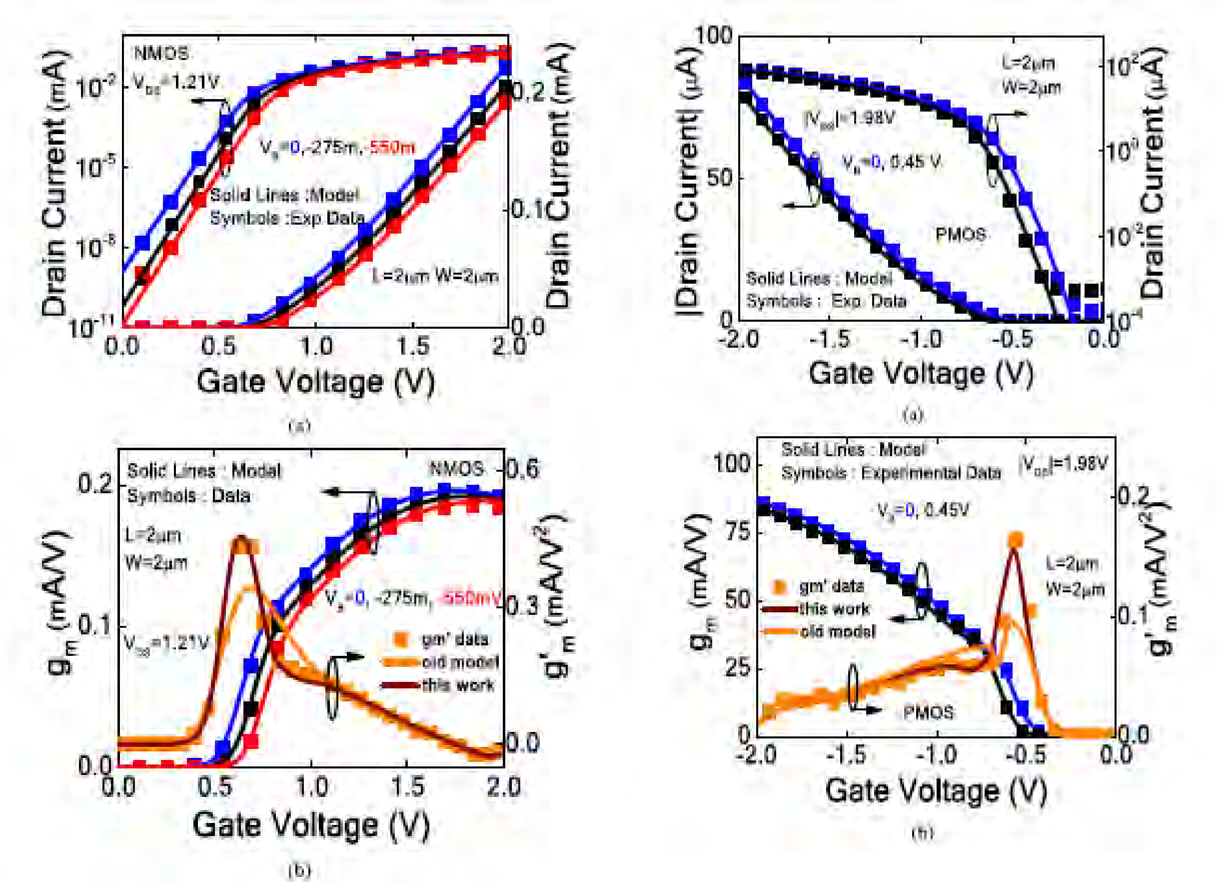
Fig. 12: **Circular quasi-ballistic InAs nanowire:** Drain current as a function of the gate and drain voltages for n-type $InAs$ nanowires, with a circular cross-section ($r = 7.5nm$), $L_g = 100nm$ and $EOT = 0.92nm$ (Device 5)[44], are shown in (a) and

Modeling of Long Channel Halo Implanted MOSFETs





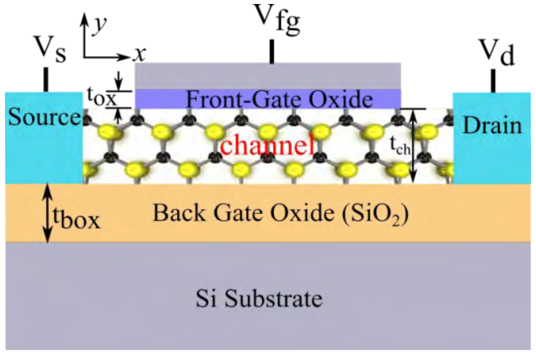
Part of BSIM-BULK (BSIM6) Model

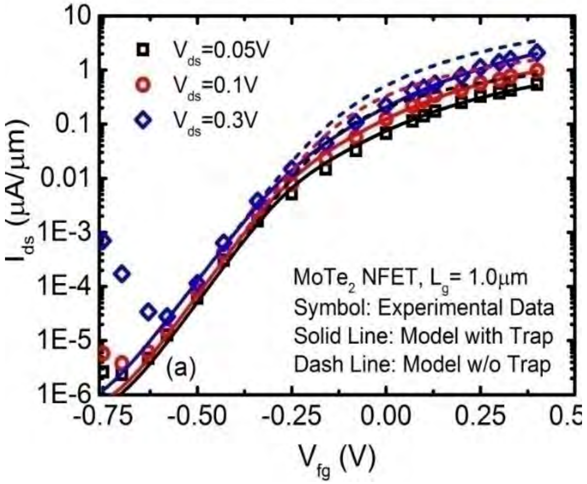


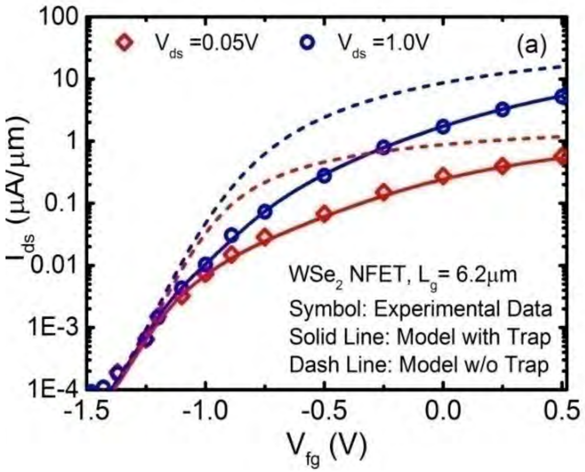
H. Agarwal et. al., "Anomalous Transconductance in Long Channel Halo Implanted MOSFETs: Analysis and Modeling", IEEE TED, Feb. 2017.

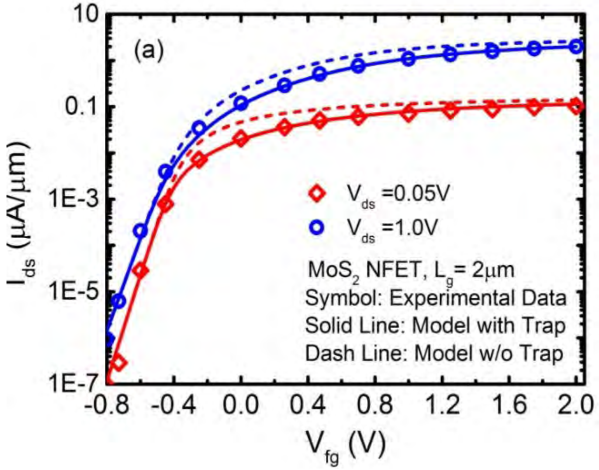
Modeling of TMD transistor

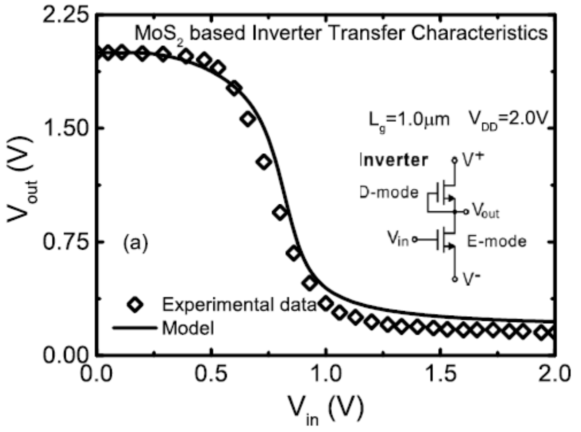
- 2D density of state
- Fermi–Dirac statistics
- Trapping effects











C. Yadav et. al. "*Compact Modeling of Transition Metal Dichalcogenide based Thin body Transistors and Circuit Validation*", IEEE TED, March 2017.

News (March 14, 2018)

- Our ASM-GaN-HEMT Model is industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

Si2 Approves IC Design Simulation Standards for Gallium Nitride Devices

March 14, 2018 / 0 Comments / in Compact Model, Frontpage /

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

http://www.si2.org/cmc/

http://www.si2.org/2018/03/14/gallium-nitride-models/

Media Coverage (April 11, 2018)

आईआईटी में बना सिमुलेशन सॉफ्टवेयर

यह सॉफ्टवेयर तैयार करने वाला दुनिया का दूसरा संस्थान बना आईआईटी कानपुर, आसानी से टेस्ट कर पाएंगे इंटीग्रेटेड सर्किट का डिजाइन

अमर उजाला ब्यूरो

कानपुर। आईआईटी कानपुर के वैज्ञानिकों ने पांच साल की मेहनत के बाद आखिरकर इंटीग्रेटेड सर्किट डिजाइन सिमुलेशन सॉफ्टवेयर तैयार कर लिया। इस सॉफ्टवेयर को तैयार करने वाला आईआईटी कानपुर दुनिया का दूसरा संस्थान है। इसके पहले अमेरिका के मैचाच्यूट्स इंस्टीट्यूट ऑफ टेक्नोलॉजी के वैज्ञानिकों ने इसे तैयार किया था।

इस सॉफ्टवेयर को इलेक्ट्रॉनिक्स विभाग के प्रो. योगेश चौहान ने तैयार किया है। इस सॉफ्टवेयर के जरिए इंटीग्रेटेड सर्किट की डिजाइन को आसानी से टेस्ट किया जा सकेगा। मतलब कोई भी सर्किट

डिजाइन करने से पहले इस

कंप्यूटर पर ही चेक किया जा

में क्या-क्या कमी है और इसे कै

सकता है। अभी तक इस सॉफ

लिए लाखों रुपये खर्च करने

आईआईटी में तैयार किया गया सिमुलेशन सॉफ्टवेयर।

आईआईटी के विशेषज्ञों ने खुद तैयार कर लिया है तो उम्मीद है कि आने वाले दिनों में देश के शिक्षण संस्थानों और देश की कंपनियों को इसके लिए कम कीमत चुकानी पड़े। प्रो. चौहान ने यह शोध अपने

बिजली की होगी बचत 5जी में भी भूमिका

सॉफ्टवेयर के जरिए जैन सेमीकंडक्टर के डिजाइन का भी परीक्षण किया जा सकेगा। इस सेमीकंडक्टर का प्रयोग बिजली की बचत के लिए किया जाता है। अभी तक इसका परीक्षण महंगा होता था लेकिन अब सॉफ्टवेयर तैयार होने से यह भी सस्ता हो जाएगा। इसके अलावा इस सॉफ्टवेयर का प्रयोग 5 जी की तकनीक विकसित करने में भी की जा सकेगी।

सभी इलेक्ट्रॉनिक डिवाइस में प्रयोग होता है इंटीग्रेटेड सर्किट

इंटीग्रेटेड सर्किट का प्रयोग हर तरह के इलेक्ट्रॉनिक और

अब झटपट बनेंगे इलेक्ट्रॉनिक उपकरण

जागरण संवाददाता, कानपुर : आइआइटी कानपुर के इलेक्ट्रिक इंजीनियरिंग विभाग के प्रो. योगेश चौहान की खोज से मजबूत और टिकाऊ इलेक्ट्रानिक उपकरण भी झटपट बन जाएंगे। उन्होंने ऐसा इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार किया है, जिसकी सहायता से चंद मिनटों में किसी भी इलेक्ट्रानिक गैजेट्स का कंप्यूटरीकृत डिजाइन बन सकेगा। इस खोज से आइआइटी कानपुर यूएसए के मैसाचुसेट्स इंस्टीट्यूट ऑफ टेक्नालाजी (एमआइटी) के बाद इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार करने वाला दुनिया का

- आइआइटी प्रोफेसर ने बनाया इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर

प्रो. योगेश चौहान

यूएस डालर : प्रो. चौहान ने आस्ट्रेलिया के सहयोगी प्रो सौरभ खंडेलवाल के साथ पांच साल की कड़ी मेहनत के बाद साफ्टवेयर तैयार किया। अनुसंधान एवं विकास के

कों को हर साल

लर का अनुदान

नक विज्ञान के

रत : साफ्टवेयर

ज्ञान के साधारण

है। किसी भी

का कैसा डिजाइन

सकी आसानी से

रक्षा क्षेत्र और अंतरिक्ष कार्यक्रम में सहयोग

प्रो. चौहान के मुताबिक साफ्टवेयर से रक्षा क्षेत्र और अंतरिक्ष कार्यक्रम में काफी सहयोग मिलेगा। 5जी के हाई स्पीड एम्पलीफायर बनाने में मदद मिलेगी। चालकरहित कार, रिमोट सर्जरी आदि बनाना संभव हो जाएगा।

'आईआईटीके' ने बनाया सर्किट सिम्यूलेशन सॉफ्टवेयर मॉडल

■ सहारा न्यूज ब्यूरो

कानपुर।

आईआईटी, कानपुर (आईआईटीके) संयुक्त राज्य अमरीका के मैसाच्यूट्स इंस्टीट्यूट ऑफ टेक्नालॉजी के वाद इंट्रीगेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार करने वाला दुनिया का दूसरा संस्थान वन गया है। यह सॉफ्टवेयर इंडस्ट्री के क्षेत्र में मील का पत्थर सावित होगा। कई सालों के कठोर परिश्रम के वाद संस्थान ने यह सफलता पायी है।

संस्थान के विद्युत अभियांत्रिकी विभाग के प्रो.योगेश सिंह चौहान की अगुवाई में डिजाइन सिम्यूलेशन तैयार किया गया है। प्रो.चौहान व उनके आस्ट्रेलियन सहयोगी सौरभ खंडेलवाल ने इस मॉडल को तैयार करने में कड़ी मेहनत की। अनुसंधान एवं विकास के लिए दोनों वैज्ञानिकों को सीएमसी द्वारा प्रतिवर्ष 70 हजार यूएस डॉलर का अनुदान स्वीकृत किया गया है। इस परियोजना के तहत शोध कार्य लंवे समय 10-15 वर्षों तक चलने की संभावना है। प्रो.चौहान एवं उनकी टीम इसरो व डीआरडीओ के साथ मिलकर परीक्षण मॉडल तथा जीएएन उपकरणों के विकास के लिए भी कार्य कर रही है।

वताया जाता है कि जीएएन सेमी कंडक्टर उपकरण वनाने वाली कंपनियां इस टीम के द्वारा विकसित मॉडल से वास्तविक उत्पादन करने से पहले अपने सर्किट का परीक्षण कर पाएंगे। इसे जीएएन सेमीकंडक्टर उपकरणों की लागत में कमी लायी जा सकेगी। पावर डिवाइसेज में जीएएन सेमी कंडक्टर का उपयोग किये जाने से ऊर्जा की वचत होगी व उसकी क्षमता वढ़ेगी। वर्तमान में सिलिकान सेमीकंडक्टर का वहुत प्रचलन है, किन्तु शीघ्र ही जीएएन का उपयोग इसके विकल्प के रूप में कई एप्लीकेशन में होने में की उम्मीद जतायी जा रही है। इसके अलावा संस्थान के विद्युत

शेष पेज 13

प्रो. योगेश सिंह चौहान

संस्थान के प्रो.योगेश चौहान ने आस्ट्रेलियन सहयोगी संग मिल तैयार किया डिजाइन

'आईआईटीके' एमआईटी अमरीका के बाद सिम्यूलेशन बनाने वाला दूसरा संस्थान

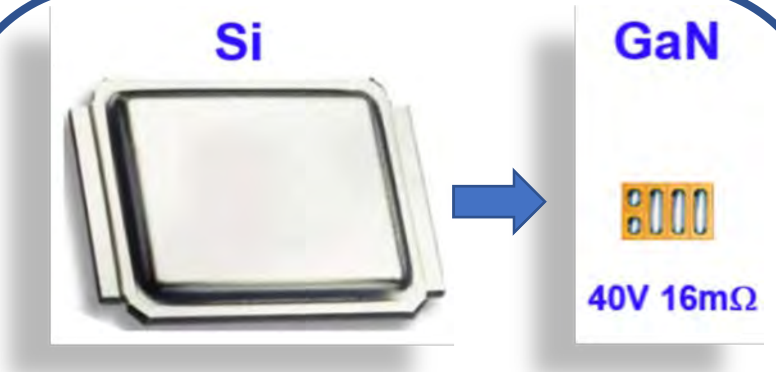
आगे अनुसंधान के लिए सीएमएसी देगा 70 हजार यूएस डॉलर प्रति वर्ष

अंतरिक्ष, रक्षा व पावर क्षेत्र के लिए उपयोगी होगा सिम्यूलेशन

पूर्व में रामानुजन फेलो सहित कई सम्मानएवार्ड से सम्मानित प्रो.योगेश कुमार चौहान ने वताया कि संवंधित सेमी कंडक्टर व साफ्टवेयर पावर एम्प्लीफायर अंतरिक्ष अनुसंधान के लिए उपयोगी होगा। संवंधित उपकरणों की उत्पादन लागत कम की जा सकेगी व पावर उपकरणों की कार्यकुशलता एक्यूरेसी वढ़ेगी। भविष्य के 5 जी तकनीक के लिए भी यह काफी उपयोगी होगा। अंतरिक्ष अनुसंधान के क्षेत्र में काम आने वाले उपकरणों की कार्यकुशलता वढ़ाने में यह सहायक सिद्ध होगा।

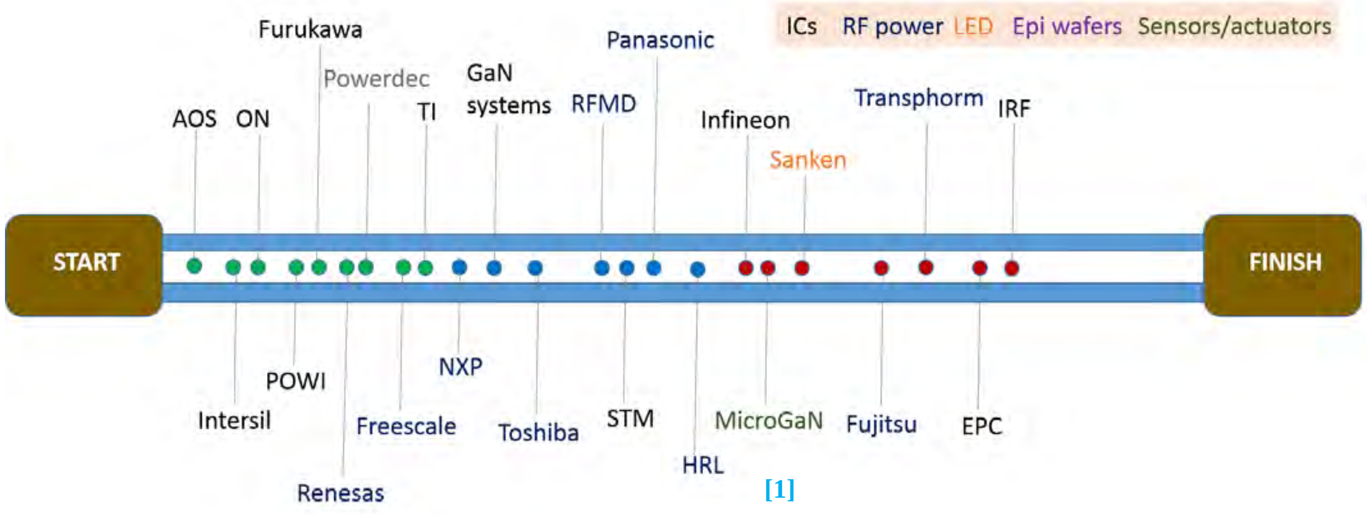
GaN Attractions & Avenues

Size Comparison



Size comparison of Si power MOSFET with GaN HEMT from EPC for same performance

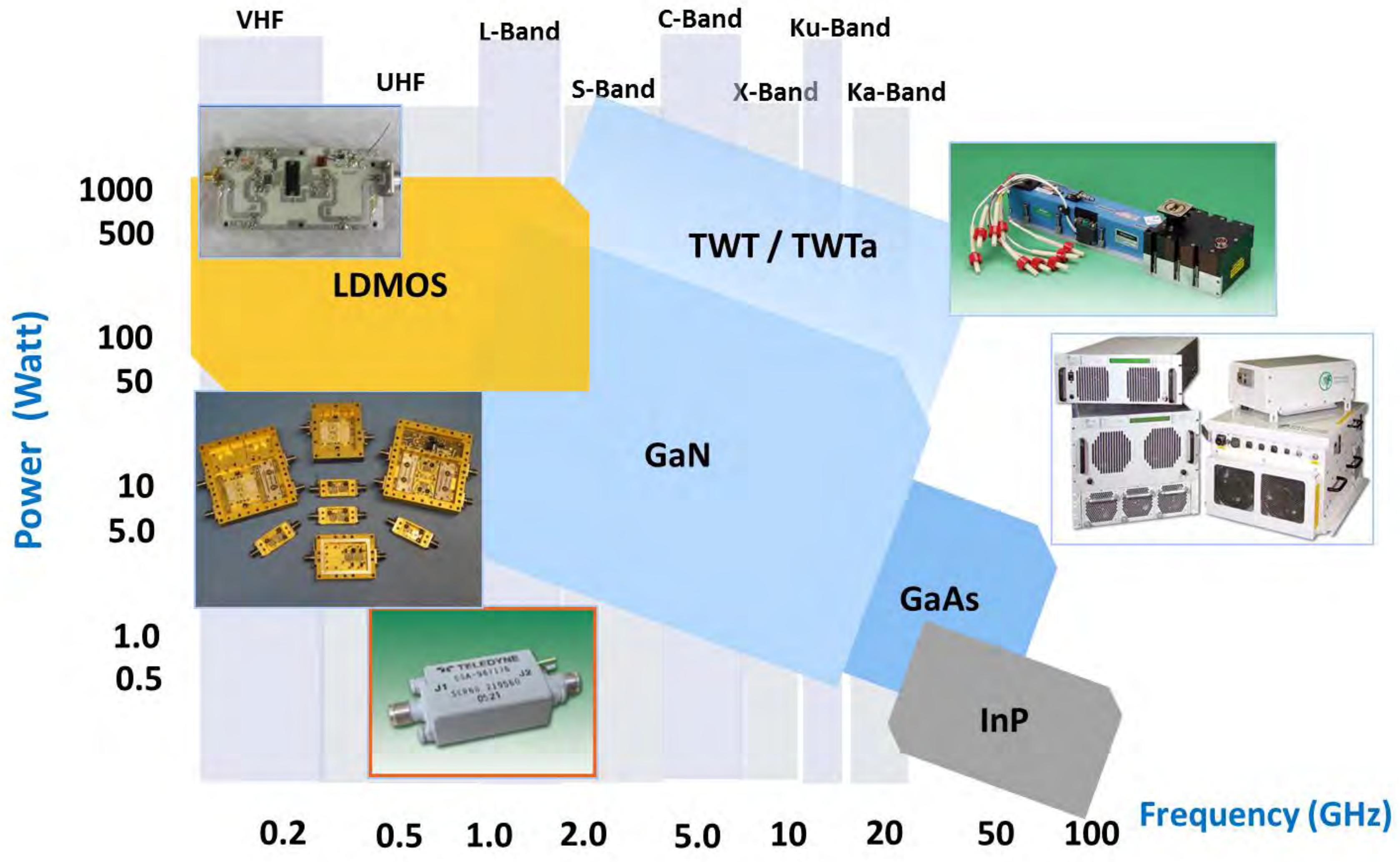
Size comparison of RF HEMTs based on GaAs and GaN technologies from Qorvo



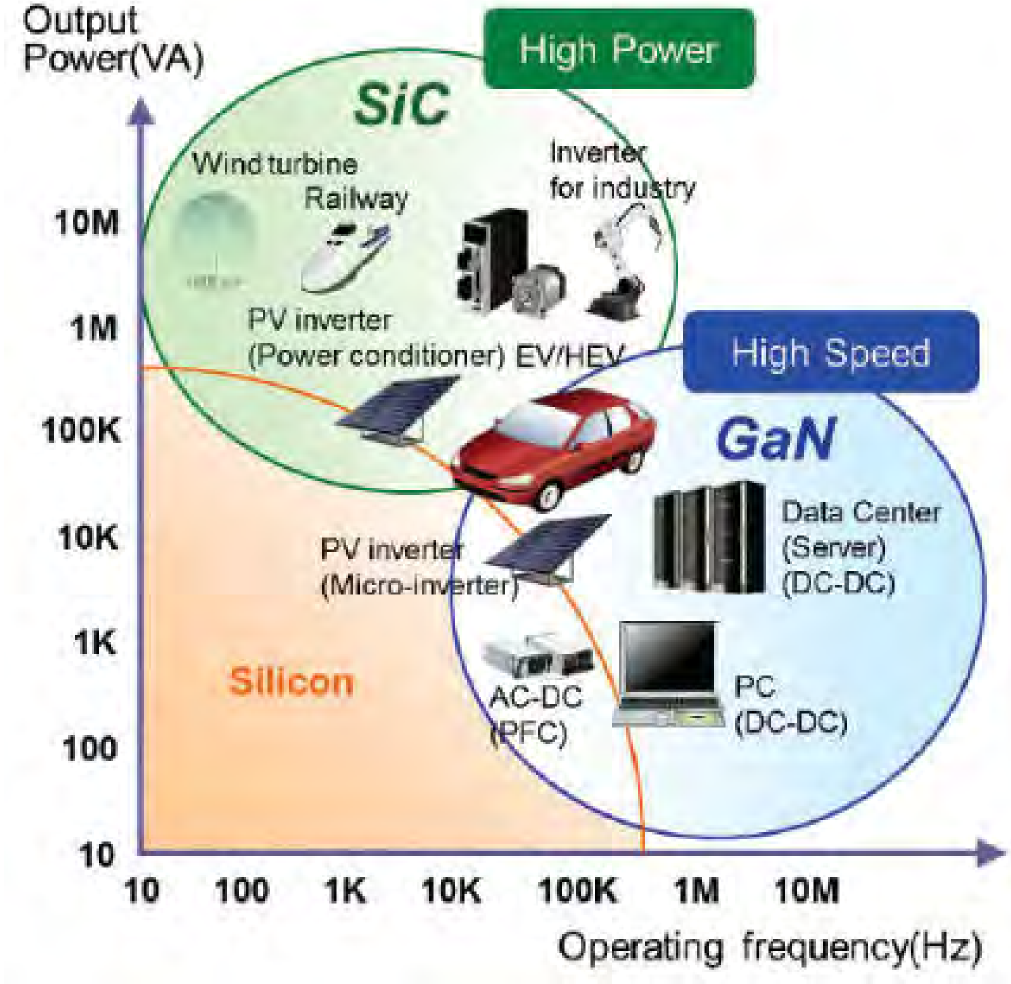
Industry players for power applications as of 2012

Source: S. Levin, Tech. Rep., Power Petrov Group, [2013]

RF Market


VHF
UHF
L-Band
S-Band
C-Band
X-Band
Ku-Band
Ka-Band
Power (Watt)
1000
500
100
50
10
5.0
1.0
0.5
LDMOS
TWT / TWTa
GaN
GaAs
InP
0.2
0.5
1.0
2.0
5.0
10
20
50
100
Frequency (GHz)

Power Transistor Market

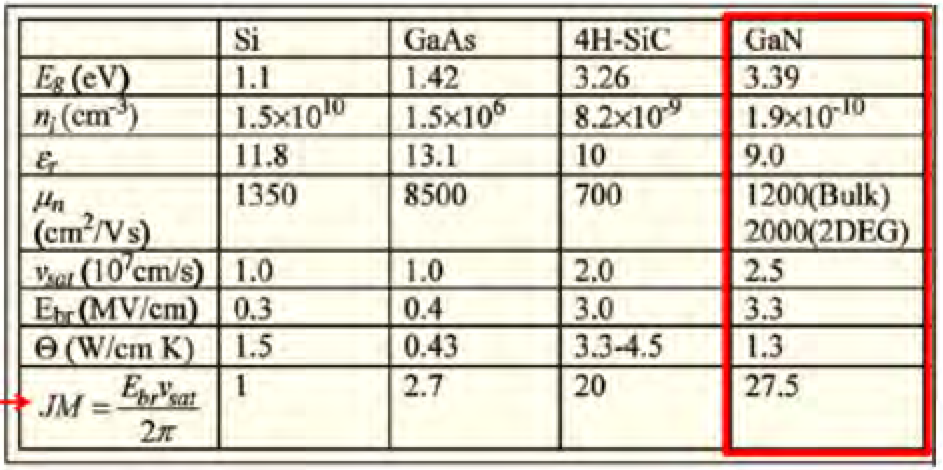


Source: Electronics Weekly

SiC for high power voltages (>1kV) with high current
= niche market

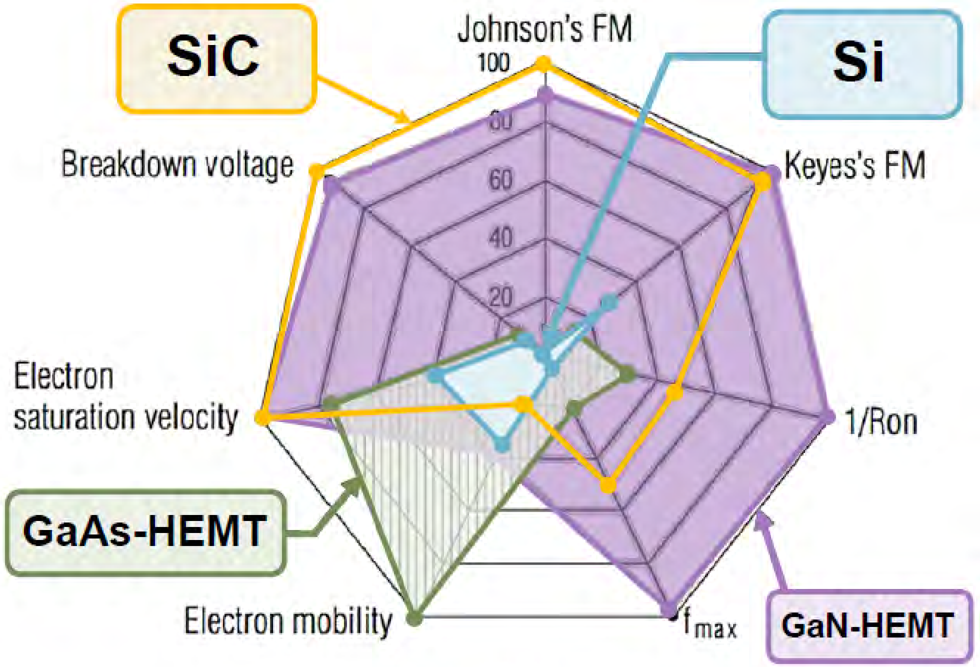
GaN on Si for high frequency at midrange voltages (<1kV, up to 100A)
= mass market

GaN Properties

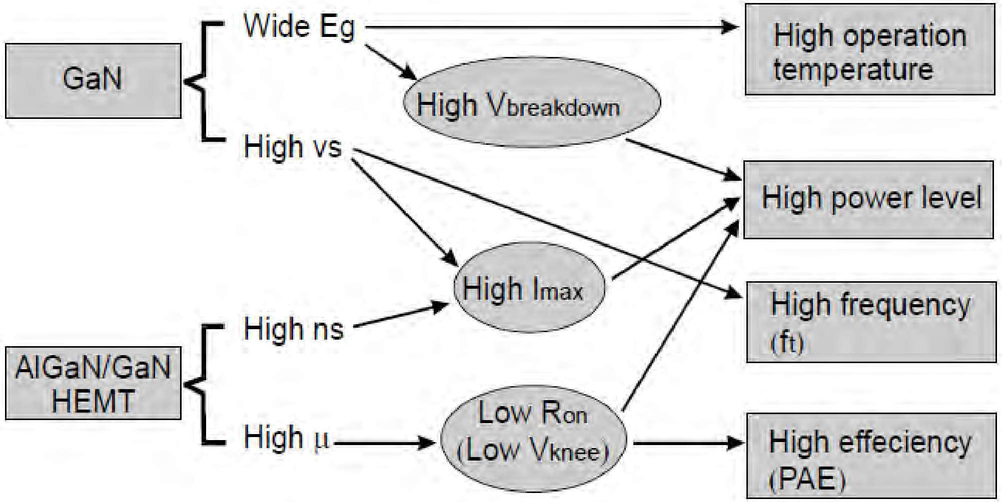


	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.1	1.42	3.26	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0
μ_n (cm^2/V s)	1350	8500	700	1200(Bulk) 2000(2DEG)
v_{sat} (10^7cm/s)	1.0	1.0	2.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5

Johnson's figure of merit (rel. to Si) →



Source: OKI Semiconductors



GaN

Wide Eg

High vs

High $V_{breakdown}$

High operation temperature

High power level

High I_{max}

High frequency (ft)

AlGaN/GaN HEMT

High ns

High μ

Low R_{on} (Low V_{knee})

High effeciency (PAE)

Device characteristics:

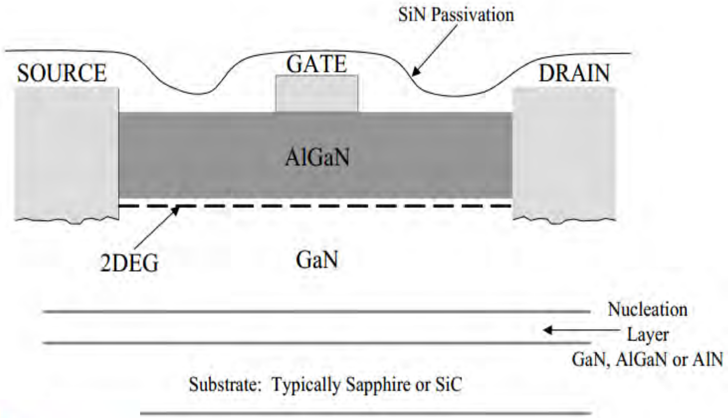
- High Breakdown Voltage (V_{BR})
- Low ON Resistance (R_{ON})

GaN HEMT

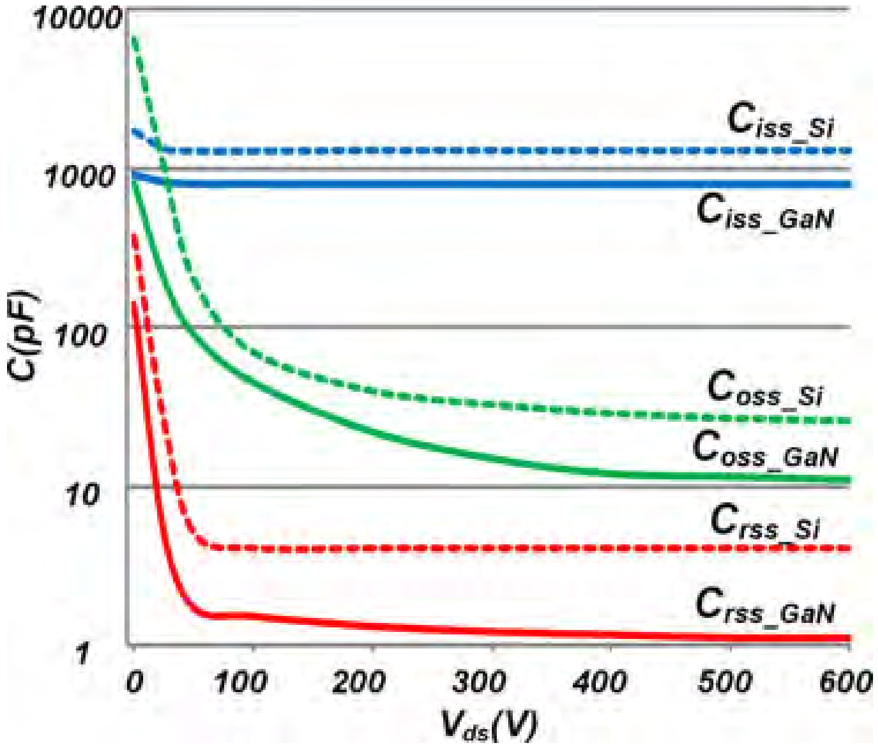
Some interesting features of III-nitride system:

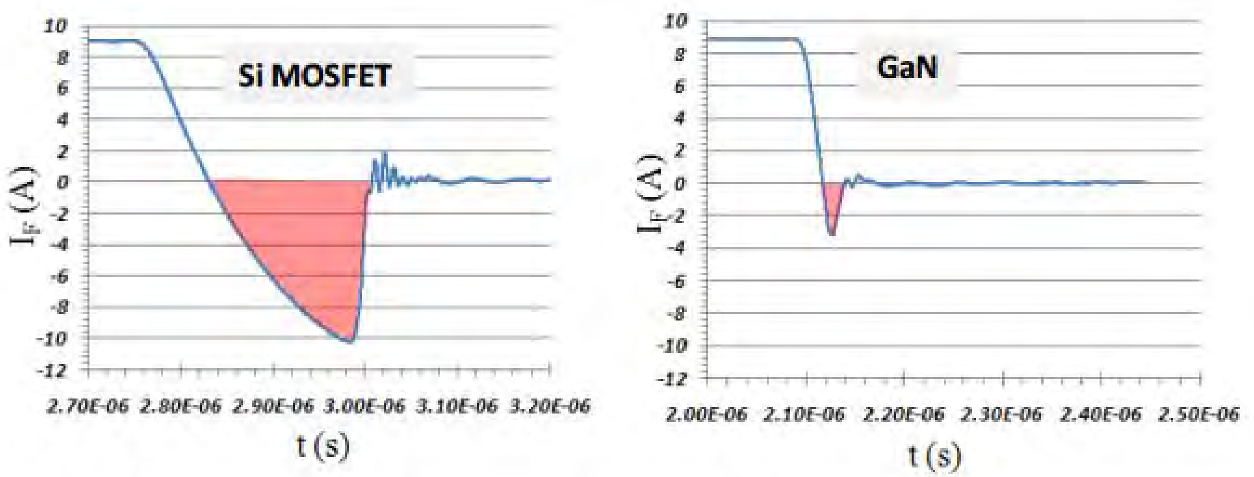
- Wide bandgap
- High 2-DEG charge density
- High electron mobility
- High breakdown voltage
- Excellent thermal conductivity
- High power density per mm of gate periphery

- GaN HEMTs are able to operate in high frequency, high power as well as high temperature device applications



High Power Switching applications

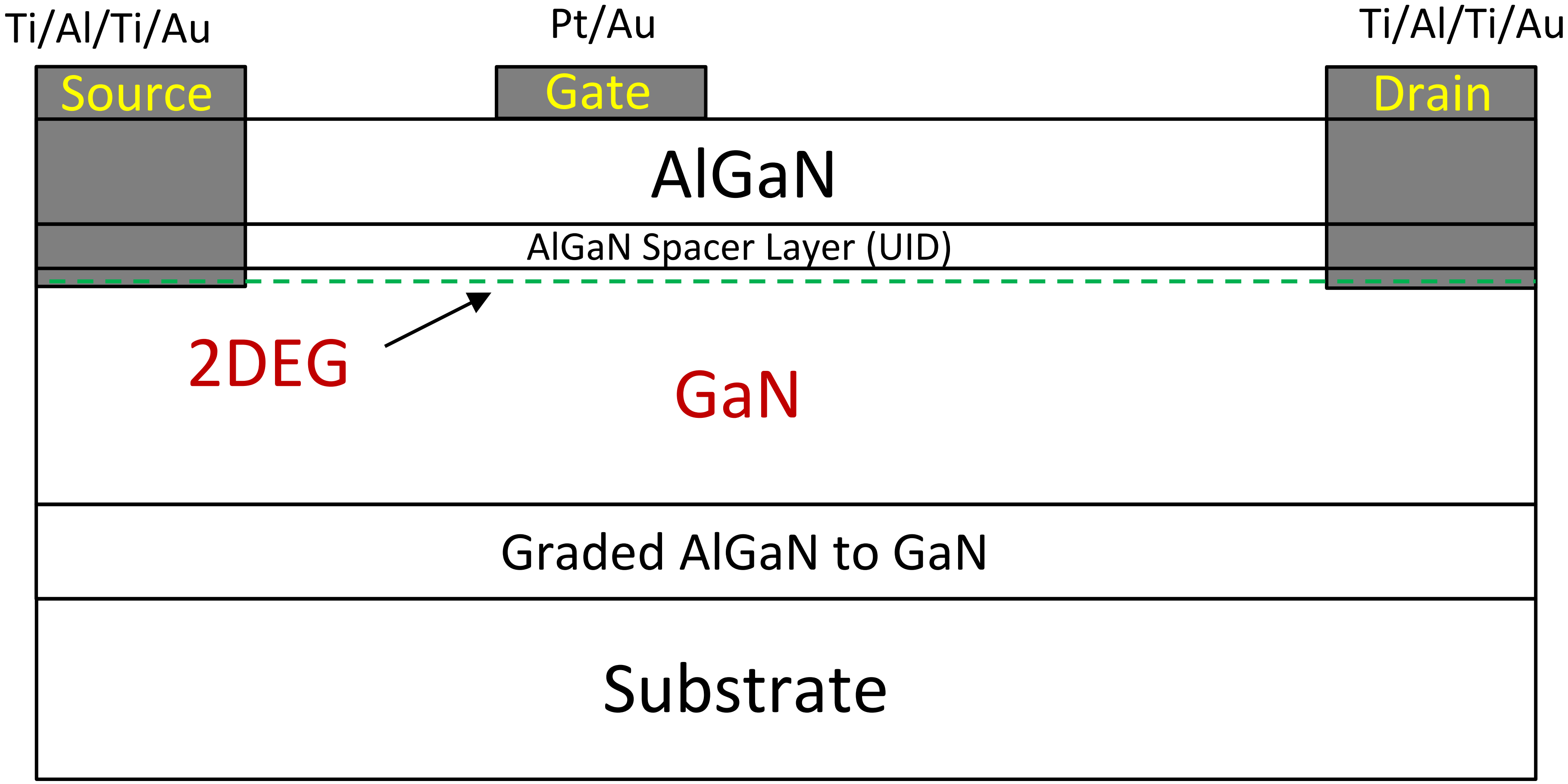




- Small terminal capacitances
- Less reverse recovery charge
- Power loss is low

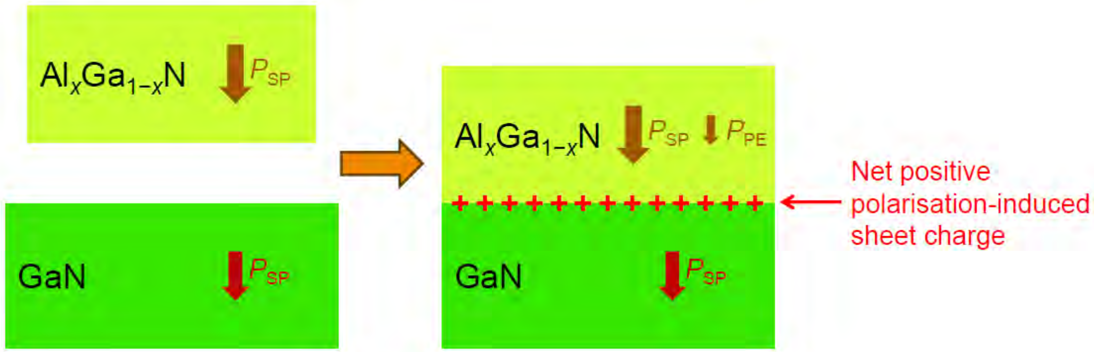
[X. Huang, *et al.*, IEEE TPEL, **29** **(5)**, 2453 (2014)]

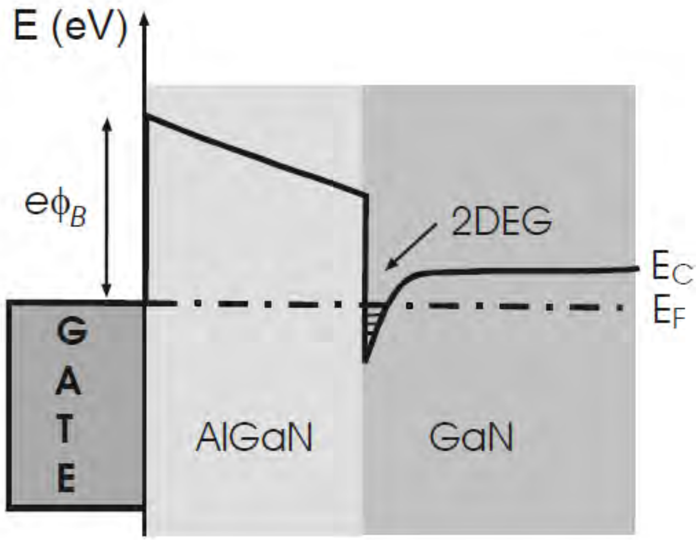
GaN HEMT Structure



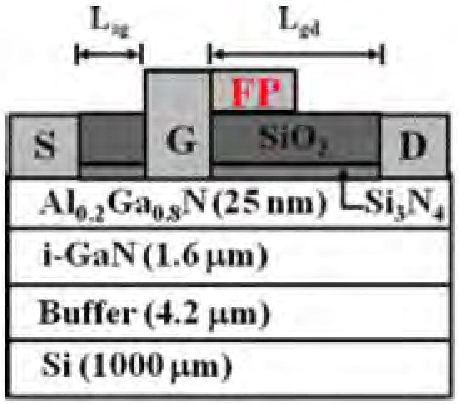
AlGaN/GaN Hetero-structure

- The AlGaN/GaN hetero-structure is used to take advantage of the two dimensional electron gas (2-DEG)
- AlGaN/GaN materials create piezoelectric and spontaneous polarization effects using an un-doped hetero-interface

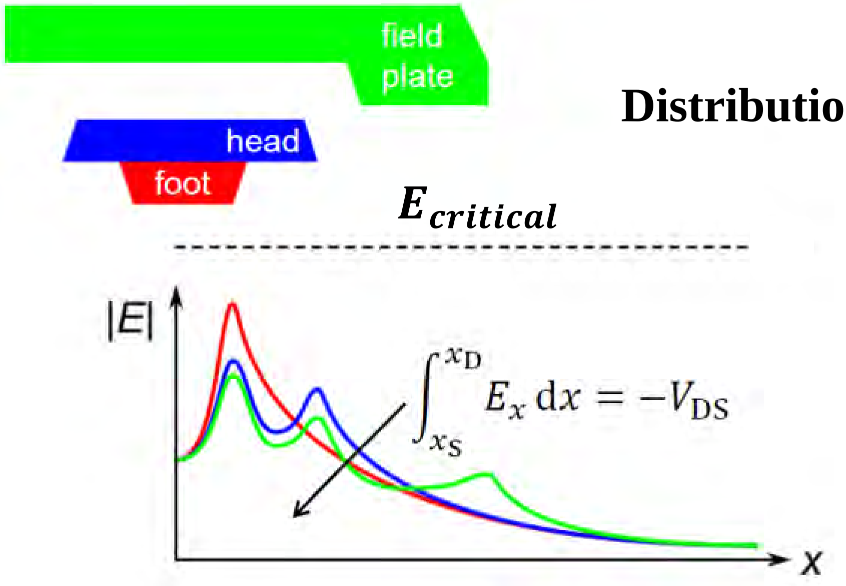




Field Plates

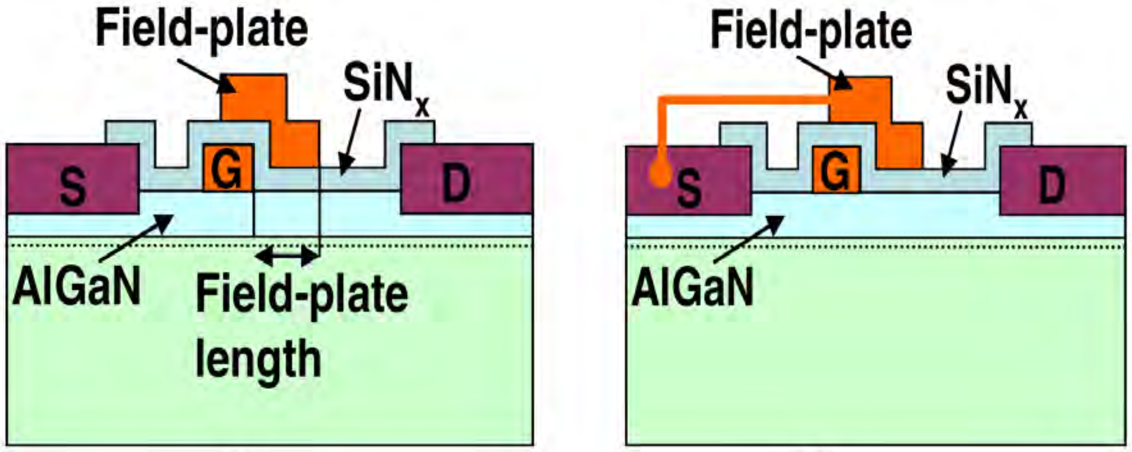


Field Plated Structure



Distribution of E

C_{gd} and C_{ds}

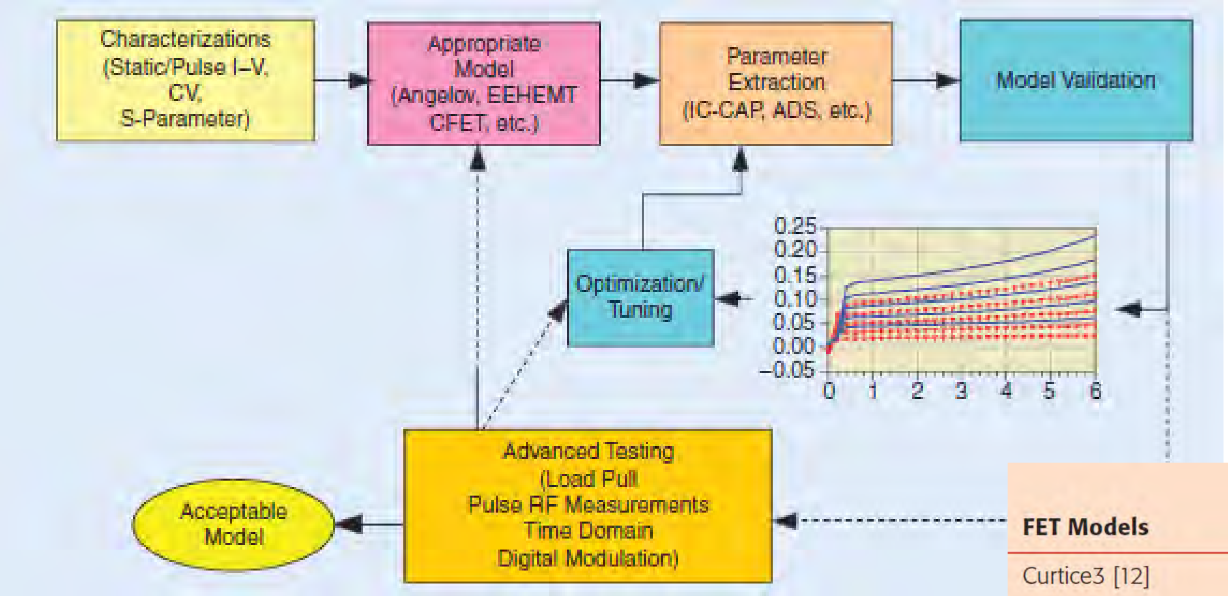


(a) (b)

[H Huang, *et al.*, IEEE TPEL, **29 (5)**, 2164 (2014)]

[W. Saito *et al.*, IEEE TED, **50 (12)**, 2528 (2003)]

Modeling GaN!



Characterizations (Static/Pulse I–V, CV, S-Parameter)

Appropriate Model (Angelov, EEHEMT CFET, etc.)

Parameter Extraction (IC-CAP, ADS, etc.)

Model Validation

Optimization/ Tuning

Advanced Testing (Load Pull Pulse RF Measurements Time Domain Digital Modulation)

Acceptable Model

Modeling Strategy

Existing Models

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

Modeling Continued…

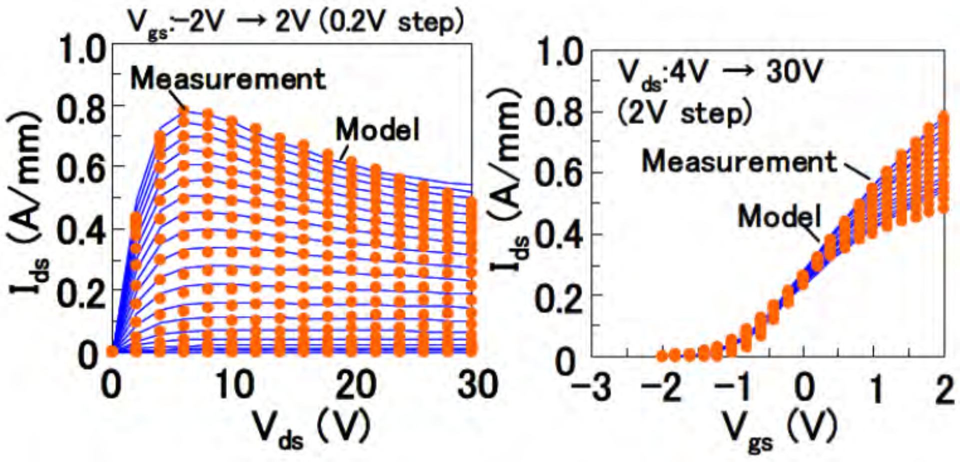
Angelov model

$$g_m = g_{mpk}\left(1 - tanh^2[p_{1m}(V_{gs} - V_k)]\right)$$

$$I_{ds} = I_{pks}\,(1 + tanh(\psi_p))\,tanh(\alpha V_{ds})\,(1 + \lambda V_{ds})$$

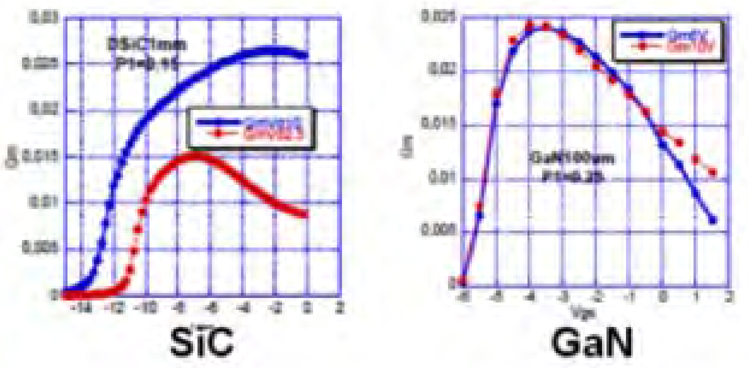
$$\psi_p = P_{1m}(V_{gs} - V_{pk0}) + P_2(V_{gs} - V_{pks})^2 + P_3(V_{gs} - V_{pksm})^3$$

$$C_{gs} = C_{gsp} + C_{gso}\,(1 + tanh(\psi_1))\,(1 + tanh(\psi_2))$$



Angelov Model Deficiencies

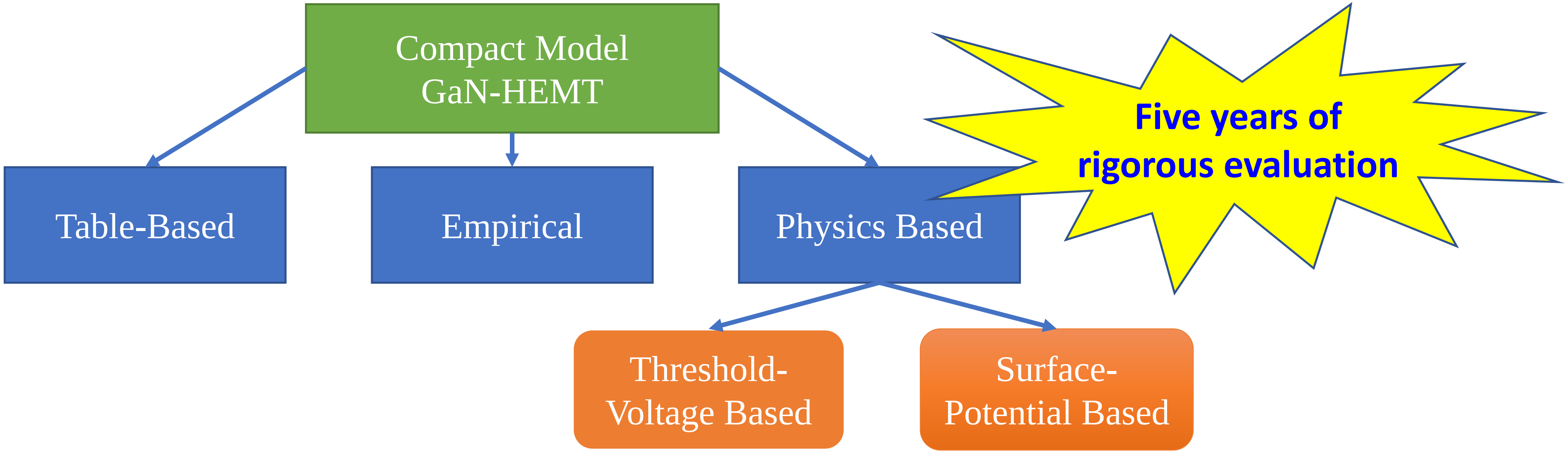
- Emperical model with ~ 90 parameters
- Fails to capture non-linear behaviour and harmonic accuracy in power circuits
- Challenging to use for multiple device dimensions



[I. Angelov *et al.*, IEEE T-MTT, **44 (10)**, 1664 (1996)]

[I. Angelov *et al.*, IEEE T-MTT, **40 (12)**, 2258 (1992)]

Status of Compact Model – GaN HEMT



Five years of rigorous evaluation

Advanced SPICE Model for GaN HEMT device

CMC candidate models for industry standardization

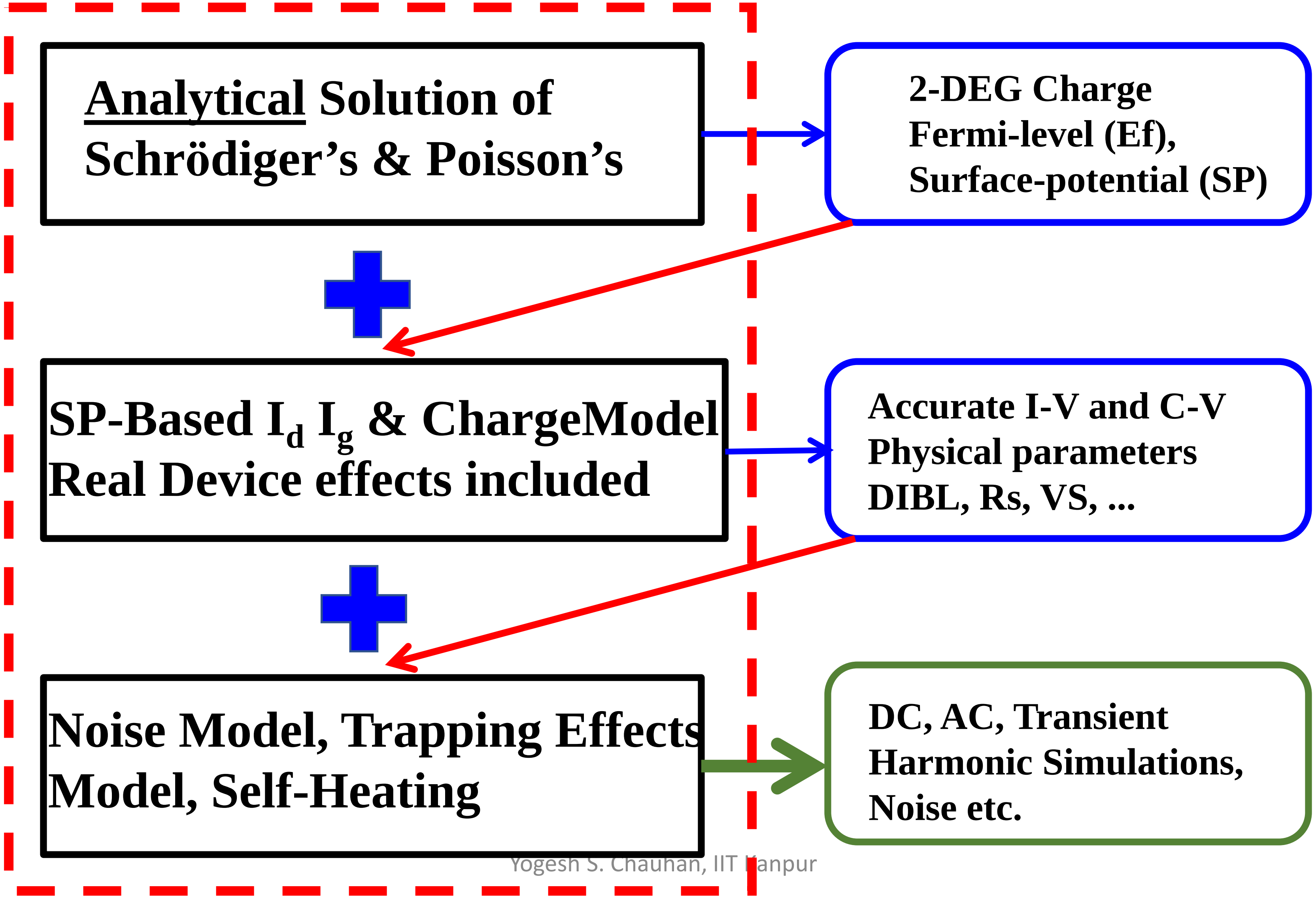
(Two models selected as industry standard)

- ASM-GaN model: Our Model (Y. S. Chauhan, IITK & S. Khandelwal, MQ)
- MIT MVSG model: MIT, Prof. D. Antoniadis

Advantages of SP-Based Model

- Better Model Scalability
- Device Insight
- Better Statistical Behavior
- Accurate Charges and Capacitances
- Better Temperature Scalability
- Less number of parameters
- Easier parameter extraction
- Uses a single expression for all regions
- Inherent Model Symmetry

ASM-HEMT Model Overview



Analytical Solution of Schrödiger's & Poisson's

2-DEG Charge
Fermi-level (Ef),
Surface-potential (SP)

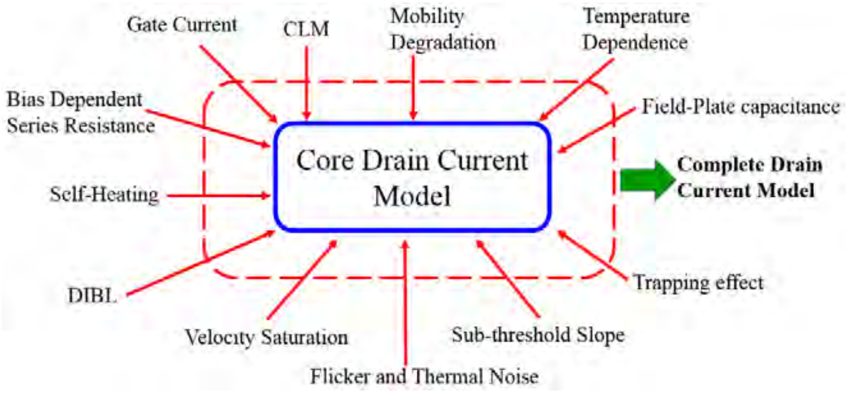
SP-Based I_d I_g & ChargeModel
Real Device effects included

Accurate I-V and C-V
Physical parameters
DIBL, Rs, VS, ...

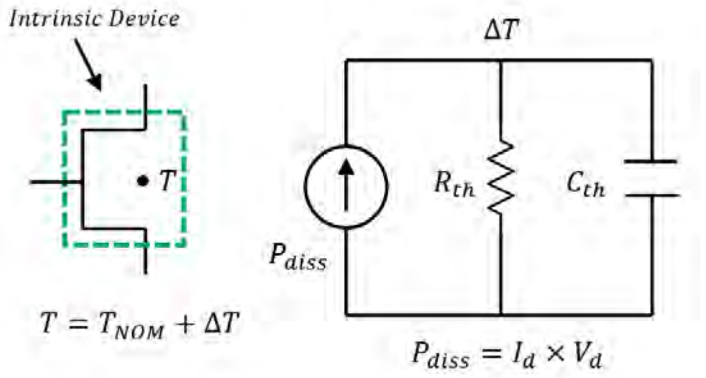
Noise Model, Trapping Effects Model, Self-Heating

DC, AC, Transient
Harmonic Simulations,
Noise etc.

Core Model & Parameters



Real Device Effects Incorporated into the Model



Self-Heating Effect

Core Model Parameters

Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	$-2.86\ V$
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	$0.325\ V^{-1}$
η_0	DIBL Parameter	0.117
U_0	Low Field Mobility	$33.29\ mm^2/Vs$
N_{S0ACCS}	AR 2DEG Density	$1.9e+17\ /m^2$
$V_{SATACCS}$	AR saturation velocity	$157.6e+3\ cm/s$
R_{TH0}	Thermal Resistance	$22\ \Omega$

Core drain current expression

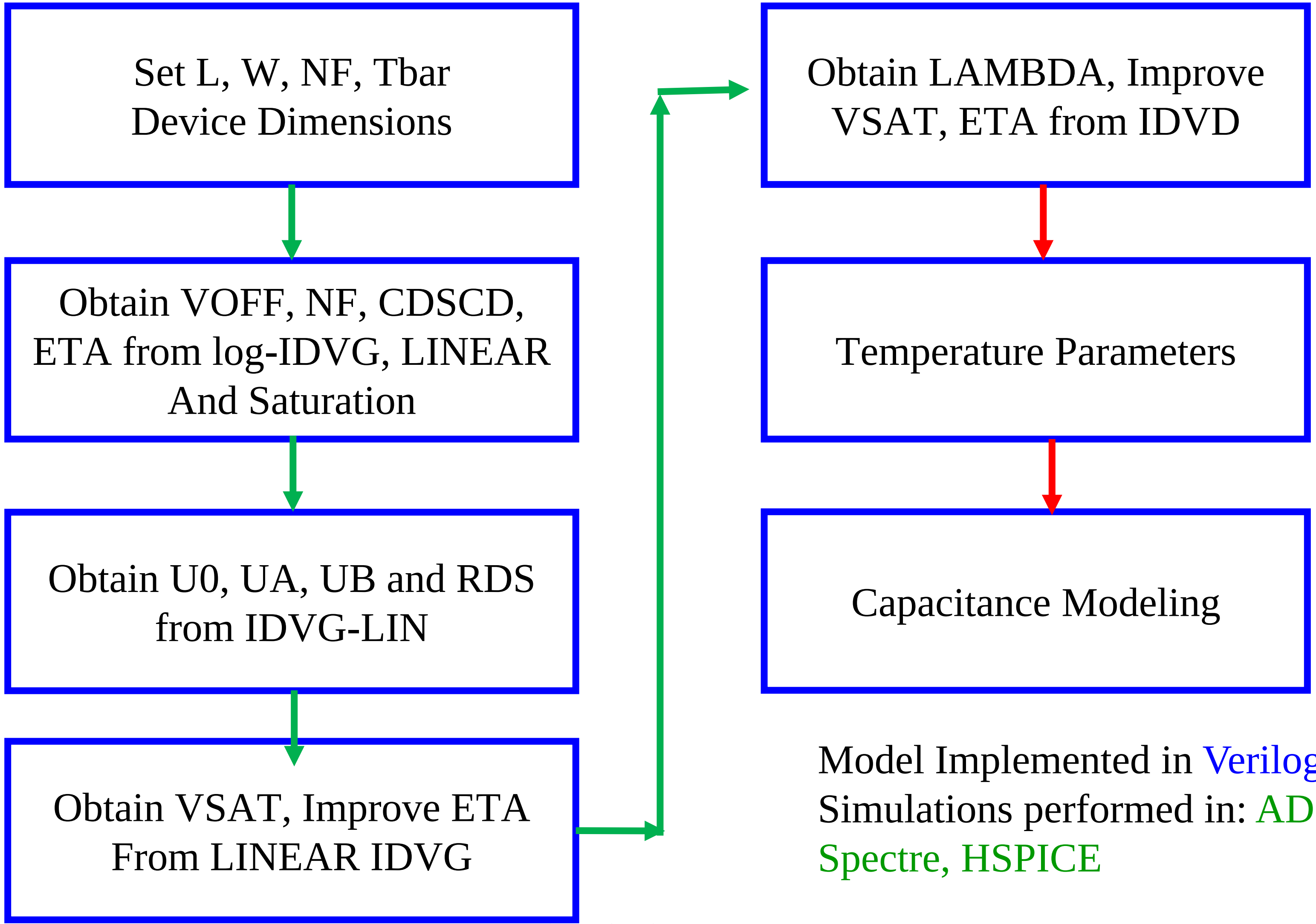
$$\mathrm{I_{ds}} = \frac{\mu_{\mathrm{eff}}}{\sqrt{1+\theta_{\mathrm{sat}}^2\psi_{\mathrm{ds}}^2}}\frac{\mathrm{W}}{\mathrm{L}}\mathrm{C_g N_f}\left[\mathrm{V_{go}} - \left(\frac{\psi_{\mathrm{s}}+\psi_{\mathrm{d}}}{2}\right) + \mathrm{V_{th}}\right] \times \psi_{\mathrm{ds}}(1+\lambda \mathrm{V_{ds}})$$

Access Resistance Model

$$\mathrm{I_{ds,acc}} = \frac{\mathrm{R_c}}{\mathrm{W{\cdot}N_f}} + \frac{\mathrm{L_{acc}}}{\mathrm{W{\cdot}N_f{\cdot}q{\cdot}N_{S0ACCS}{\cdot}U_{0ACCS}}} \times \left(1 - \left(\frac{\mathrm{I_{ds}}}{\mathrm{W{\cdot}N_f{\cdot}N_{S0ACCS}{\cdot}V_{SATACCS}}}\right)^2\right)^{-1/2}$$

Model Parameter Extraction

Parameter Extraction in ICCAP Software



Set L, W, NF, Tbar
Device Dimensions

Obtain VOFF, NF, CDSCD,
ETA from log-IDVG, LINEAR
And Saturation

Obtain U0, UA, UB and RDS
from IDVG-LIN

Obtain VSAT, Improve ETA
From LINEAR IDVG

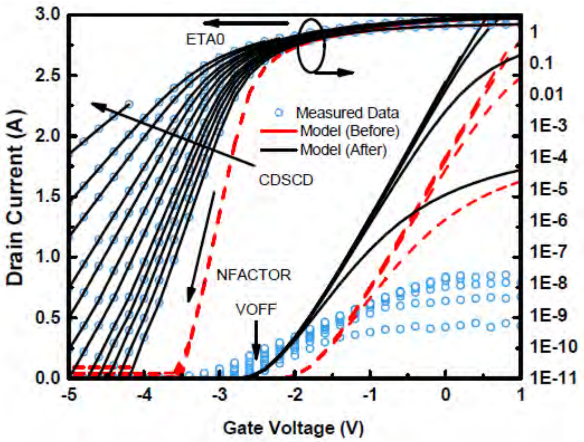
Obtain LAMBDA, Improve
VSAT, ETA from IDVD

Temperature Parameters

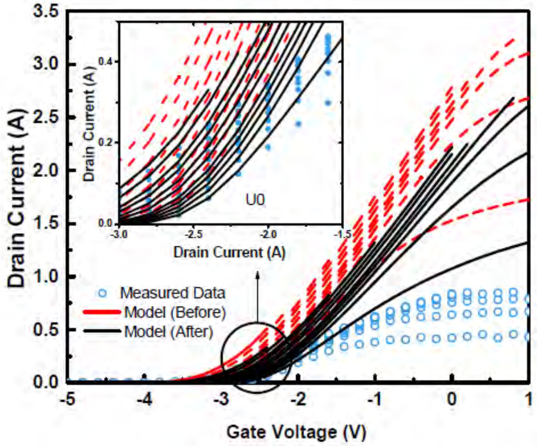
Capacitance Modeling

Model Implemented in Verilog-A
Simulations performed in: ADS,
Spectre, HSPICE

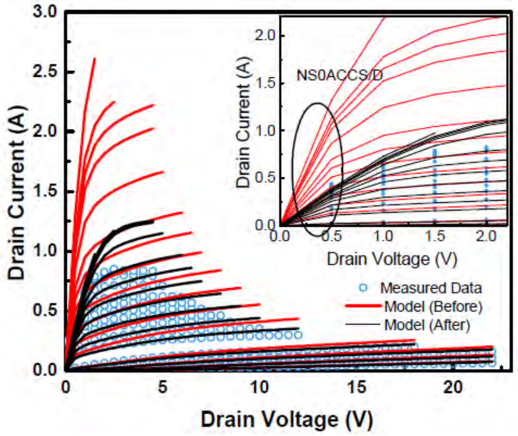
DC-Parameter Extraction



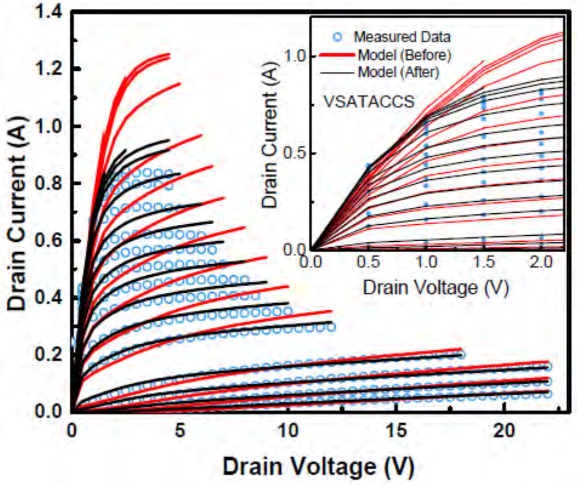
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



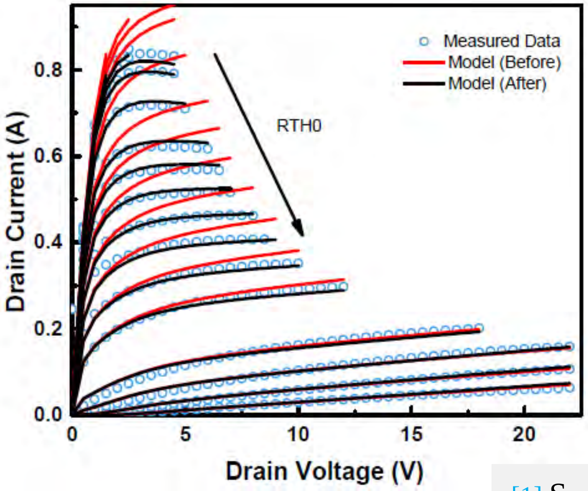
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



$I_d - V_d$ (Extract $V_{SATACCS}$)

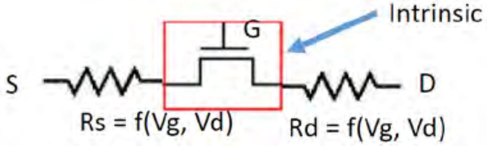


$I_d - V_d$ (Extract R_{TH0})

[1] S. A. Ahsan *et al.*, *MOS-AK Workshop*, Shanghai, [2016]

Nonlinear source/drain access region resistance model

$$R_J = \frac{L_J}{q \mu_n n_{s0}} \qquad J = S, D$$



$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R / V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

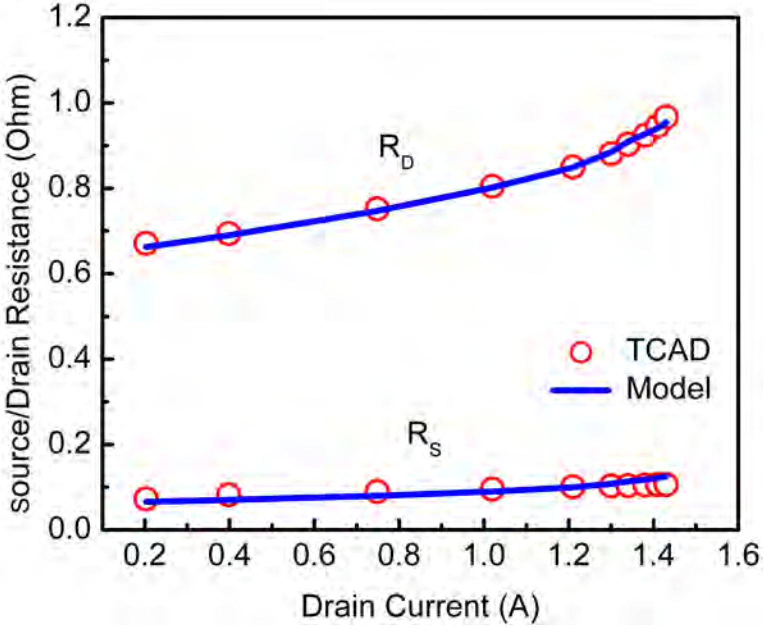
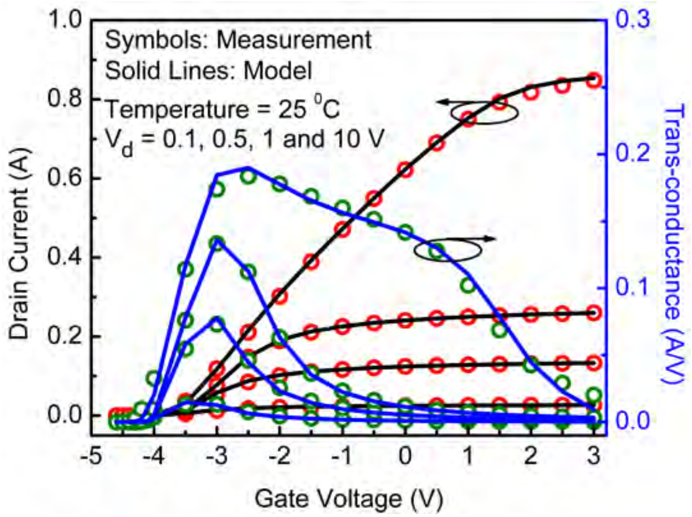
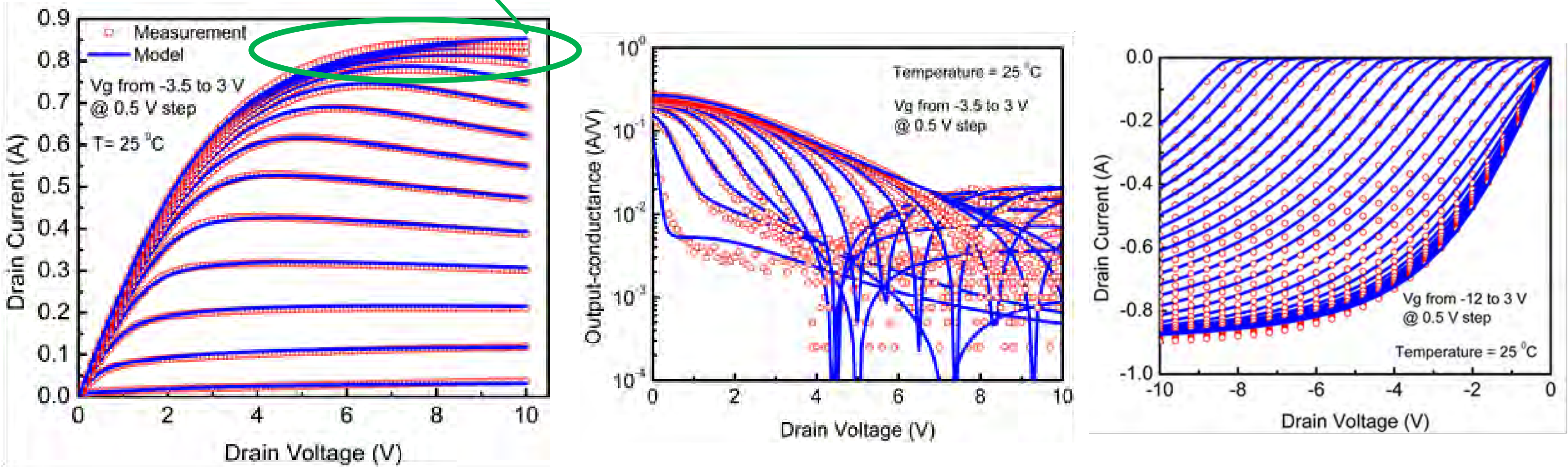


Fig.: Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

$R_{d/s}$ Model Validation with Measurement



Different slopes in g_m-V_g: self-heating governs the first slope while velocity saturation in access region affects second slope.



Effect of high access region resistance at high V_g

Fig.: (a) Ids-Vds, (b) g_{ds} and (c) reverse Ids-Vds fitting with experimental data. The non-linear $R_{s/d}$ model shows correct behavior for the higher Vg curves in the Id - Vd plot.

Modeling of Temperature dependence

$R_{d/s}$ increases significantly with increase in temperature.

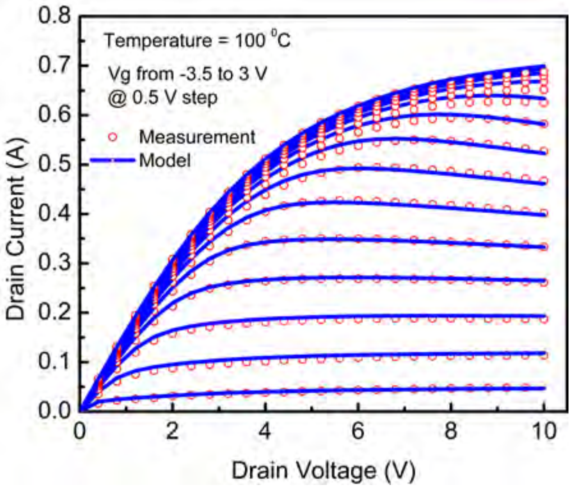
2-DEG charge density in the drain or source side access region:

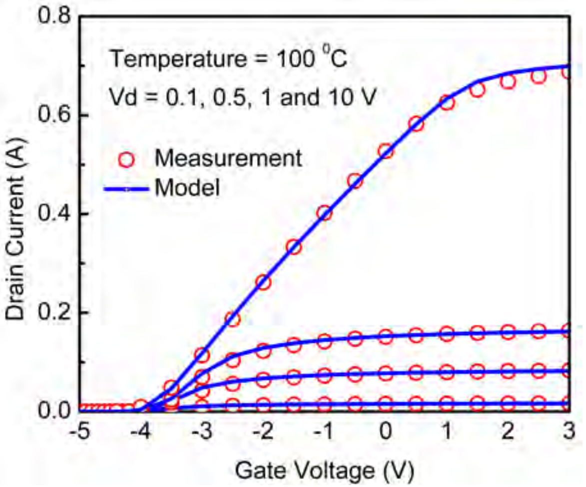
$$n_{s0}(T) = NS0ACC\cdot\left(1 - KNS0\cdot\left(\frac{T}{TNOM}-1\right)\right)$$

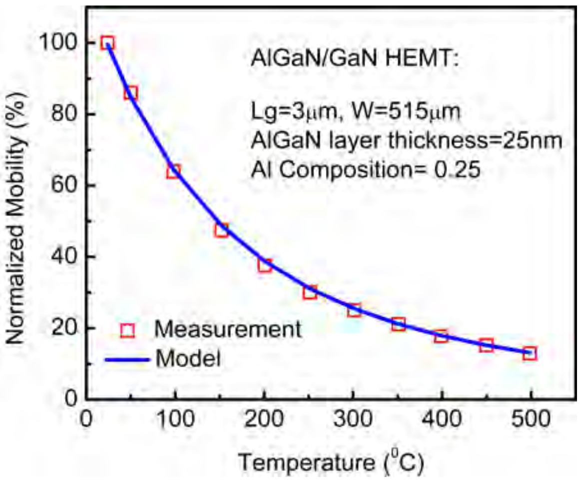
Saturation Velocity:

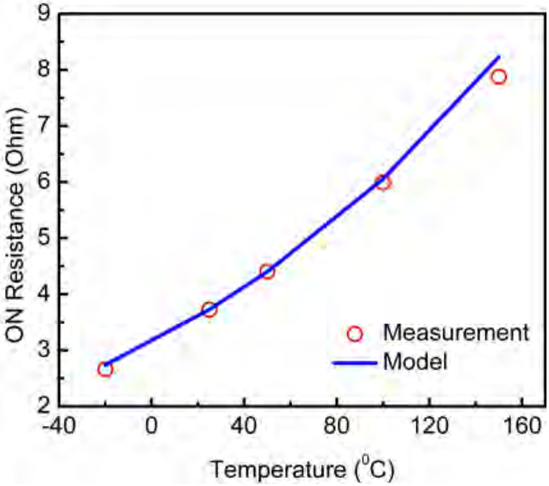
$$V_{sat}(T) = VSATACCS\cdot[1+ATS(T-TNOM)]$$

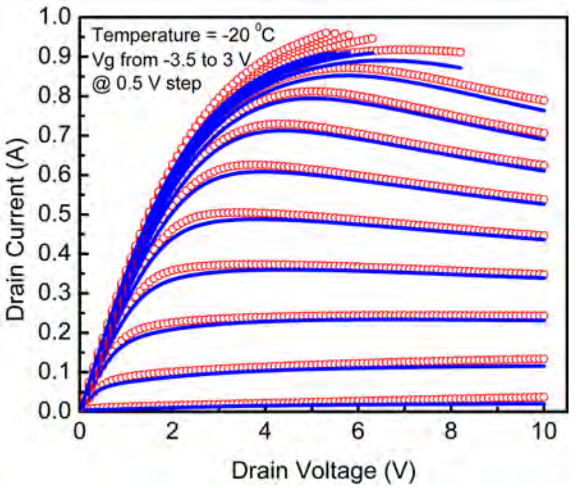
Electron Mobility: $\mu_{acc}(T) = U0ACC\cdot\left(\frac{T}{TNOM}\right)^{UTEACC}$

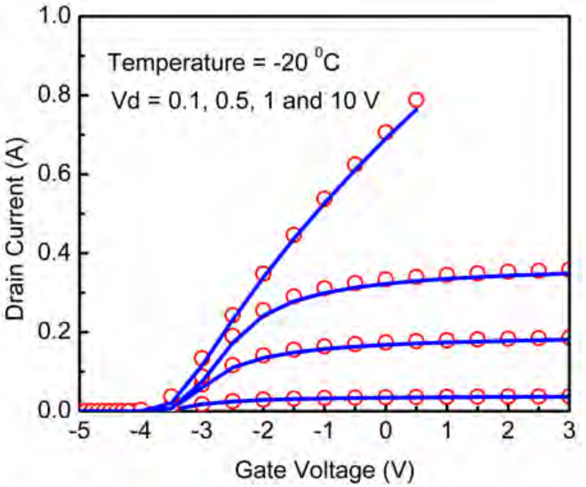




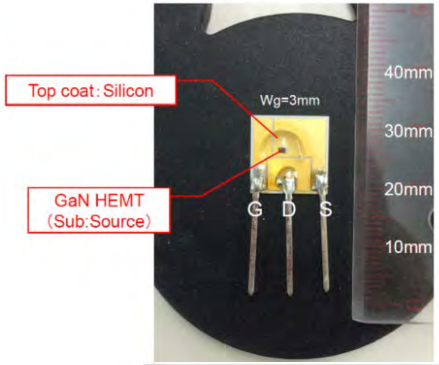


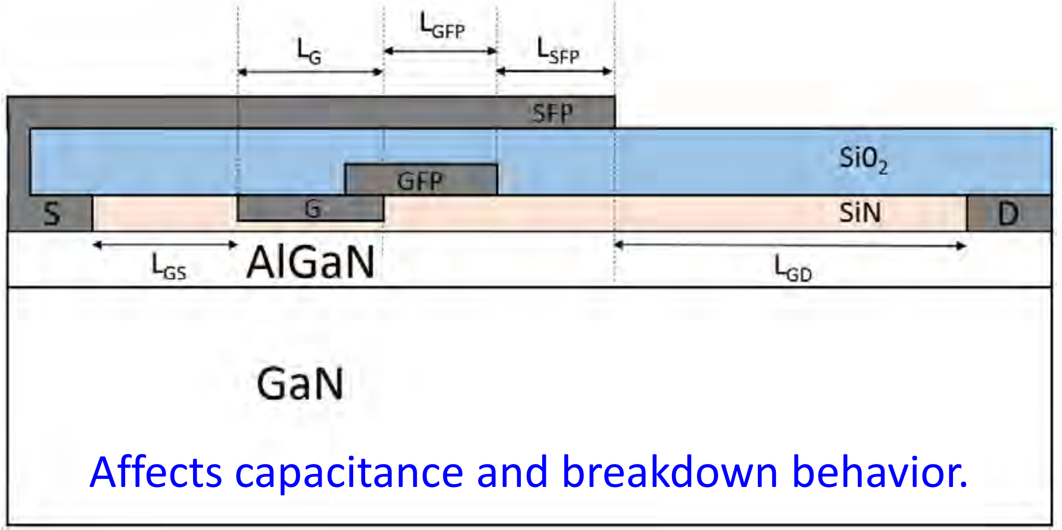




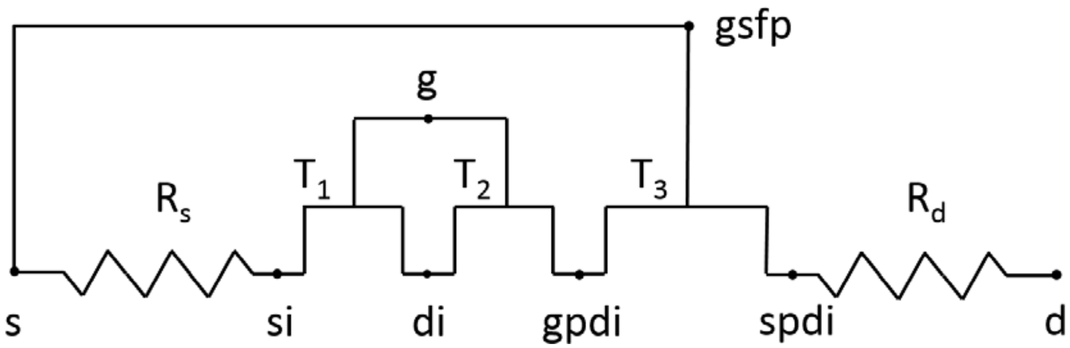


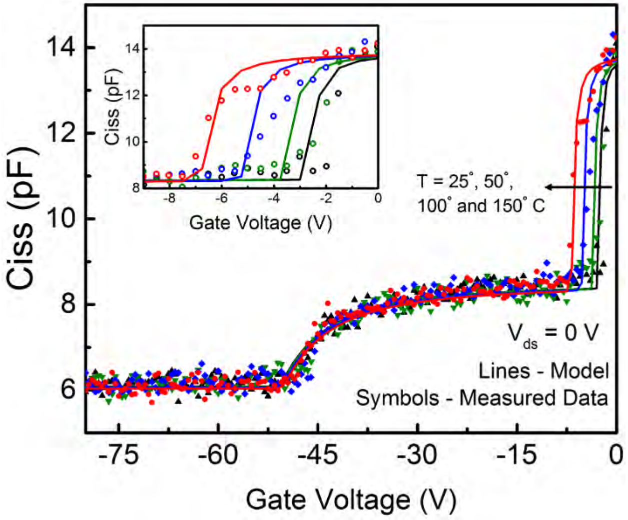
Modeling of Field-Plates in HEMTs

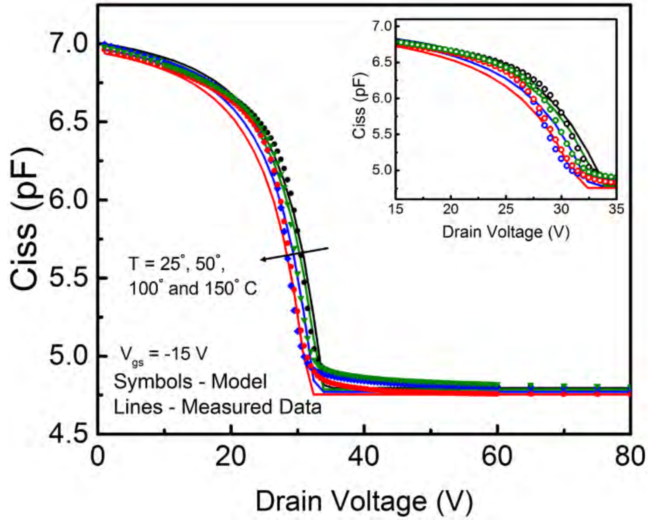


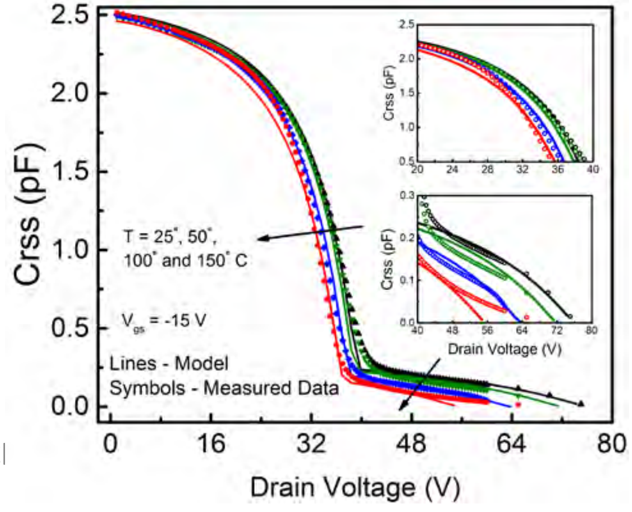


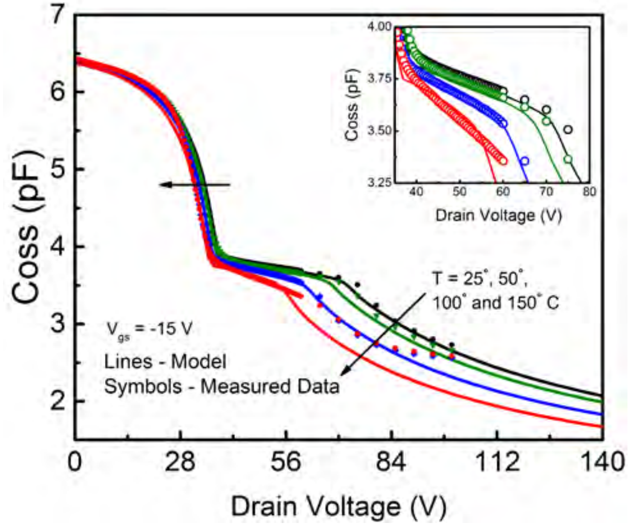
Affects capacitance and breakdown behavior.





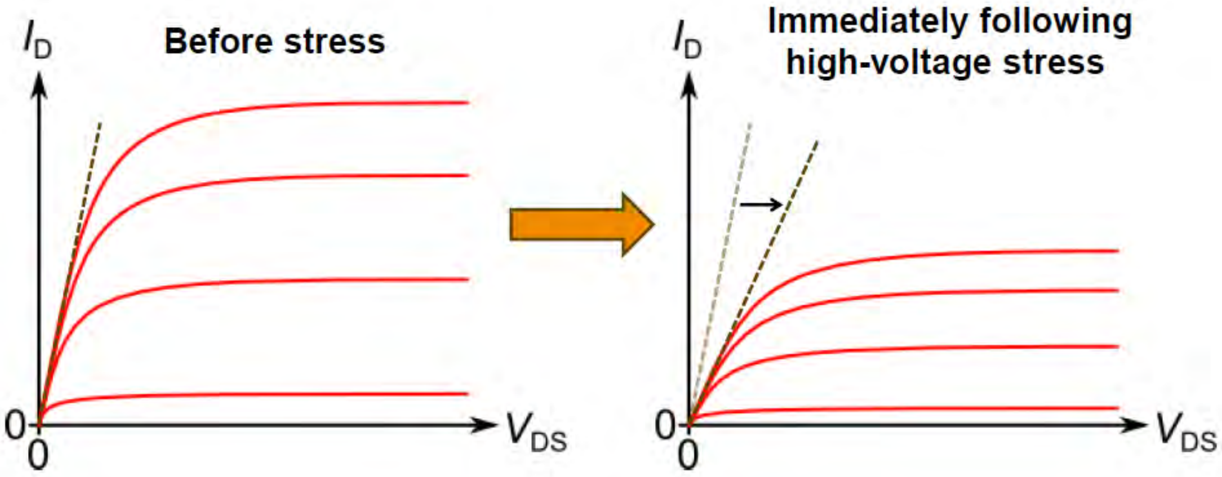




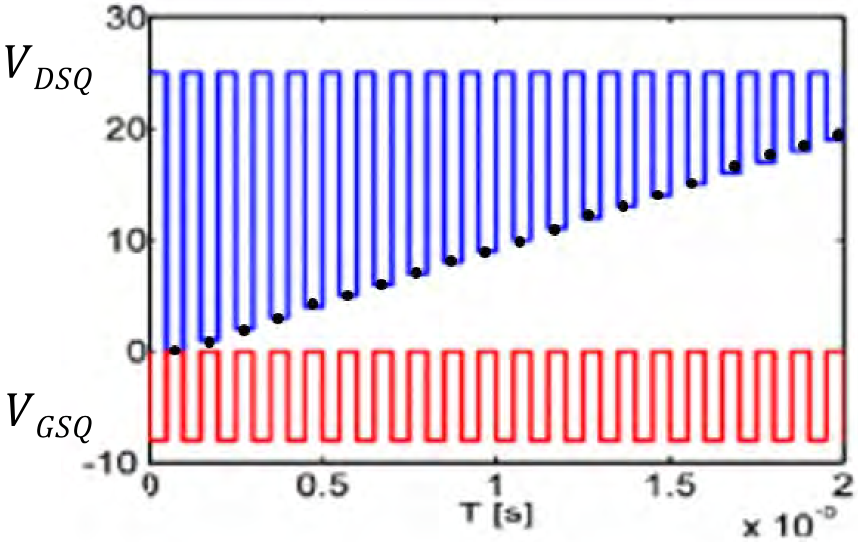


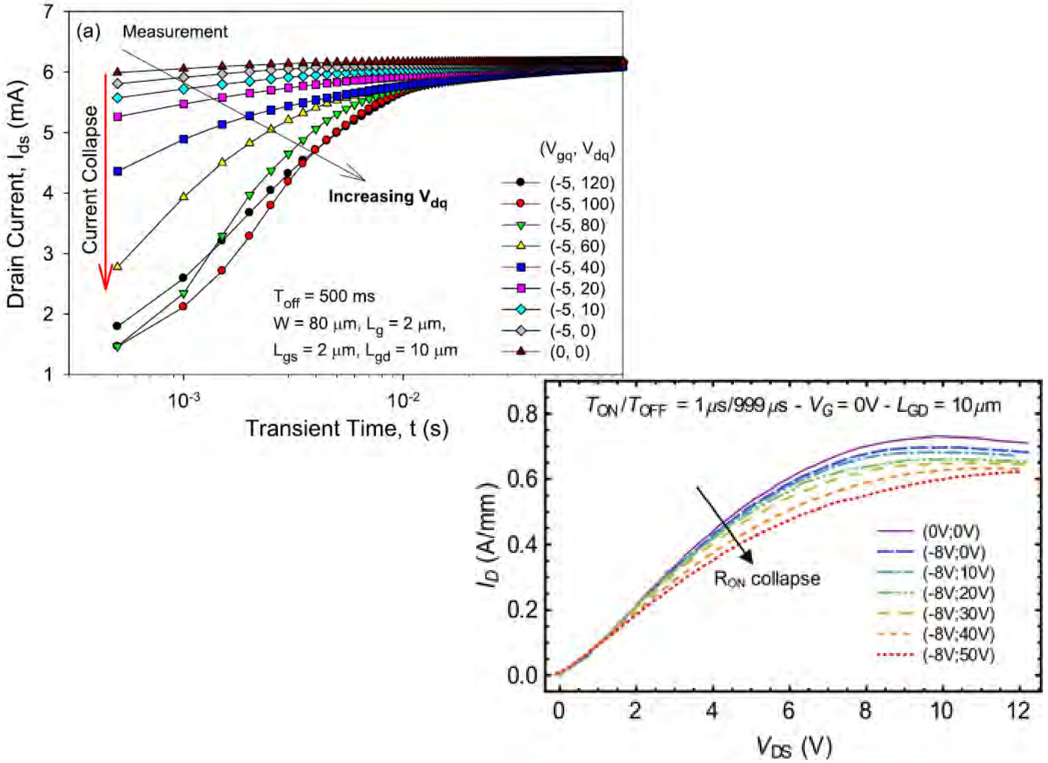
Current Collapse

- On-state current temporarily reduced following off-state stress



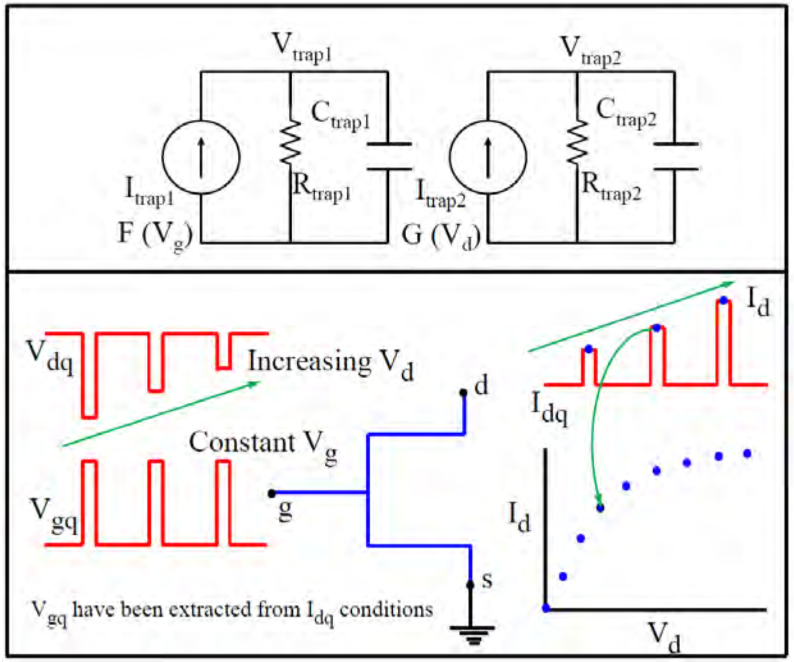
- Also known as **dynamic R_{on}**
  - On-state resistance depends on recent history of device biasing





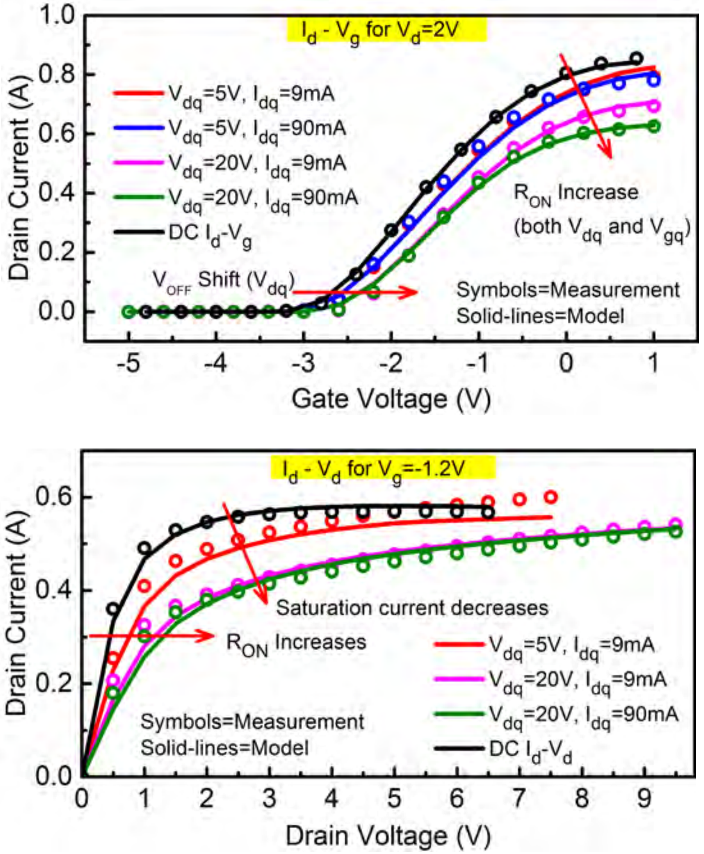
Source: Stephen Sque - ESSDERC tutorial Sept. 2013

Trap Model



Pulsed-IV Scheme used to simulate the P-IV Characteristics in IC-CAP

$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$
$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$
$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$
$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$



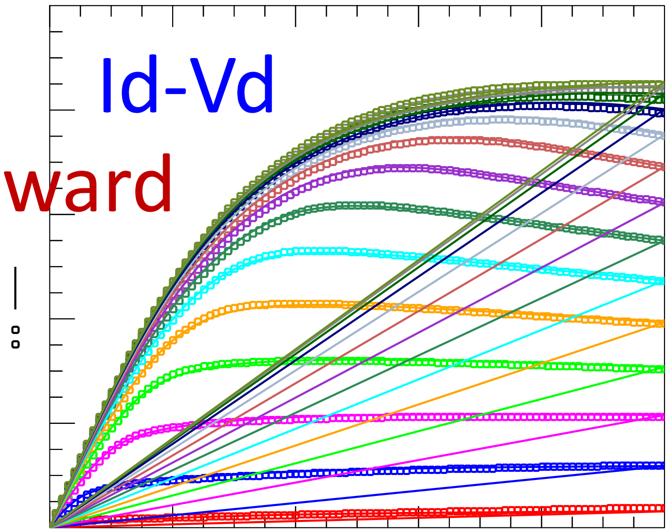
Pulsed – IV chacteristics for multiple quiescent conditions

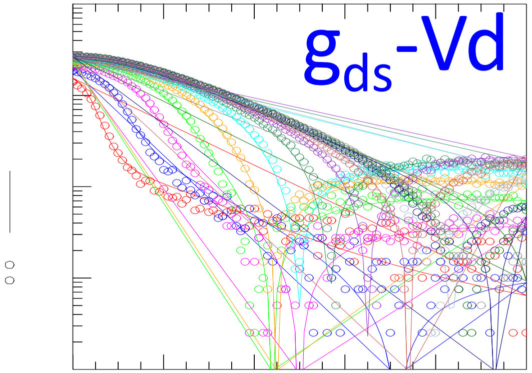
Pulse Width – 200 ns,
Duty-cycle 0.02 %

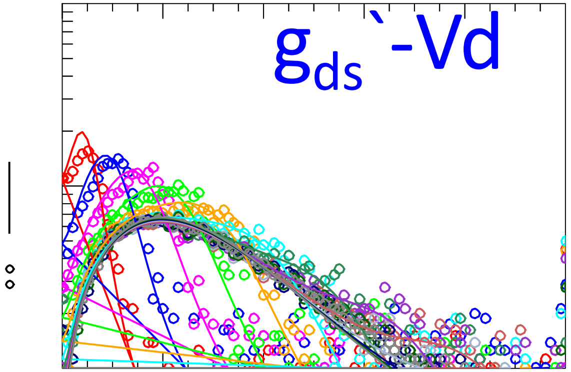
DC I-V Results from Toshiba Power GaN Transistor

Room Temperature Id-Vd Plots

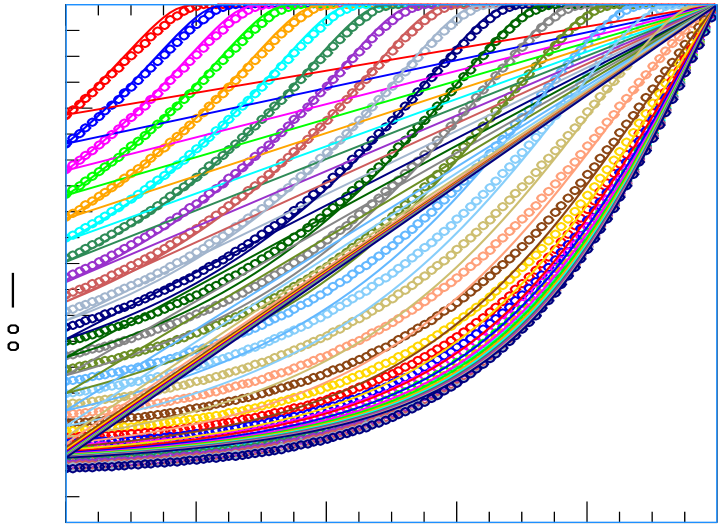
Forward

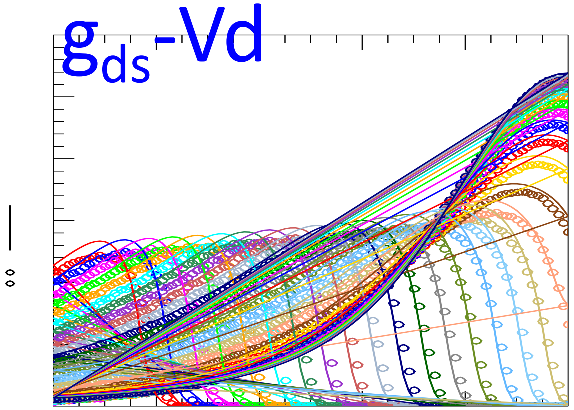


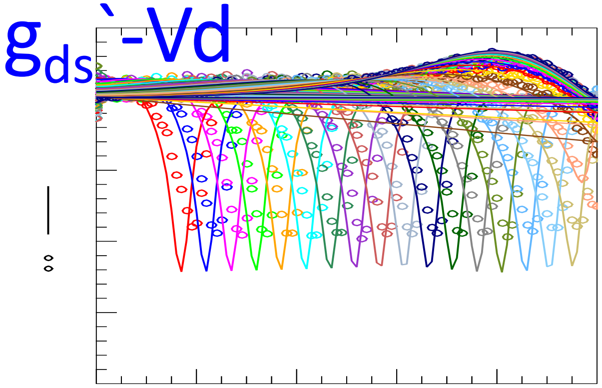




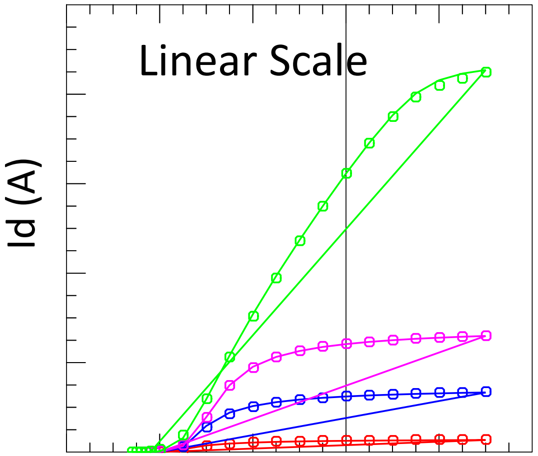
Reverse

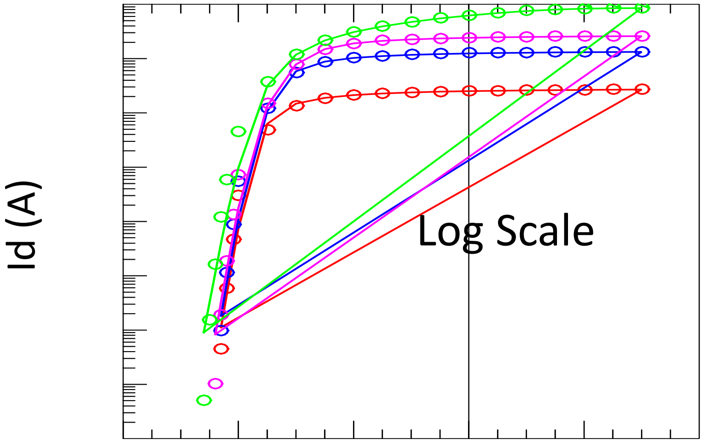


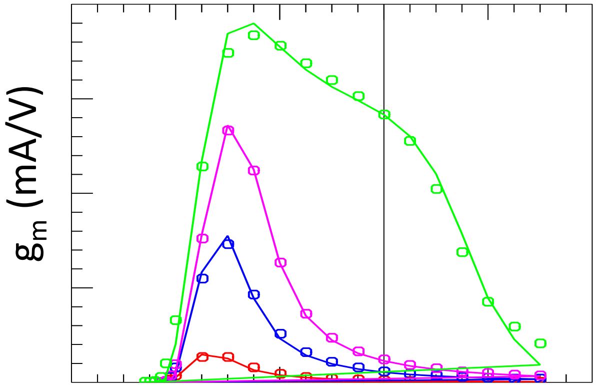


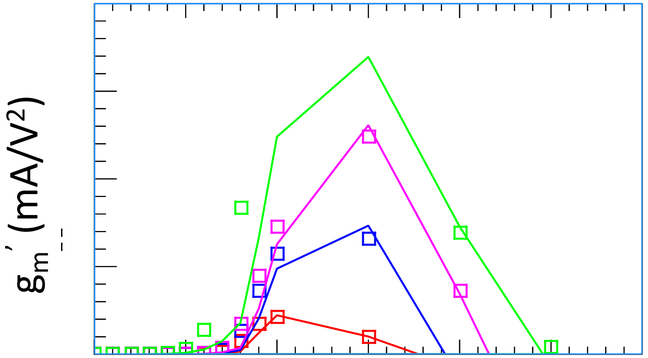


Room Temperature Id-Vg Plots

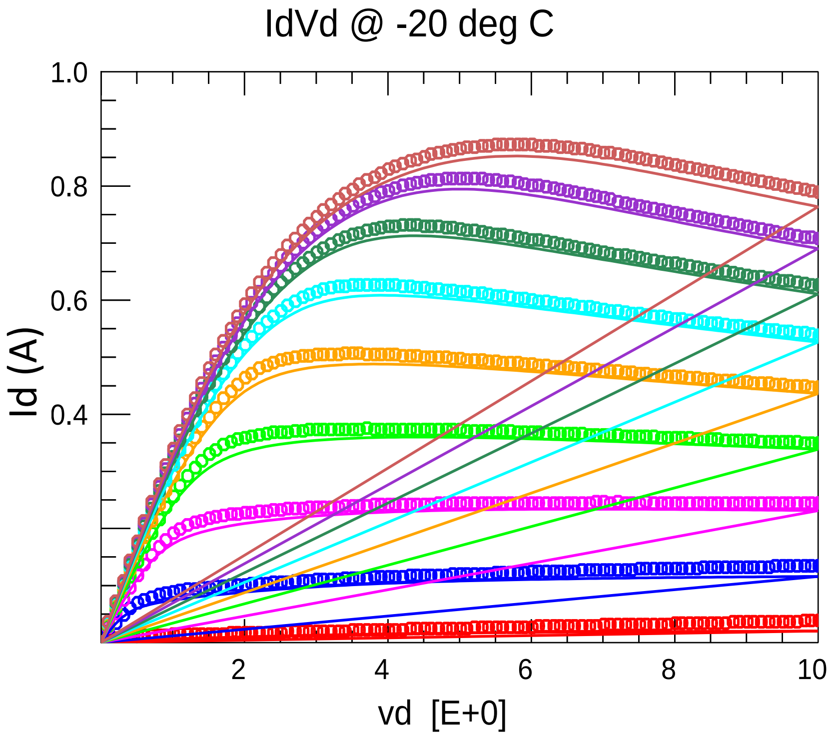




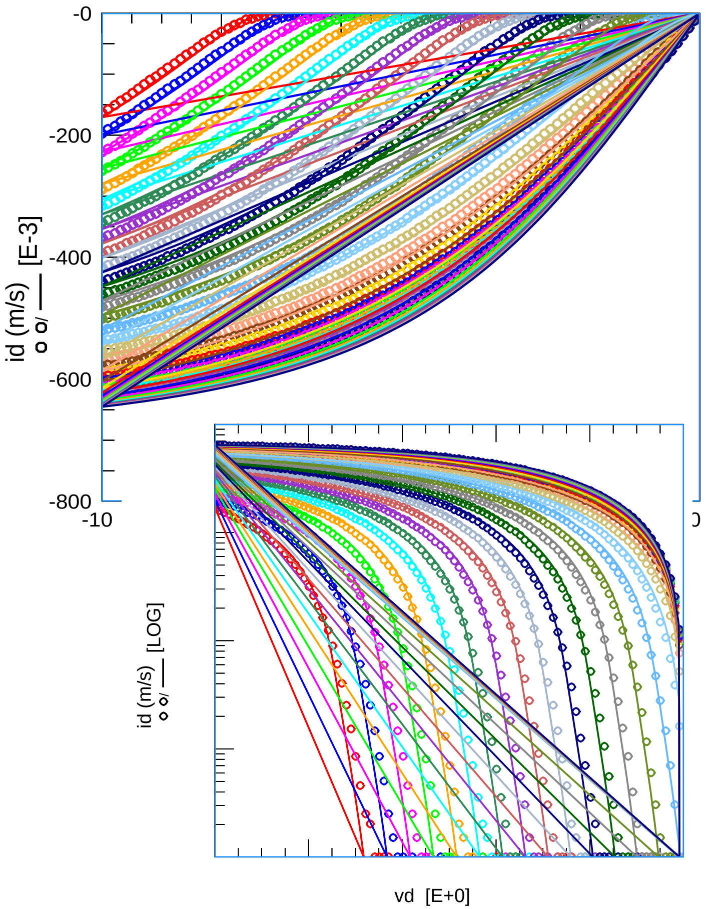




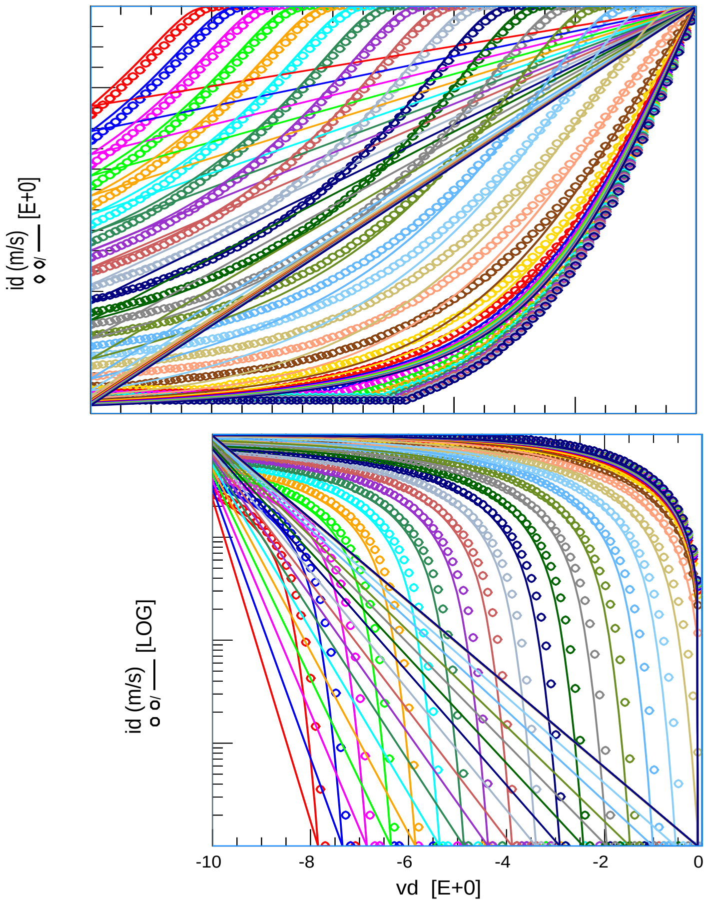
Other temperatures



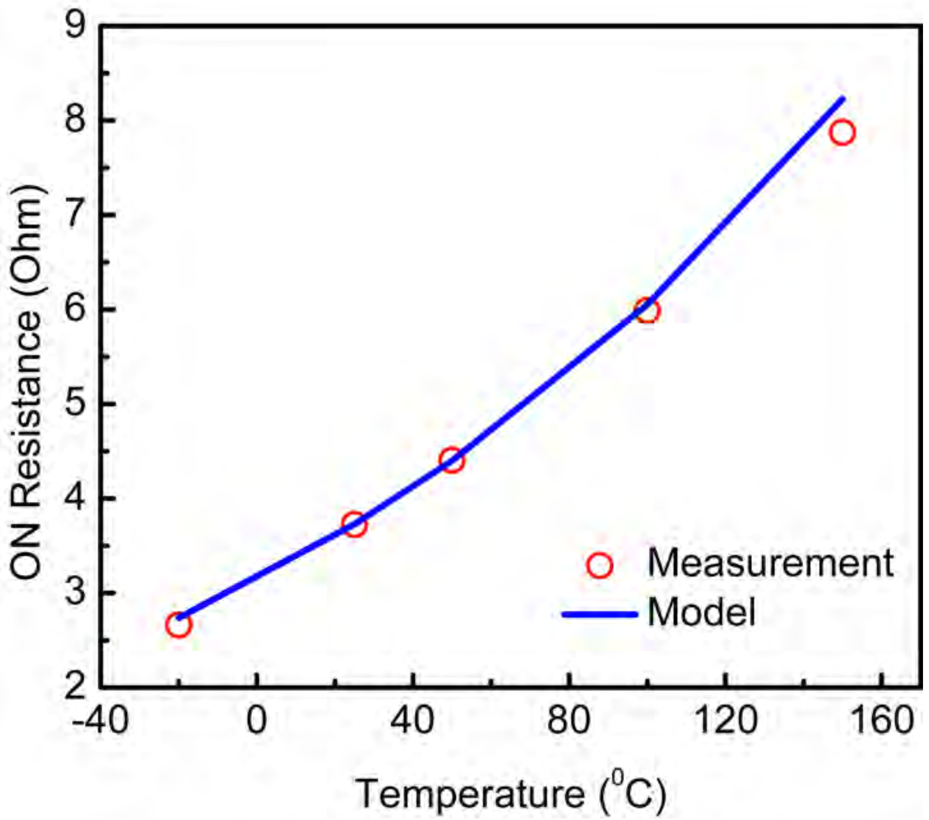
Rev IdVd @ T=150 C

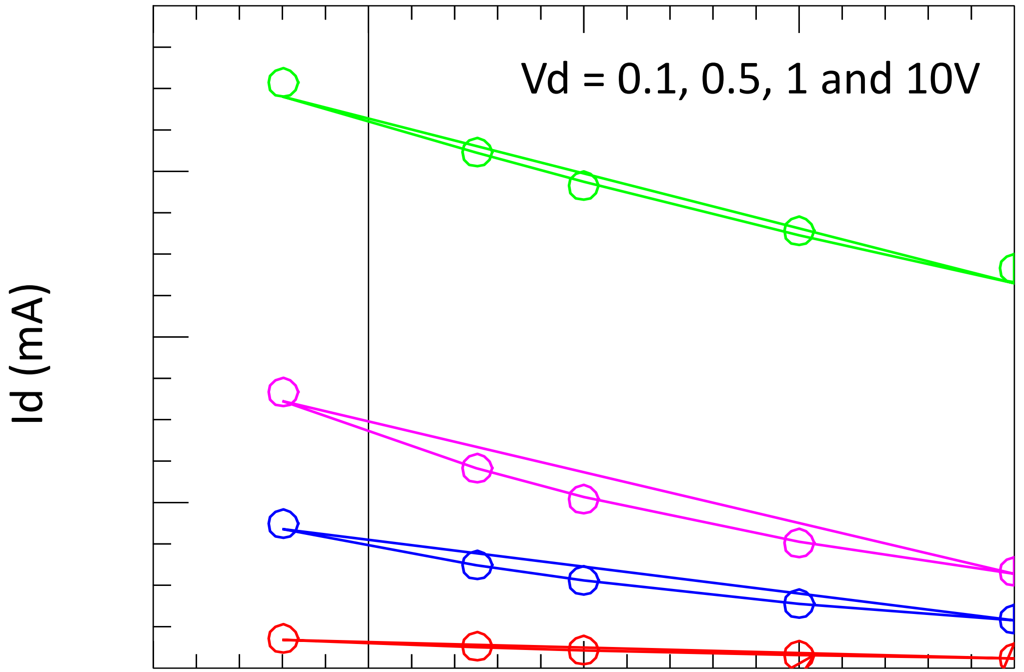


Rev IdVd @ T=-20 C



Temperature Scaling

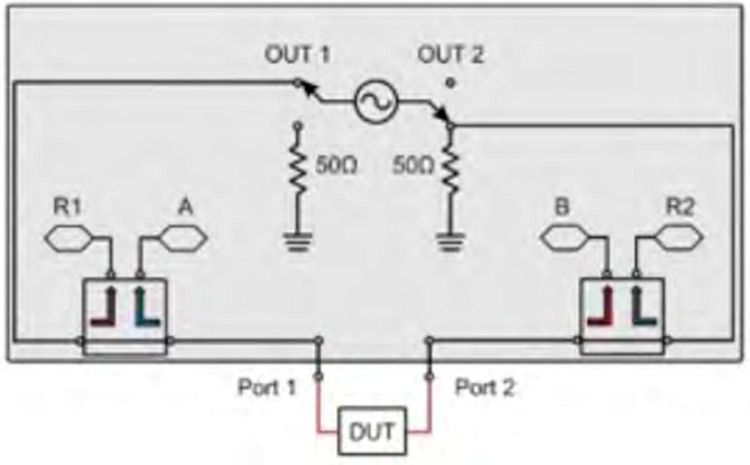




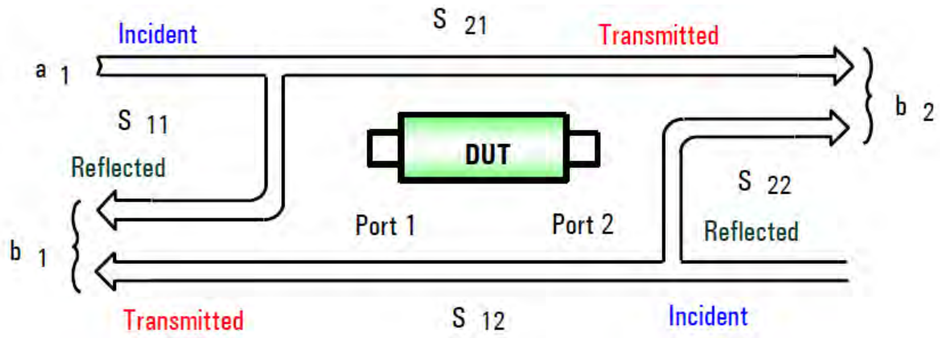
RF Measurements

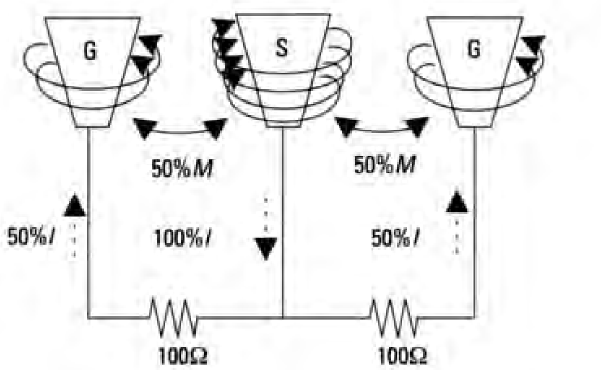
S-Parameters

- Easy for high frequencies (hard to do open/short for Z/Y)
- Calculate other quantities
- Cascadable
- Transformation
- Compatibility with simulation tools



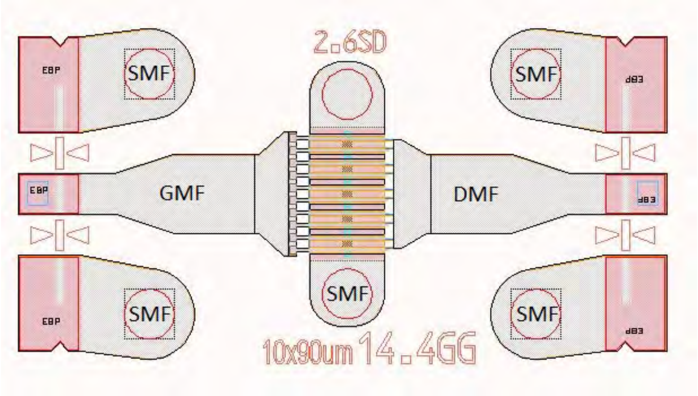
VNA Architecture



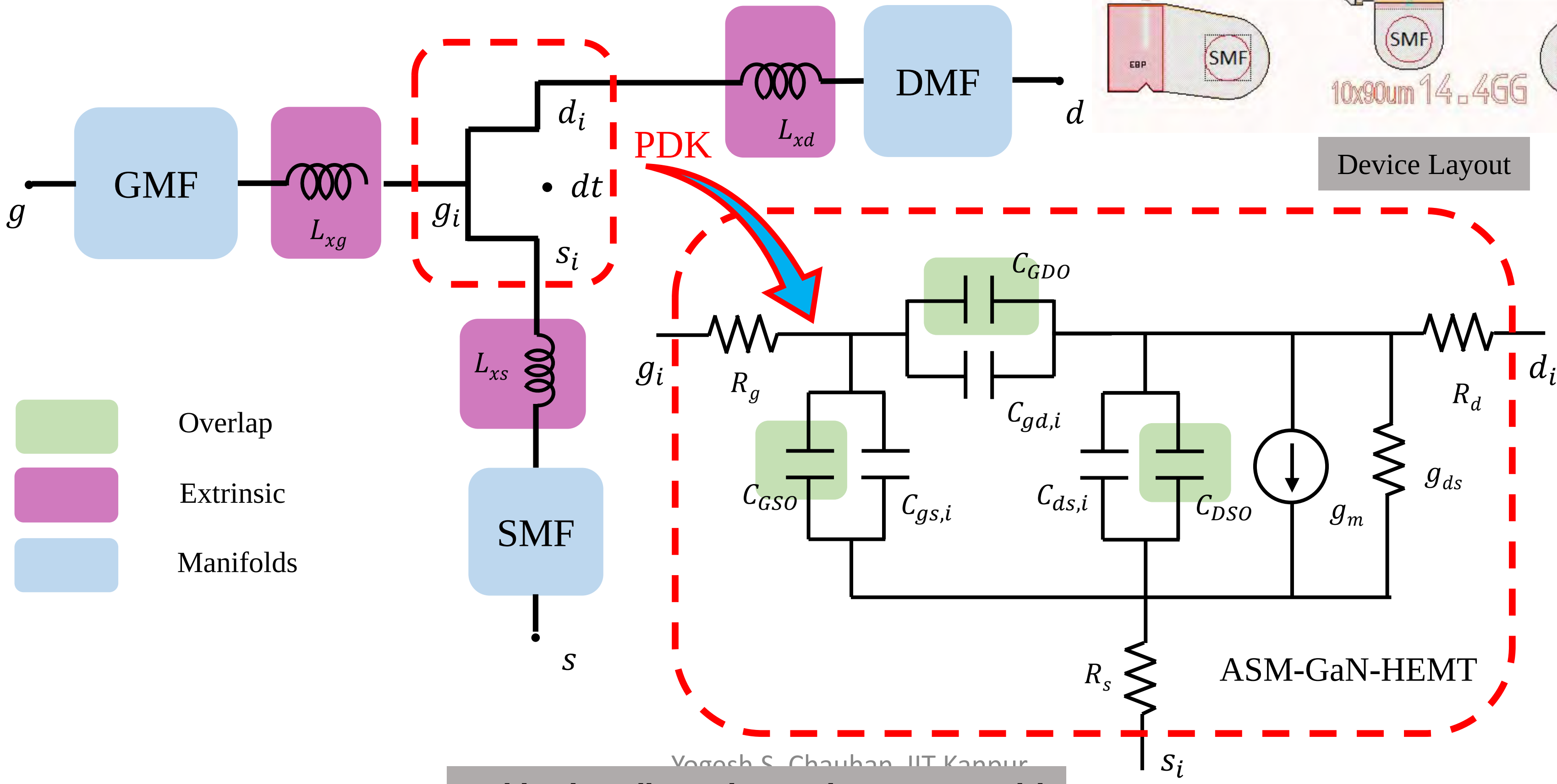


RF Model & Extraction (i)

- Model
    - Core surface potential based PDK
    - Access region resistances included in core
    - Bus-inductances in extrinsics

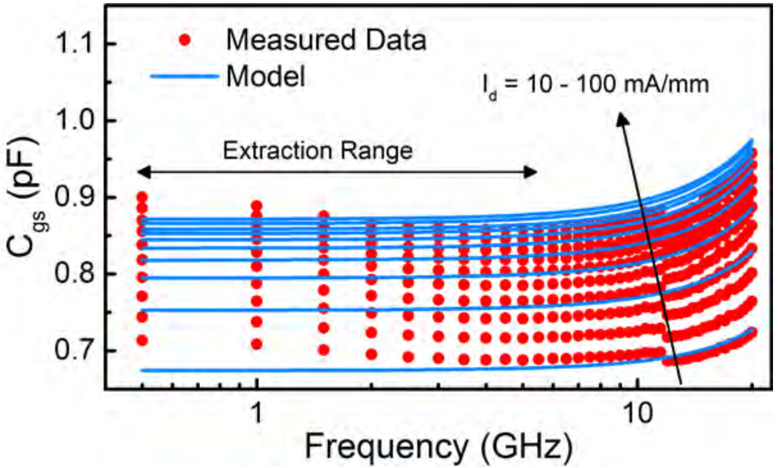


Device Layout

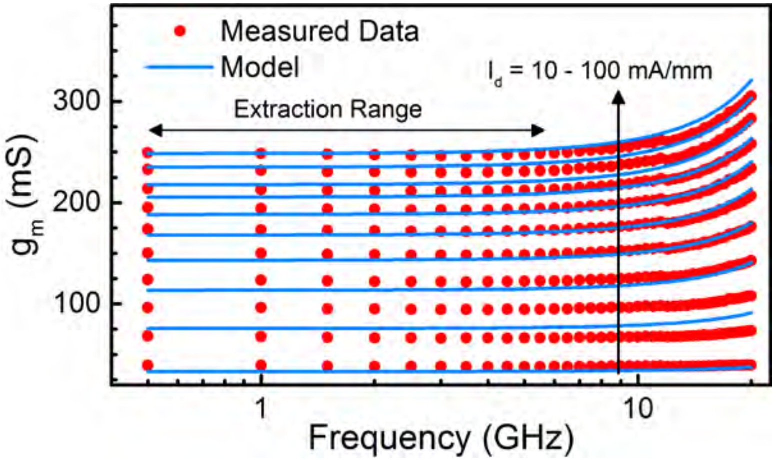


Pad-level Small Signal Equivalent Circuit Model

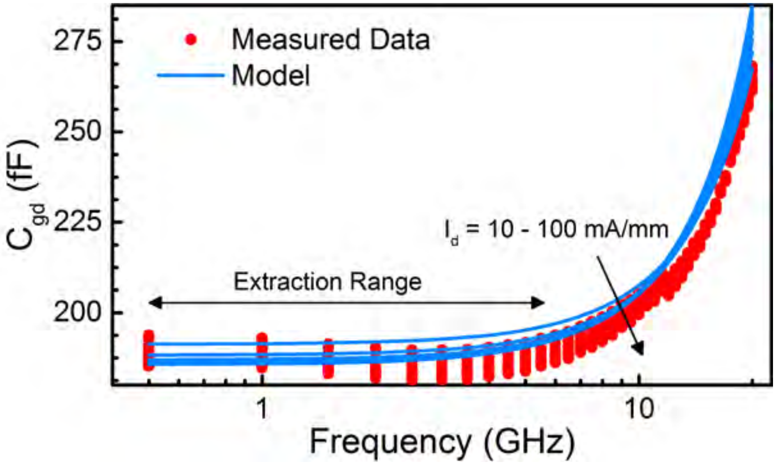
RF Parameter Extraction (ii)



Extract C_{GSO}

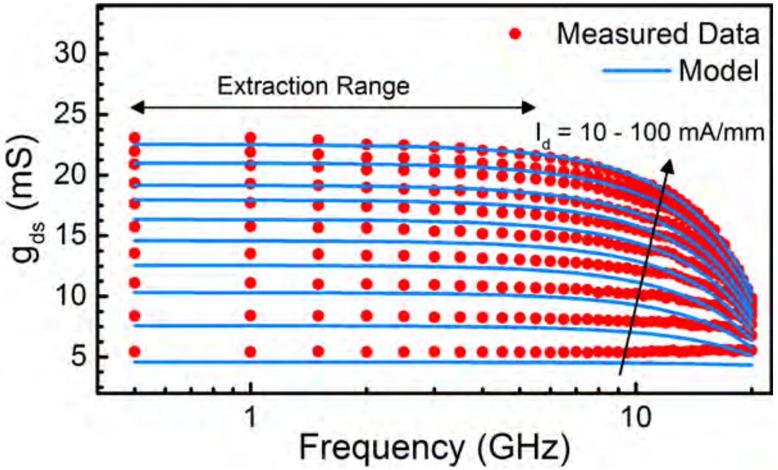


g_m dispersion handled by trap model



Extract C_{GDO}

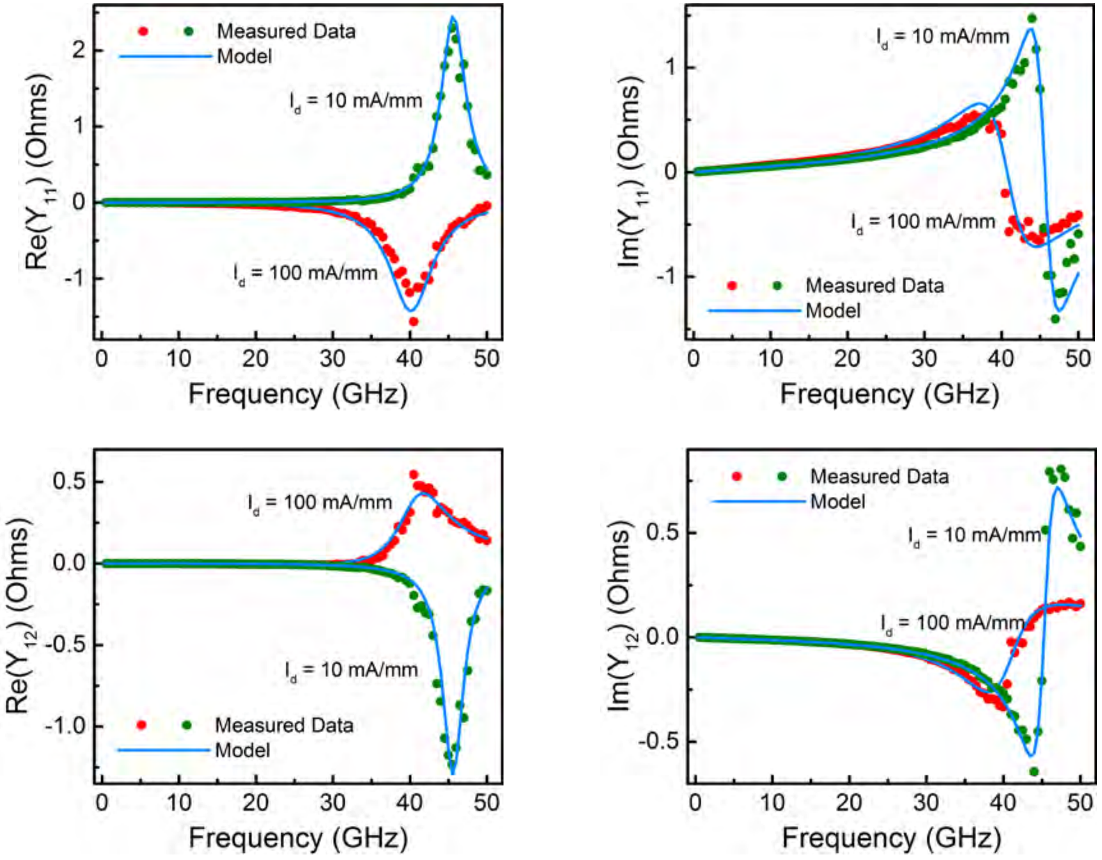
C_{GSO}	C_{GDO}	C_{DSO}
510 fF	165 fF	182 fF



g_{ds} dispersion handled by trap model

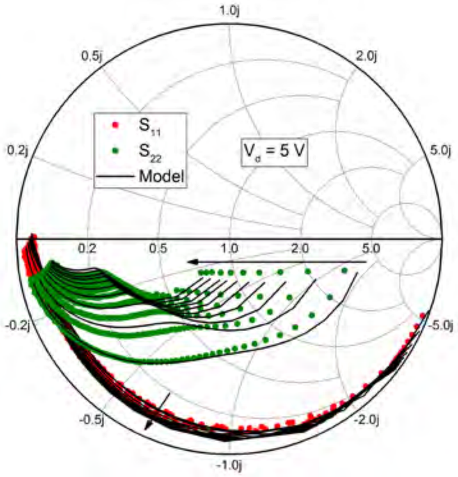
[1] Q. Fan *et al.*, *Proc. IEEE*, **98 (7),** [2010]

RF Parameter Extraction (iii)

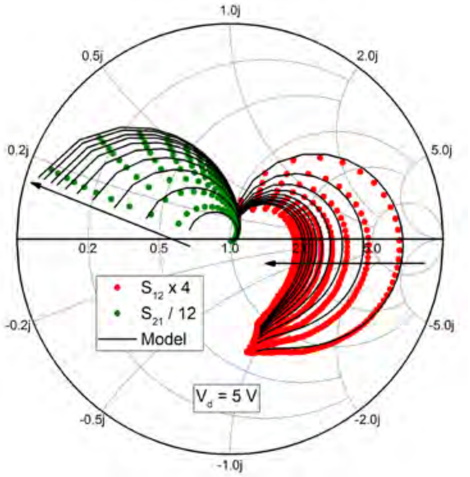


Resonant peaks due to interaction of inductances with intrinsic capacitances

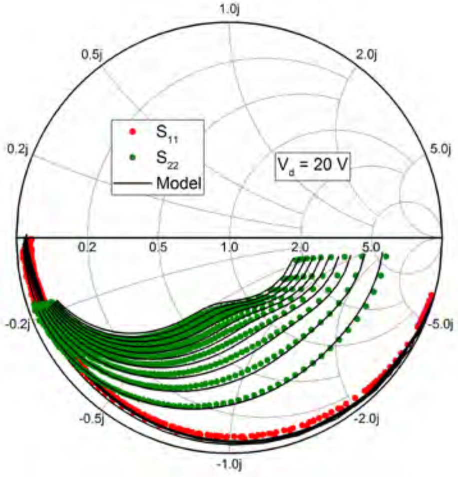
L_{xg}	L_{xs}	L_{xd}
$10.1\ pH$	$-6.08\ pH$	$8.25\ pH$



S_{11} & S_{22} (5V)



S_{12} & S_{21} (5V)



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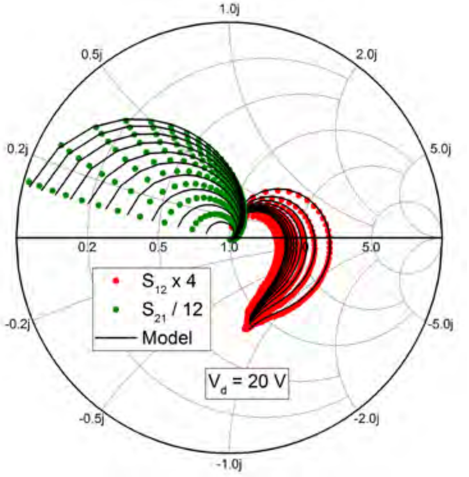
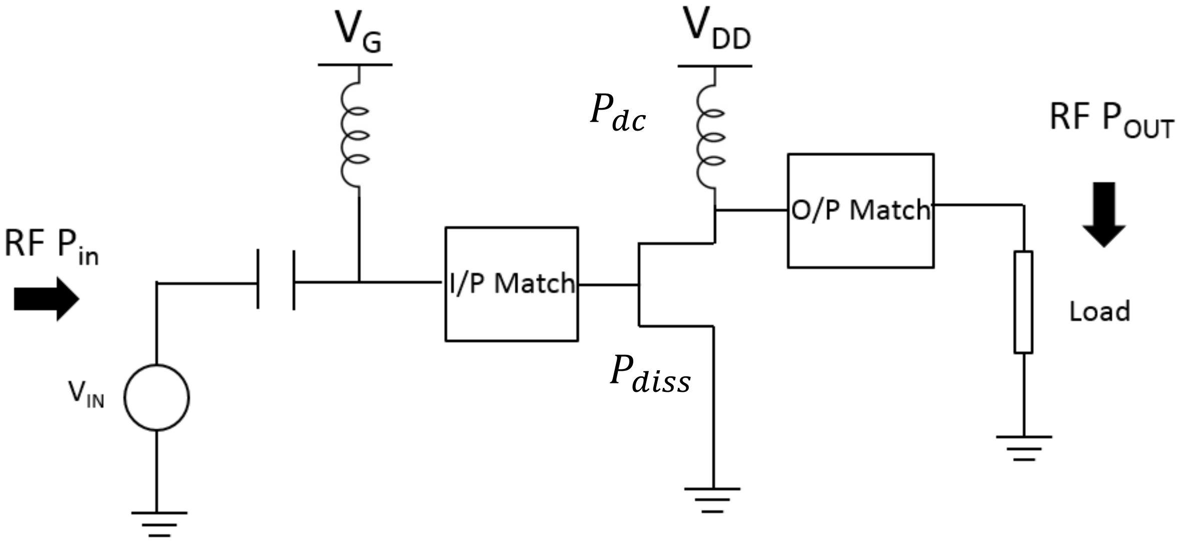


S_{12} & S_{21} (20V)

[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Power Amplifier Design Goals



$$Gain = \frac{P_{out}}{P_{in}}$$

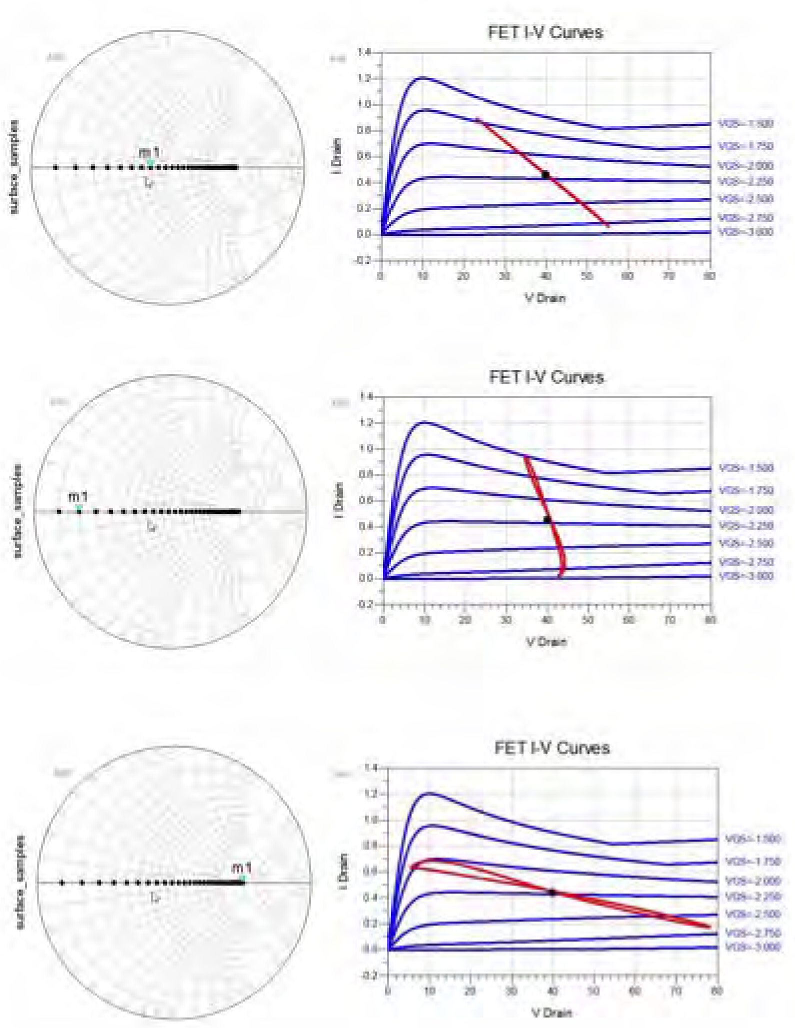
$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$

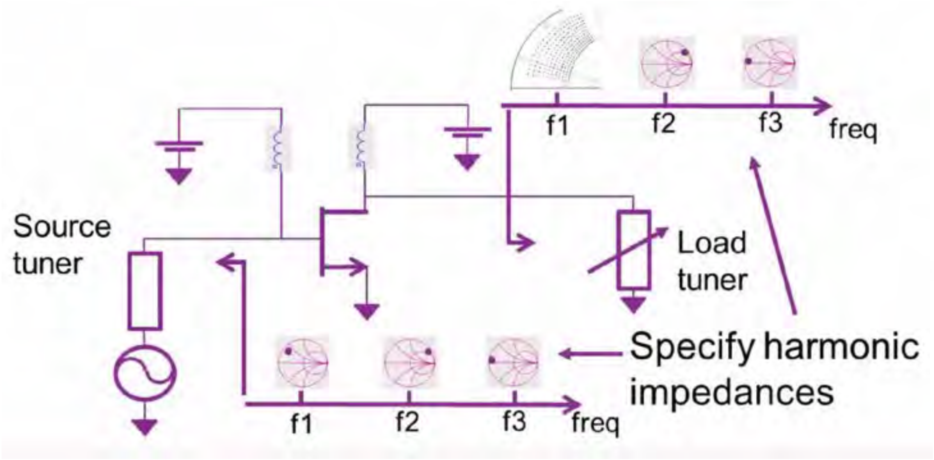
$$Drain\ Efficiency = \frac{P_{out}}{P_{dc}}$$

Load Pull Technique

Helps us:

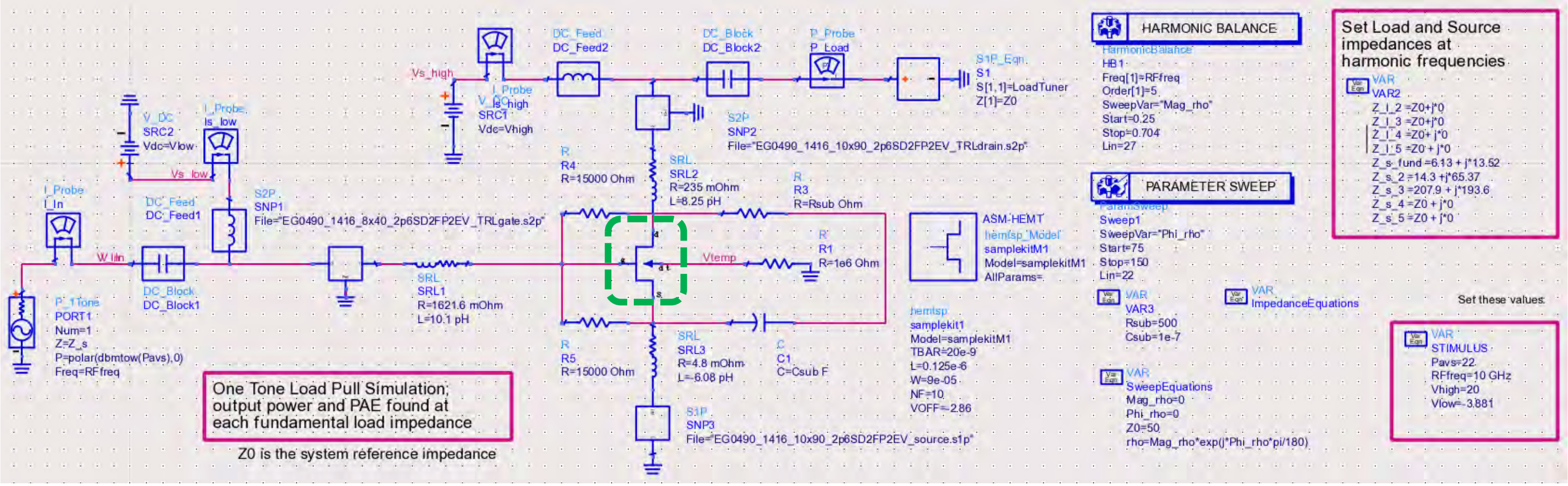
- Determine Optimum load impedance for maximum Pout and PAE performance
- Matching networks
- Understand tradeoffs!





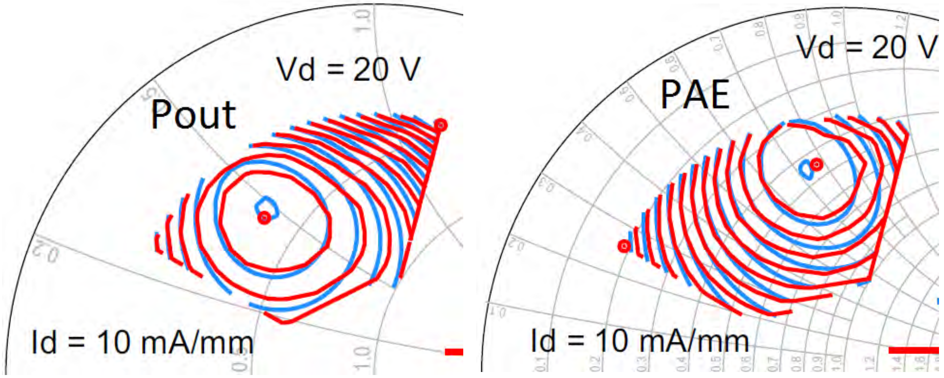
[M. S. Hashmi *et. al*, *IEEE Instrum. Meas. Mag.*, **16 (2)**, Feb., (2013)]

Large-Signal Model Validation

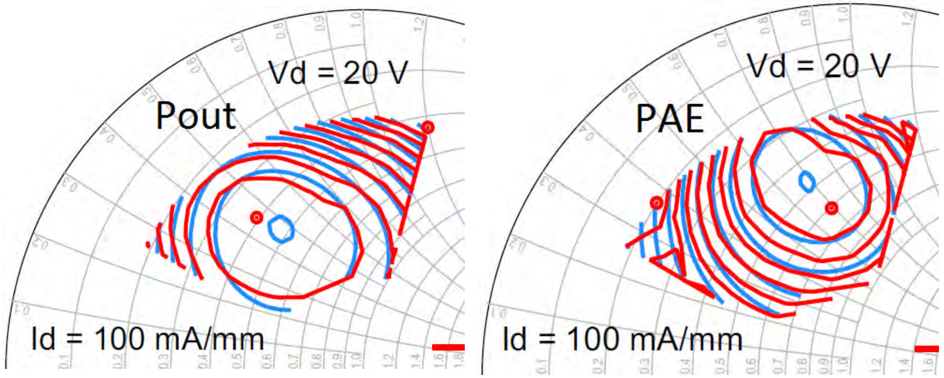


ADS Schematic for simulation of load-pull contours

22 dBm signal @ 10 GHz



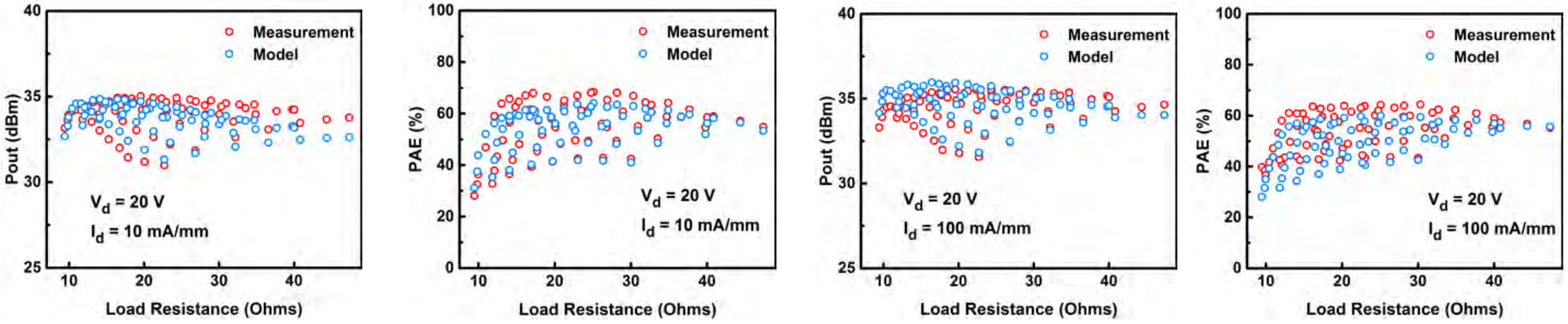
Pout & PAE load pull contours for 10 mA/mm



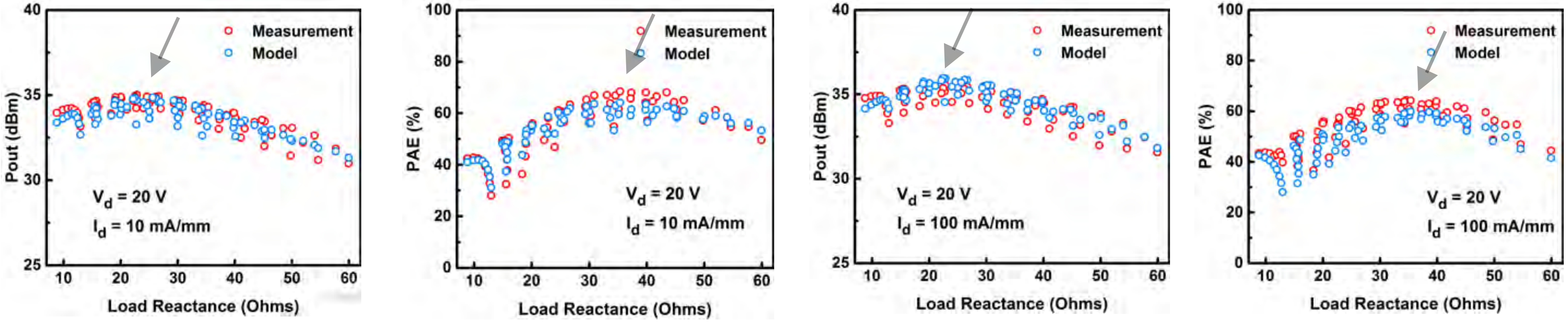
Pout & PAE load pull contours for 100 mA/mm

[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Validation – Real & Imag Loads



Pout & PAE against load resistance (real load)

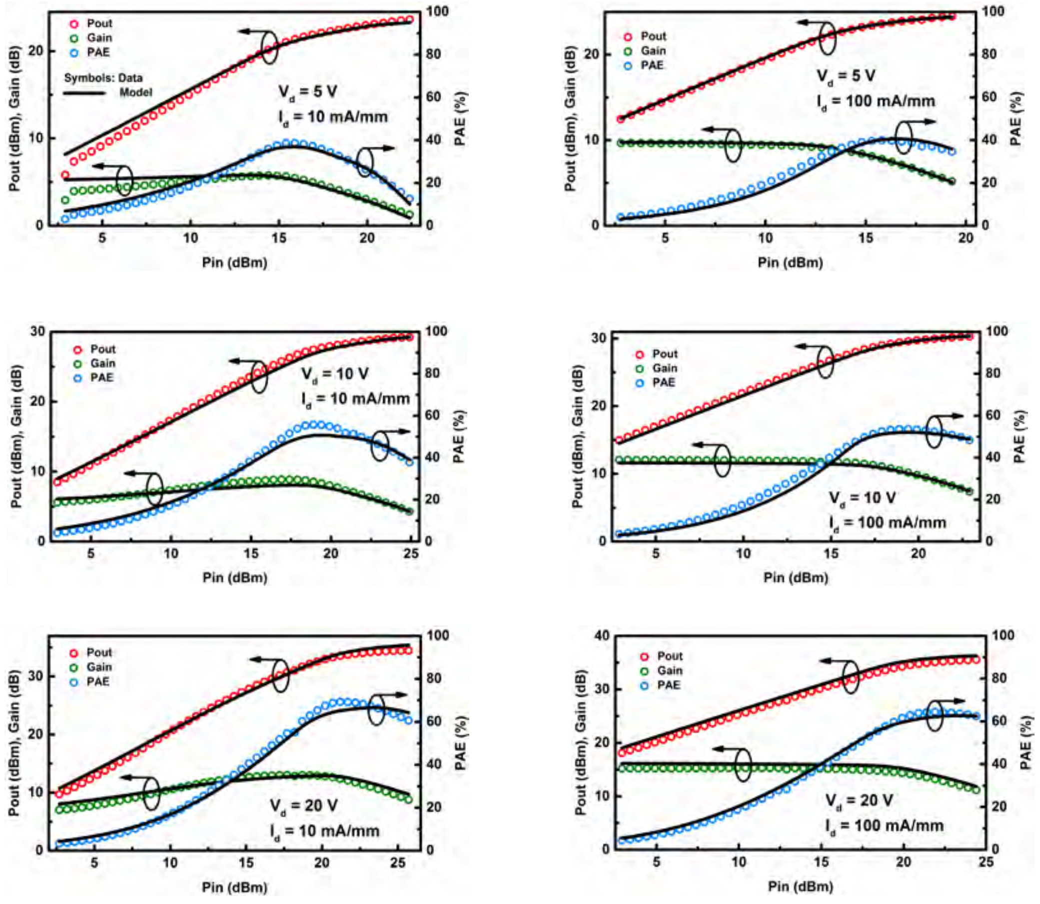


Pout & PAE against load reactance (imaginary load)

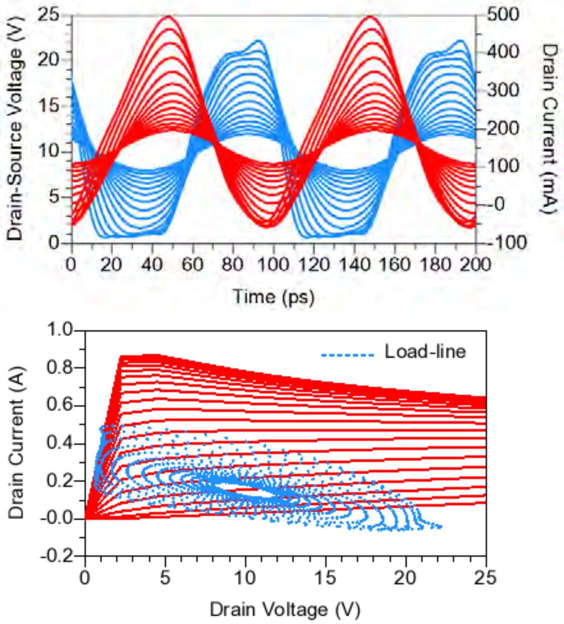
- Fairly accurate in predicting the maxima for Pout & PAE

[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep. [2017]

Validation – Drive-up (HB)



Harmonic balance drive-up characteristics showing Pout, PAE & Gain



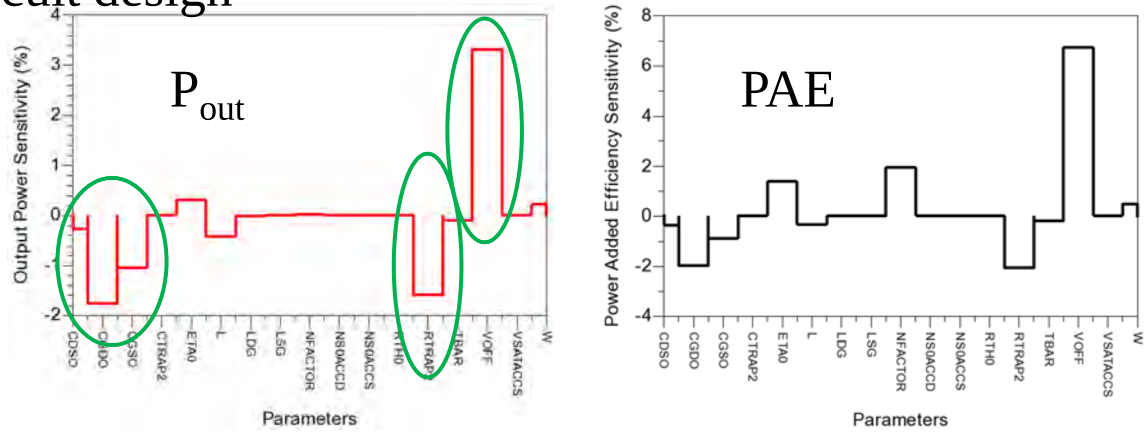
Time domain waveforms of drain voltage & current.
Load line contours spanning the IV plane

	Frequency	10 mA/mm	100 mA/mm
$Max. PAE$	f_0	$22.46 + j38.54$	$30.53 + j34.35$
	f_1	$40.61 - j93.39$	$37.32 - j73.44$
	f_2	$11.39 - j0.07$	$14.77 + j10.83$
$Max. P_{OUT}$	f_0	$19.57 + j22.83$	$19.57 + j22.83$
	f_1	$253.48 - j65.72$	$253.48 - j65.72$
	f_2	$15.66 - j31.21$	$15.66 - j31.21$

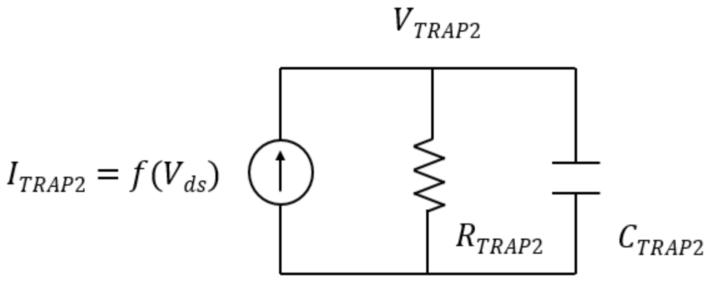
[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Statistical Simulation using Model

- The need for a statistical simulations
  - Variation in device performance
  - Obtain a production-level yield-oriented optimized circuit design



Sensitivity Analysis for Output power & PAE across key parameters



RC Circuit used for Trap Modeling

Parameter List

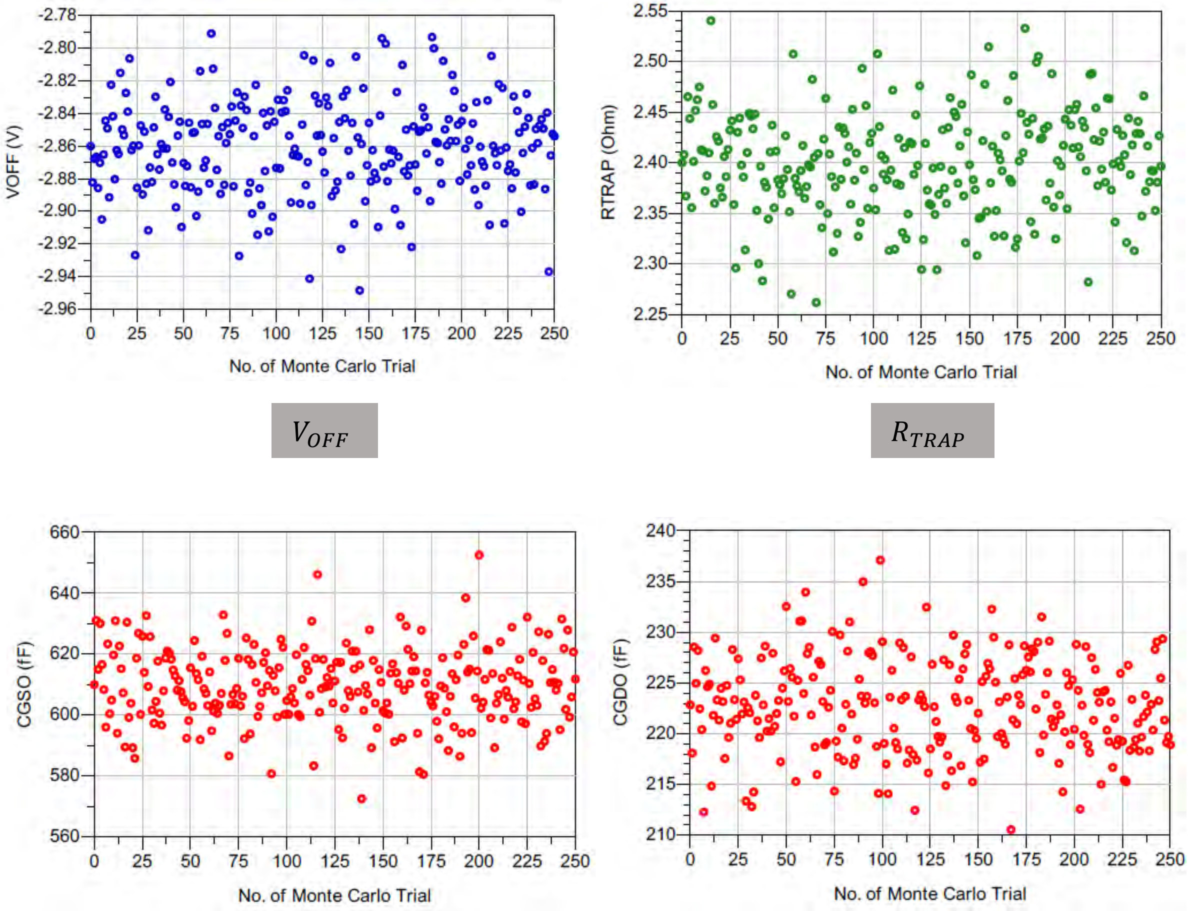
Model Element	Description
W	Width
L	Length
$L_{SG,DG}$	Access region length
T_{BAR}	AlGaN Barrier Thickness
V_{OFF}	Cutoff Voltage
U_0	Low Field Mobility
N_{FACTOR}	Subthreshold Slope Factor
η_0	DIBL Parameter
$N_{S0ACCS/D}$	AR 2DEG Density
$V_{SATACCS/D}$	AR saturation velocity
R_{TH0}	Thermal Resistance
R_{TRAP}	Trap Resistance
C_{GS0}	Gate-Source Overlap Cap.
C_{GD0}	Gate-Drain Overlap Cap.
C_{DS0}	Drain-Source Overlap Cap.

Monte Carlo Simulation

- Monte Carlo Controller
  - Number of trials = 250
  - Parameters included in simulation $V_{OFF}, C_{GSO}, C_{GDO}$ & R_{TRAP}

Mean & standard deviation values used for Monte Carlo Simulation

Parameter	$\boldsymbol{\mu}$	$\boldsymbol{\sigma_{\%}}$
V_{OFF}	$-2.86\ V$	1
R_{TRAP}	$2.4\ \Omega$	2
C_{GS0}	$610\ fF$	2
C_{GD0}	$225\ fF$	2



V_{OFF} R_{TRAP}

C_{GS0} C_{GD0}

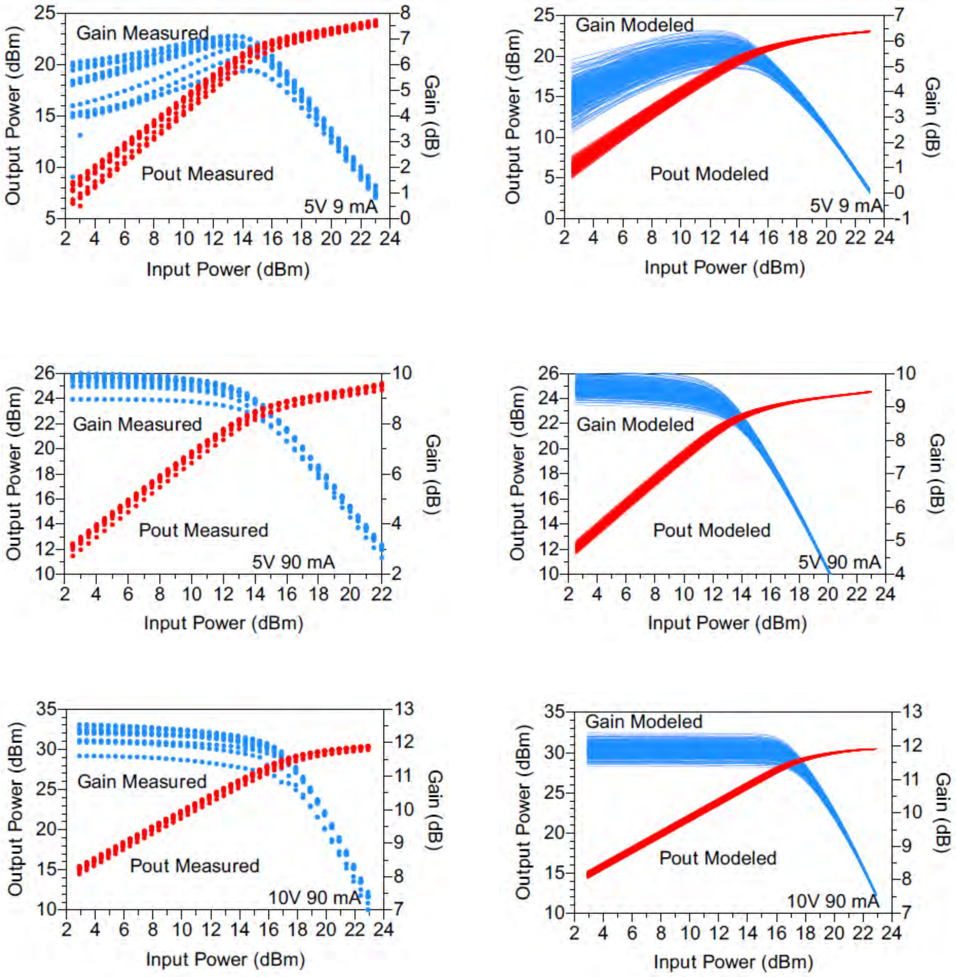
Distribution of parameter values to carry out statistical simulation using Monte Carlo

[1] S. A. Ahsan *et al.*, *Proc. IEEE Int. Conf. Emerging Electronics (ICEE)*, Mumbai, Dec. [2016]

Statistical Simulation Results

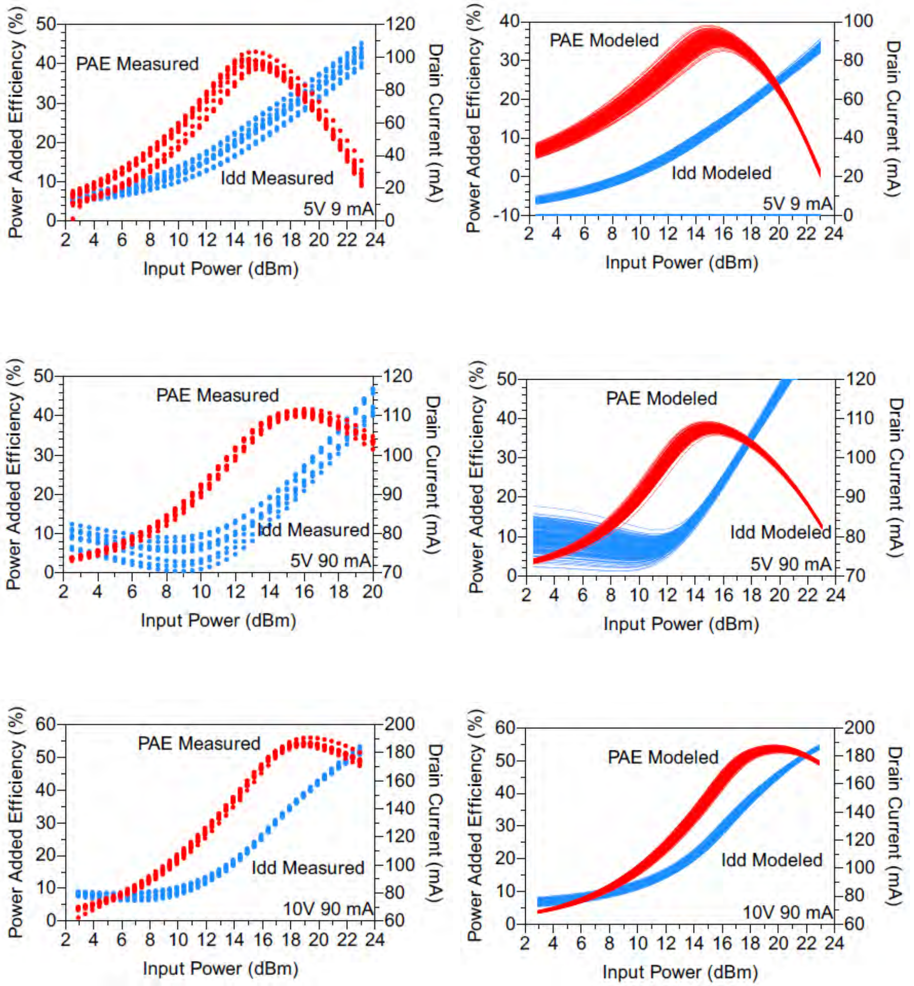
Measured

Model



Measured

Model



Pout, Gain & PAE & Idd for 250 trials of MC & measured data for a batch of 10 devices

Summary

- **Physics:** Physics-based fully analytical model for the GaN HEMTs
- **Accuracy:** Excellent agreement with the measured data @T, W and L
- **Flexibility:** Model is implemented in the **Verilog-A** code
  - Will be soon available in major commercial simulators
- **For industry:** ASM-GaN has been selected as industry standard model at Si2-CMC

Related Journal Publications

1. S. A. Ahsan, A. Pampori, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "A New Small-signal Parameter Extraction Technique for large gate-periphery GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 10, Oct. 2017.
2. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Multi-bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow", IEEE Journal of the Electron Devices Society, Vol. 5, Issue 5, Sept. 2017.
3. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Pole-Zero Approach to Analyze and Model the Kink in Gain-Frequency Plot of GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 3, Mar. 2017.
4. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Cross-Coupling and Substrate Capacitance in GaN HEMTs for Power-Electronic Applications", IEEE Transactions on Electron Devices (Special Issue), Vol. 64, Issue 3, Mar. 2017.
5. A. Dasgupta and Y. S. Chauhan, "Modeling of Induced Gate Thermal Noise in HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 26, Issue 6, June 2016.
6. S. A. Ahsan, S. Ghosh, A. Dasgupta, K. Sharma, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling in Dual Field Plate Power GaN HEMT for Accurate Switching Behaviour", IEEE Transactions on Electron Devices, Vol. 63, Issue 2, Feb. 2016.
7. A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Surface potential based Modeling of Thermal Noise for HEMT circuit simulation", IEEE Microwave and Wireless Components Letters, Vol. 25, Issue 6, June 2015.
8. S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan, "Surface-Potential-Based Compact Modeling of Gate Current in AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 62, Issue 2, Feb. 2015.
9. A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Compact Modeling of Flicker Noise in HEMTs", IEEE Journal of Electron Devices Society, Vol. 2, Issue 6, Nov. 2014.
10. S. Khandelwal, C. Yadav, S. Agnihotri, Y. S. Chauhan, A. Curutchet, T. Zimmer, J.-C. Dejaeger, N. Defrance and T. A. Fjeldly, "A Robust Surface-Potential-Based Compact Model for GaN HEMT IC Design", IEEE Transactions on Electron Devices, Vol. 60, Issue 10, Oct. 2013.
11. S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, "Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices", IEEE Transactions on Electron Devices, Vol 59, Issue 8, Oct. 2012.

Related Conference Publications

1. S. Khandelwal, S. Ghosh, S. A. Ahsan and Y. S. Chauhan, "Dependence of GaN HEMT AM/AM and AM/PM Non-Linearity on AlGaN Barrier Layer Thickness", IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpur, Malaysia, Nov. 2017.
2. S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Surface-potential-based Gate-periphery-scalable Small-signal Model for GaN HEMTs", IEEE Compound Semiconductor IC Symposium (CSICS), Miami, USA, Oct. 2017.
3. S. Ghosh, S. A. Ahsan, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "GaN HEMT Modeling for Power and RF Applications using ASM-HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
4. S. Ghosh, A. Dasgupta, A. K. Dutta, S. Khandelwal, and Y. S. Chauhan, "Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
5. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Statistical Simulation for GaN HEMT Large Signal RF performance using a Physics-based Model", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
6. A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, N. Defrance, and Y. S. Chauhan, "Modeling DC, RF and Noise behavior of GaN HEMTs using ASM-HEMT Compact Model", IEEE International Microwave and RF Conference (IMaRC), Delhi, India, Dec. 2016.
7. S. A. Ahsan, S. Ghosh, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "ASM-HEMT: Advanced SPICE Model for Gallium Nitride High Electron Mobility Transistors", International Conference of Young Researchers on Advanced Materials (ICYRAM), Bangalore, India, Dec. 2016.
8. S. Ghosh, S. A. Ahsan, S. Khandelwal and Y. S. Chauhan, "Modeling of Source/Drain Access Resistances and their Temperature Dependence in GaN HEMTs", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
9. S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Modeling of Kink-Effect in RF Behaviour of GaN HEMTs using ASM-HEMT Model", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
10. R. Nune, A. Anurag, S. Anand and Y. S. Chauhan, "Comparative Analysis of Power Density in Si MOSFET and GaN HEMT based Flyback Converters", IEEE International Conference on Compatibility and Power Electronics, Bydgoszcz, Poland, June 2016.
11. S. Agnihotri, S. Ghosh, A. Dasgupta, A. Ahsan, S. Khandewal, and Y. S. Chauhan, "Modeling of Trapping Effects in GaN HEMTs", IEEE India Conference (INDICON), New Delhi, India, Dec. 2015.
12. S. Ghosh, S. Agnihotri, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Trapping Effects in RF GaN HEMTs under Pulsed Conditions", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
13. S. Agnihotri, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Impact of Gate Field Plate on DC, C-V, and Transient Characteristics of Gallium Nitride HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
14. K. Sharma, S. Ghosh, A. Dasgupta, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Capacitance Analysis of Field Plated GaN HEMT", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
15. S. A. Ahsan, S. Ghosh, J. Bandarupalli, S. Khandelwal, and Y. S. Chauhan, "Physics based large signal modeling for RF performance of GaN HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
16. S. Khandelwal, S. Ghosh, Y. S. Chauhan, B. Iniguez, T. A. Fjeldly and C. Hu, "Surface-Potential-Based RF Large Signal Model for Gallium Nitride HEMTs", IEEE Compound Semiconductor IC Symposium (CSICS), New Orleans, USA, Oct. 2015.
17. S. A. Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling of a GaN HEMT with Gate and Source Field Plates", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015.
18. A. Dasgupta and Y. S. Chauhan, "Surface Potential Based Modeling of Induced Gate Thermal Noise for HEMTs", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015.
19. S. Khandelwal, Y. S. Chauhan, B. Iniguez, and T. Fjeldly, "RF Large Signal Modeling of Gallium Nitride HEMTs with Surface-Potential Based ASM-HEMT Model", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015. (Invited)
20. A. Dasgupta, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "ASM-HEMT: Compact model for GaN HEMTs", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 2015.
21. K. Sharma, A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Effect of Access Region and Field Plate on Capacitance behavior of GaN HEMT", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 2015.
22. S. Ghosh, K. Sharma, S. Khandelwal, S. Agnihotri, T. A. Fjeldly, F. M. Yigletu, B. Iniguez, and Y. S. Chauhan, "Modeling of Temperature Effects in a Surface-Potential Based ASM-HEMT model", IEEE International Conference on Emerging Electronics (ICEE), Bangalore, India, Dec. 2014.

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- Avirup Dasgupta (UCB)

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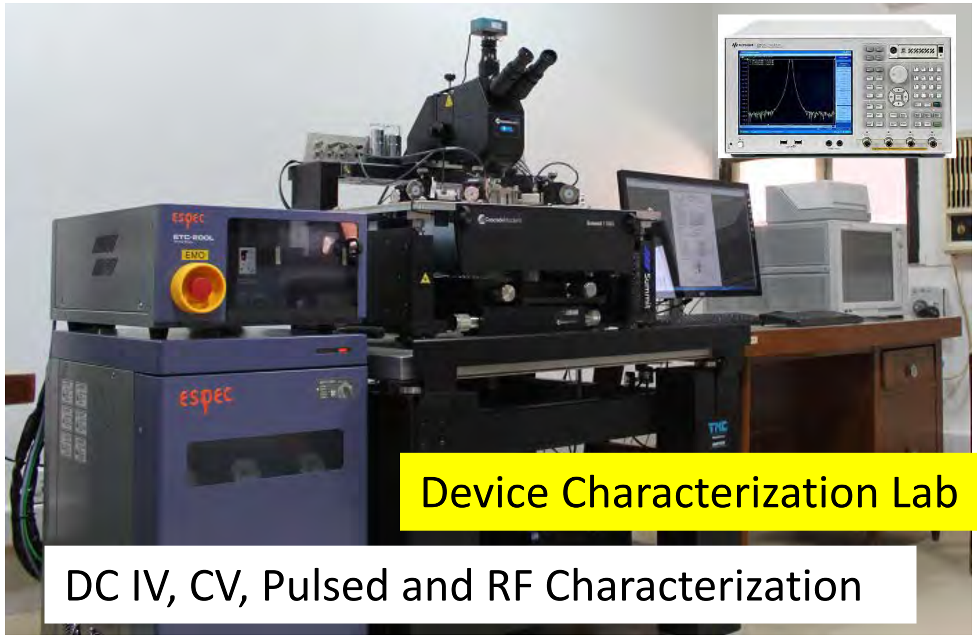

DC IV, CV, Pulsed and RF Characterization

Publications:

	2018	2017	2016	2015	2014	2013
Books	1*			1		
Journal	20*	19	18	9	5	3
Conference	10	11	30	30	8	4