SPICE and Compact Modeling

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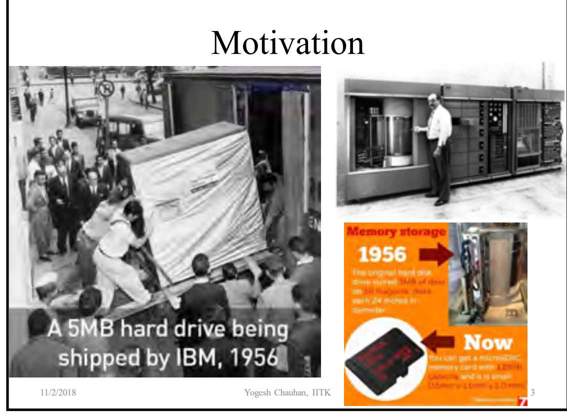
Outline

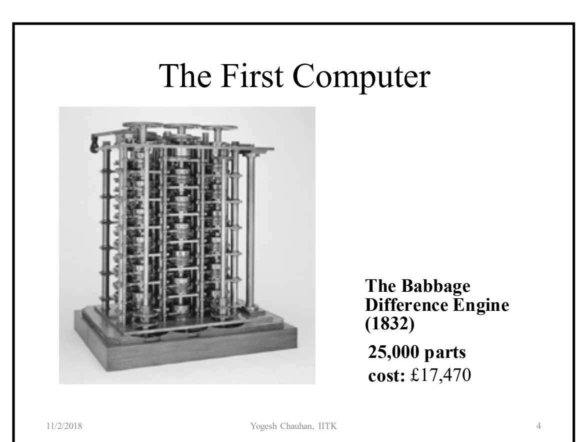
- Introduction to SPICE
- Compact Modeling

Motivation



Memory storage
1956
Now

The First Computer



The Babbage Difference Engine (1832)

25,000 parts
cost: £17,470

ENIAC - The first electronic computer (1946)

- 17,468 vacuum tubes
- 7200 crystal diodes
- 1500 relays
- 70,000 resistors
- 10,000 capacitors
- Weight > 27 Ton
- 1800 sq. ft.
- 150 kW of electricity

Semiconductors – Heart of technological progress and innovation

- The semiconductor is one of the most pervasive and powerful inventions in human history.

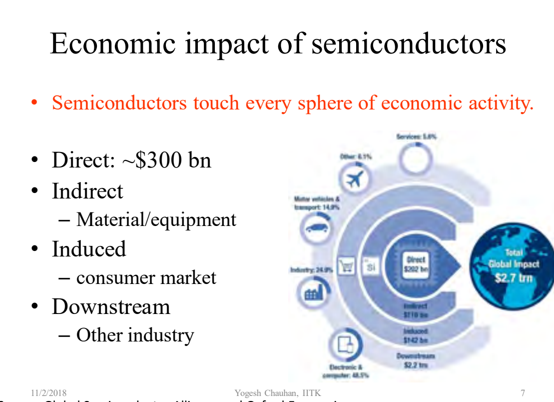
Top innovations since the wheel:
Printing Press Electricity Penicillin

Nobel Prize in Physics 2014
"invention of efficient blue LEDs"

Economic impact of semiconductors

- Semiconductors touch every sphere of economic activity.

- Direct: ~$300 bn
- Indirect
  - Material/equipment
- Induced
  - consumer market
- Downstream
  - Other industry



Source: Global Semiconductor Alliance and Oxford Economics

Modeling and Simulation

- Modeling – Approximation (different levels)
- Simulation – Trade-off (different considerations)
- Why simulation?
  - Prediction: Faster than measurements (Measurement/technology not available)
  - Understanding
    - Measurable parameters
    - Non-measurable parameters

- “Everything should be made as simple as possible, but not any simpler” – A. Einstein

Courtesy: X. Zhou

Spectrum of Approaches to Analyzing Electronic System

The “Big Picture”

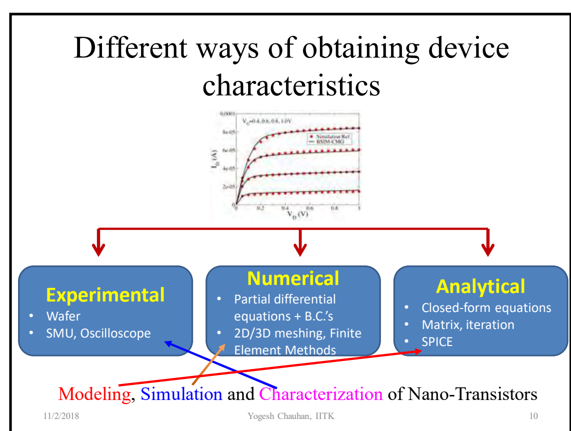
Physics — Engineering

Device | Circuit | System

Quantum mechanics | Semiclassical | Monte Carlo | Hydro-dynamic | Drift-diffusion | Device | Circuit | Electrical | Behavioral | Logic | Timing | Switch | Gate | RTL | Functional | Structural | Behavioral

Courtesy: X. Zhou

Different ways of obtaining device characteristics



Experimental
- Wafer
- SMU, Oscilloscope

Numerical
- Partial differential equations + B.C.’s
- 2D/3D meshing, Finite Element Methods

Analytical
- Closed-form equations
- Matrix, iteration
- SPICE

Modeling, Simulation and Characterization of Nano-Transistors

SPICE

- SPICE (*Simulation Program with Integrated Circuits Emphasis*) is a powerful general purpose *circuit simulation* program that is used to verify circuit designs and to predict the circuit behavior.

- Original SPICE program, SPICE1, was developed at University of California, Berkeley and released for public use in May 1972.
- SPICE2 was released in 1975 written in Fortran.
- SPICE3 was released in March 1985 written in C.
- The free distribution by Berkeley is a key factor contributing to the universal acceptance of SPICE.

Ref. MOSFET Models for SPICE Simulation by William Liu

SPICE Development

- SPICE was developed out of a graduate *class project* at University of California, Berkeley

Laurence W. Nagel — Ronald A. Rohrer — Donald O. Pederson

L. W. Nagel and D. O. Pederson, “SPICE (Simulation Program with Integrated Circuit Emphasis),” Memorandum No. ERL-M382, University of California, Berkeley, Apr. 1973. http://www.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html

SPICE programs

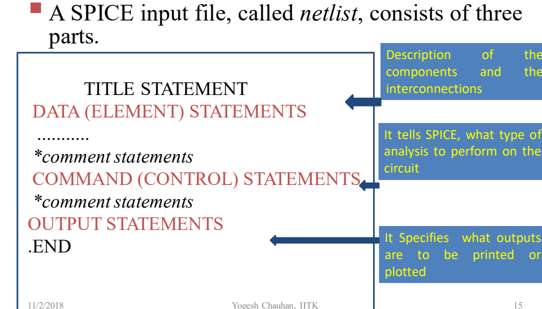
- Berkeley SPICE: Original SPICE. Available in public domain and can be run on UNIX platforms. Latest version is SPICE3f5 and supports upto BSIM3v3.1.
- I-SPICE: Interactive SPICE, developed in the late 1970s and first commercial version of SPICE.
- HSPICE: Created by Meta-Software, later owned by Avant and now owned by Synopsys. Popular for interactive user interfaces.
- PSPICE: PC based version of SPICE created by Micro-Sim, which was acquired by Orcad and then acquired by Cadence.
- SPECTRE: An improved Berkeley SPICE that addresses several numerical problems and inadequacies in simulation for RF circuits created by Cadence
- ADS: Agilent's SPICE software popular for RF circuit design.
- ELDO: Mentor Graphics' SPICE software.
- SMASH: Developed by Dlophin Integration France. Free!
- Ngspice: Open source

SPICE Simulation Models and Netlists

- SPICE has the ability to simulate components ranging from the most basic passive elements (R, C) to sophisticated semiconductor devices such as MOSFETs.
  - Commercial simulators include more than 15,000 different components.
- The quality of SPICE models can vary, and not all SPICE models are applicable to every application.
  - Using a SPICE model inappropriately can lead to inaccurate results, or even generate an error in some circumstances.
- A circuit must be presented to SPICE in the form of a netlist.
  - The netlist is a text description of all circuit elements such as transistors and capacitors, and their corresponding connections.
  - Modern schematic capture and simulation tools allow users to draw circuit schematics, and automatically translate the circuit diagrams into netlists.

Circuit Topology and Analysis in SPICE

- A SPICE input file, called *netlist*, consists of three parts.



Description of the components and the interconnections

It tells SPICE, what type of analysis to perform on the circuit

It Specifies what outputs are to be printed or plotted

Circuit Components

- Independent DC Sources
  - Voltage source: Vname N1 N2 AnalysisType Value
  - Current source: Iname N1 N2 AnalysisType Value
- Resistors
  - Rname N1 N2 Value
- Capacitors and Inductors
  - Cname N1 N2 Value <initial condition>
  - Lname N1 N2 Value <initial condition>

Circuit Components

- Semiconductor Devices – MOSFETs
  - Semiconductor device is specified by two command lines: an element line (assigned a unique name) and model statement line (.MODEL).
- *Element Statement*:
  - Mname ND NG NS NB ModName L=1u W= 1u
- *Model statement*:
  - .MODEL ModName NMOS (KP= VT0= lambda= gamma=)

Type of Analysis

- .OP Statement
  - Instructs SPICE to compute the DC operating points (voltage at the nodes, current in each voltage source)
- .DC Statement
  - Allows you to increment (sweep) an independent source over a certain range with a specified step.
  - .DC Sourcename START STOP STEP
- .TRAN Statement
  - Specifies the time interval over which the transient analysis takes place, and the time increments.
  - .TRAN TSTEP TSTOP <TSTART <TMAX>> <UIC>

Use initial condition

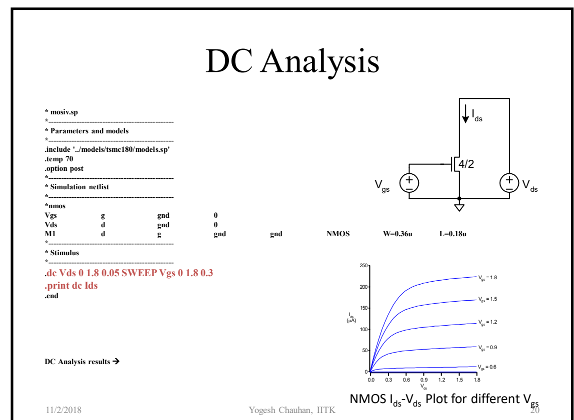
Output Statements

- These statements will instruct SPICE what output to generate.
- Two types of outputs are *prints* (table of data points) and *plots* (graphical representation).

```
.PRINT TYPE OV1 OV2 OV3 ...
.PLOT TYPE OV1 OV2 OV3 ...
```

Type of analysis: DC,TRAN,AC

Output variables are OV1, OV2 and can be voltage or currents in voltage sources



How SPICE solves circuit bias points?

- Why do we care how SPICE works internally?
  - When things go wrong with a simulation, having some insight into the operation of the program helps you figure out how to make your simulation run and also allows you to use the program in a more efficient way.
- We will look in detail at how SPICE solves DC bias point simulations and then look briefly at some other types of simulation.
  - DC type calculations are fundamental to the operation of the other types of simulation and (with the exception of transient simulations) - easy to extend the DC analysis that SPICE does to the other types of analysis.

How SPICE Works

- Example: Simple circuit

```
R1  n1  n2  5
R2  n0  n2  10
R3  n2  n3  5
R4  n0  n3  10
I1  n0  n1  3
```

Circuit: V_1 (n1), 5Ω, V_2 (n2), 5Ω, V_3 (n3); 3A source, 10Ω, 10Ω, n0

Resistor R1, value = 5ohm, connected between node n1, n2

Keyword Rx : for resistor /* Resistor name must start from R. Similarly for others*/

Cx : for capacitor

Ix / Vx: for independent Current/Voltage sources

A Simple Example

SPICE firstly forms a set of nodal equations for a circuit is it trying to solve. These are formed from the netlist.

Nodal equations based on KCL

$$-3+\frac{V_1-V_2}{5}=0$$

$$\frac{V_2-V_1}{5}+\frac{V_2}{10}+\frac{V_2-V_3}{5}=0$$

$$\frac{V_3-V_2}{5}+\frac{V_3}{10}=0$$

Circuit: V_1 (n1), 5Ω, V_2 (n2), 5Ω, V_3 (n3); 3A, 10Ω, 10Ω, n0

The matrix solution is then obtained

A Simple Example

- These are rearranged and written in matrix form:

$$-3+\frac{V_1-V_2}{5}=0$$

$$\frac{V_2-V_1}{5}+\frac{V_2}{10}+\frac{V_2-V_3}{5}=0$$

$$\frac{V_3-V_2}{5}+\frac{V_3}{10}=0$$

$$\Rightarrow \begin{bmatrix} 0.2 & -0.2 & 0 \\ -0.2 & 0.5 & -0.2 \\ 0 & -0.2 & 0.3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 3 \\ 0 \\ 0 \end{bmatrix}$$

A Simple Example

- **Gaussian Elimination**

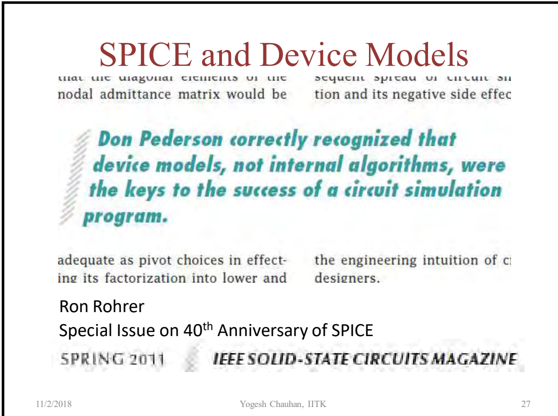
$$\begin{bmatrix} 0.2 & -0.2 & 0 \\ -0.2 & 0.5 & -0.2 \\ 0 & -0.2 & 0.3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 3 \\ 0 \\ 0 \end{bmatrix} \Rightarrow \begin{bmatrix} 0.2 & -0.2 & 0 \\ 0 & 0.3 & -0.2 \\ 0 & 0 & 0.25 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 3 \\ 3 \\ 3 \end{bmatrix}$$

Easy to solve on computer, no matter how big it is

Outline

- Introduction to SPICE
- Compact Modeling

SPICE and Device Models



Ron Rohrer
Special Issue on 40th Anniversary of SPICE

Device Model

- Good SPICE model should be
  - Accurate
    - Produce trustworthy simulations
  - Simple
    - Simulation time is minimum
    - Easy parameter extraction
- Balance between accuracy and simplicity depends on end application

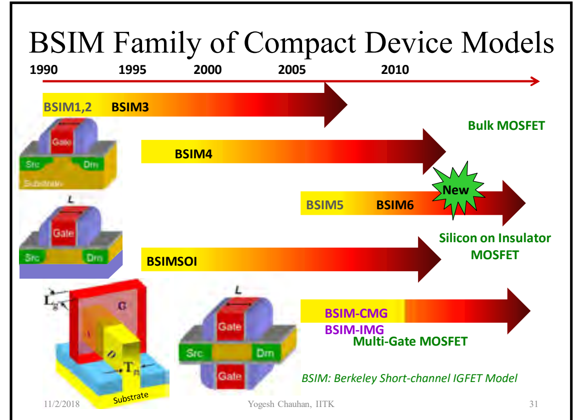
Creating a model that is both accurate and simple is by no means a simple task.

Model Types

- Types of Models
  - Look Up Table
  - Physical
  - Empirical
  - Compact

SPICE models for MOSFET

- **First-generation models (Level 1, 2, and 3)**
  - Emphasize the device physics.
  - Physically accurate representation without equal consideration to mathematical representation often creates numerical problems during circuit simulation.
- **Second generation models (BSIM, BSIM2 and HSPICE Level28)**
  - corrects numerical issues with greater focus on mathematical implementation.
  - Several empirical parameters without clear physical meanings are incorporated.
  - Improved convergence
  - Complicated parameter extraction procedure as well as weakening the link between model parameters and fabrication process.
- **Third generation models (BSIM3 and MM9)**
  - Reintroduces physical basis to the model.
  - Maintains mathematical robustness using smoothing functions.


BSIM Family of Compact Device Models
1990
1995
2000
2005
2010
BSIM1,2
BSIM3
Bulk MOSFET
BSIM4
BSIM5
BSIM6
New
Silicon on Insulator MOSFET
BSIMSOI
BSIM-CMG
BSIM-IMG
Multi-Gate MOSFET
BSIM: Berkeley Short-channel IGFET Model
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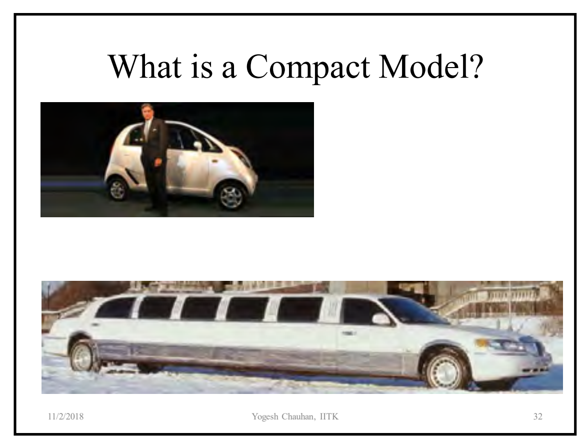
What is a Compact Model?
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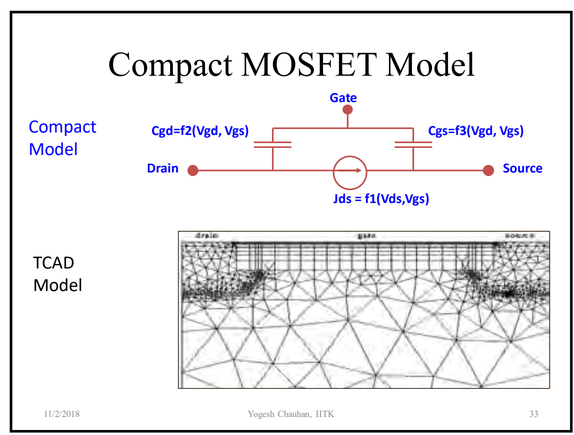
Compact MOSFET Model
Compact Model
Gate
Cgd=f2(Vgd, Vgs)
Cgs=f3(Vgd, Vgs)
Drain
Source
Jds = f1(Vds,Vgs)
TCAD Model
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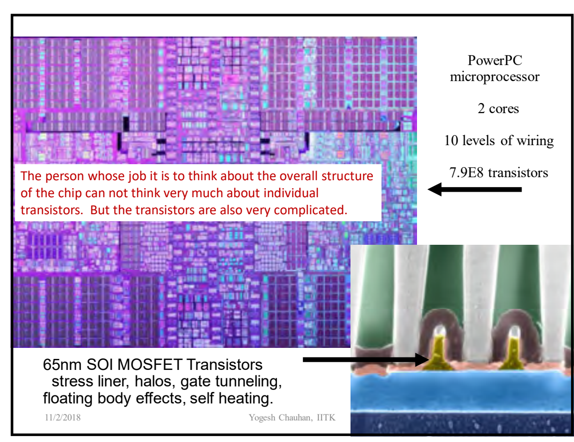
PowerPC microprocessor
2 cores
10 levels of wiring
7.9E8 transistors
The person whose job it is to think about the overall structure of the chip can not think very much about individual transistors. But the transistors are also very complicated.
65nm SOI MOSFET Transistors
stress liner, halos, gate tunneling,
floating body effects, self heating.
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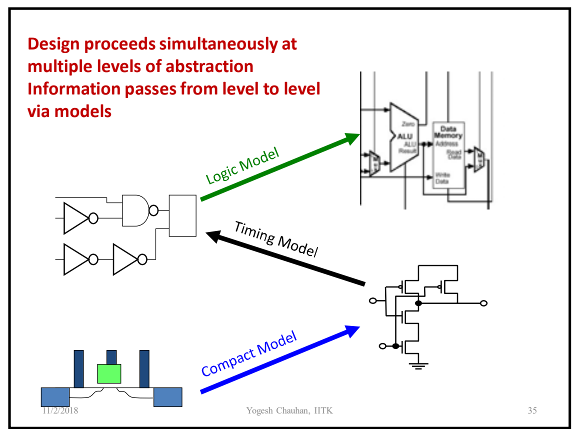
Design proceeds simultaneously at multiple levels of abstraction
Information passes from level to level via models
Logic Model
Timing Model
Compact Model
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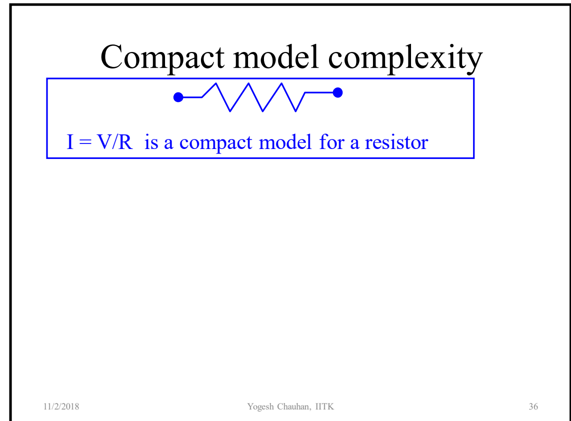
Compact model complexity
I = V/R is a compact model for a resistor
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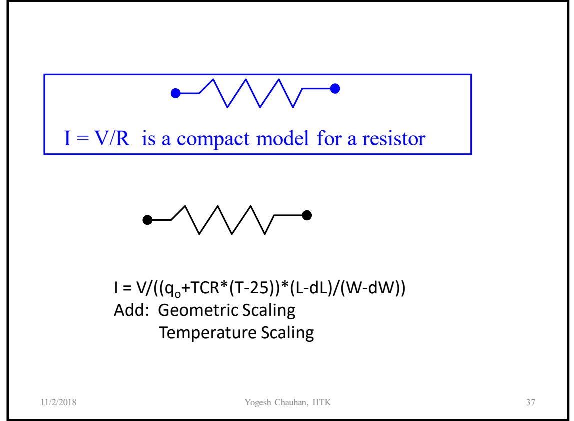

I = V/R is a compact model for a resistor
I = V/((qo+TCR*(T-25))*(L-dL)/(W-dW))
Add: Geometric Scaling
Temperature Scaling
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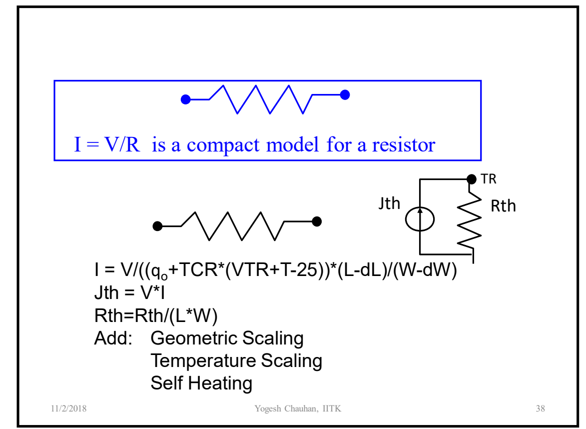

I = V/R is a compact model for a resistor
TR
Jth
Rth
I = V/((qo+TCR*(VTR+T-25))*(L-dL)/(W-dW)
Jth = V*I
Rth=Rth/(L*W)
Add: Geometric Scaling
Temperature Scaling
Self Heating
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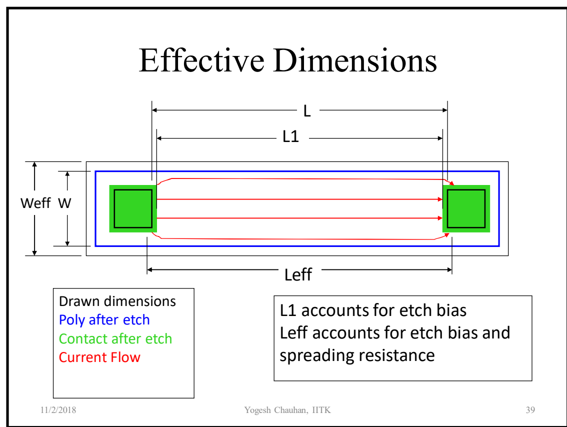

Effective Dimensions
L
L1
Weff W
Leff
Drawn dimensions
Poly after etch
Contact after etch
Current Flow
L1 accounts for etch bias
Leff accounts for etch bias and spreading resistance
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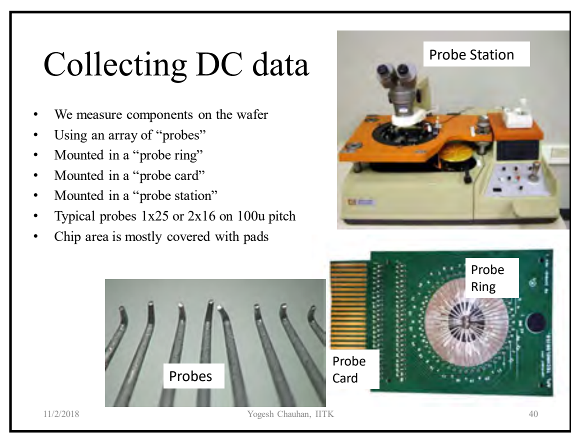

Collecting DC data
We measure components on the wafer
Using an array of "probes"
Mounted in a "probe ring"
Mounted in a "probe card"
Mounted in a "probe station"
Typical probes 1x25 or 2x16 on 100u pitch
Chip area is mostly covered with pads
Probe Station
Probe Ring
Probe Card
Probes
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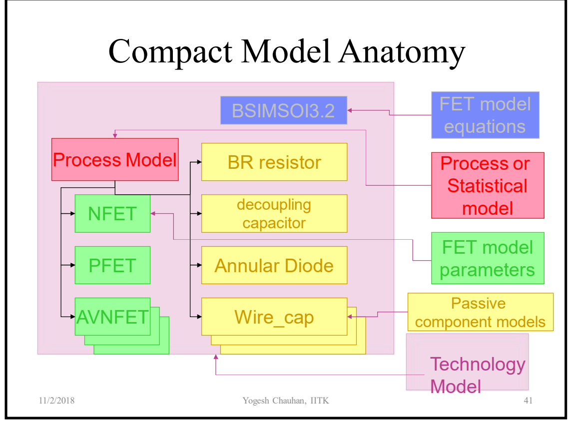

Compact Model Anatomy
BSIMSOI3.2
FET model equations
Process Model
BR resistor
Process or Statistical model
NFET
decoupling capacitor
FET model parameters
PFET
Annular Diode
AVNFET
Wire_cap
Passive component models
Technology Model
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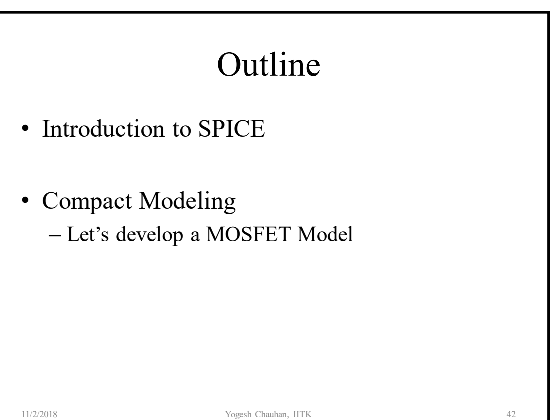

Outline
Introduction to SPICE
Compact Modeling
– Let's develop a MOSFET Model
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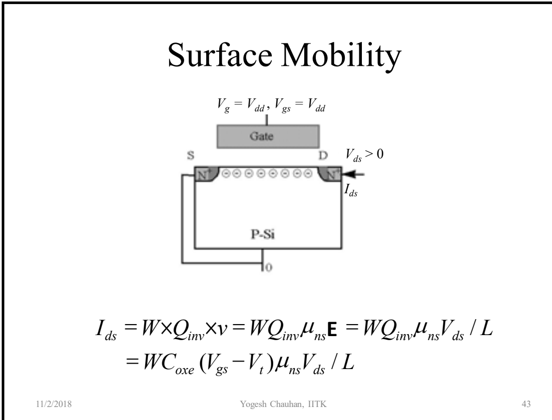


Effective Mobility & Effective Electric Field

- Experiments show – Inversion layer mobility vs. E_{eff} is a function of the doping concentration, the gate and substrate bias and the oxide thickness.
- The effective mobility, is a spatial average of the mobility profile in the inversion layer.
- The effective field for the electrons in the inversion layer is defined as the average of the normal electric field $E_y(y)$ experienced by the electrons weighted by the electron concentration .

$$E_{eff} = \frac{\int_0^{y_i} E_y(y) \cdot n(y) \cdot dy}{\int_0^{y_i} n(y) \cdot dy} \qquad \mu_{eff} = \frac{\int_0^{y_i} \mu_y(y) \cdot n(y) \cdot dy}{\int_0^{y_i} n(y) \cdot dy}$$

The integration is performed over the depth of the inversion layer y_i.

Effective Field

- In terms of the field at the top (E_t) and bottom (E_b) of the inversion layer, the effective field becomes

$$E_{eff} = \frac{E_t + E_b}{2} = \frac{1}{\varepsilon_{Si}}\left(Q_{dep} + \frac{Q_{inv}}{2}\right) \qquad E_t = \frac{Q_{inv} + Q_{dep}}{\varepsilon_{Si}} \qquad E_b = \frac{Q_{dep}}{\varepsilon_{Si}}$$

- Q_{inv} and Q_{dep} denote the inversion and depletion charge densities, respectively.

$$Q_{inv} = -q\int_0^{y_i} n(y) \cdot dy$$

$$Q_{dep} = \sqrt{2\varepsilon_{Si}(2\phi_b)N_{sub}/q}$$

General definition

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(Q_{dep} + \eta Q_{inv}\right)$$

The parameter η is dependent on the orientation of the crystal surface and can assume values different from ½ due to valley repopulation effects.

η=1/2 for (100) orientation
η=1/3 for (110) and (111) orientation

Surface Mobility

- Mobility is a function of the average of the fields at the bottom and the top of the inversion charge layer, E_b and E_t .

From Gauss's Law, $\mathbf{E}_b = -Q_{dep}/\varepsilon_s$

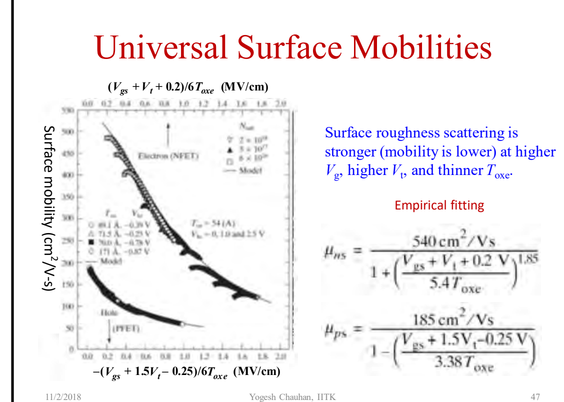
$$V_g = V_{fb} + \psi_s + V_{ox} \Rightarrow V_t = V_{fb} + \phi_{st} - Q_{dep}/C_{oxe}$$

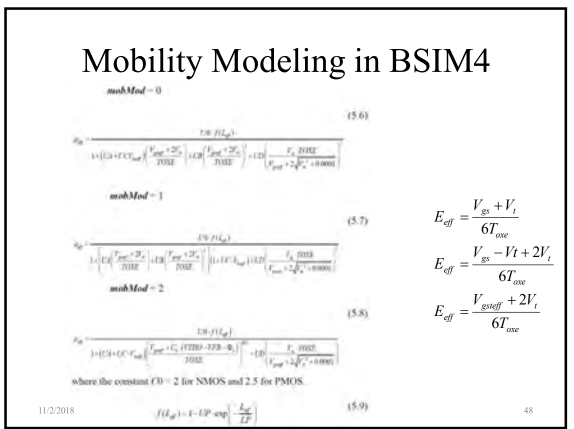
Therefore, $\mathbf{E}_b = \frac{C_{oxe}}{\varepsilon_s}(V_t - V_{fb} - \phi_{st})$

$$\mathbf{E}_t = -(Q_{dep} + Q_{inv})/\varepsilon_s$$
$$= \mathbf{E}_b - Q_{inv}/\varepsilon_s = \mathbf{E}_b + \frac{C_{oxe}}{\varepsilon_s}(V_{gs} - V_t)$$
$$= \frac{C_{oxe}}{\varepsilon_s}(V_{gs} - V_{fb} - \phi_{st})$$

$$\therefore \frac{1}{2}(\mathbf{E}_b + \mathbf{E}_t) = \frac{C_{oxe}}{2\varepsilon_s}(V_{gs} + V_t - 2V_{fb} - 2\phi_{st})$$
$$\approx \frac{C_{oxe}}{2\varepsilon_s}(V_{gs} + V_t + 0.2\ \mathrm{V})$$
$$= \frac{V_{gs} + V_t + 0.2\ \mathrm{V}}{6T_{oxe}}$$

NMOS with n+ poly-Si gate
V_{fb}≈-0.5 and ψ_{st}≈0.4





MOSFET Charges

- The total semiconductor charge for a p-type substrate is as given below

$$Q_c' = -\text{sgn}(\psi_S)\sqrt{2q\varepsilon_s N_A}\sqrt{\phi_t e^{-\psi_s/\phi_t} + \psi_s - \phi_t + e^{-(2\phi_f + V_{CB})/\phi_t}\left(\phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t\right)}$$

- According to charge balance, potential balance and the gate charge relation it must satisfy

$$Q_C'(\psi_S) = -C_{ox}'(V_{GB} - V_{FB} - \psi_S) \qquad V_{GB} = V_{FB} + \psi_S - \frac{Q_C'(\psi_S)}{C_{ox}'}$$

or

$$V_{GB} = V_{FB} + \psi_S + \text{sgn}(\psi_S)\gamma\sqrt{\phi_t e^{-\psi_s/\phi_t} + \psi_s - \phi_t + e^{-(2\phi_f + V_{CB})/\phi_t}\left(\phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t\right)}$$

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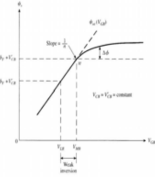
Source: Operation and Modeling of MOS Transistor by Y Tsividis

Accumulation and Depletion

- In accumulation, $\psi_s < 0$ by several ϕ_t

$$Q_c' \approx \sqrt{2q\varepsilon_s N_A \phi_t}\, e^{-\psi_s/2\phi_t}$$

- In depletion, $\psi_s > 0$ by several ϕ_t but less than φ_f



$$Q_c' \approx -\sqrt{2q\varepsilon_s N_A \psi_s} \quad \text{or,} \quad V_{GB} = V_{FB} + \psi_S + \gamma\sqrt{\psi_S}$$

or, $$\psi_s \approx \psi_{sa} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}}\right)^2$$

Defining $$n = \frac{1}{\left(\frac{d\psi_{sa}}{dV_{GB}}\right)}$$ we get $$n = 1 + \frac{\gamma}{2\sqrt{\varphi_{sa}(V_{GB})}}$$

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Inversion

- In inversion: $$Q_c' = -\sqrt{2q\varepsilon_s N_A}\sqrt{\psi_s + \left(\phi_t e^{[\psi_s - (2\phi_f + V_{CB})]/\phi_t}\right)}$$

Charge sheet approximation (inversion layer thickness is negligible) $$Q_B' = -\sqrt{2q\varepsilon_s N_A}\sqrt{\psi_s} = -\gamma C_{ox}'\sqrt{\psi_s}$$

Then, $$Q_I' = -\sqrt{2q\varepsilon_s N_A}\left(\sqrt{\psi_s + \phi_t e^{(\psi_s - (2\phi_f + V_{CB}))/\phi_t}} - \sqrt{\psi_s}\right)$$

- We can also write:

$$Q_I' + Q_B' = -C_{ox}'(V_{GB} - V_{FB} - \psi_S)$$
$$Q_I' = -C_{ox}'\left(V_{GB} - V_{FB} - \psi_S - \gamma\sqrt{\psi_S}\right)$$
$$V_{GB} = V_{FB} + \psi_S + \gamma\sqrt{\psi_s + \phi_t e^{[\psi_S - (2\phi_f + V_{CB})]/\phi_t}}$$

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Threshold Voltage

- In strong inversion, $\psi_s = \phi_0 + V_{CB}$ where $\phi_0 = 2\phi_f + (3-4)\phi_t$

$$Q_I' = -C_{ox}'\left(V_{GB} - V_{FB} - \psi_S - \gamma\sqrt{\psi_S}\right)$$
$$Q_I' = -C_{ox}'\left(V_{GB} - V_{CB} - V_{FB} - (\psi_S - V_{CB}) - \gamma\sqrt{\psi_S}\right)$$
$$Q_I' = -C_{ox}'(V_{GB} - V_{CB} - V_{TH}) \qquad Q_I' = -C_{ox}'(V_{GC} - V_{TH})$$

$$V_{TH} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0 + V_{CB}}$$
$$V_{TH} = V_{T0} + \gamma\left(\sqrt{\phi_0 + V_{CB}} - \sqrt{\phi_0}\right)$$

V_{T0} is V_{TH} at V_{CB}=0

$$V_{T0} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0}$$

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Weak inversion ($V_{GS} < V_{TH}$)

- We have $$Q_I' = -\sqrt{2q\varepsilon_s N_A}\left(\sqrt{\psi_s + \phi_t e^{(\psi_s - (2\phi_f + V_{CB}))/\phi_t}} - \sqrt{\psi_s}\right)$$

- Linearizing the square root, $\psi_s < 2\phi_f + V_{CB}$

$$Q_I' = -\sqrt{2q\varepsilon_s N_A}\sqrt{\psi_S}\left[\left(1 + \frac{1}{2}\frac{\phi_t}{\psi_S}e^{[\psi_S - (2\phi_f + V_{CB})]/\phi_t}\right) - 1\right]$$

$$Q_I' = -\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{\psi_S}}\left(\phi_t e^{[\psi_S - (2\phi_f + V_{CB})]/\phi_t}\right)$$

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Weak Inversion

- In weak inversion, $\psi_S = \psi_{sa}$,

$$\psi_{sa} \approx \psi_{sa} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}}\right)^2$$

$$Q_I' = -\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{\psi_{sa}}}\left(\phi_t e^{[\psi_{sa} - 2\phi_f]/\phi_t}\right) \cdot e^{-V_{CB}/\phi_t}$$

Dependent on V_{GB} only — Dependent on V_{CB} only

- Variation in $\sqrt{\psi_{sa}}$ is small compared to variation in $e^{\psi_{sa}}$ → Thus $\sqrt{\psi_{sa}} \approx \sqrt{\psi_{sa}}$ *at the onset of strong inversion*

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Weak Inversion

$$Q_i^{'} = -\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{2\phi_f + V_{CB}^{'}}}\left(\phi_t e^{\left[\psi_{sa}-(2\phi_f+V_{CB}^{'})\right]/\phi_t}\right)$$

- From figure, for linear part in weak inversion

$$\psi_{sa} - (2\phi_f + V_{CB}^{'}) \approx \frac{1}{n}(V_{GB} - V_{MB}) \approx \frac{1}{n}(V_{GC} - V_M)$$

$$Q_i^{'} = -\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{2\phi_f + V_{CB}^{'}}}\left(\phi_t e^{\frac{V_{GC}-V_M}{n\phi_t}}\right)$$

$\frac{1}{n}$ is slope and n is evaluated at point M

V_M can be considered at V_T for simple analysis.

Current in subthreshold region

- Subthreshold conduction
  - Transistor is in depletion
  - Surface potential is determined by the depletion under the gate, which is constant everywhere ($\psi_S \approx \psi_{sa}$).

$$I_{ds}(x) = \mu_{eff} W Q_i \frac{dV_{CB}}{dx}$$

Current in subthreshold region

- Integrating from source to drain,

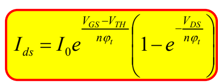
$$\int_0^L I_{ds}(x)dx = \int_0^L \mu_{eff} \cdot W \cdot Q_i \cdot dV_{CB}$$

$$I_{ds} = \mu_{eff}\frac{W}{L}\int_{V_{SB}}^{V_{DB}} Q_i \cdot dV_{CB}$$

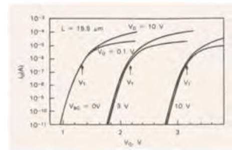
$$I_{ds} = \mu_{eff}\frac{W}{L}\int_{V_{SB}}^{V_{DB}}\left(\frac{\sqrt{2q\varepsilon_s N_A}}{2\sqrt{2\phi_f + V_{CB}^{'}}}\phi_t\left(e^{\frac{V_{GB}-V_{CB}-V_{TH}}{n\phi_t}}\right)\right)\cdot dV_{CB}$$

$$I_{ds} = I_0\left(e^{\frac{V_{GS}-V_{TH}}{n\varphi_t}} - e^{\frac{V_{GD}-V_{TH}}{n\varphi_t}}\right) \Rightarrow I_{ds} = I_0 e^{\frac{V_{GS}-V_{TH}}{n\varphi_t}}\left(1 - e^{-\frac{V_{DS}}{n\varphi_t}}\right)$$

Current in subthreshold region



$$I_{ds} = I_0 e^{\frac{V_{GS}-V_{TH}}{n\varphi_t}}\left(1 - e^{-\frac{V_{DS}}{n\varphi_t}}\right)$$



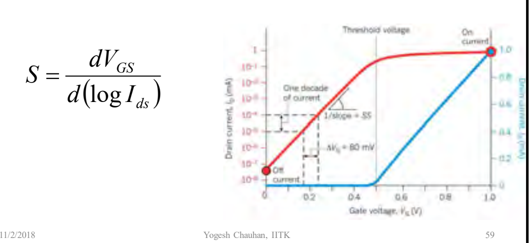
- Note – V_{TH} is a function of body bias.
  - If V_B increases in negative direction, V_{TH} increases.

$$V_{TH} = V_{T0} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right)$$

Subthreshold slope

- It is defined as the amount of gate voltage required to change the gate current by 1-decade.

$$S = \frac{dV_{GS}}{d(\log I_{ds})}$$



Subthreshold slope

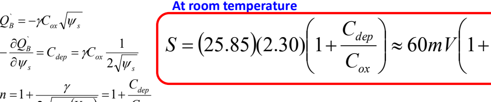
- For small V_{ds}, $I_{ds} \approx I_0 e^{\frac{V_{GS}-V_{TH}}{n\varphi_t}}$

$$V_{GS} - V_{TH} \approx n\varphi_t \cdot \ln\left(\frac{I_{ds}}{I_0}\right) = n\varphi_t \cdot \ln(10) \cdot \log\left(\frac{I_{ds}}{I_0}\right)$$

$$S = \frac{\partial V_{GS}}{\partial \log(I_{ds})} = n\varphi_t \cdot \ln(10) = 2.3 n\varphi_t$$

$$S = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{dep}}{C_{ox}}\right)$$

At room temperature



$$Q_B = -\gamma C_{ox}\sqrt{\psi_s}$$

$$-\frac{\partial Q_B}{\partial \psi_s} = C_{dep} = \gamma C_{ox}\frac{1}{2\sqrt{\psi_s}}$$

$$n = 1 + \frac{\gamma}{2\sqrt{\psi_{sa}(V_{GB})}} = 1 + \frac{C_{dep}}{C_{ox}}$$

$$S = (25.85)(2.30)\left(1 + \frac{C_{dep}}{C_{ox}}\right) \approx 60mV\left(1 + \frac{C_{dep}}{C_{ox}}\right)$$

Subthreshold slope

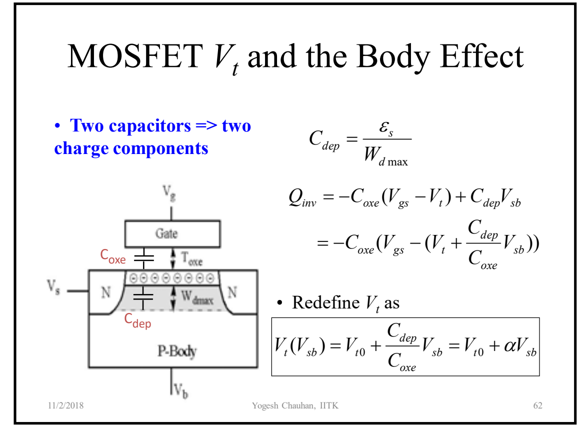
$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_{dep}}{C_{ox}}\right)$$

- Minimum value of S is 60mV/decade.
- I_{off} is determined by VTH and S
- If I_{ds} at V_{TH} is $100nA\frac{W}{L}$

$$I_{ds}(nA) = 100\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{nkT/q}} = 100\frac{W}{L}10^{\frac{V_{GS}-V_{TH}}{S}}$$

$$I_{off}(nA) = 100\frac{W}{L}10^{-\frac{V_{TH}}{S}}$$

- To minimize I_{off}
  - Increase V_{TH} – Not good as I_{ON} decreases (low speed!)
  - Reduce S
    - Increase Cox – Thin oxide
    - Decrease Cdep (Increase Wdep) – Use substrate bias or low doping
    - Decrease Temperature – cost?



MOSFET V_t and the Body Effect

- ***Body effect***: V_t is a function of V_{sb}. When the source-body junction is reverse-biased, $|V_t|$ increases.
- ***Body effect coefficient***:

$$V_t = V_{t0} + \alpha V_{sb}$$

$$\alpha = C_{dep}/C_{oxe} = 3T_{oxe}/W_{dep}$$

Body effect slows down circuits? How can it be reduced?

When multiple FETs are connected in series, they share a common body (the silicon substrate) but their sources do not have the same voltage. Clearly some transistors' source–body junctions are reversed biased. This raises their V_t and reduces I_{ds} and the circuit speed. Circuits therefore perform best when V_t is as insensitive to V_{sb} as possible, i.e., the body effect should be minimized. This can be accomplished by minimizing the $Tox/Wdmax$ ratio.

Threshold Voltage Modeling

- Halo Doping – Effective channel doping concentration gets higher, which changes the body bias effect as well.

$$V_{th} = VTH0 + K1\left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K2\cdot V_{bs} + K1\left(\sqrt{1+\frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_s}$$

Threshold Voltage Modeling

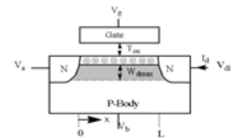
- Non-Uniform *Lateral* Doping or Pocket/Halo Implant: Doping concentration near the S/D junctions is higher than middle of channel.
  - V_{TH} increases as channel length gets shorter

Threshold Voltage Modeling

- The complete V_{th} model implemented in SPICE as

$$V_{th} = VTH0 + \left(K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K1\cdot\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{bseff}$$
$$+ K_{1ox}\left(\sqrt{1+\frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_s} + \left(K3 + K3B\cdot V_{bseff}\right)\frac{TOXE}{W_{eff}' + W0}\Phi_s$$
$$- 0.5\cdot\left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W_{eff}'}{l_{tw}}\right)-1} + \frac{DVT0}{\cosh\left(DVT1\frac{L_{eff}}{l_t}\right)-1}\right](V_{bi} - \Phi_s)$$
$$- \frac{0.5}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right)-1}\left(ETA0 + ETAB\cdot V_{bseff}\right)V_{ds} - nv_t\ln\left(\frac{L_{eff}}{L_{eff} + DVTP0\cdot(1+e^{-DVTP1\cdot V_{ds}})}\right)$$
$$-\left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP3}}\right)\cdot\tanh(DVTP4\cdot V_{ds})$$

Drain Current and Q_{inv} in MOSFET



- Channel voltage $V_c = V_s$ at $x = 0$ and $V_c = V_d$ at $x = L$.

$Q_I' = -C_{ox}'(V_{GC} - V_{TH}) = -C_{ox}'(V_{GC} - V_{t0} - \alpha V_{cb})$

- $Q_{inv} = -C_{ox}(V_{gs} - V_{cs} - V_{t0} - \alpha(V_{sb} + V_{cs})$
- $= -C_{ox}(V_{gs} - V_{cs} - (V_{t0} + \alpha V_{sb}) - \alpha V_{cs})$
- $Q_{inv} = -C_{ox}(V_{gs} - mV_{cs} - V_t)$
- m ≡ 1 + α = 1 + $3T_{oxe}/W_{dmax}$ ≈1.2
- m is called the body-effect factor or bulk-charge factor.

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Mobility and Drain Curent

$I_{ds} = WQ_{inv}v$

The drift velocity is related to electric field by a parameter called *mobility* as follows:

$v = \mu_{ns}E$

$I_{ds} = WQ_{inv}\mu_{ns}E$

$Q_{inv} = C_{ox}(V_{gs} - mV_{cs} - V_t)$

$E = dV_{cs}/dx$

V_{cs} = Channel voltage w.r.t. source

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Drain Current Calculation

Now,

$I_{ds} = WC_{oxe}(V_{gs} - mV_{cs} - V_t)\mu_{ns}dV_{cs}/dx$

Integrating the above equation over the channel length L, gives the current voltage relation as follows:

$$\int_0^L I_{ds}dx = WC_{oxe}\mu_{ns}\int_0^{V_{ds}}(V_{gs} - mV_{cs} - V_t)dV_{cs}$$

$$I_{ds}L = WC_{oxe}\mu_{ns}(V_{gs} - V_t - mV_{ds}/2)V_{ds}$$

$$I_{ds} = \mu_{ns}C_{oxe}\frac{W}{L}\left(V_{gs} - V_t - \frac{m}{2}V_{ds}\right)V_{ds}$$

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Drain Current Observations

$$I_{ds} = \mu_{ns}C_{oxe}\frac{W}{L}\left(V_{gs} - V_t - \frac{m}{2}V_{ds}\right)V_{ds}$$

- From drain current equation, we can be say:

$I_{ds}\,\alpha W$ — Drain current is proportional to channel width

$I_{ds}\,\alpha\,\mu_{ns}$ — Drain current is proportional to electron mobility

$I_{ds}\,\alpha\,\frac{V_{ds}}{L}$ — Drain current is proportional to average electric field in the channel

$I_{ds}\,\alpha\,C_{oxe}(V_{gs} - V_t - \frac{m}{2}V_{ds})$ — Drain current is proportional to average inversion charge in the channel

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Drain Current & V_{ds}

$$I_{ds} = \mu_{ns}C_{oxe}\frac{W}{L}\left(V_{gs} - V_t - \frac{m}{2}V_{ds}\right)V_{ds}$$

- If V_{ds} is small then $mV_{ds}/2$ term will be negligible in I_{ds}, and I_{ds} will become a linear function of V_{ds} as follows:

$$I_{ds}\,\alpha\,V_{ds}$$

- In this region of operation transistor behaves as a resistor.
- If V_{ds} is ↑ further, then the average inversion charge in the channel reduces as a result dI_{ds}/dV_{ds} decreases.
- The value of V_{ds} at the point when dI_{ds}/dV_{ds} becomes zero is the boundary condition for the linear region and the saturation region of operation.

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I-V characteristics

$$\frac{dI_{ds}}{dV_{ds}} = 0$$

$$\frac{W}{L}C_{oxe}\mu_{ns}(V_{gs} - V_t - mV_{dsat}) = 0$$

$$V_{dsat} = \frac{V_{gs} - V_t}{m}$$

Linear Region Saturation region

$V_{ds} < V_{dsat}$ → Linear Region

$V_{ds} \geq V_{dsat}$ → Saturation region

Drain current in saturation regi

$$I_{dsat} = \frac{W}{2mL}C_{oxe}\mu_{ns}(V_{gs} - V_t)^2$$

- transconductance: $g_m = dI_{ds}/dV_{gs}$ $g_{msat} = \frac{W}{mL}C_{oxe}\mu_{ns}(V_{gs} - V_t)$

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I-V characteristics

What happens at $V_{ds}=V_{dsat}$ & why I_{ds} remains constant beyond V_{dsat}

✓ At $V_{ds}=V_{dsat}$, Q_{inv} near the drain end of the channel becomes zero ! i.e. Pinch off.

$I_{ds} = WQ_{inv}\mu_{ns}E$ (Large E and and negligible Q_{inv})

✓ At $V_{ds} > V_{dsat}$, A very short region near the drain end where the $Q_{inv} = 0$, a very high electric field exist due to the drop of the additional $V_{ds} - V_{dsat}$.

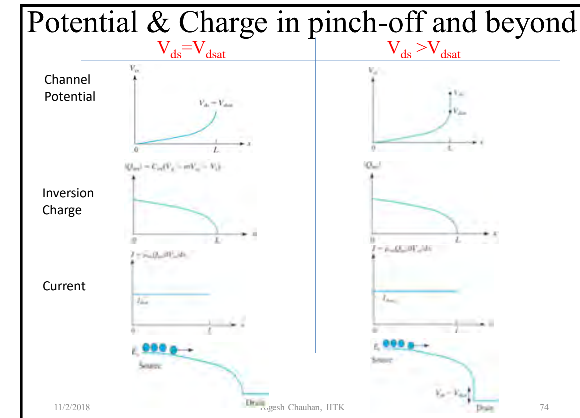
Potential & Charge in pinch-off and beyond

$V_{ds}=V_{dsat}$ | $V_{ds}>V_{dsat}$

Channel Potential

Inversion Charge

Current



How can a current flow through the pinch-off region (depletion region)?

- Depletion region does not stop current flow as long as there is a supply of the right carriers.
  - For example, in solar cells and photodiodes, current can flow through the depletion region of PN junctions.
- Similarly, when the electrons reach the pinch-off region of a MOSFET, they are swept down the steep potential drop in previous slide.
  - Therefore, the pinch-off region does not present a barrier to current flow.
- Furthermore, band bending in previous slide show that the electron flow rates (current) are equal in the two cases because they have the same drift field and Q_{inv} in the channel.
- In other words, the current is independent of V_{ds} beyond V_{dsat}.
  - The situation is like a mountain stream feeding into a waterfall. The slope of the river bed (dE_c/dx) and the amount of water in the stream determine the water flow rate in the stream, which in turn determines the flow rate down the waterfall. The height of the waterfall ($Vds - Vdsat$), whether 1 or 100 m, has no influence over the flow rate.

Channel Voltage profile

$$\int_0^x I_{DS}\,dx = WC_{ox}\mu\int_0^{V_{CS}}(V_{gs}-mV_{CS}-Vt)dV_{cs}$$

- or

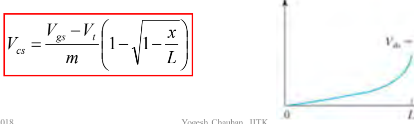
$$I_{DS}x = WC_{ox}\mu(VgsVcs - \frac{m}{2}V_{CS}^2 - VtVcs)$$

- When $I_{ds}=I_{dsat}$,

$$\frac{W}{2mL}C_{ox}\mu(Vgs-Vt)^2 = \frac{WC_{ox}\mu}{x}(VgsVcs - \frac{m}{2}V_{CS}^2 - VtVcs)$$

- Solving this

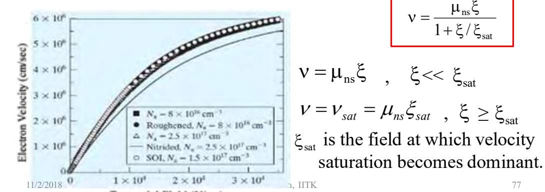
$$V_{cs} = \frac{V_{gs}-V_t}{m}\left(1-\sqrt{1-\frac{x}{L}}\right)$$



Velocity Saturation

- At low E → $v = \mu_{ns}E$
- The inversion-layer electron velocity saturates at high field regardless of the body doping concentration and surface treatment

$$v = \frac{\mu_{ns}\xi}{1+\xi/\xi_{sat}}$$



$v = \mu_{ns}\xi$, $\xi << \xi_{sat}$

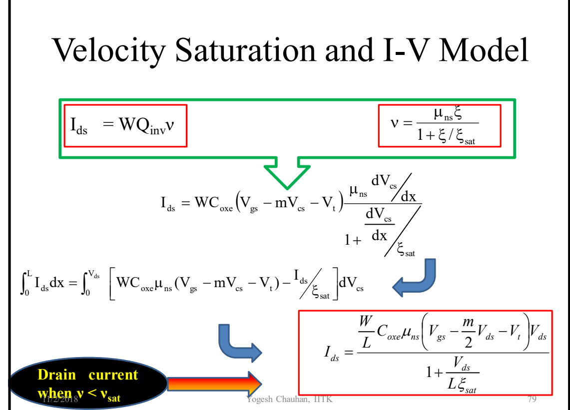
$v = v_{sat} = \mu_{ns}\xi_{sat}$, $\xi \geq \xi_{sat}$

ξ_{sat} is the field at which velocity saturation becomes dominant.

I-V Model with Velocity Saturation

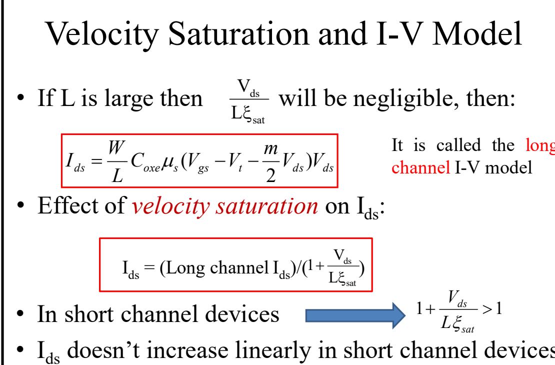
- A major weakness of the basic MOSFET IV model is that a finite current flows through the pinch-off region, where $Q_{inv} = 0$.
- This requires the carrier velocity to be infinite, a physical impossibility. We will now remove this shortcoming.

Velocity Saturation and I-V Model



Velocity Saturation and I-V Model

- If L is large then $\frac{V_{ds}}{L\xi_{sat}}$ will be negligible, then:

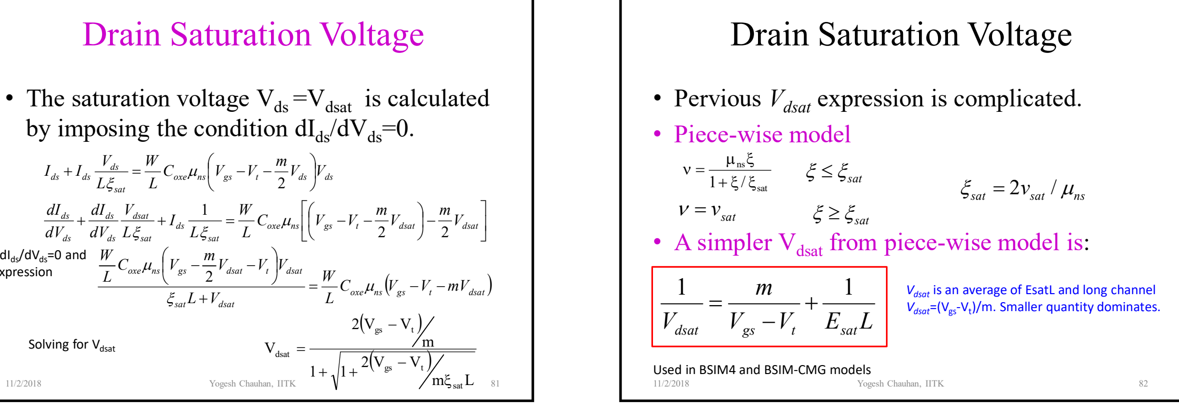


It is called the long channel I-V model

- Effect of *velocity saturation* on I_{ds}:
- In short channel devices
- I_{ds} doesn't increase linearly in short channel devices

Drain Saturation Voltage

- The saturation voltage $V_{ds}=V_{dsat}$ is calculated by imposing the condition $dI_{ds}/dV_{ds}=0$.



Drain Saturation Voltage

- Pervious V_{dsat} expression is complicated.
- Piece-wise model
- A simpler V_{dsat} from piece-wise model is:

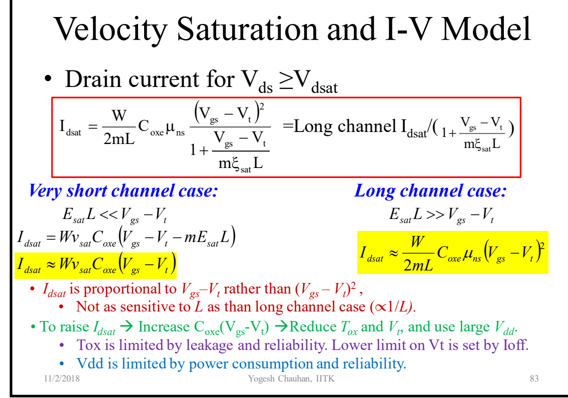
$$\frac{1}{V_{dsat}} = \frac{m}{V_{gs} - V_t} + \frac{1}{E_{sat}L}$$

V_{dsat} is an average of EsatL and long channel V_{dsat}=(V_{gs}-V_t)/m. Smaller quantity dominates.

Used in BSIM4 and BSIM-CMG models

Velocity Saturation and I-V Model

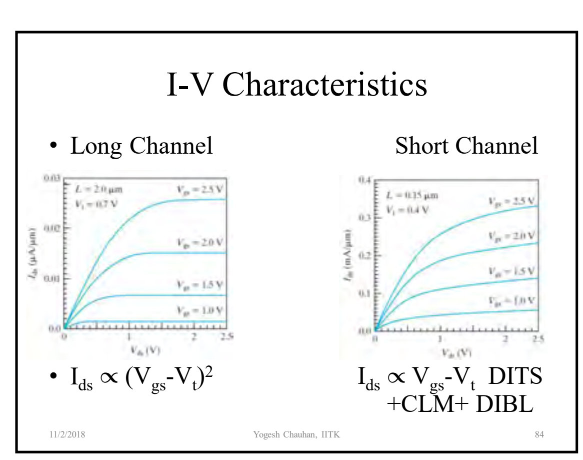
- Drain current for $V_{ds} \ge V_{dsat}$



- I_{dsat} is proportional to $V_{gs}-V_t$ rather than $(V_{gs}-V_t)^2$,
  - Not as sensitive to L as than long channel case ($\propto 1/L$).
- To raise I_{dsat} → Increase $C_{oxe}(V_{gs}-V_t)$ →Reduce T_{ox} and V_t, and use large V_{dd}.
  - Tox is limited by leakage and reliability. Lower limit on Vt is set by Ioff.
  - Vdd is limited by power consumption and reliability.

I-V Characteristics

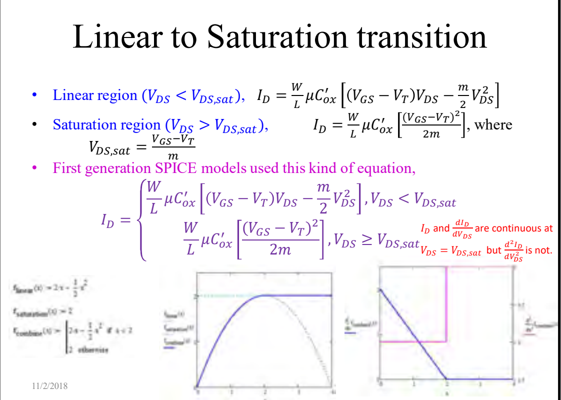
- Long Channel — Short Channel



- $I_{ds} \propto (V_{gs}-V_t)^2$ — $I_{ds} \propto V_{gs}-V_t$ DITS +CLM+ DIBL

Smoothing function and I-V Model

- Smoothing function is required for a smooth transition between two functions.
  - This stems from the need to have a single equation valid in all regions of operation.
- BSIM3 introduced use of smoothing functions to get single equation valid in all regions of biases.
  - This gave continuous and smooth I-V and C-V making it popular model for analog design.



Linear to Saturation transition

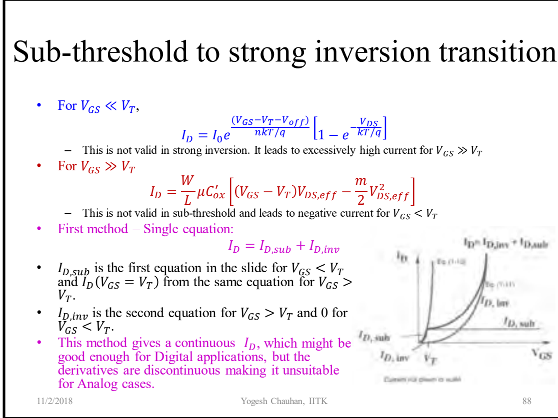
- For numerical robustness, the derivatives of arbitrary order must be continuous at all voltage values of interest. This property is sometimes referred to as ∞-differentiability.
- **Single equation approach used in BSIM3**. Define an effective drain-source bias V_{DSeff},

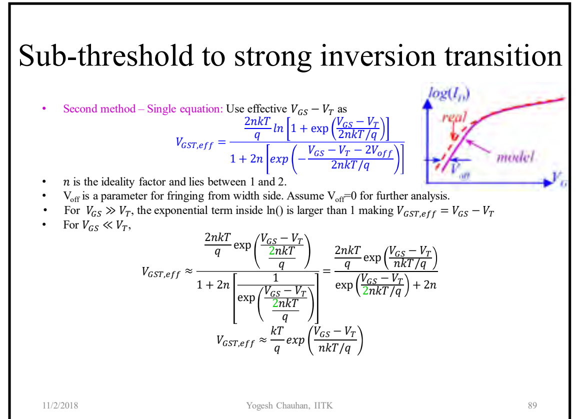
$$V_{DS,eff} = V_{DS,sat} - \frac{1}{2}\left(V_{DS,sat} - V_{DS} - \Delta + \sqrt{(V_{DS,sat} - V_{DS} - \Delta)^2 + 4\Delta V_{DS,sat}}\right)$$

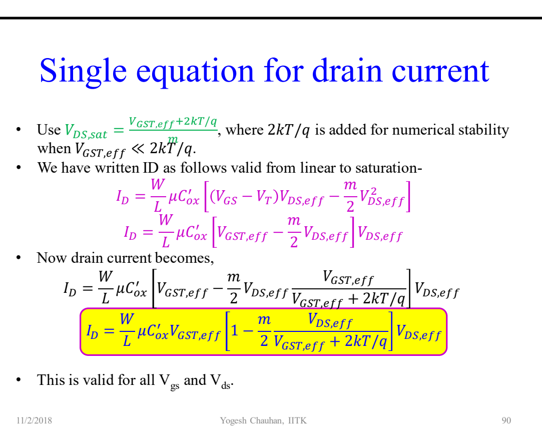
- $V_{DS} \ll V_{DS,sat}$, $V_{DS,eff} \approx V_{DS}$
- For $V_{DS} \gg V_{DS,sat}$, $V_{DS,eff} \approx V_{DS,sat}$
- Drain current equation becomes ($V_{GS} > V_T$),
- $I_D = \frac{W}{L}\mu C'_{ox}\left[(V_{GS}-V_T)V_{DS,eff} - \frac{m}{2}V_{DS,eff}^2\right]$
- Derivatives are continuous.

Increasing Δ

Δ determines the degree of smoothness.







Regional analysis of single I-V equation

- Remember $V_{DS,sat} = \frac{V_{GST,eff}+2kT/q}{m}$ and $I_D = \frac{W}{L}\mu C'_{ox} V_{GST,eff}\left[1 - \frac{m}{2}\frac{V_{DS,eff}}{V_{GST,eff}+2kT/q}\right]V_{DS,eff}$
- **For $V_{GS} \ll V_T$ and $V_{DS} \ll V_{DS,sat}$** → $V_{GST,eff} \ll \frac{2kT}{q}$,

$$I_D \approx \mu \frac{W}{L} C'_{ox}\left(V_{GST,eff}\right)\left(V_{DS,eff}\right) = \mu \frac{W}{L} C'_{ox} \frac{kT}{q} e^{\frac{(V_{GS}-V_T)}{nkT/q}}\left(V_{DS,eff}\right)$$

- **For $V_{GS} \ll V_T$ and $V_{DS} \gg V_{DS,sat}$** → $V_{GST,eff} \ll \frac{2kT}{q}$ and $V_{DS} = V_{DS,sat} \approx \frac{2kT/q}{m}$,

$$I_D \approx \mu \frac{W}{L} C'_{ox}\left(V_{GST,eff}\right)\left(V_{DS,sat}\right) = \mu \frac{W}{L} C'_{ox} 2\left(\frac{kT}{q}\right)^2 e^{\frac{(V_{GS}-V_T)}{nkT/q}}$$

- **For $V_{GS} \gg V_T$** → $V_{GST,eff} \gg \frac{2kT}{q}$,

$$I_D \approx \mu \frac{W}{L} C'_{ox}\left(V_{GST,eff} - \frac{m}{2} V_{DS,eff}\right) V_{DS,eff}$$

- Compare these results from previous results.

References and Recommended Reading

- "MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4" by William Liu
- Modern Semiconductor Devices for Integrated Circuits by Chenming C. Hu
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- Andrei Vladimirescu, "The SPICE BOOK", Wiley
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- Ron Kielkowski, "Inside SPICE, overcoming the obstacles of circuit simulation", McGraw-Hill Inc.
- Muhammad H. Rashid, "SPICE for circuits and electronics using PSpice", Prentice Hall
- Compact Modeling: Principles, Techniques and Applications by Gennady Gildenblat
- Compact MOSFET Models for VLSI Design by A. B. Bhattacharyya
- BSIM4 and MOSFET Modeling for IC Simulation by W. Liu and Chenming Hu