Physics and Modeling of Nano-Transistors

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Outline

- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET
- ASM-GaN-HEMT Model

My Group and Nanolab

Current members – 35
- Postdoc – 4
- Ph.D. – 19
- Ten PhD graduated

	2020	2019	2018	2017	2016
Books		1			1
Journal	9	14	20	19	18
Conference	8	15	19	11	30

Device Characterization Lab
- Pulsed IV/RF
- PNA-X 43.5GHz
- High Power IV
- Load Pull

Alumni (PhD) of Nanolab

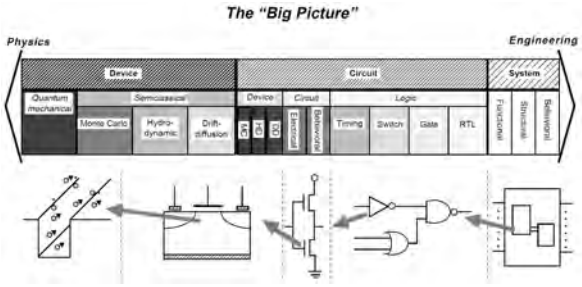
S. No.	Year	Name	Current Status
10.	2020	Girish Pahwa	Postdoc at UC Berkeley
9.	2020	Shantanu Agnihotri	Asst. Prof. at PEC Chandigarh
8.	2020	Chetan Gupta	Micron Hyderabad
7.	2018	Priyank Rastogi	Intel Bangalore
6.	2018	Prateek Jain	Postdoc at IIT Bombay
5.	2018	Avirup Dasgupta	Postdoc at UC Berkeley
4.	2017	Sheikh Aamir Ahsan	Asst. Prof. at NIT Srinagar
3.	2017	Chandan Yadav	Asst. Prof. at NIT Calicut
2.	2017	Harshit Agarwal	Asst. Prof. at IIT Jodhpur
1.	2017	Pragya Kushwaha	SAC, ISRO

Compact Modeling – Industrial Research

- Bulk MOSFET Modeling (DC to RF)
  - BSIM4 and BSIM6
- Partially Depleted SOI MOSFET Modeling (DC to RF)
  - BSIM-SOI
- Multigate MOSFET Modeling
  - FinFET & Nanowire Transistor – BSIM-CMG
  - Fully Depleted SOI (FDSOI) Transistor– BSIM-IMG
- High Voltage LDMOS Modeling using BSIM6 – BSIM-HV
- GaN HEMT Modeling
  - ASM-HEMT: industry standard
- DC, CV and RF Characterization
  - All models are validated on measured data
- Working as BSIM Group member/consultant

Joint Development & Collaboration

Spectrum of Approaches to Analyzing Electronic System



Source: Xing Zhou, NTU

Circuit simulation

- Circuit simulation is an important part of any design process.
- Explosive growth of integrated circuit market in the 1970's resulted in the rise of importance of circuit simulation.
  - With integrated circuits, prototypes were expensive to build and difficult to troubleshoot.
  - As designs became larger and more complicated, the need to use circuit simulators increased.
- Time to market and cost.

SPICE Simulation

- SPICE (*Simulation Program with Integrated Circuits Emphasis*) is a powerful general purpose *circuit simulation* program that is used to verify circuit designs and to predict the circuit behavior.
- SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley in early part of 1970.
- SPICE can do several types of circuit analyses.
  - Non-linear DC / Transient analysis, Linear AC Analysis
  - Noise analysis, Sensitivity analysis, Distortion analysis

SPICE Development

- SPICE was developed out of a graduate *class project* at University of California, Berkeley


Laurence W. Nagel


Ronald A. Rohrer


Donald O. Pederson

L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis), " Memorandum No. ERL-M382, University of California, Berkeley, Apr. 1973.
http://www.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html

SPICE and Device Models

nodal admittance matrix would be ... tion and its negative side effec

> ***Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.***

adequate as pivot choices in effect- ... the engineering intuition of ci ... ing its factorization into lower and ... designers.

Ron Rohrer

Special Issue on 40th Anniversary of SPICE

SPRING 2011 IEEE SOLID-STATE CIRCUITS MAGAZINE

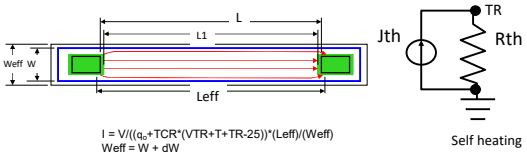
Model Types

- Look Up Table – Store measured or simulated data in a table.
- Physical model generally does not have parameters but does not fit with data accurately.
- Empirical models are mathematical models written to reflect measured characteristics
  - Angelov model for HEMT
- Compact SPICE models are the physics based model but parametrized to fit measured data.

What is a Compact Model?

Compact model complexity: What's so hard about fitting Curves?

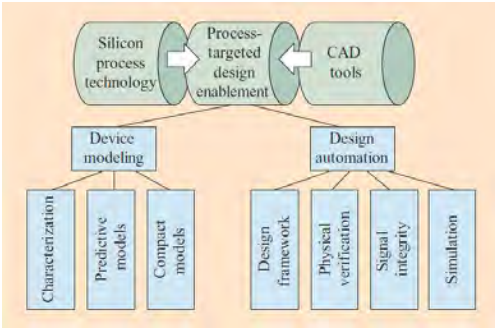
I = V/R is a compact model for a resistor



I = V/((q$_0$+TCR*(VTR+T+TR-25))*(Leff)/(Weff)
Weff = W + dW
Leff = L + dL
Jth = V*I
Rth=Rth0/(Leff*Weff) + Rth1/(Leff+Weff) + Rth2
Add: Geometric Scaling
Temperature Scaling
Self Heating

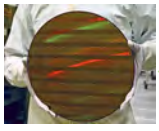
PDK and Compact Model

Enablers of a silicon chip design



Source: David HARAME et. al., IBM J. RES. & DEV. MARCH/MAY 2003

Compact Modeling or SPICE Modeling



Medium of information exchange

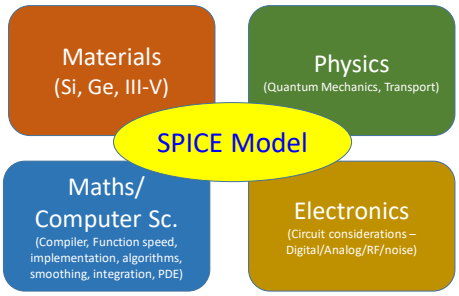
- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~μsec
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM-BULK, BSIM-CMG, BSIM-IMG

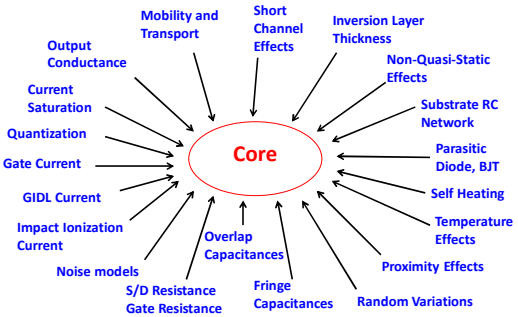
Industry Standard Compact Models

- Standardization Body – Compact Model Coalition
- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

Challenges in Compact Modeling

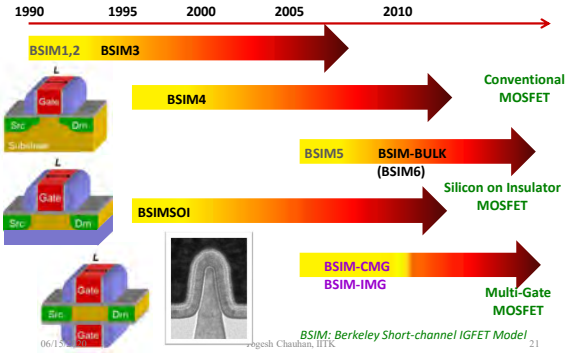


Compact Model is Art Based on Science



Y. S. Chauhan et.al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET," IEEE TED, 2014.

BSIM Family of Compact Device Models



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Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$$

- Drain current in MOSFET (OFF operation)

$$I_{OFF} \propto 10^{\left(\frac{V_{GS}-V_{TH}}{S}\right)}$$

$C_{ox}=\varepsilon_{ox}/t_{ox}$=oxide cap.
S – Subthreshold slope

- Desired
  - High I_{ON} (↓L, ↑Cox, ↑V_{DD}-V_{TH})
  - Low I_{OFF} (↑V_{TH}, ↑S)

Technology Scaling

- Each time the minimum line width is reduced, we say that a new ***technology node*** is introduced.
- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.

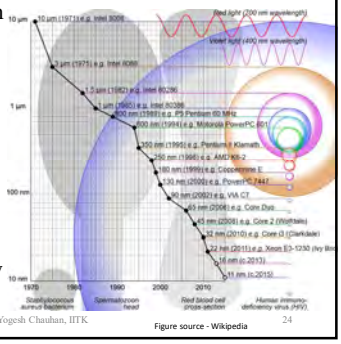
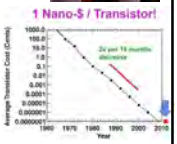


Figure source - Wikipedia

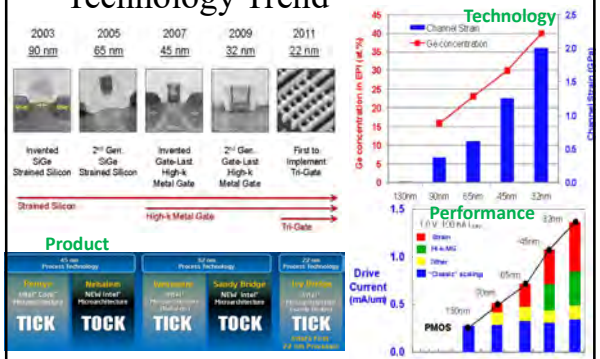
IC industry for >40 years

- Closer distance between elements – *Pitch*
  - *Faster* signal transfer and processing rate
- For the same Chip size (or cost), *more functionality*
- *Mass production* – Wafer size doubled every 10years.
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - *Price* of memory/logic gates has dropped 100 million times.
- The primary engine that powered the proliferation of electronics is "*miniaturization*".
- More circuits on each wafer → cheaper circuits.
- Miniaturization is key to the improvements in *speed and power consumption* of ICs.



It's not technology! → It's economy.

Technology Trend



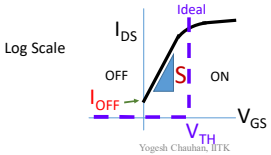
Source : www.intel.com

Wasn't that smooth ride?

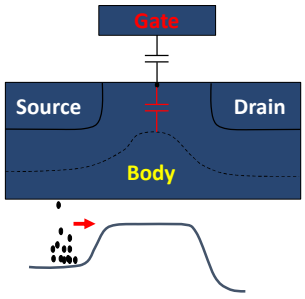
- Where is the bottleneck?

$$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$$

- V_{TH} and Subthreshold Slope can't be decreased

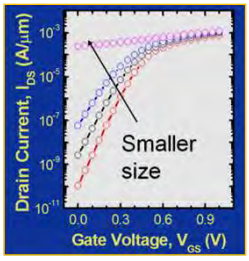


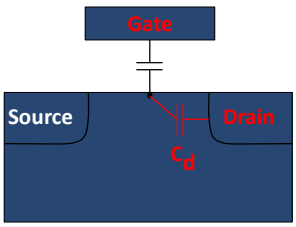
Thin Depletion Layer - Problem



- $Q_G = Q_i + Q_b$
- Charge sharing

Short Channel – Big Problem

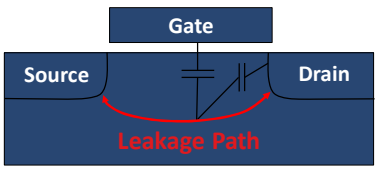




MOSFET becomes "resistor" at small L.

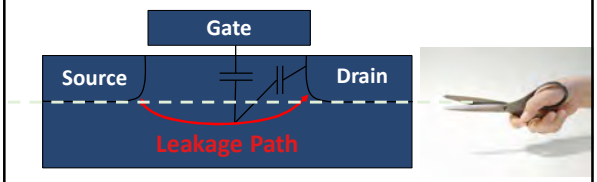
Chenming Hu, "Modern Semiconductor Devices for ICs" 2010, Pearson

Making Oxide Thin is Not Enough



Gate cannot control the leakage current paths that are far from the gate.

What can we do?



MOSFET in sub-22nm era

FinFET FDSOI

New Transistor Grows in the Third Dimension

Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices

New platform enables planar FD technology, the only planar solution to sustain Moore's law

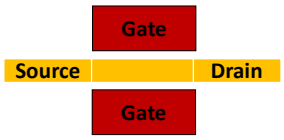
From the Semicon West trade show, San Francisco, July 12, 2010 – The Soitec Group (Euronext Paris), the world's leading supplier of engineered substrates for the microelectronics industry, announced today that the company is ready with the Ultra-Thin Buried Oxide (UTBOX) extension to its Ultra-Thin (UT) silicon-on-insulator (SOI) platform, thereby providing a robust substrate solution for chip designers tackling the performance, power and density challenges of mobile consumer devices. Fully Depleted (FD) planar body transistors are now recognized as the right path on the CMOS roadmap for the 22nm generation and beyond. With FD planar transistor technology on UTBOX wafers, chip designers can enhance their usual design flows and techniques. High-volume capacity is available for the 22nm node at Soitec's manufacturing sites in France and Singapore.

"Soitec is ready with the UTBOX wafers for planar FD architectures: the infrastructure, the process maturity, yield and the capacity are all in place to support demand," said Soitec president and chairman, André-Jacques Auberton-Hervé. "Industry leaders confirm that FD planar technology is the right choice for mobile consumer products, which need higher performance without compromising power. Our UTBOX offering shows the critical role our materials play as the starting point for energy-efficient, state-of-the-art electronics."

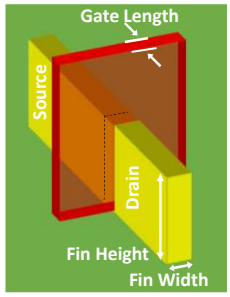
NY Times SOITEC

One Way to Eliminate Si Far from Gate

Thin body controlled
By multiple gates.



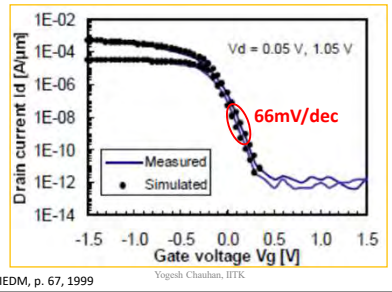
FinFET body is a thin Fin.



N. Lindert et al., DRC paper II.A.6, 2001

40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.

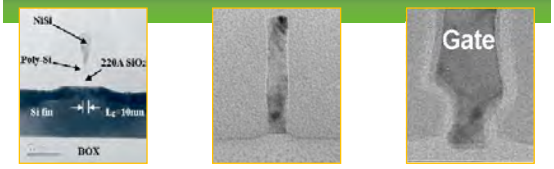


X. Huang et al., IEDM, p. 67, 1999

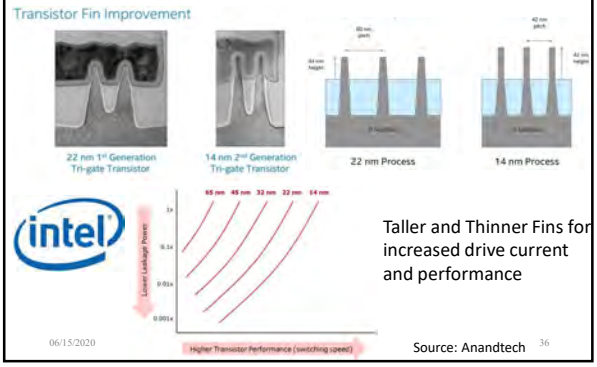
Introduced New Scaling Rule

Leakage is well suppressed if
Fin thickness < Lg

10nm Lg AMD 2002 IEDM	5nm Lg TSMC 2004 VLSI	3nm Lg KAIST 2006 VLSI



State-of-the-Art 14nm FinFET

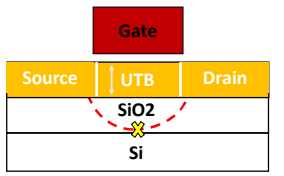


Taller and Thinner Fins for increased drive current and performance

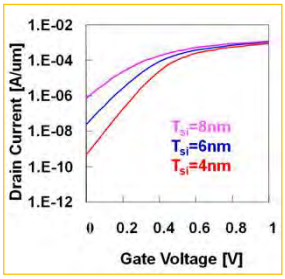
Source: Anandtech

2nd Way to Eliminate Si far from Gate

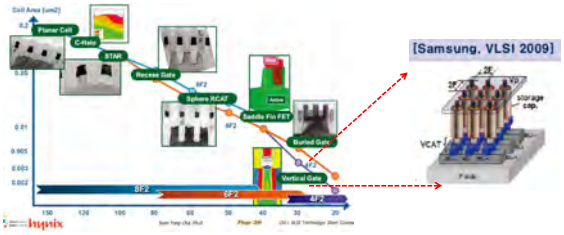
Ultra-thin-body SOI (UTB-SOI)



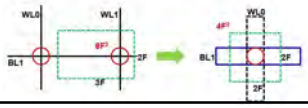
Y-K. Choi, IEEE EDL, p. 254, 2000



Another MOSFET architecture – Gate-All-Around or Surround Gate



- DRAM Cell Transistor – $4F^2$ layout



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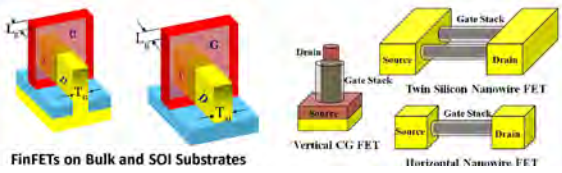
BSIM-CMG and BSIM-IMG

- **Berkeley Short-channel IGFET Model**
- **First industry standard SPICE model for IC simulation**
- **Used by hundreds of companies for IC design since 1997**
- **BSIM FinFET model became industry standard in March 2012**

It's Free

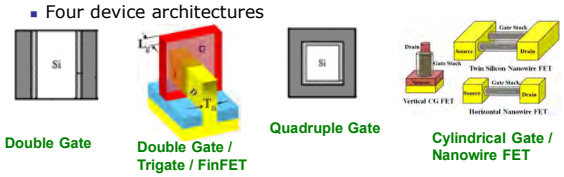
BSIM-CMG: Industry standard FinFET model

- Selected as Industry standard 2012



BSIM-CMG Core Models

- Four device architectures



- Three core models
  - Intrinsic Double Gate Core (*Y. Taur et al, IEEE EDL, 2004*)
  - Perturbation based DG Core for high-doping
  - Cylindrical Gate Core
- Bulk and SOI Substrate

Short Channel (2D) Effects

$$\frac{1}{r}\cdot\frac{\partial}{\partial r}\left(r\frac{\partial\psi}{\partial r}\right)+\frac{\partial^2}{\partial y^2}\psi=\frac{qN_a}{\varepsilon_{si}}$$

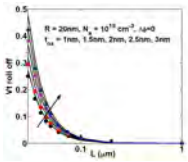
- Along the channel – 2D
- Quasi-2D analysis

$$\frac{d^2\psi_c}{dy^2}+\frac{V_{gs}-V_{fb}-\psi_c}{\lambda^2}=\frac{qN_a}{\varepsilon_{si}}$$

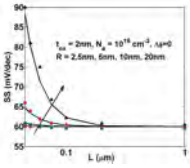
Characteristic Length

$$\lambda=\sqrt{\left(\frac{R^2}{4}+\frac{\varepsilon_{si}}{2\varepsilon_{ox}}R\cdot EOT\right)}$$

- Similar expression for Double Gate and FinFET/Trigate
- Analytical expressions model
  - Threshold Voltage roll off
  - Drain induced barrier lowering (DIBL)
  - Sub-threshold swing degradation



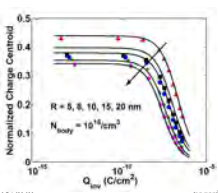
Symbols: TCAD Results; Lines: Model

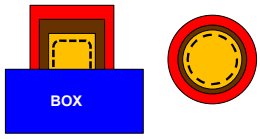


Auth and Plummer, IEEE EDL, 2007

Quantum Mechanical Effects

- Predictive model for confinement induced V_{th} shift due to band splitting present in the model
- Can choose to use an effective t_{ox} that accounts for charge centroid behavior with bias
- Effective Width model that accounts for reduction in width for a triple / quadruple / surround gate structure





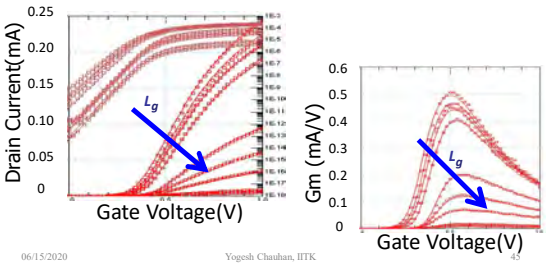
Width reduction due to structural confinement of inversion charge. (Dotted lines represent the effective width perimeter)

S. Venugopalan et. al., IEEE TED, 2013

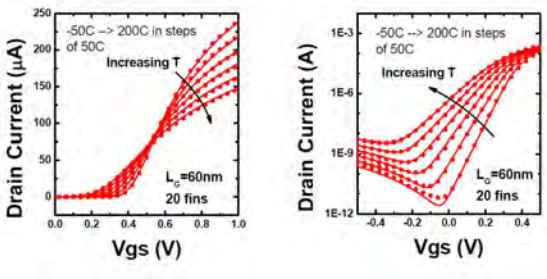
Verification: 30nm to 10μm FinFETs

Each curve is for one Lg

Symbols: Data; Lines: BSIM-CMG Model

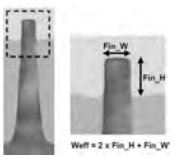


Temperature Model verified for FinFET

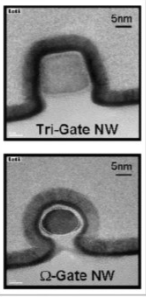


FinFET's Various Complex Cross-Sections

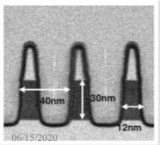
TSMC, IEDM 2010



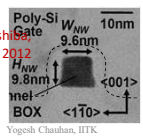
Leti, VLSI 2012



IBM, VLSI 2012



Toshiba, VLSI 2012

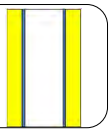


Prior Models Available for Two Simple Cross-Sections Only – Deductive model

1. Double-Gate FinFET:

Charge Equation :

$$V_G-V_{FB}+\frac{t_{ox}}{2\varepsilon_{ox}}Q_d-V=-\frac{t_{ox}}{2\varepsilon_{ox}}Q_c+v_T\ln\frac{Q_c(Q_c+Q_d)/(4v_T\varepsilon_{si}/W_{si})}{q\frac{n_i^2}{N_{ch}}W_{si}\left[1-\exp\frac{W_{si}}{4v_T\varepsilon_{si}}(Q_c+Q_d)\right]}$$



2. Cylindrical FinFET:

Charge Equation:

$$V_G-V_{FB}+\frac{\ln(1+t_{ox}/R)}{2\pi\varepsilon_{ox}}Q_{d,Cyl}-V=-\frac{\ln(1+t_{ox}/R)}{2\pi\varepsilon_{ox}}Q_{c,Cyl}+v_T\ln\frac{-Q_{c,Cyl}}{q\frac{n_i^2}{N_{ch}}\pi v_T R^2}+v_T\ln\frac{-(Q_{d,Cyl}+Q_{c,Cyl})/4\varepsilon_{si}\pi}{1-\exp\frac{Q_{d,Cyl}+Q_{c,Cyl}}{4\varepsilon_{si}\pi v_T}}$$

New Unified Model for Complex FinFET Cross-Sections – Inductive model

$$v_G - v_O - v_{CH} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{-q_t} - q_t - 1}\right)$$

$$v_O = v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{v_t C_{ins} N_{ch}}\right) \qquad q_t = (q_m + q_{dep})\frac{A_{ch} C_{ins}}{\varepsilon_{ch} W^2}$$

Model Parameters:

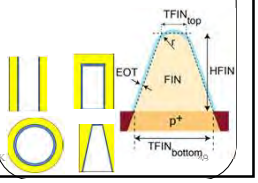
Fin Area: A_{ch}

Channel Doping: N_{ch}

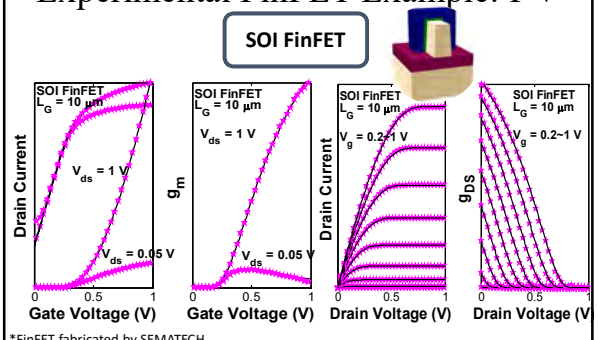
Channel Width: W

Insulator Cap: C_{ins}

Unified Model for **various Fin shapes**



Experimental FinFET Example: I-V



*FinFET fabricated by SEMATECH

3D Model for Short Channel Effects

- SCEs are 3-D effects
  - Need to solve the 3-D Poisson's equation. $\nabla^2\psi(x,y,x) = -\frac{qN_{ch}}{\varepsilon_{ch}}$
- **DIBL Equations:** $\Delta V_{TH} = f(\vec{V},\lambda) \quad SS = g(\vec{V},\lambda)$

λ: characteristic field penetration length

$$\lambda_{DG} \approx \sqrt{\frac{\varepsilon_{ch} T_{ch} t_{ins}}{\varepsilon_{ins}}}$$

K. Suzuki, EDL 1996

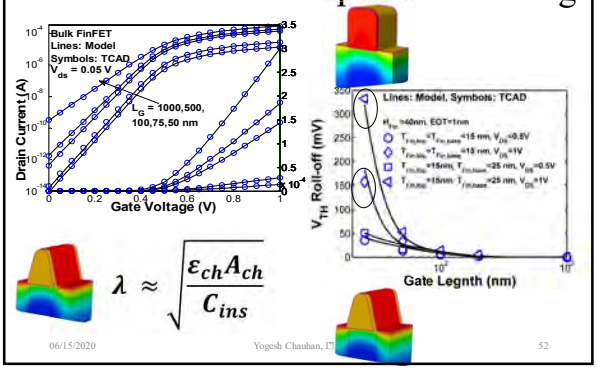
$$\lambda_{CyG} \approx \sqrt{\frac{2\varepsilon_{ch} R^2 ln\left(1 + \frac{t_{ins}}{R}\right)}{\varepsilon_{ins}}}$$

C. P. Auth, EDL 1997

Unified λ

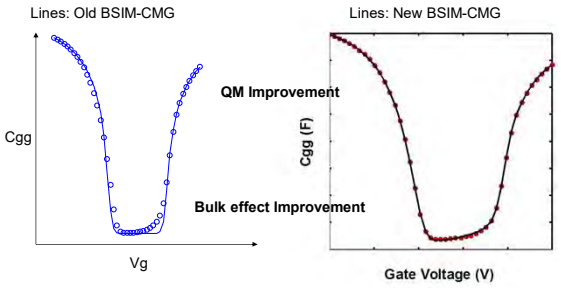
$$\lambda \approx \sqrt{\frac{\varepsilon_{ch} A_{ch}}{C_{ins}}}$$

TCAD FinFET Example: I-V: Scaling



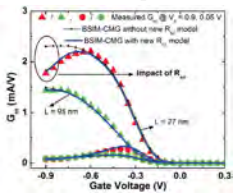
$$\lambda \approx \sqrt{\frac{\varepsilon_{ch} A_{ch}}{C_{ins}}}$$

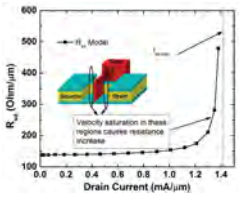
Experimental FinFET on Bulk Example: New QM Effects + Body Bias model



Modeling SiGe FinFETs with Thin Fin

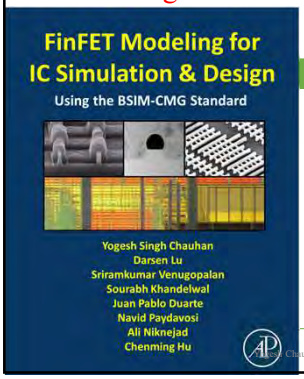
- Current Dependent Source/Drain Resistance





S. Khandelwal et. al., IEEE Electron Device Letters.

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

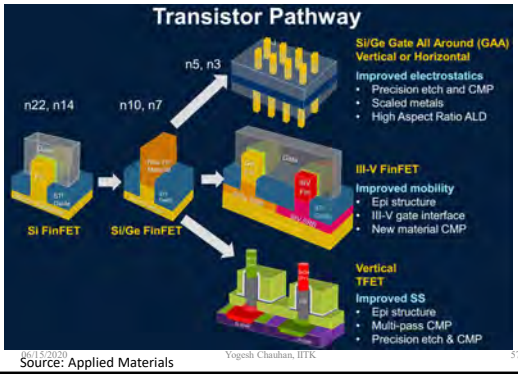
Available online on Elsevier.

Industry Standard FDSOI Compact Model BSIM-IMG for IC Design

Chapters

1. Fully Depleted Silicon on Oxide Transistor and Compact Model
2. Core Model for Independent Multigate MOSFETs
3. Channel Current Model With Real Device Effects in BSIM-IMG
4. Leakage Current and Thermal Effects
5. Model for Terminal Charges and Capacitances in BSIM-IMG
6. Parameter Extraction With BSIM-IMG Compact Model
7. Testing BSIM-IMG Model Quality
8. High-Frequency and Noise Models in BSIM-IMG

Future – 10nm and beyond



Source: Applied Materials

Key points for 10nm and beyond

- Reduced leakage – Better sub-threshold slope
  - Ultra-thin channel
  - Electrostatic control → Nanosheet transistors
- Higher mobility channel
  - Si NMOS and PMOS
  - Ge PMOS
  - SiGe
  - III-V materials NMOS – InAs, InGaAs etc.?

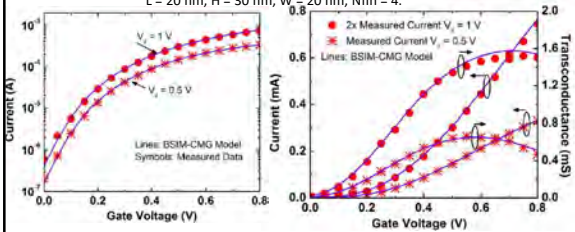
$$I_{off}(nA) = 100\frac{W}{L}10^{-\frac{V_{TH}}{S}}$$

$$I_{dsat} = \frac{W}{2L}C_{ox}\mu_{eff}(V_{gs} - V_t)^2$$

InGaAs FinFET Modeling

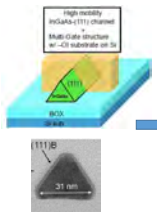
- BSIM-CMG with the **new Quantum Effects model** used to model InGaAs FinFETs

L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.

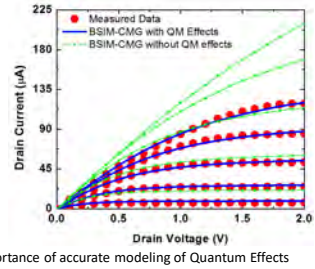


S. Khandelwal, J. P. Duarte, N. Paydavosi, Y. S. Chauhan, J. J. Gu, M. Si, P. D. Ye, and C. Hu, "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Workshop on Compact Modeling, 2014.

InGaAs FinFETs with Triangular Cross-section

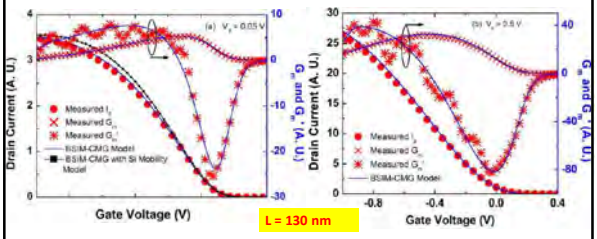


T. Irisawa et al. IEDM 2013



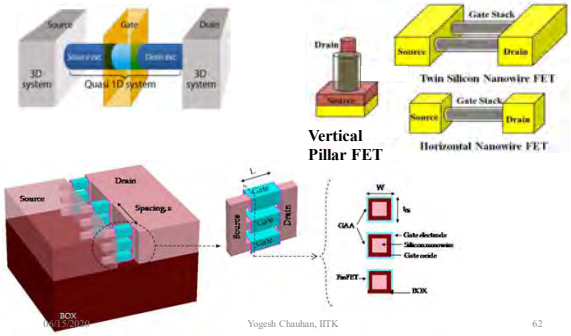
Importance of accurate modeling of Quantum Effects

BSIM-CMG Model Results for Ge pFinFETs



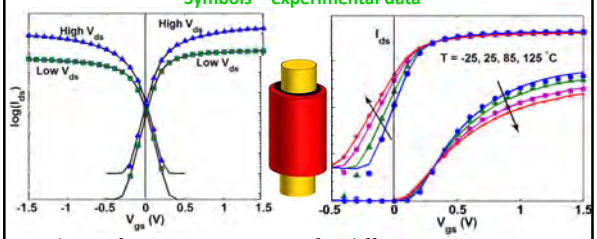
S. Khandelwal et. al., "Modeling 20nm Germanium FinFET with the Industry Standard FinFET Model", IEEE Electron Device Letters, Vol. 35, Issue 7, July 2014.

Modeling of GAA Nanowire FET



Validation on Asymmetric Nanowire FET

Symbols – experimental data



Ids-Vgs for N-type Nanowire for different temperatures

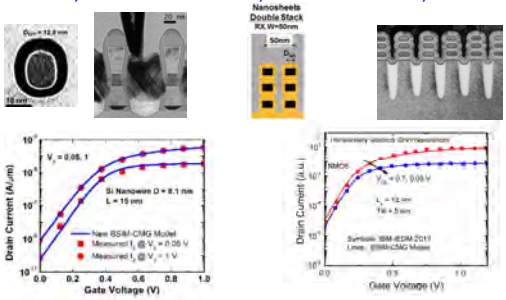
S. Venugopalan et. al., "Modeling Intrinsic and Extrinsic Asymmetry of 3D Cylindrical Gate/ Gate-All-Around FETs for Circuit Simulations", IEEE Non-Volatile Memory Technology Symposium, Shanghai, China, Nov. 2011.

Nanosheet Transistor

Modeling of Gate-All-Around FETs

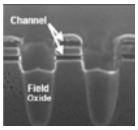
IBM, Nanowire, IEDM 2013

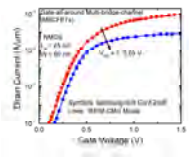
IBM, Stacked Nanosheet, VLSIT 2017



Samsung Multibridge & Twin Nanowire

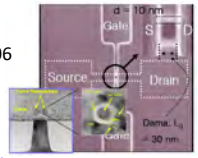
Samsung, SOI Conf. 2006

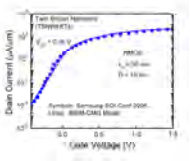




Multi-bridge-channel MOSFET

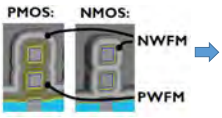
Samsung, SOI Conf. 2006



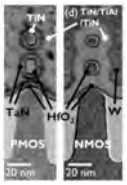


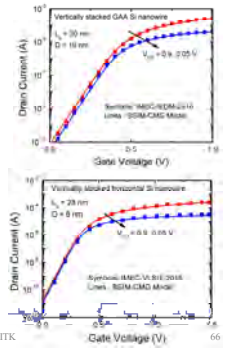
Twin silicon nanowire MOSFET

Stacked GAA Si NW MOSFETs



IMEC, IEDM 2016





TCAD Validation for different cross-sections of GAA Transistors

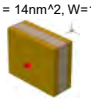
Ach = 28nm^2, W=18nm, Cins=0.86nF/m

Circular GAA

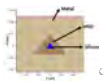
Ach = 22nm^2, W=18nm, Cins=0.76nF/m

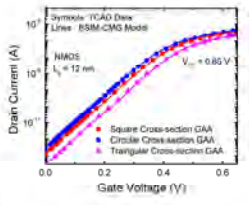
Square GAA

Ach = 14nm^2, W=18nm, Cins=0.73nF/m



Triangular GAA





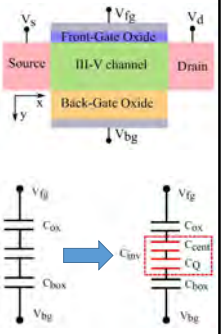
7nm & beyond – Would it be a smooth ride?

- Effects in ultra-thin Si/Ge/III-V Transistors
  - Quantum Capacitance
  - Charge centroid
  - Source to Drain Tunneling
  - Bandgap variation with thickness
  - Effective mass variation with thickness

Quantum Capacitance

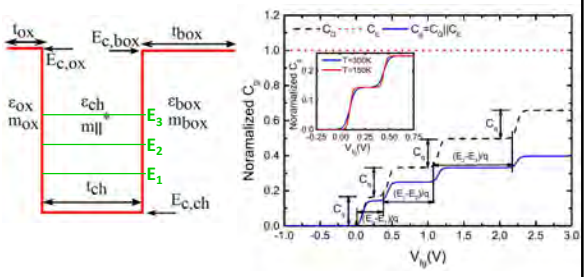
- Quantum capacitance originates when vertical electric field partially penetrates the inversion charge in channel.
- The quantum capacitance depends on 2-D density of states $\rho_{2D} = \frac{m_{||}^*}{\pi\hbar^2}$ and valley degeneracy factor (g_v)
- Quantum Capacitance

$$C_Q = \frac{q^2 g_v m_{||}^*}{\pi\hbar^2}$$



Quantum Capacitance

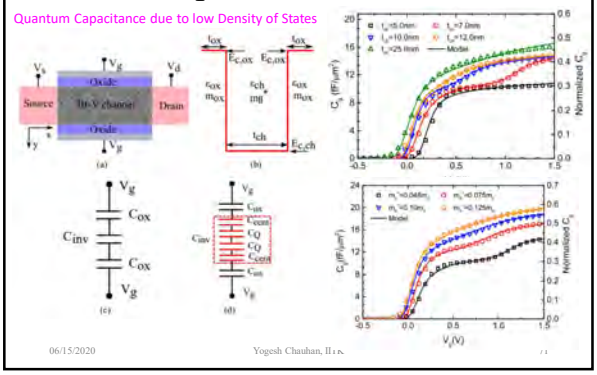
Thin body device is a 2D system.



C. Yadav et. al., submitted in Solid State Electronics.

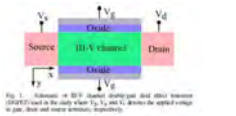
Quantum Capacitance in III-V FinFETs

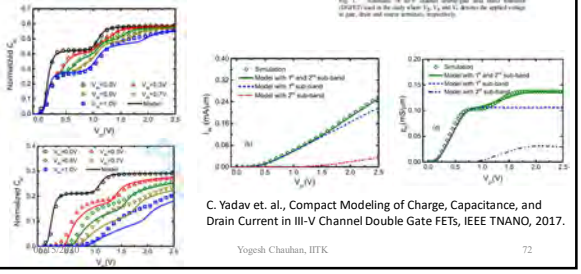
Quantum Capacitance due to low Density of States



Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

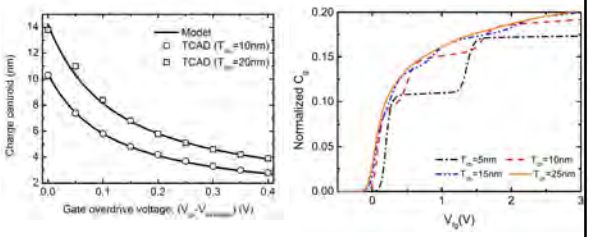




C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.

Charge centroid

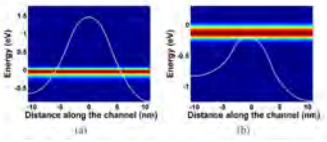
- Charge centroid in conjunction with Quantum capacitance can deteriorate C-V further.



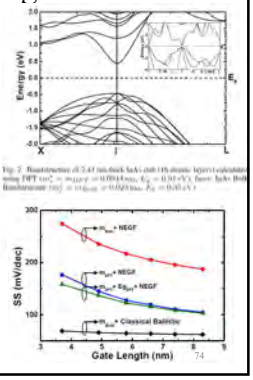
Source to Drain Tunneling in III-V FETs

- Under the barrier transport

$$T(E) = exp\left(\frac{-2}{\hbar}\int\sqrt{2m_e^*(E_{barrier}(x)-E)}\,dx\right)$$



T. Dutta et. al., "Source to Drain Tunneling in III-V MOSFETs", submitted in IEEE Electron Device Letters.



Modeling of Quasi-ballistic Nanowire FETs

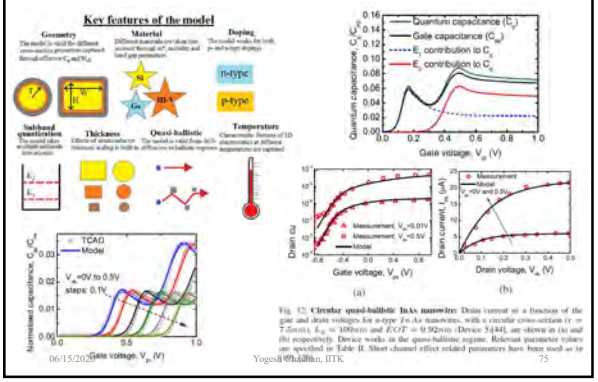
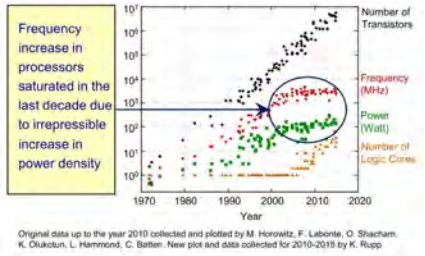


Fig. 12. Circular quad-ballistic InAs nanowire: Drain current as a function of the gate and drain voltages for n-type InAs nanowires with a circular cross-section (r = 7.5nm), L_g = 100nm and EOT = 0.92nm (Device 3 [44]), are shown in (a) and (b) respectively. Device works in the quasi-ballistic regime. Relevant parameter values are specified in Table II. Short channel effect related parameters have been used as in

Outline

- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET
- ASM-GaN-HEMT Model

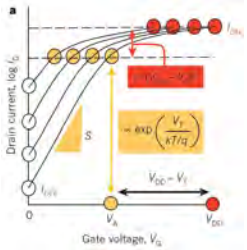
Microprocessor trends



$$P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC}$$

[1] Karl Rupp: 40 Years of Microprocessor Trend Data. [Online]. Available: https://www. karlrupp.net/tag/processors/

Power challenge



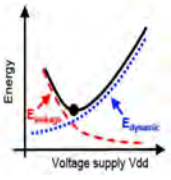
Scaling both the V_{DD} and V_T maintains same performance (I_{ON}) by keeping the overdrive (V_{DD} - V_T) constant.

A.M. Ionescu, H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", *Nature* 479, 329 (2011)

$$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$$

$$I_{OFF} \propto 10^{\left(\frac{-V_{TH}}{SS}\right)}$$

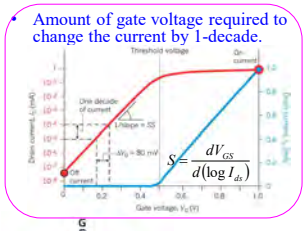
$$P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC}$$

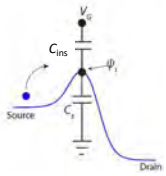


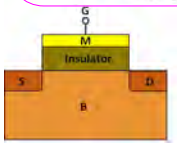
A. M. Ionescu, Kathy Boucart, "Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch", *IEDM 2009.*

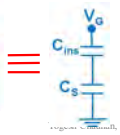
Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.









$$S = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial \psi_S}\frac{\partial \psi_S}{\partial \log_{10} I_D}$$
$$= \left(1 + \frac{C_S}{C_{ins}}\right).60\text{mV/decade}$$

As $1 + \frac{C_S}{C_{ins}} \geq 1, S \geq 60mV/decade$

Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as
- 1: $C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1}$ = inverse curvature of free energy density
- 2: $C_{ins} = \frac{\partial P}{\partial E}$ = slope of the polarization vs electric field curve

P = Polarization in dielectric, G = Free energy density
E = Externally applied electric field

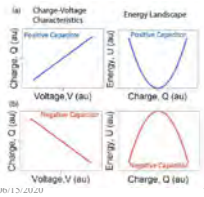
- Two types of non-linear dielectrics:
  - Paraelectric : No polarization when electric field is removed.
  - Ferroelectric : Two possible states of polarization when electric field is removed.

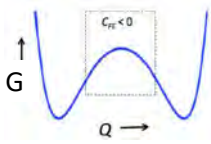
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!

$C_{ins} < 0$ and $\frac{C_S}{C_{ins}} < 0$, then $\left(1 + \frac{C_S}{C_{ins}}\right) < 1 \rightarrow S < 60\text{mV/decade}$

- For a capacitor
  - Energy $G = \frac{Q^2}{2C} \rightarrow$ Capacitance $C = 1/\frac{d^2G}{dQ^2} = 1/Curvature$





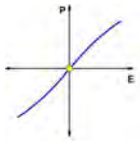
Energy landscape of ferroelectric

$Q = \epsilon E + P \cong P$

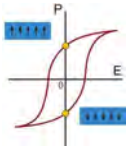
Ref. – S. Salahuddin et. al., *Nano Letters*, 2008

Para- and Ferro-electric Materials

- Paraelectric : No polarization when electric field is removed.
- Ferroelectric : Two possible states of polarization when electric field is removed –Spontaneous/Remnant Polarization.



Paraelectric



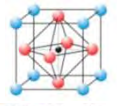
Ferroelectric

Ferroelectricity

Requirements:
- Spontaneous electric polarization: Non-Centrosymmetricity (for crystalline materials)
- Reversible polarization state by the application of electric field

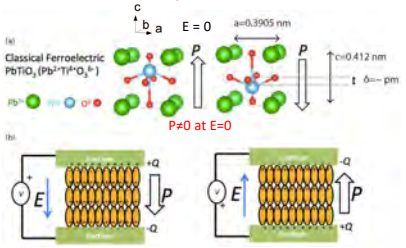
e.g. Lead titanate $PbTiO_3$, HZO

Centrosymmetric:- Paraelectric



P=0 at E=0

Non-Centrosymmetric:- Ferroelectric



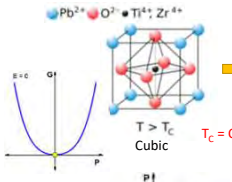
P≠0 at E=0

[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.
[2] A.I. Khan, "*Negative Capacitance for Ultra-low Power Computing*" PhD thesis, University of California at Berkeley, 2015.

Paraelectric to Ferroelectric Phase Transition

e.g. $Pb[Zr_xTi_{1-x}]O_3$ Lead Zirconium Titanate (PZT)

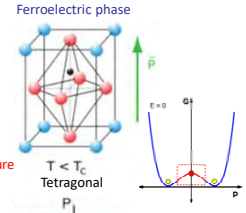
Paraelectric phase



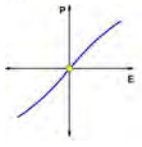
$T > T_C$
Cubic

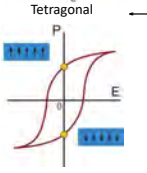
T_C = Curie Temperature

Ferroelectric phase



$T < T_C$
Tetragonal





[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as
$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$
- α and β can be +ve or –ve but γ is always +ve for stability reasons.
- Dynamics of G is given by $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$ (δ = Polarization damping factor)
- In the steady state, $\frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

For $\alpha > 0$ and at $E = 0$, there exit only one real root $P = 0$
A Paraelectric Material

For $\alpha < 0$ and at $E = 0$, there exit three real roots
$P = 0, \pm P_r$ where $P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$
A Ferroelectric Material has a non-zero P at zero E.

Assumptions

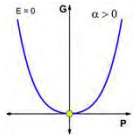
Free energy of a non-linear dielectric
$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- Polarization and Electric field are uniaxial. (perpendicular to electrodes)
- Polarization and Electric field magnitudes are uniform throughout the ferroelectric.
- Piezo-electricity is ignored.

L-K explanation of Phase Transition

For E = 0, $G = \alpha P^2 + \beta P^4 + \gamma P^6$ and $\alpha = \alpha_0(T - T_0), \alpha_0 > 0$

Paraelectric Material

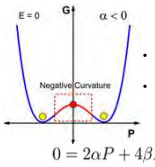


$$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

- $\alpha > 0$ i.e. for $T > T_0$; at $E = 0$, there exists only one real root, $P = 0$
- i.e. No polarization when electric field is removed

$$[P = 0 \text{ at } E = 0]$$

Ferroelectric Material



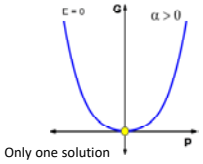
- Note, P = 0 has a maximum.
- Not possible in an isolated ferroelectric.

$$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

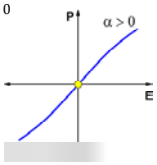
- $\alpha < 0$ i.e. for $T < T_0$; at $E = 0$, there exist three real roots
$P = 0, \pm P_r$ where
$$P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$$
- Two possible states of polarization when electric field is removed.

[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

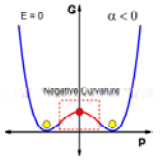
Positive and Negative Capacitances

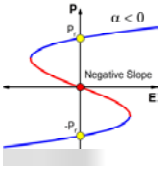


Only one solution at $E = 0$



Paraelectric
A Positive Capacitor





Ferroelectric
A Conditionally Negative Capacitor

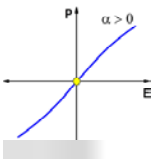
Three possible solutions at $E = 0$

$P = 0$ is not possible in a isolated Ferroelectric due to maxima of energy or a negative capacitance

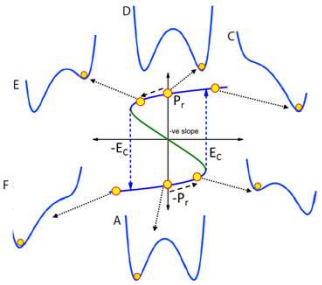
$$C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1} = \frac{\partial P}{\partial E} < 0$$

Application of Electric Field

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$
$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$



Paraelectric
[A Positive Capacitor]

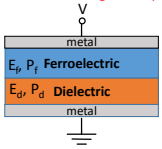


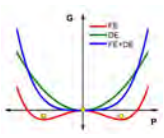
Isolated Ferroelectric
[A Conditionally Negative Capacitor]

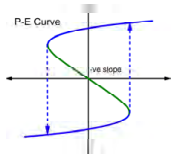
[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.
[2] A.I. Khan, *Negative Capacitance for Ultra-low Power Computing*, PhD thesis, University of California at Berkeley, 2015.

How to stabilize a Negative Capacitance?

Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.







Total energy of the FE + DE system
$$G = G_f + G_d$$
$$Q = \epsilon_0 E_f + P_f = \epsilon_0 E_d + P_d$$

For a stable system $\frac{\partial^2 G}{\partial Q^2} > 0$ (minimum)

Assuming V is small
$$Q \approx P_f \approx P_d$$

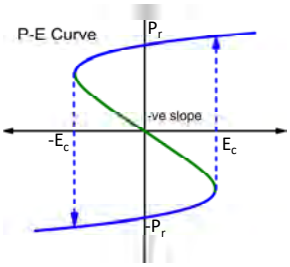
$$\Rightarrow \frac{1}{C_{tot}} = \frac{1}{C_f} + \frac{1}{C_d} > 0$$

$$\Rightarrow \frac{\partial^2 G}{\partial Q^2} = \frac{\partial^2 G_f}{\partial Q^2} + \frac{\partial^2 G_d}{\partial Q^2}$$

$$C_{tot} = \frac{C_d . |C_f|}{|C_f| - C_d} > 0$$

For a stable system
$|C_f| > C_d$
$C_{tot} > C_d$

Negative Capacitance in Ferroelectric



$$C_{ins} = C_{fe}$$

Negative slope region can be stabilized if

$$C_{total} = \left(\frac{1}{-|C_{fe}|} + \frac{1}{C_S}\right)^{-1} > 0$$

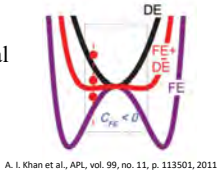
or,

$$|C_{fe}| > C_S$$

S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008.

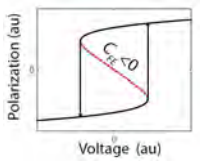
How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

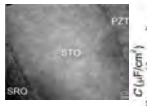


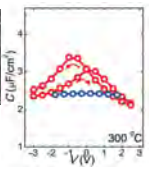
A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011

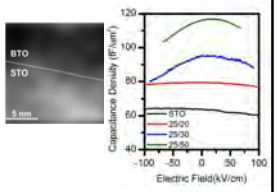
- $\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0$
- $C_{DE} < |C_{FE}|$ and $C_{FE} < 0$
- $C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$



Ferroelectric-Dielectric Systems







A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011.

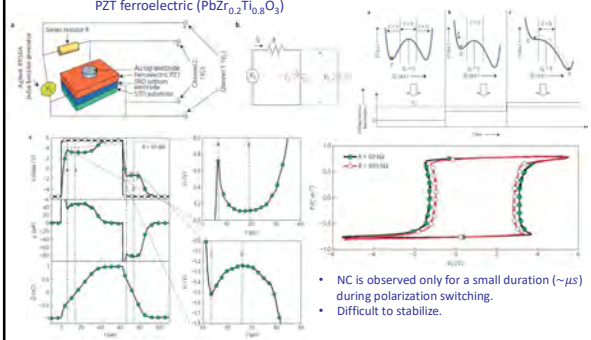
D. J. Appleby et al., Nano Letters, vol. 14, no.7, pp. 3864–3868, 2014.

Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.

$$C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$$

Ferroelectric-Resistor System

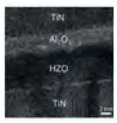
PZT ferroelectric ($PbZr_{0.2}Ti_{0.8}O_3$)



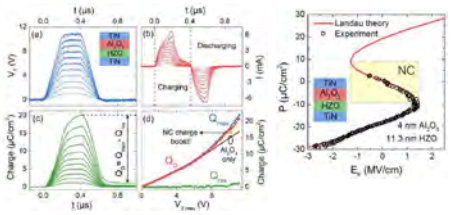
- NC is observed only for a small duration (~μs) during polarization switching.
- Difficult to stabilize.

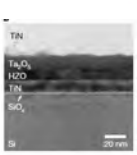
A. I. Khan *et al.*, "Negative capacitance in a ferroelectric capacitor," *Nature Mater.*, vol. 14, no. 2, pp. 182–186, 2015.

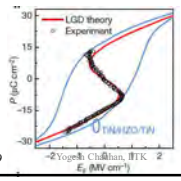
First ever demonstration of S-curve

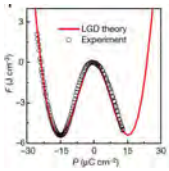


Hoffmann et al. *IEDM*, Dec 2018



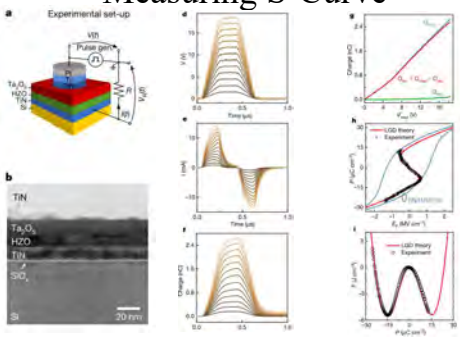






Hoffmann et al. *Nature Lett.*, Jan 2019

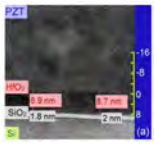
Measuring S-Curve



Ref. – Thomas Mikolajick et al., "Unveiling the double-well energy landscape in a ferroelectric layer", Nature, Jan. 2019.

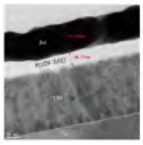
Negative Capacitance FETs

$PbZr_{0.52}Ti_{0.48}O3$ FE with HfO_2 buffer interlayer



S. Dasgupta et al., IEEE JESCDC, 2015.

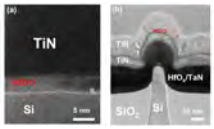
$P(VDF_{0.75}\text{-}TrFE_{0.25})$ Organic Polymer FE



J. Jo et al., Nano Letters, 2015

HfZrO FE

CMOS compatible FE

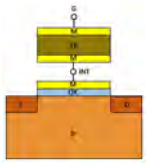


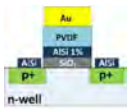
K.-S. Li et al., in IEEE IEDM, 2015.

NCFET Structures

MFMIS Structure

Metal
Ferroelectric
Metal
Insulator
Semiconductor



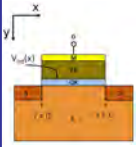


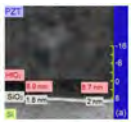
46 mV/decade
[Rusu et al. IEDM '10]

NC-FinFET
(FE: $Hf_{0.42}Zr_{0.58}O_2$)
Lg = 30 nm
[Li et al. IEDM '15]

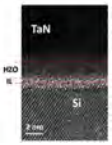
MFIS Structure

Metal
Ferroelectric
Insulator
Semiconductor





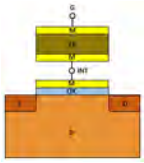
13 mV/decade
Lg = 10 µm
[Dasgupta et al., IEEE JESCDC, '15]

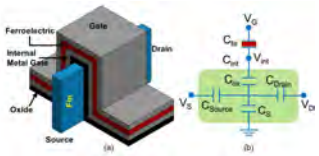


52 mV/decade
t_{ox} = 1.5 nm
[Lee et al., IEDM '16]

MFMIS NCFET Modeling

MFMIS Structures

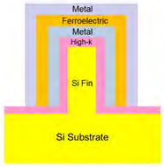


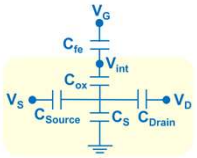


- Metal internal gate → equipotential surface with a spatially constant V_{int}.
- Ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire → Simplified modeling

Device Structure

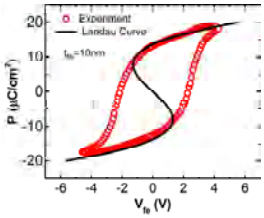
Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)





- Metal internal gate provides an equipotential surface with a spatially constant V_{int}.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.

Experimental Calibration of L-K Model



Calibration of L-K with P-V_{fe} curve for Y-HfO2 with 3.6 mol% content of $YO_{1.5}$[3]

$\alpha = -1.23 \times 10^9$ m/F
$\beta = 3.28 \times 10^{10}$ m/F
$\gamma = 0$ (2nd order phase transition)

[3] J. Müller et al., JAP, vol. 110, no. 11, pp. 114113, 2011.

Gibb's Energy,
$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$

Dynamics of G is given by
$\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$

In the steady state, $\frac{dP}{dt} = 0$

$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

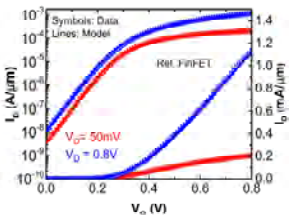
$P = Q - \varepsilon E \approx Q$ (Gate Charge)

[1] Devonshire et al., The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 40, no. 309, pp. 1040–1063, 1949.

[2] Landau, L. D. & Khalatnikov, I. M. On the anomalous absorption of sound near a second order phase transition point. Dokl. Akad. Nauk **96**, 469472 (1954).

Calibration of Baseline FinFET

Calibration of baseline FinFET with 22 nm node FinFET.

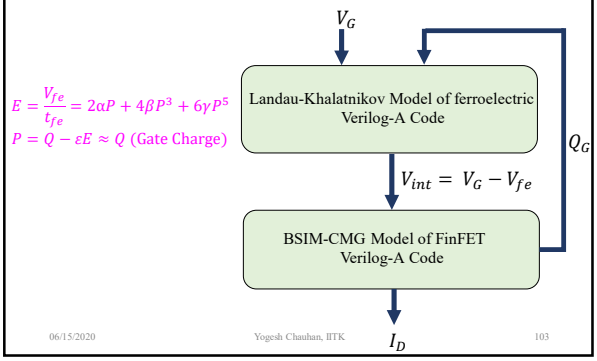


C. Auth et al., in VLSIT, 2012, pp. 131–132.

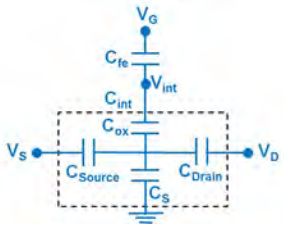
BSIM-CMG model is used to model baseline FinFET.

Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

Complete Modeling Flowchart



Capacitances and Voltage Amplification



$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

$$C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)}$$

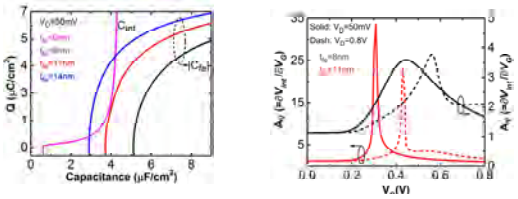
$$\frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}}$$

Capacitance matching between $|C_{fe}|$ and C_{int} increases the gain.

Internal Voltage Gain,

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

Capacitance Matching



- Capacitance matching increases with t_{fe} which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.

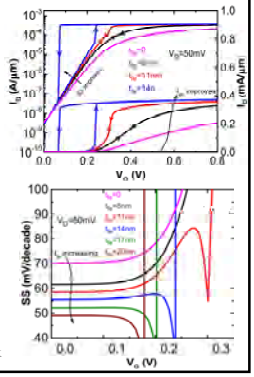
- Increase in V_D reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.

I_D-V_G Characteristics – SS region

- As t_{fe} increases
  - Capacitance matching is better
  - C_S and C_{ins} are better matched

$$S = \left(1 - \frac{C_S}{|C_{ins}|}\right).60\text{mV/dec}$$

- As t_{fe}↑ → SS↓

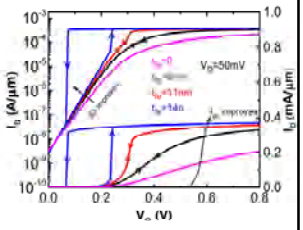


I_D-V_G Characteristics – ON region

- As t_{fe} increases
  - Capacitance matching is better

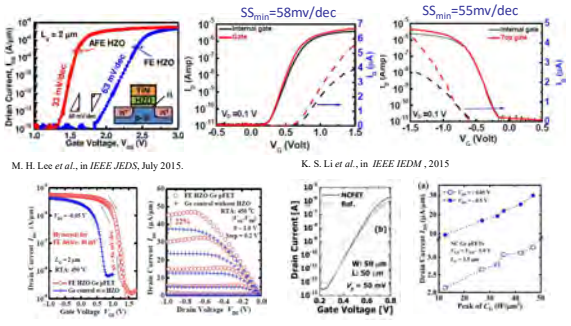
$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, I_{ON} increases.



Note the significant improvement in I_{ON} compared to SS.

I_D-V_G Experimental Demonstration



M. H. Lee *et al.*, in *IEEE JEDS*, July 2015.

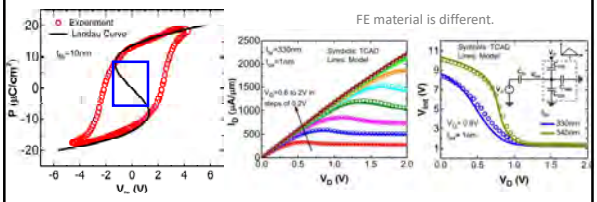
K. S. Li *et al.*, in *IEEE IEDM* , 2015

J. Zhou et al., in IEEE IEDM, 2016.

D. Kwon et al., in IEEE EDL, 2018

Jing Li et al., in IEEE EDL, 2018

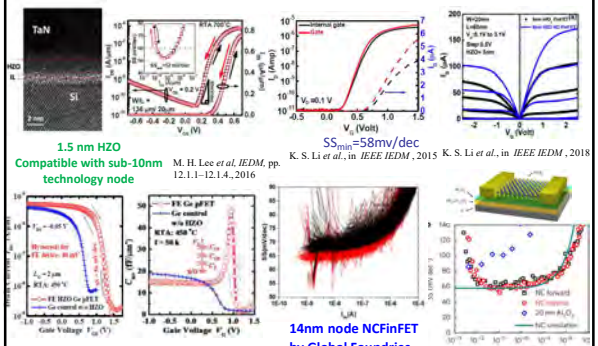
I_D-V_D Characteristics



- NCFET is biased in negative capacitance region.
  - Q_G or P is positive → V_{fe} is negative.
- V_{DS}↑ → Q_G or P↓ → $|V_{fe}|$ ↓ → $V_{int}=V_G+|V_{fe}|$ ↓ → A_V ↓ → Current reduces

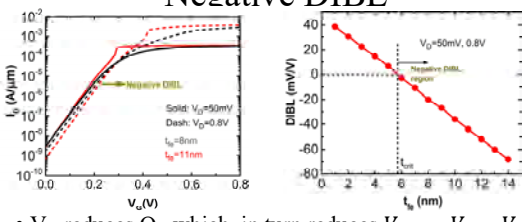
G. Pahwa, ..., Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance", IEEE TED, Dec. 2016.

Experimental Demonstration



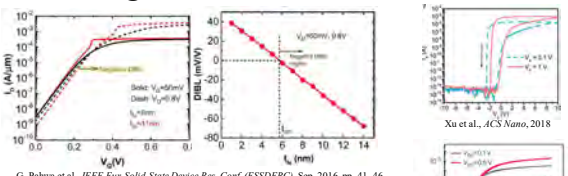
J. Zhou *et al.*, *IEDM*, 2016, pp. 12.2.1-12.2.4.
Krivokapic et al., *IEDM*, 2017, pp. 15.1.1–15.1.4.
M. Si et al., *Nature Nanotechnol.*, vol. 13 , pp. 24–28, 2018.

Negative DIBL



- V_D reduces Q_G which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with t_{fe} due to increased V_{fe} drop.
- V_{th} increases with V_D instead of decreasing.
  - Higher I_{ON} still lower I_{OFF}!

Negative DIBL/DIBR Effect

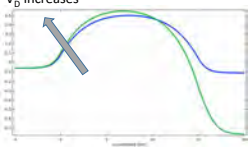


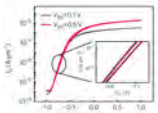
G. Pahwa et al., *IEEE Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2016, pp. 41–46.

Xu et al., *ACS Nano*, 2018

V_D ↑, Q_G ↓, V_{fe} ↑, V_{int} ↓, V_{th}↑

V_D increases



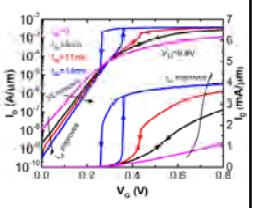


M. Si et al., *Nature Nanotechnol.*, vol. 13 , pp. 24–28, 2018.

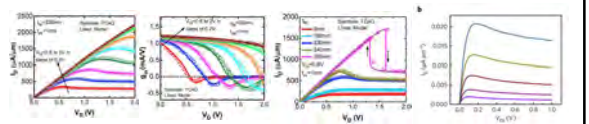
- V_{th} increases with V_D instead of decreasing. Higher I_{ON} still lower I_{OFF}!
- Negative DIBL increases with t_{fe} due to increased V_{fe} drop.

I_D-V_G Characteristics – High V_{DS}

- Hysteresis appears for $|C_{fe}| < C_{int}$ which is the region of instability.
- As t_{fe} increases
  - SS reduces, I_{ON} increases.
  - I_{OFF} reduces for high V_D.
- Width of hysteresis at larger thicknesses can be controlled with V_D.

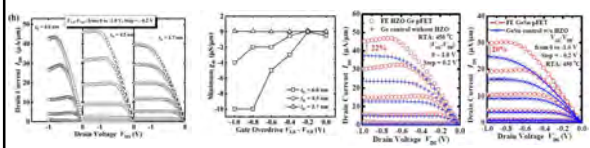


Negative Output Differential Resistance



G. Pahwa *et al.*," *IEEE TED*, Dec. 2016

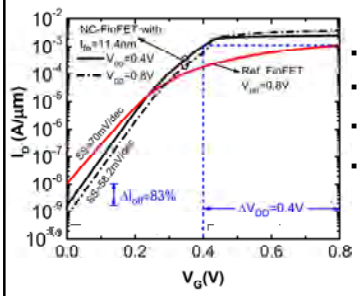
Mengwei Si *et al., Nature Nanotechnology, 2018*



J. Zhou *et al., IEEE, JEDS, 2018*

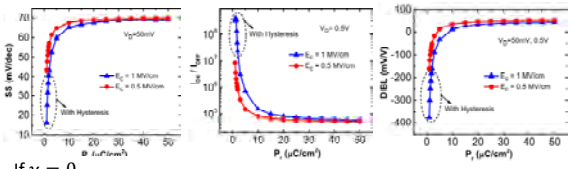
J. Zhou *et al., IEDM 2016*

Optimum NC-FinFET



- Same I_{ON} as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- V_{DD} reduction by 0.4 V.
- I_{OFF} reduction by 83 %.

Ferroelectric Parameters Variation



If $\gamma = 0$,

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{P_r^3}$$

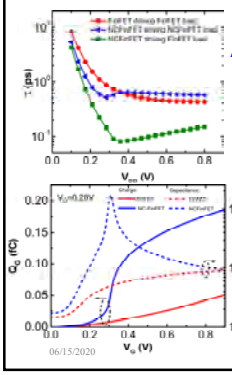
P_r = Remnant Polarization
E_c = Coercive Field

$$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$$

- Low P_r and high E_c
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I_{ON} but reduce I_{OFF} due to a more negative DIBL ⇒ high I_{ON}/I_{OFF}.

D. Ricinschi et al., JPCM, vol. 10, no. 2, p. 477, 1998.

Intrinsic Delay

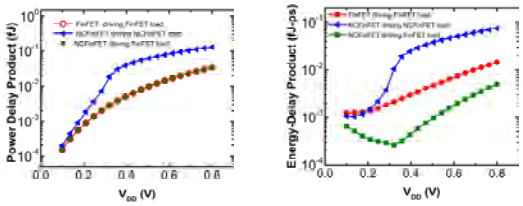


Delay, $\tau = \frac{\Delta Q_G}{I_{ON}}$

$\Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD})$

- NC-FinFET driving NC-FinFET
  - For high V_{DD}, high I_{ON} advantage is limited by large amount of ΔQ_G to be driven.
  - Outperforms FinFET at low V_{DD}.
  - Minimum at $V_{DD} \approx 0.28$ V corresponds to a sharp transition in Q_G.
- NC-FinFET driving FinFET load provides full advantage of NC-FinFET.

Power and Energy Delay Products

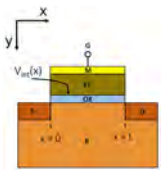


$PDP = \Delta Q_G . V_{DD}$

$EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}}$

- NC-FinFET driving NC-FinFET shows advantage only for low V_{DD}.
- NC-FinFET driving FinFET load is the optimum choice.

Modeling of MFIS NCFET



Contrast with MFIMS structure:

- P and V_{int} vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models[1,2]:
Implicit equations – tedious iterative numerical solutions

[1] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.
[2] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct. 2010.

Explicit Modeling of Charge

$$V_{fe} = Et_{fe} = aQ_G + bQ_G^3$$

Voltage Balance:

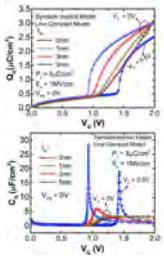
$$V_G - V_{FB} = V_{fe} + \frac{Q_G}{C_{ox}} + \psi_S = a_{eff} Q_G + bQ_G^3 + \psi_S$$

$Q_G - \psi_S$ relation[1]

$$Q_G = \text{sign}(\psi_S)\gamma C_{ox}\left[\psi_S + V_t(e^{-\psi_S/V_t} - 1) + e^{-(2\phi_F + V_C)/V_t}(V_t e^{\psi_S/V_t} - \psi_S - V_t)\right]^{1/2}$$

→ Implicit equation in Q_G

→ **Goal:** Explicit Model with good initial guesses for each region of NCFET operation

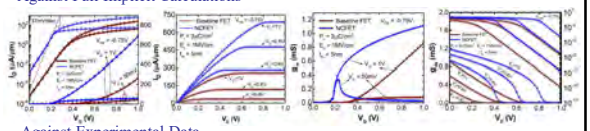


Both the Q_G and its derivatives match well with implicit model

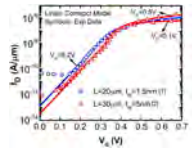
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," in *IEEE Transactions on Electron Devices*, March 2017.

Drain Current Model Validation

Against Full Implicit Calculations



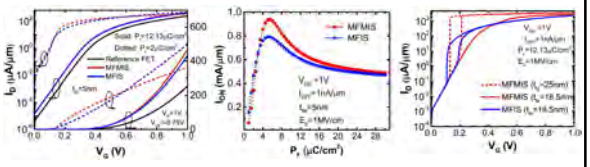
Against Experimental Data



G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," *IEEE Transactions on Electron Devices*, March 2017.

[1] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.1.1–12.1.4. [2] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.5.1–22.5.4.

MFIS Vs MFMIS



- MFIS excels MFMIS for low P_r ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", accepted in *IEEE Transactions on Electron Devices*, 2018.

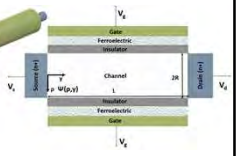
Compact Modeling of MFIS GAA-NCFET

$$V_{fe} = a_0 Q + b_0 Q^3$$

Radial Dependence in Ferroelectric Parameter:
(Ignored in others work)

$$a_0 = 2aR\ln[1 + t_{fe}/(R + t_{ins})]$$

$$b_0 = 2bR^3[1/(R + t_{ins})^2 - 1/(R + t_{ins} + t_{fe})^2]$$



Mobile Charge Density:

$$Q = \varepsilon_{si}\left(\frac{d\psi}{dy}\right)\Big|_{y=R} = \left(\frac{2\varepsilon_{si}}{R}\right)\left(\frac{2kT}{q}\right)\left(\frac{\beta^2}{1-\beta^2}\right)$$

Voltage Balance:

$$V_g - \Delta\phi - \psi_s = (a_0 + 1/C_{ins})Q + b_0 Q^3$$

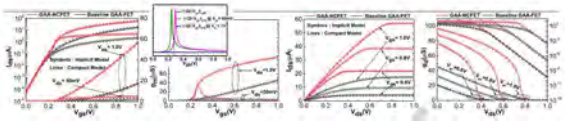
Implicit Equation in β:

$$\ln(\beta) - \ln(1-\beta^2) + m\left(\frac{\beta^2}{1-\beta^2}\right) + n\left(\frac{\beta^2}{1-\beta^2}\right)^3 - G = 0$$

→ **Goal:** Explicit Model for β with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.

Drain Current Model Validation

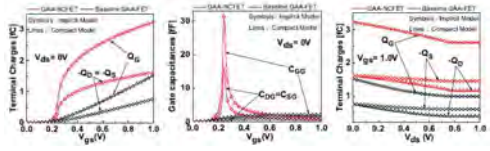
Against Full Implicit Calculations



- In contrast to bulk-NCFETs
  - Multi-gate NCFETs with an undoped body exhibit same I_{OFF} and V_{th} due to absence of bulk charges.
  - GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.

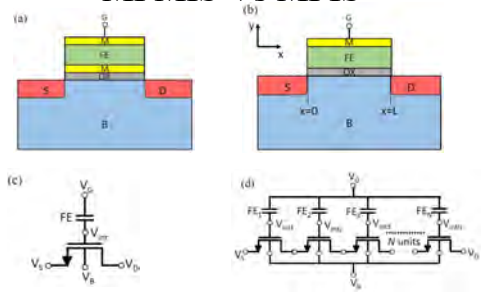
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.

Terminal Charges in GAA-NCFET



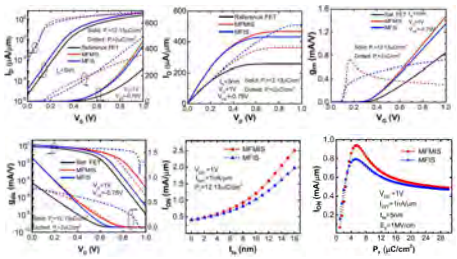
- Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
- For high V_{DS}, the Q_G for GAA-NCFET is saturates to $(4/5)^{th}$ of the maximum value (at Vds = 0) in contrast to conventional devices for which it saturates to $(2/3)^{rd}$ of the maximum value.

MFMIS Vs MFIS



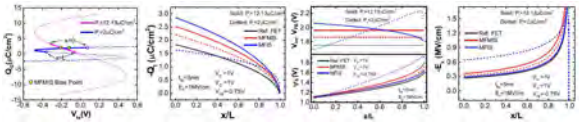
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

Comparing I_D-V_G and I_D-V_D Characteristics (long channel)



- MFIS excels MFMIS for low P_r ferroelectrics only, in long channel NCFETs.

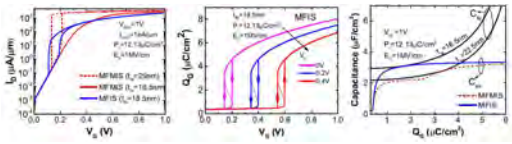
Understanding different trends with P_r



- Total current in ON regime ≈ drift current = inversion charge * horizontal electric field
- For high P_r, charge is higher for MFIS, but electric field in channel is low due to a decreasing V_{int} profile from source to drain, which results in lower current than MFMIS.
- For low P_r, charge is lower for MFIS, but electric field in channel is high due to a increasing V_{int} profile from source to drain, which results in higher current than MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, *"Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures"*, IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

Hysteresis Behavior



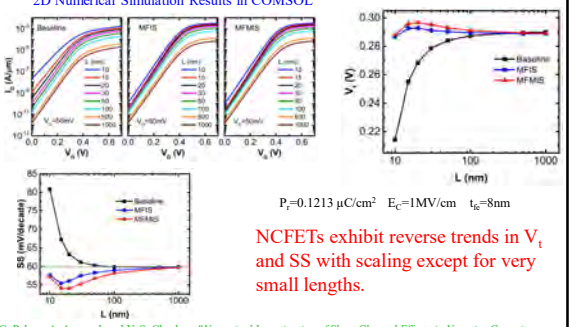
- Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
- Source end dipole switches, first, owing to its least hysteresis threshold.
- Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, *"Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures"*, IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

MFMIS vs MFIS: Short Channel Effects

OFF Regime (low V_D)

2D Numerical Simulation Results in COMSOL

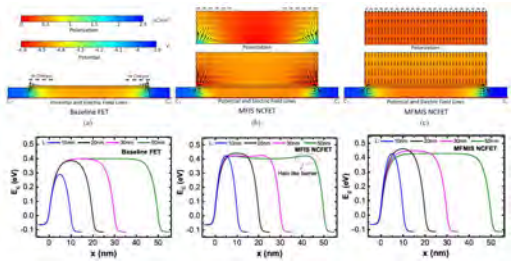


P_r=0.1213 μC/cm² E_C=1MV/cm t_{fe}=8nm

NCFETs exhibit reverse trends in V_t and SS with scaling except for very small lengths.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, *"Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures"*, IEEE Transactions on Electron Devices.

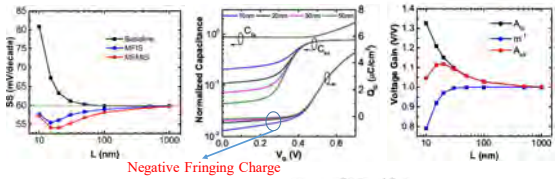
Reverse V_t Shift with Scaling



- Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.
- In MFIS, fringing effect remains localized to channel edges only → Halo Like barriers.
- In MFMIS, internal metal extends this effect to the entire channel → larger V_t than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, *"Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures"*, IEEE Transactions on Electron Devices.

Reverse SS trends with Scaling



Negative Fringing Charge

$$SS = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial \psi_c}{\partial \log_{10} I_D} \frac{m}{A_{fe}}$$

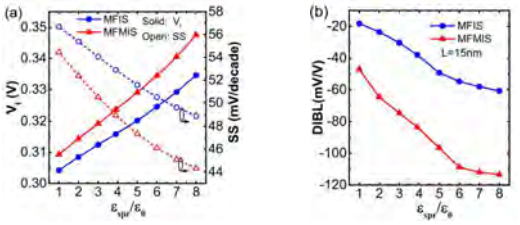
$m = \partial V_{int}/\partial \psi_c$ = Body Factor

$A_{fe} = \partial V_{int}/\partial V_G$ = Ferroelectric gain

$$A_{eff} = m^{-1} A_{fe} = \frac{1}{1 - \frac{C_{int}}{|C_{fe}|}}$$

$L \downarrow, \frac{C_{int}}{|C_{fe}|} \uparrow, A_{fe} \uparrow, m \downarrow, A_{eff} \uparrow, SS \downarrow$ (except for very small lengths where m dominates). G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures*", IEEE Transactions on Electron Devices.

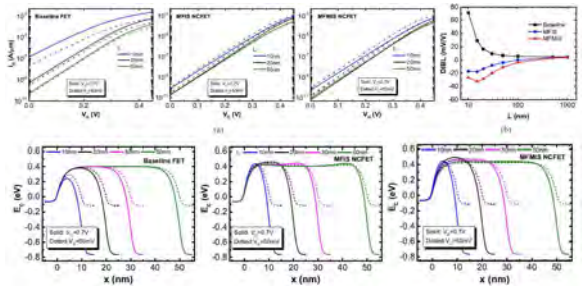
Impact of Spacer Permittivity



Increasing the spacer permittivity enhances the outer fringing electric field, which leads to a rise in Vt and reduction in SS and DIBL.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior*", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130–5136, Nov. 2018.

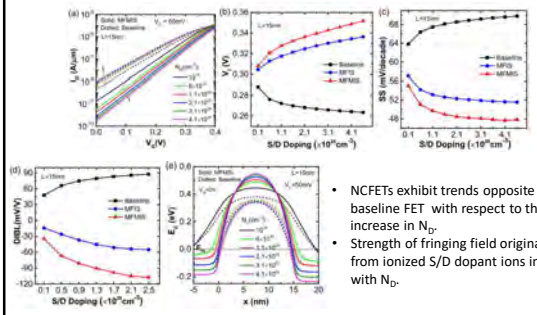
OFF Regime (high V_{DS}): Negative DIBL



- Negative DIBL effect increases with Scaling.
- More pronounced in MFMIS than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures*", IEEE Transactions on Electron Devices.

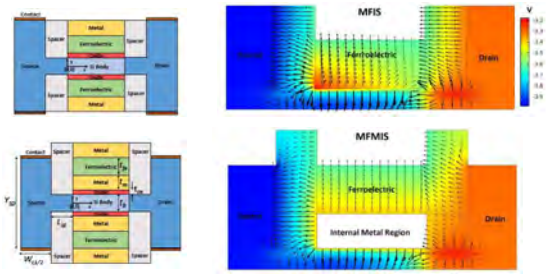
Impact of S/D doping



- NCFETs exhibit trends opposite to baseline FET with respect to the increase in N_D.
- Strength of fringing field originated from ionized S/D dopant ions increases with N_D.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior*", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130–5136, Nov. 2018.

ON Regime: Potential and field distribution

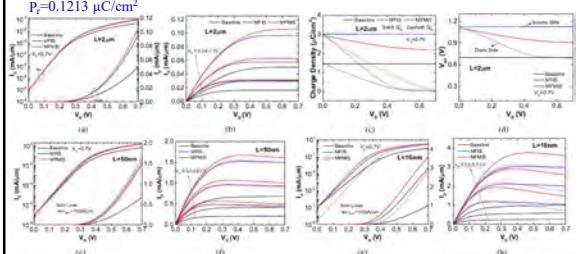


- The internal floating metal gate maintains a uniform electrical field distribution throughout the ferroelectric and a uniform potential (Vint) at ferroelectric-oxide interface.
- In the MFIS, however, electric field distribution and Vint at the interface are non-uniform.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior*", accepted in IEEE Transactions on Electron Devices, 2019.

ON Regime: Electrical Characteristics

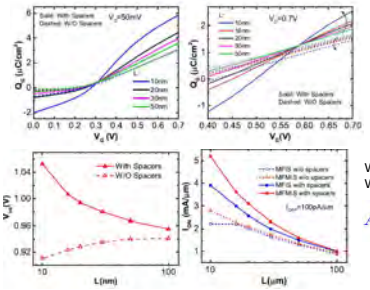
P_r=0.1213 μC/cm^2



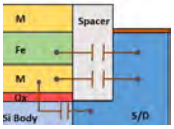
- Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling → lower V_{DSat} of MFIS results in lower I_{DS}.
- However, internal metal in MFMIS helps V_{DS} impact to easily reach source side→ Q_{iS} ↓ → Larger NDR effect in MFMIS than MFIS.
- In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former for iso-V_{FB} case only.

G. Pahwa et al., IEEE Transactions on Electron Devices, 2019.

ON Regime: Impact of Spacers



G. Pahwa et al., IEEE Transactions on Electron Devices, 2019.

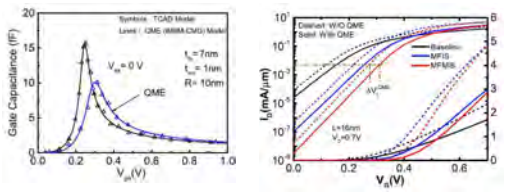


Without Spacers: Inner Fringing Only
With Spacers: Inner + Outer Fringing

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- C_{int} increases with scaling in NCFETs with spacers due to outer fringing capacitances→increases gain.
- For W/O spacers, V_{int} decreases due to absence of outer fringing, uncompensated drain side inner fringing, and increased drain to channel coupling.

Impact of Quantum Mechanical Effects

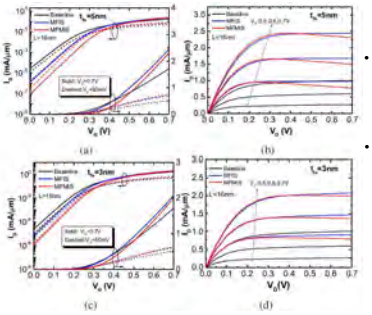


- The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.

A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior*", accepted in IEEE Transactions on Electron Devices, 2019.

Impact of Ferroelectric Thickness

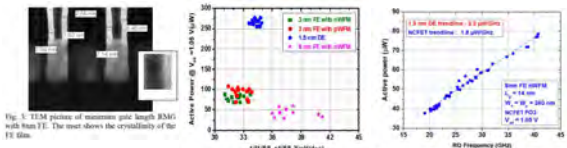


- NC influence decreases with t_{fe} which also starts to homogenise the internal gate potential.
- Thus, relative difference between MFIS and MFMIS diminishes as t_{fe} is decreased.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior*", accepted in IEEE Transactions on Electron Devices, 2019.

Does polarization damping really limit operating frequency of NC-FinFET based circuits?

Recent Demonstration by Global Foundries on 14nm NC-FinFET



[1] Krivokapic, Z. et al., IEDM 2017

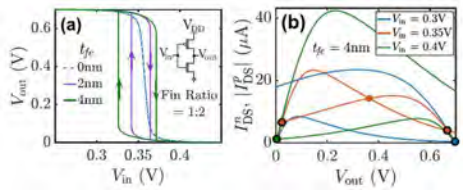
Fig. 13: Active power of FO3 inverter RO vs. effective SS for V_{dd}=1.05V.

Fig. 14: Active power of NCFET FO3 inverter RO with W_{fe}=W_g=360nm, L=14nm.

- Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power[1].
- Another theoretical study predicted intrinsic delay due to polarization damping in NCFET to be very small (270 fs)[2].

[2] Chatterjee, K., Rosner, A. J. & Salahuddin, IEEE Electron Device Letters 38, 1328–1330 (2017).

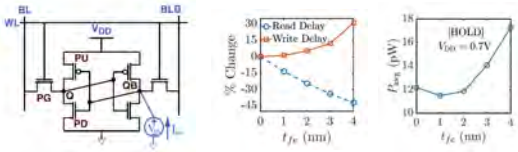
NC-FinFET based inverters



- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

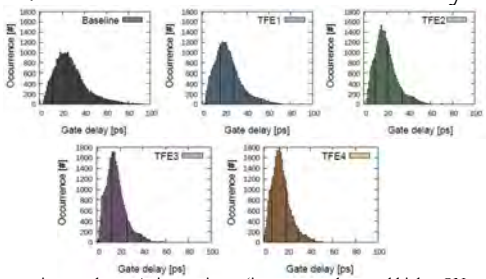
NC-FinFET based SRAM



- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- P_{avg}: NC-SRAM performs better with lower standby leakage only at small t_{fe}, taking advantage of the lower subthreshold currents

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

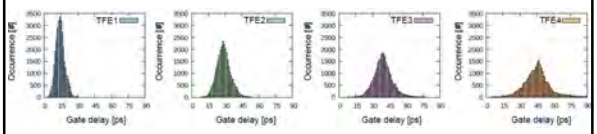
Effects of NCFET on standard cells: 7nm FinFET standard cell library



- Increasing t_{fe} – larger A_v in transistors (i.e., steeper slope and higher ON current) → Delay of cells become smaller.

IEEE Access

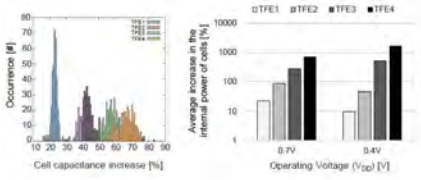
Effects of NCFET on standard cells: 7nm FinFET standard cell library



Using a ferroelectric with 1nm, 2nm, 3nm and 4nm thickness provides a speedup of around 15%, 30%, 40% and 45% respectively, in the delay of gates at the operating voltage of 0.7V.

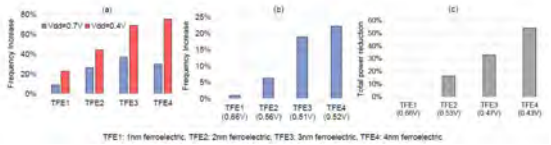
- Quantifying the relative delay decrease/improvement of cells within the 7nm FinFET standard cell library due to NCFET **at V_{DD} = 0.7V**.

Effects of NCFET on standard cells: 7nm FinFET standard cell library



- Increase in t_{fe} leads to an increase in the total cells' capacitance which further increases internal power of the cells.
- Same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.

Effects of NCFET on future processor design

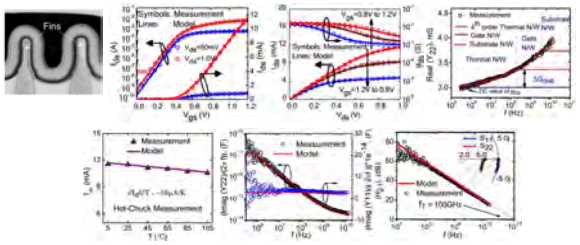


(a) What is the frequency increase due to NCFET under the same voltage constraint?
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?
(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance", IEEE Access, 2018.

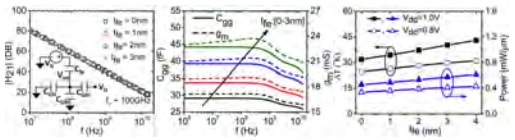
NC-FinFET RF Performance

- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis



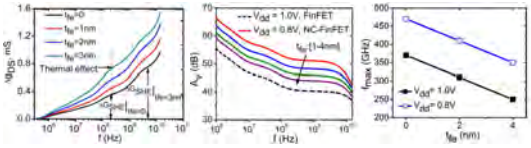
R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook, and A. Dixit, "Evaluation of 10nm Bulk FinFET RF Performance - Conventional vs. NC-FinFET", IEEE Electron Device Letters, Aug. 2018.

NC-FinFET RF Performance



- Current gain ($\propto {}^{g_m}/_{C_{gg}}$) is almost independent of t_{fe} as both the g_m and C_{gg} increase with t_{fe} almost at a constant rate.
  - Cut-off frequency (f_T) remains identical for both the Baseline and NC-FinFET.
- Temperature rise and Power consumption due to self-heating increase with t_{fe} as I_d increases. Reduce V_{dd} to achieve energy efficient performance.

NC-FinFET RF Performance

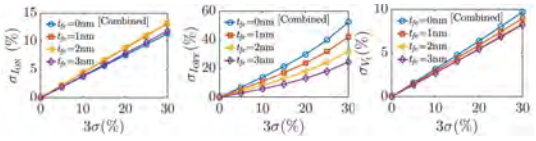


- g_{ds} and self heating ($\Delta G_{SHE} \propto g_{ds}(f) - g_{ds}(dc)$) both increase with t_{fe} due to increased capacitance matching between C_{fe} and C_{int}.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\partial I_{ds}}{\partial V_{int}} * \frac{\partial V_{int}}{\partial V_{ds}} = g_m^{int} * A_V^D \quad \text{where} \quad A_V^D = \frac{-C_{GDI}}{|C_{fe}|-C_{int}}$$

- Voltage gain ($A_V = g_m/g_{ds} = C_{fe}/C_{GDI}$) decreases with t_{fe} due to decrease in C_{fe}.
- Maximum oscillation frequency (f_{max}) also reduces with t_{fe} which can be compensated by reducing V_{dd}.

Impact of Process Variations

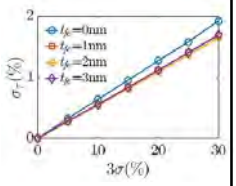


- Variability in I_{ON}, I_{OFF}, and V_t due to combined impact of variability in L_g, T_{fin}, H_{fin}, EOT, t_{fe}, E_c, and P_r
- I_{ON}: Improvement is non-monotonic with t_{fe}
- I_{OFF}: Decreases monotonically with t_{fe}
- V_t: Decreases monotonically with t_{fe}

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, 2018.

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.



11-stage Ring-Oscillator: Variation in τ due to combined variation

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, 2018.

Open Questions

- Is NC a static or transient phenomenon?
- Physical explanation of NC effect
- Second order effects
  - Impact of grain boundaries and their sizes
  - Impact of multi-domain effects
  - Impact of traps
  - Impact of FE thickness
  - Reliability, Variability
- Impact of NDR/NDIBL on circuits

Relevant Publications

- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior," in IEEE Transactions on Electron Devices, 2019.
- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Modeling of Inner Fringing Charges and Short Channel Effects in Negative Capacitance MFIS Transistor", accepted in Electron Devices Technology and Manufacturing (EDTM), 2019.
- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior," in IEEE Transactions on Electron Devices, Nov. 2018.
- Karishma Qureshi, G. Pahwa and Y.S. Chauhan, "Impact of Linear Intergranular Variation in Remnant Polarization on Negative Capacitance Field Effect Transistor", ICEE, 2018.
- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Compact Modeling of Drain Current in Double Gate Negative Capacitance MFIS Transistor", ICEE, 2018.
- H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance," IEEE Access, Sep. 2018.
- A.D. Gaidhane, G. Pahwa, A. Verma, Y. S. Chauhan, "Compact Modeling of Drain Current, Charges, and Capacitances in Long-Channel Gate-All-Around Negative Capacitance MFIS Transistor," IEEE Transactions on Electron Devices, May 2018.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Mar. 2018.
- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, Jan. 2018.

Relevant Publications

- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan,"Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS Structure", IEEE Transactions on Electron Devices, Mar. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part I, Model description", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part II, Model validation", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", IEEE ICEE, Dec. 2016. (Best Paper Award)
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE ESSDERC, Switzerland, Sept. 2016. (Invited)
- G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Compact Modeling of Negative Capacitance Transistor with Experimental Validation", IWPSD, Dec. 2015.

Outline

- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET
- ASM-GaN-HEMT Model

News (March 14, 2018)

- Our ASM-GaN-HEMT Model is industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

http://www.si2.org/2018/03/14/gallium-nitride-models/

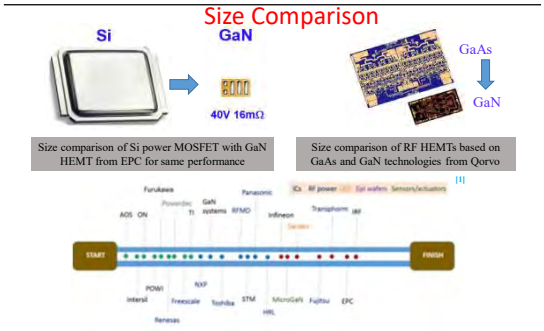
Media Coverage (April 11, 2018)


आईआईटी में बना सिमुलेशन सॉफ्टवेयर

अब झटपट बनेंगे इलेक्ट्रॉनिक उपकरण

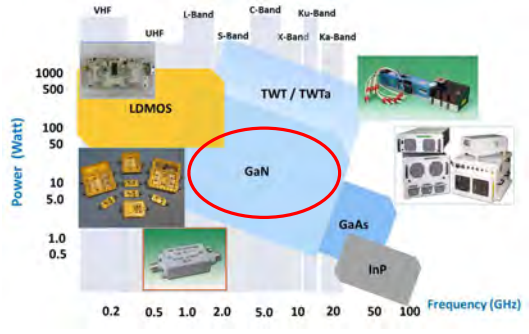
'आईआईटीके ने बनाया सर्किट सिम्यूलेशन सॉफ्टवेयर मॉडल

GaN Attractions & Avenues

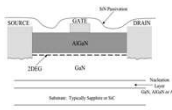


[1] S. Levin, Tech. Rep., Power Petrov Group, [2013]

RF Market



GaN HEMT

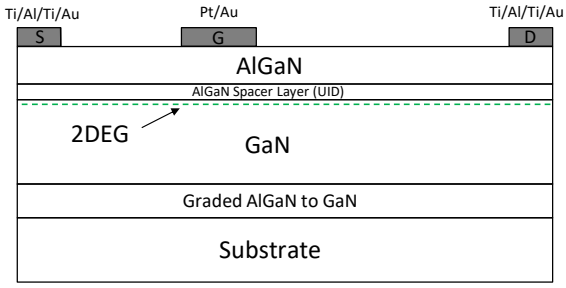


Some interesting features of III-nitride system:

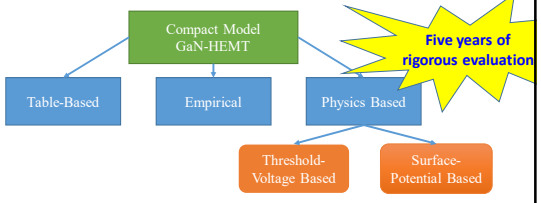
- Wide bandgap
- High 2-DEG charge density
- High electron mobility
- High breakdown voltage
- Excellent thermal conductivity
- High power density per mm of gate periphery

- GaN HEMTs are able to operate in high frequency, high power as well as high temperature device applications

GaN HEMT Structure



Status of Compact Model – GaN HEMT



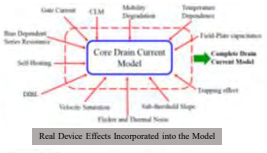
Advanced SPICE Model for GaN HEMT device

CMC candidate models for industry standardization

(Two models selected as industry standard)

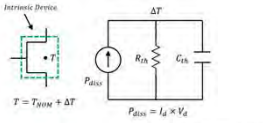
- ASM-GaN model: Our Model
- MIT MVSG model: MIT, Prof. D. Antoniadis

Core Model & Parameters



Core Model Parameters

Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	$-2.86\ V$
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	$0.325\ V^{-1}$
η_0	DIBL Parameter	0.117
U_0	Low Field Mobility	$33.29\ mm^2/Vs$
N_{SOACCS}	AR 2DEG Density	$1.9e+17\ /m^2$
$V_{SATACCS}$	AR saturation velocity	$157.6e+3\ cm/s$
R_{TH0}	Thermal Resistance	$22\ \Omega$



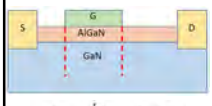
Core drain current expression

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2 v_{ds}^2}} \frac{W}{L} C_g N_f \left[V_{go} - \left(\frac{\psi_s + \psi_d}{2} \right) + V_{th} \right] \times \psi_{ds} (1 + \lambda V_{ds})$$

$$I_{ds(eff)} = \frac{R_c}{W \cdot N_f \cdot q \cdot N_{SOACCS} \cdot U_{OACCS}} \times \left(\frac{1}{m} - \left(\frac{I_{ds}}{W \cdot N_f \cdot q \cdot N_{SOACCS} \cdot V_{SATACCS}} \right)^2 \right)^{-1/2}$$

Access Resistance Model

Nonlinear source/drain access region resistance model



$$R_{I} = \frac{L_I}{q\mu_n N_{s0}} \quad I = S, D$$

$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R / V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

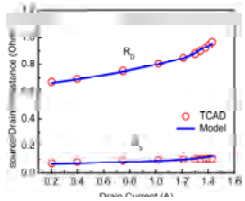


Fig. 1: Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

$R_{d/s}$ Model Validation with Measurement

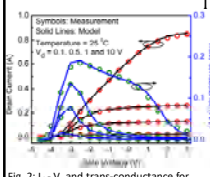


Fig. 2: I_d - V_g and trans-conductance for the Toshiba power HEMT. Different slopes above V_{on} in g_m-V_g: self-heating governs the first slope while velocity saturation in access region affects second slope.

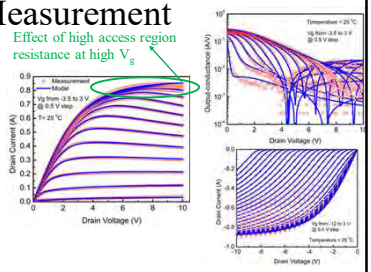
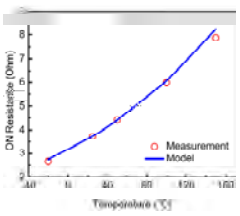
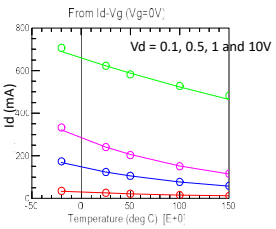


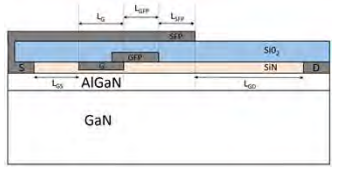
Fig. 3: (a) Ids-Vds, (b) g_{ds} and (c) reverse Ids-Vds fitting with experimental data. The non-linear $R_{s/d}$ model shows correct behavior for the higher Vg curves in the Id - Vd plot; the S-P based model can accurately capture the reverse output characteristics.

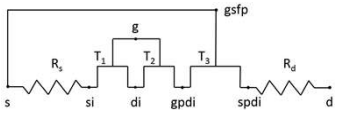
Temperature Scaling





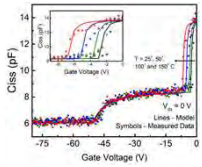
Modeling of Field-Plates in HEMTs

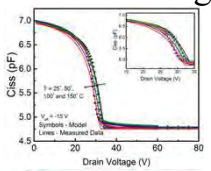


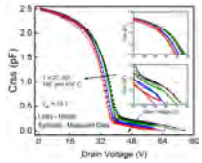


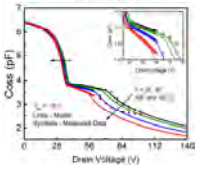
Affects capacitance and breakdown behavior.

Field-Plate Capacitance Modeling

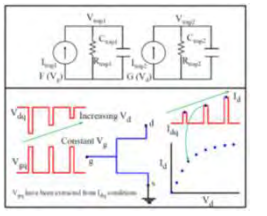




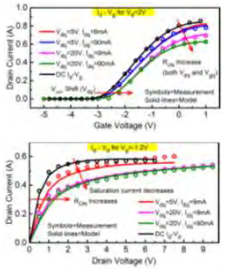




Trap Model



Pulsed-IV Scheme used to simulate the P-IV Characteristics in IC-CAP



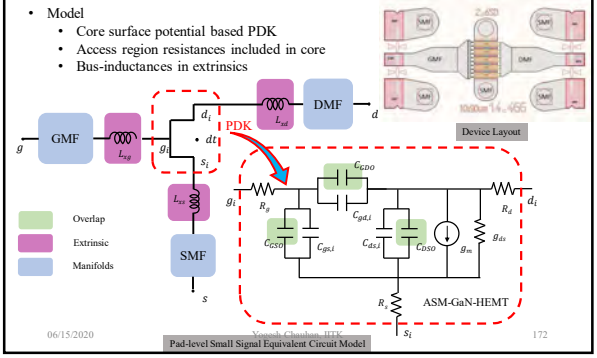
Pulsed – IV chacteristics for multiple quiescent conditions

$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$
$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$
$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$
$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$

Pulse Width – 200 ns,
Duty-cycle 0.02 %

RF Model & Extraction (i)

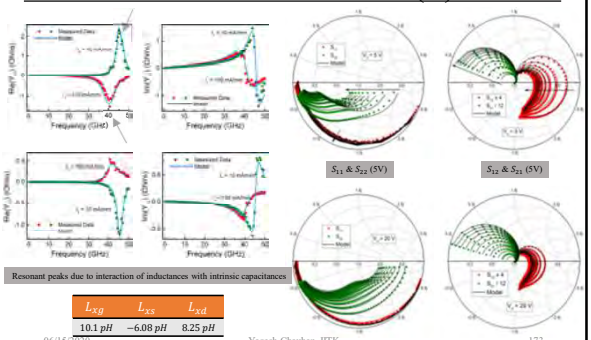
- Model
  - Core surface potential based PDK
  - Access region resistances included in core
  - Bus-inductances in extrinsics



Device Layout

Pad-level Small Signal Equivalent Circuit Model

RF Parameter Extraction (ii)

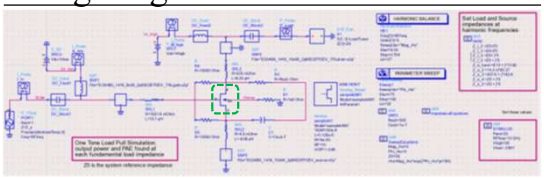


Resonant peaks due to interaction of inductances with intrinsic capacitances

L_{xg}	L_{xs}	L_{xd}
10.1 pH	−6.08 pH	8.25 pH

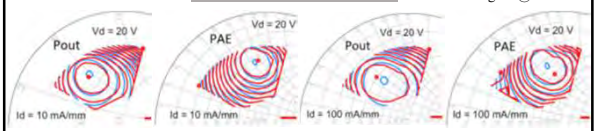
[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Large-Signal Model Validation



ADS Schematic for simulation of load-pull contours

22 dBm signal @ 10 GHz



Pout & PAE load pull contours for 10 mA/mm

Pout & PAE load pull contours for 100 mA/mm

[1] S. A. Ahsan *et al.*, *IEEE J. Electron Devices Society*, Sep., [2017]

Summary

- Industry standard model development @ IITK
- All models are implemented in the **Verilog - A** code
  - Tested on commercial **simulators**
  - Validated with real device data
- Working with major semiconductor and EDA companies