Physics and Modeling of Nano-Transistors

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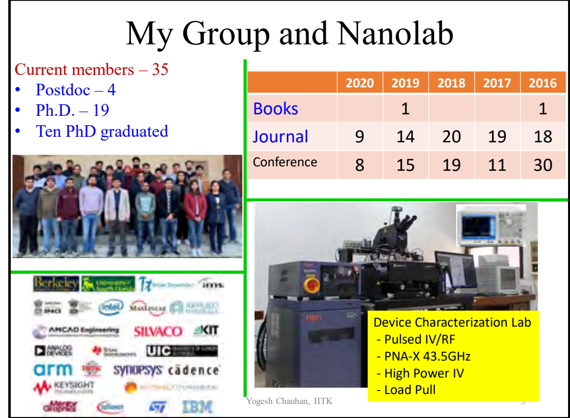
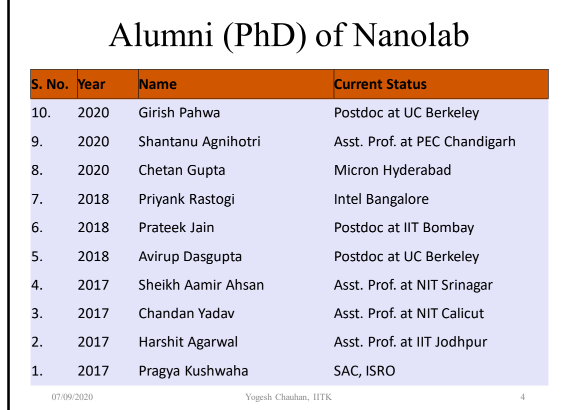
Outline

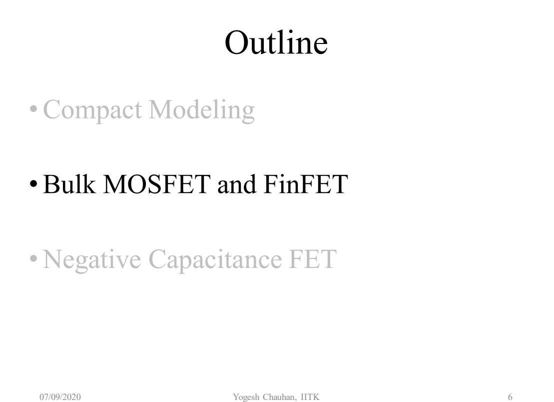
- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET



	2020	2019	2018	2017	2016
Books		1			1
Journal	9	14	20	19	18
Conference	8	15	19	11	30



S. No.	Year	Name	Current Status
10.	2020	Girish Pahwa	Postdoc at UC Berkeley
9.	2020	Shantanu Agnihotri	Asst. Prof. at PEC Chandigarh
8.	2020	Chetan Gupta	Micron Hyderabad
7.	2018	Priyank Rastogi	Intel Bangalore
6.	2018	Prateek Jain	Postdoc at IIT Bombay
5.	2018	Avirup Dasgupta	Postdoc at UC Berkeley
4.	2017	Sheikh Aamir Ahsan	Asst. Prof. at NIT Srinagar
3.	2017	Chandan Yadav	Asst. Prof. at NIT Calicut
2.	2017	Harshit Agarwal	Asst. Prof. at IIT Jodhpur
1.	2017	Pragya Kushwaha	SAC, ISRO



Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$$

- Drain current in MOSFET (OFF operation)

$$I_{OFF} \propto 10^{\left(\frac{V_{GS}-V_{TH}}{S}\right)}$$

$C_{ox}=\varepsilon_{ox}/t_{ox}$=oxide cap.
S – Subthreshold slope

- Desired
  - High I_{ON} (↓L, ↑Cox, ↑V_{DD}-V_{TH})
  - Low I_{OFF} (↑V_{TH}, ↑S)

Technology Scaling

- Each time the minimum line width is reduced, we say that a new ***technology node*** is introduced.
- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.

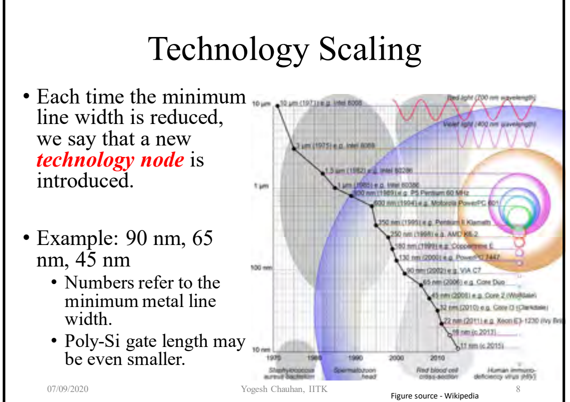


Figure source - Wikipedia

IC industry for >40 years

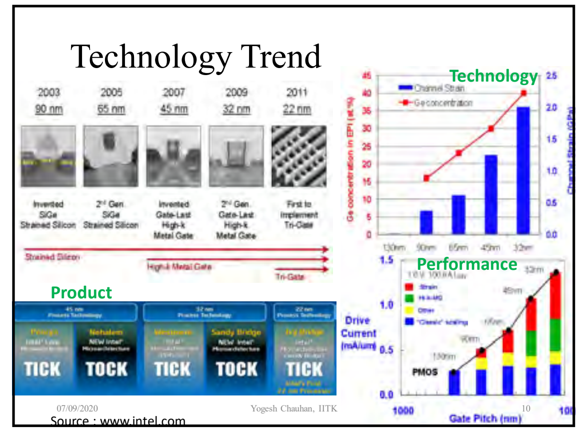
- Closer distance between elements – *Pitch*
  - *Faster* signal transfer and processing rate
- For the same Chip size (or cost), *more functionality*
- *Mass production* – Wafer size doubled every 10years.
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - *Price* of memory/logic gates has dropped 100 million times.
- The primary engine that powered the proliferation of electronics is "*miniaturization*".
- More circuits on each wafer → cheaper circuits.
- Miniaturization is key to the improvements in *speed and power consumption* of ICs.

Moore's Law

1 Nano-$ / Transistor!

It's not technology! → It's economy.

Technology Trend



Source : www.intel.com

Wasn't that smooth ride?

- Where is the bottleneck?

$$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$$

- V_{TH} and Subthreshold Slope can't be decreased

Log Scale

I_{DS}

Ideal

OFF

SI

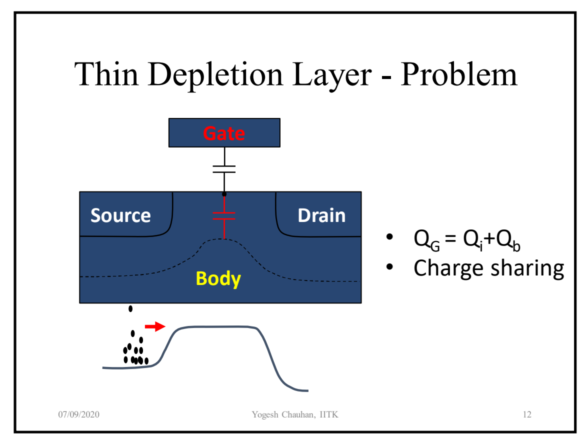
ON

I_{OFF}

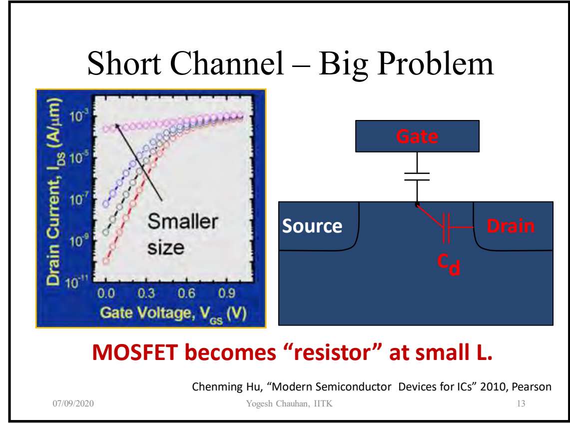
V_{GS}

V_{TH}

Thin Depletion Layer - Problem



- $Q_G = Q_i + Q_b$
- Charge sharing


Short Channel – Big Problem
Drain Current, I_DS (A/μm)
10^-3
10^-5
10^-7
10^-9
10^-11
Smaller size
0.0 0.3 0.6 0.9
Gate Voltage, V_GS (V)
Gate
Source
Drain
C_d
MOSFET becomes "resistor" at small L.
Chenming Hu, "Modern Semiconductor Devices for ICs" 2010, Pearson
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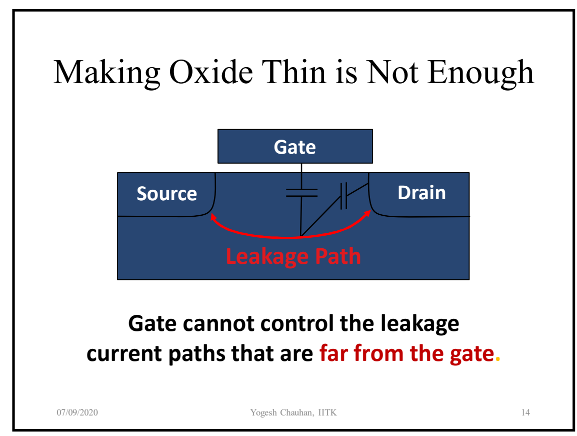
Making Oxide Thin is Not Enough
Gate
Source
Drain
Leakage Path
Gate cannot control the leakage current paths that are far from the gate.
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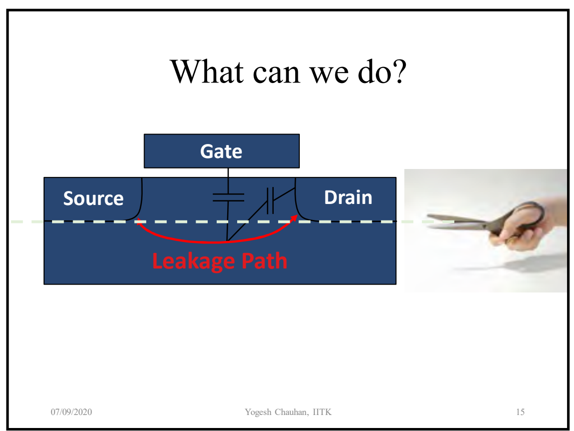
What can we do?
Gate
Source
Drain
Leakage Path
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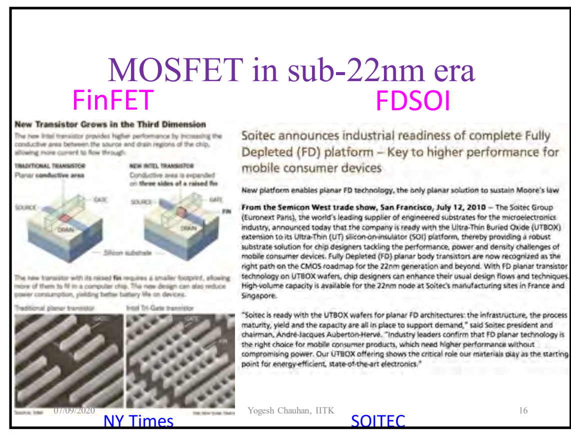
MOSFET in sub-22nm era
FinFET
FDSOI
New Transistor Grows in the Third Dimension
Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices
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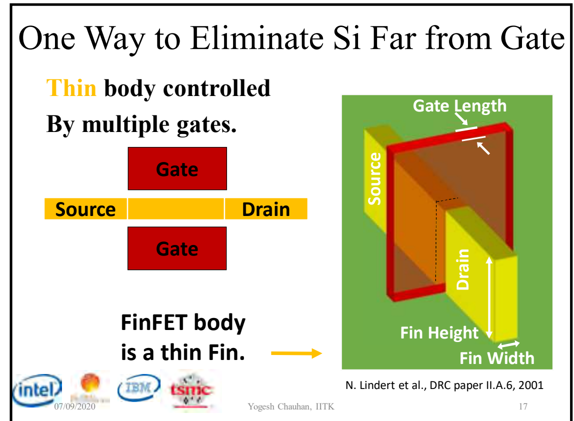
NY Times
SOITEC


One Way to Eliminate Si Far from Gate
Thin body controlled
By multiple gates.
Gate
Source
Drain
Gate
FinFET body
is a thin Fin.
Gate Length
Source
Drain
Fin Height
Fin Width
N. Lindert et al., DRC paper II.A.6, 2001
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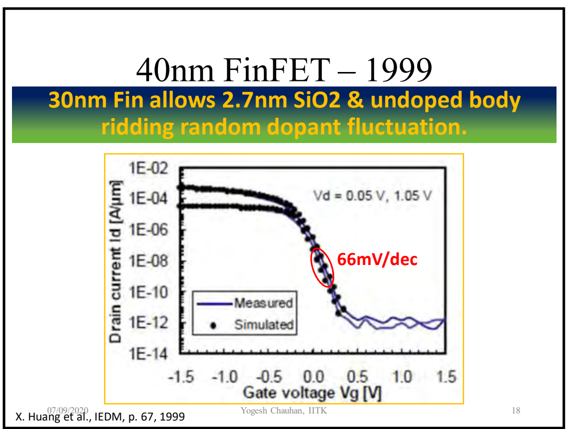
40nm FinFET – 1999
30nm Fin allows 2.7nm SiO2 & undoped body
ridding random dopant fluctuation.
Drain current Id [A/μm]
1E-02
1E-04
1E-06
1E-08
1E-10
1E-12
1E-14
Vd = 0.05 V, 1.05 V
66mV/dec
Measured
Simulated
-1.5 -1.0 -0.5 0.0 0.5 1.0 1.5
Gate voltage Vg [V]
X. Huang et al., IEDM, p. 67, 1999
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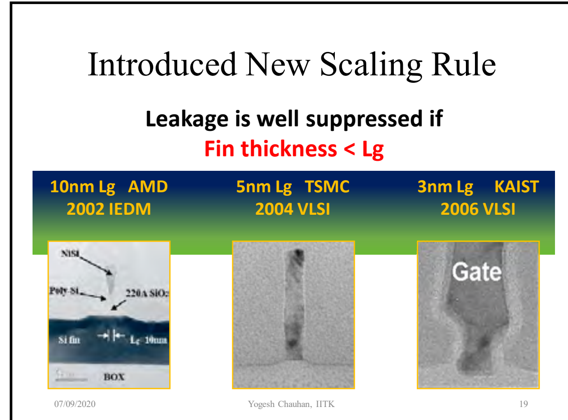
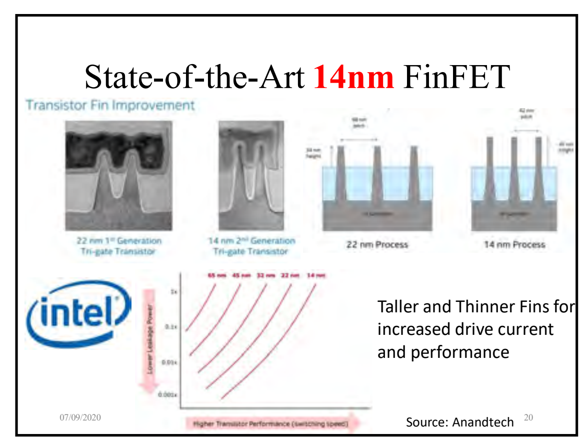
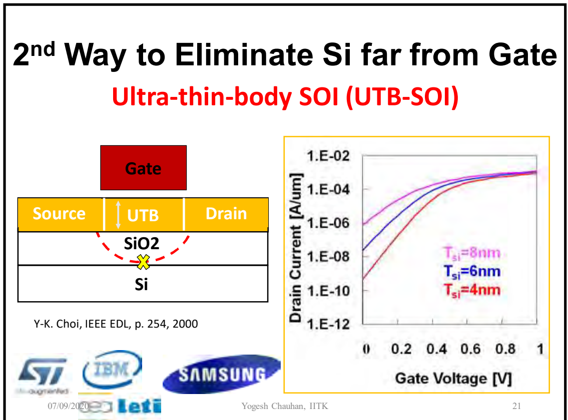
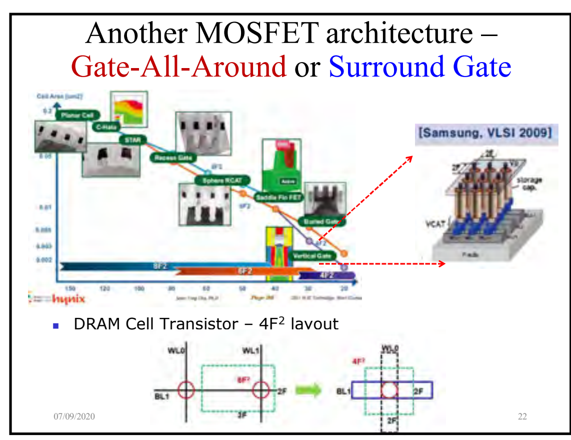








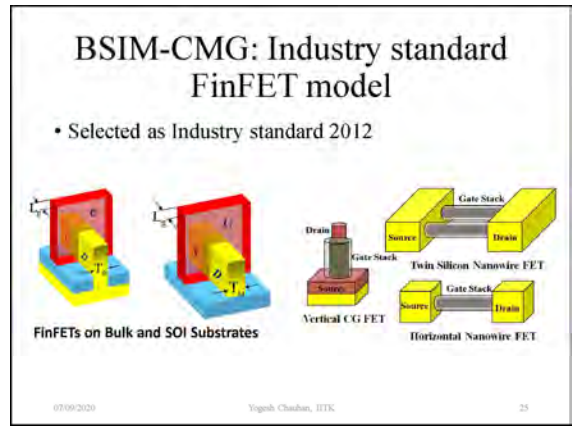
Outline

- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET

BSIM-CMG and BSIM-IMG

- **Berkeley Short-channel IGFET Model**
- **First industry standard SPICE model for IC simulation**
- **Used by hundreds of companies for IC design since 1997**
- **BSIM FinFET model became industry standard in March 2012**

It's Free


BSIM-CMG: Industry standard FinFET model
• Selected as Industry standard 2012
FinFETs on Bulk and SOI Substrates
Gate Stack
Twin Silicon Nanowire FET
Vertical CG FET
Horizontal Nanowire FET
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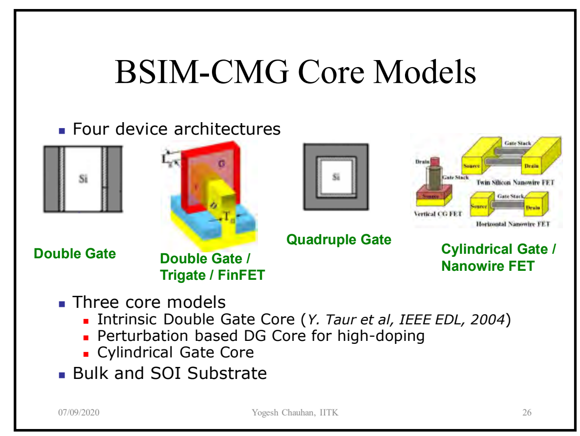
BSIM-CMG Core Models
Four device architectures
Double Gate
Double Gate / Trigate / FinFET
Quadruple Gate
Cylindrical Gate / Nanowire FET
Three core models
Intrinsic Double Gate Core (Y. Taur et al, IEEE EDL, 2004)
Perturbation based DG Core for high-doping
Cylindrical Gate Core
Bulk and SOI Substrate
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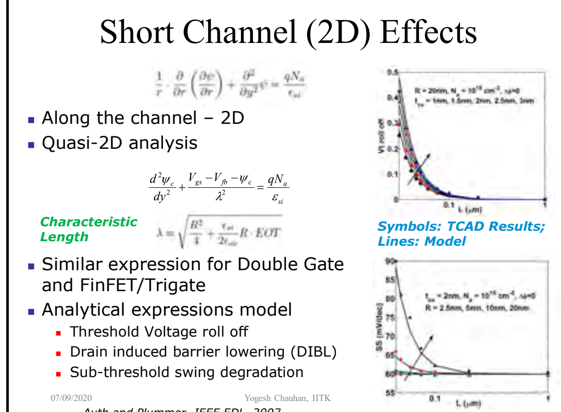
Short Channel (2D) Effects
Along the channel – 2D
Quasi-2D analysis
Characteristic Length
Symbols: TCAD Results; Lines: Model
Similar expression for Double Gate and FinFET/Trigate
Analytical expressions model
Threshold Voltage roll off
Drain induced barrier lowering (DIBL)
Sub-threshold swing degradation
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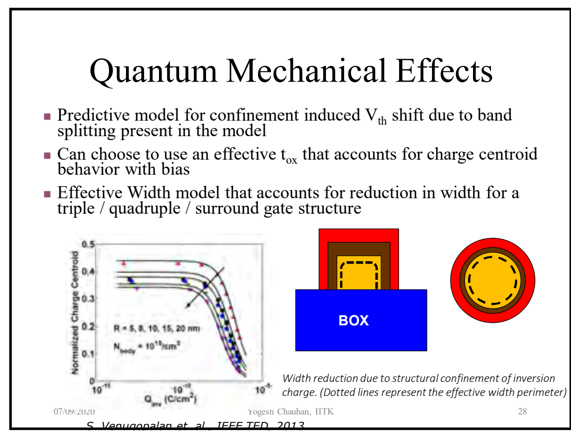
Auth and Plummer, IEEE EDL, 2007


Quantum Mechanical Effects
Predictive model for confinement induced Vth shift due to band splitting present in the model
Can choose to use an effective tox that accounts for charge centroid behavior with bias
Effective Width model that accounts for reduction in width for a triple / quadruple / surround gate structure
BOX
Width reduction due to structural confinement of inversion charge. (Dotted lines represent the effective width perimeter)
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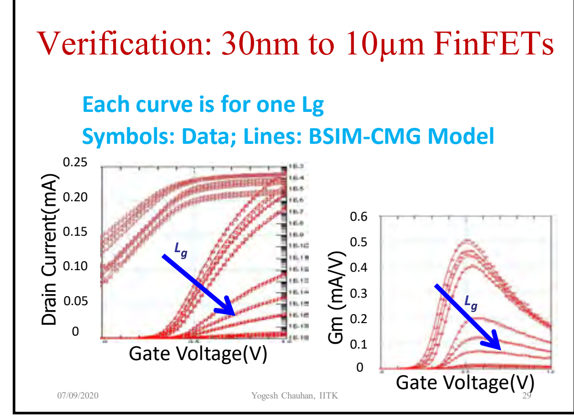
S. Venugopalan et. al., IEEE TED, 2013


Verification: 30nm to 10µm FinFETs
Each curve is for one Lg
Symbols: Data; Lines: BSIM-CMG Model
Drain Current(mA)
Gate Voltage(V)
Gm (mA/V)
Gate Voltage(V)
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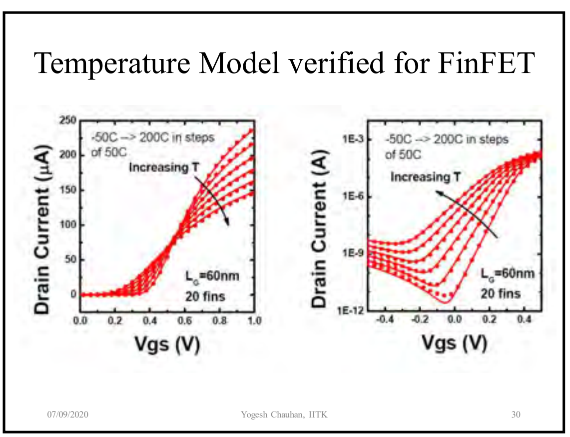
Temperature Model verified for FinFET
-50C --> 200C in steps of 50C
Increasing T
LG=60nm
20 fins
Drain Current (µA)
Drain Current (A)
Vgs (V)
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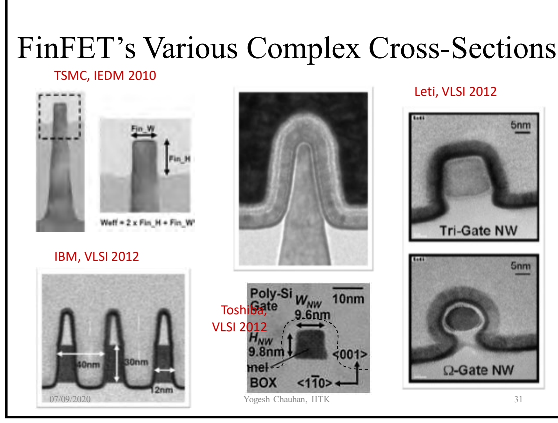
FinFET's Various Complex Cross-Sections
TSMC, IEDM 2010
Leti, VLSI 2012
IBM, VLSI 2012
Toshiba, VLSI 2012
Tri-Gate NW
Ω-Gate NW
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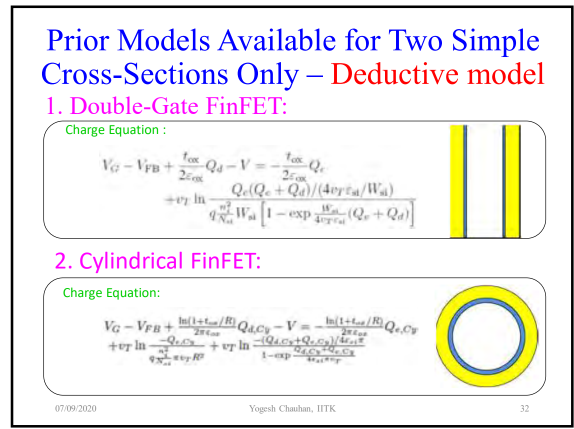
Prior Models Available for Two Simple Cross-Sections Only – Deductive model
1. Double-Gate FinFET:
Charge Equation :
2. Cylindrical FinFET:
Charge Equation:
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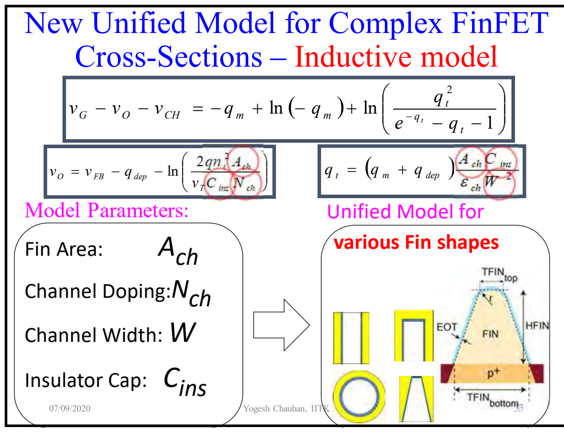
New Unified Model for Complex FinFET Cross-Sections – Inductive model
Model Parameters:
Fin Area:
Channel Doping:
Channel Width:
Insulator Cap:
Unified Model for
various Fin shapes
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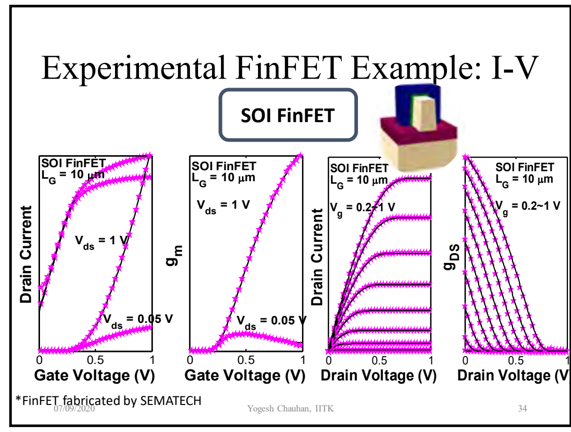
Experimental FinFET Example: I-V
SOI FinFET
Drain Current
Gate Voltage (V)
Drain Voltage (V)
*FinFET fabricated by SEMATECH
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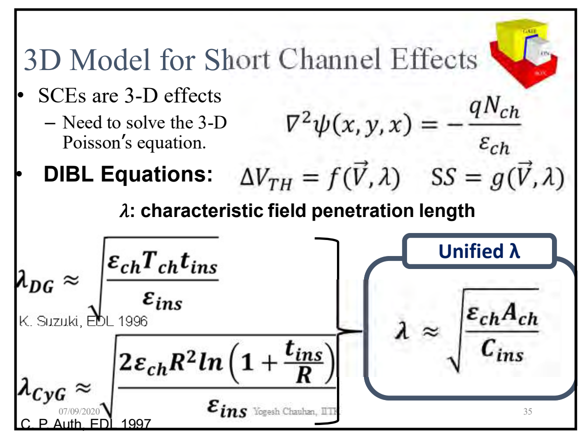
3D Model for Short Channel Effects
SCEs are 3-D effects
– Need to solve the 3-D Poisson's equation.
DIBL Equations:
λ: characteristic field penetration length
K. Suzuki, EDL 1996
C. P. Auth, EDL 1997
Unified λ
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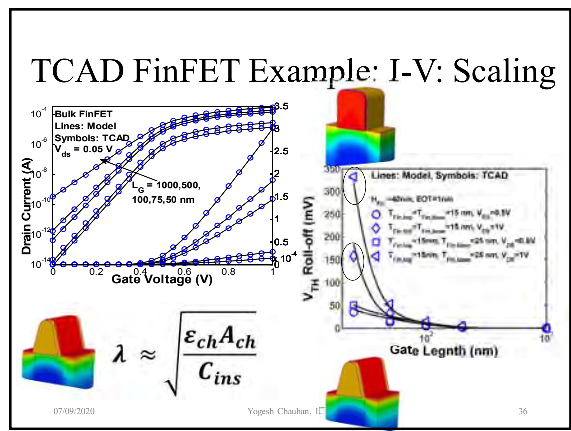
TCAD FinFET Example: I-V: Scaling
Bulk FinFET
Lines: Model
Symbols: TCAD
Drain Current (A)
Gate Voltage (V)
Lines: Model, Symbols: TCAD
Gate Legnth (nm)
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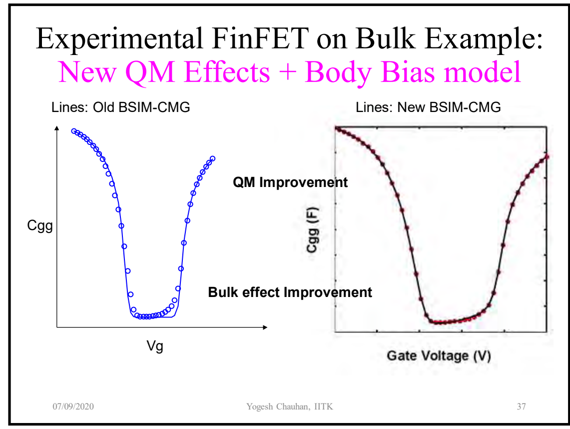

Experimental FinFET on Bulk Example:
New QM Effects + Body Bias model
Lines: Old BSIM-CMG
Lines: New BSIM-CMG
Cgg
Vg
QM Improvement
Bulk effect Improvement
Cgg (F)
Gate Voltage (V)
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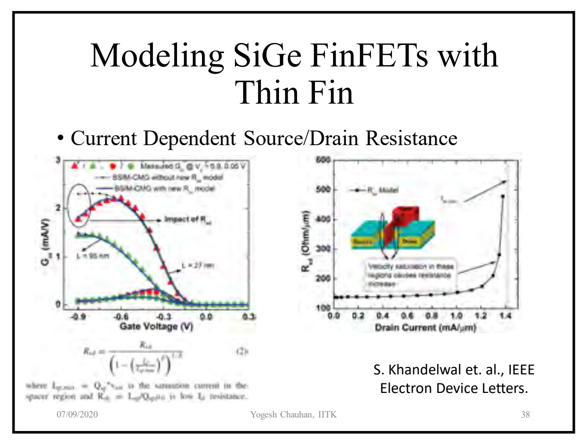

Modeling SiGe FinFETs with Thin Fin
• Current Dependent Source/Drain Resistance
Gate Voltage (V)
Drain Current (mA/μm)
S. Khandelwal et. al., IEEE Electron Device Letters.
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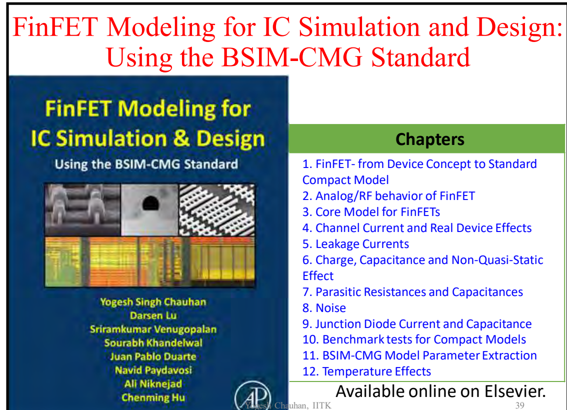

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard
FinFET Modeling for IC Simulation & Design
Using the BSIM-CMG Standard
Yogesh Singh Chauhan
Darsen Lu
Sriramkumar Venugopalan
Sourabh Khandelwal
Juan Pablo Duarte
Navid Paydavosi
Ali Niknejad
Chenming Hu
Chapters
1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
9. Junction Diode Current and Capacitance
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects
Available online on Elsevier.
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Industry Standard FDSOI Compact Model BSIM-IMG for IC Design
INDUSTRY STANDARD FDSOI COMPACT MODEL BSIM-IMG FOR IC DESIGN
Chapters
1. Fully Depleted Silicon on Oxide Transistor and Compact Model
2. Core Model for Independent Multigate MOSFETs
3. Channel Current Model With Real Device Effects in BSIM-IMG
4. Leakage Current and Thermal Effects
5. Model for Terminal Charges and Capacitances in BSIM-IMG
6. Parameter Extraction With BSIM-IMG Compact Model
7. Testing BSIM-IMG Model Quality
8. High-Frequency and Noise Models in BSIM-IMG
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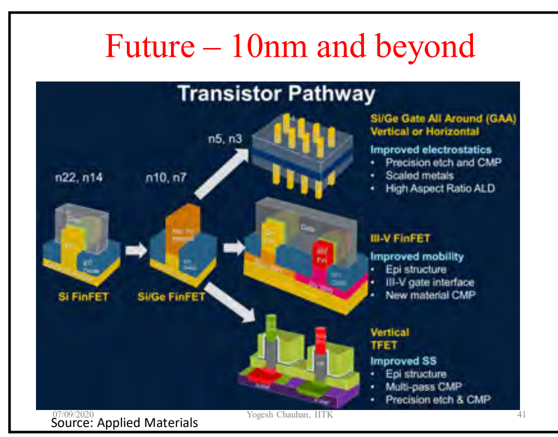

Future – 10nm and beyond
Transistor Pathway
n22, n14
n10, n7
n5, n3
Si FinFET
SiGe FinFET
Si/Ge Gate All Around (GAA) Vertical or Horizontal
Improved electrostatics
Precision etch and CMP
Scaled metals
High Aspect Ratio ALD
III-V FinFET
Improved mobility
Epi structure
III-V gate interface
New material CMP
Vertical TFET
Improved SS
Epi structure
Multi-pass CMP
Precision etch & CMP
Source: Applied Materials
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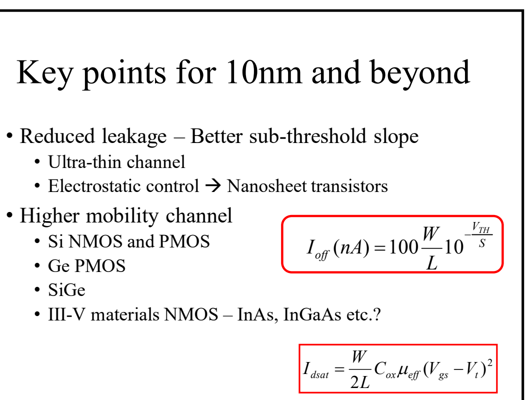

Key points for 10nm and beyond
• Reduced leakage – Better sub-threshold slope
• Ultra-thin channel
• Electrostatic control → Nanosheet transistors
• Higher mobility channel
• Si NMOS and PMOS
• Ge PMOS
• SiGe
• III-V materials NMOS – InAs, InGaAs etc.?
$I_{off}(nA) = 100\frac{W}{L}10^{-\frac{V_{TH}}{S}}$
$I_{dsat} = \frac{W}{2L}C_{ox}\mu_{eff}(V_{gs}-V_t)^2$
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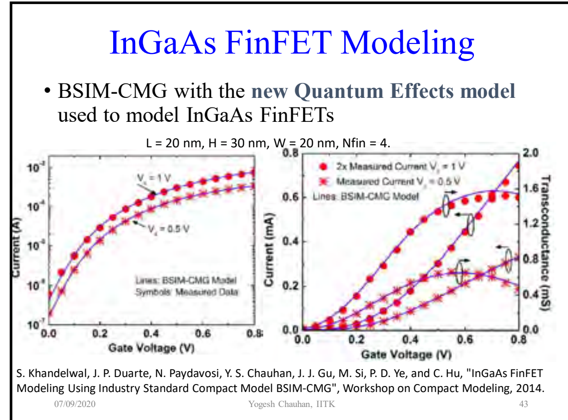
InGaAs FinFET Modeling
• BSIM-CMG with the new Quantum Effects model used to model InGaAs FinFETs
L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.
Lines: BSIM-CMG Model
Symbols: Measured Data
Gate Voltage (V)
Current (A)
Current (mA)
Transconductance (mS)
Lines: BSIM-CMG Model
S. Khandelwal, J. P. Duarte, N. Paydavosi, Y. S. Chauhan, J. J. Gu, M. Si, P. D. Ye, and C. Hu, "InGaAs FinFET Modeling Using Industry Standard Compact Model BSIM-CMG", Workshop on Compact Modeling, 2014.
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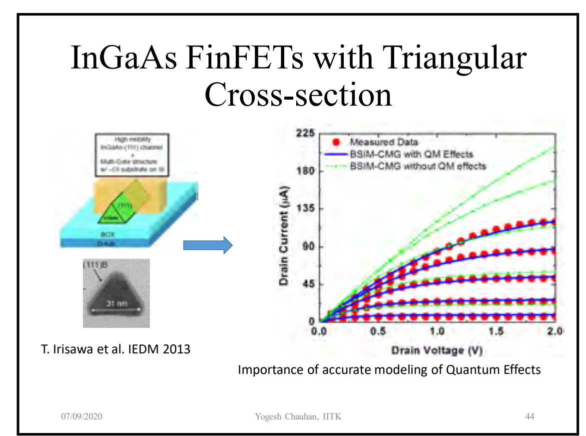
InGaAs FinFETs with Triangular Cross-section
Measured Data
BSIM-CMG with QM Effects
BSIM-CMG without QM effects
Drain Current (μA)
Drain Voltage (V)
T. Irisawa et al. IEDM 2013
Importance of accurate modeling of Quantum Effects
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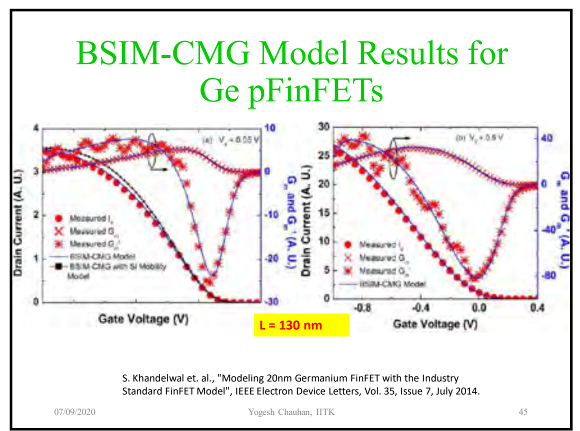
BSIM-CMG Model Results for Ge pFinFETs
Drain Current (A. U.)
Gate Voltage (V)
L = 130 nm
S. Khandelwal et. al., "Modeling 20nm Germanium FinFET with the Industry Standard FinFET Model", IEEE Electron Device Letters, Vol. 35, Issue 7, July 2014.
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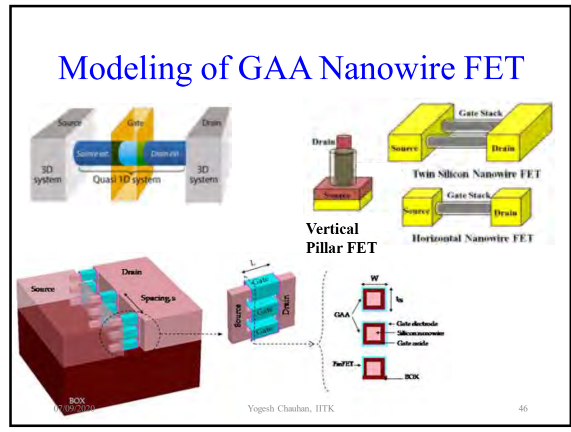
Modeling of GAA Nanowire FET
Vertical Pillar FET
Twin Silicon Nanowire FET
Horizontal Nanowire FET
Source
Drain
Gate Stack
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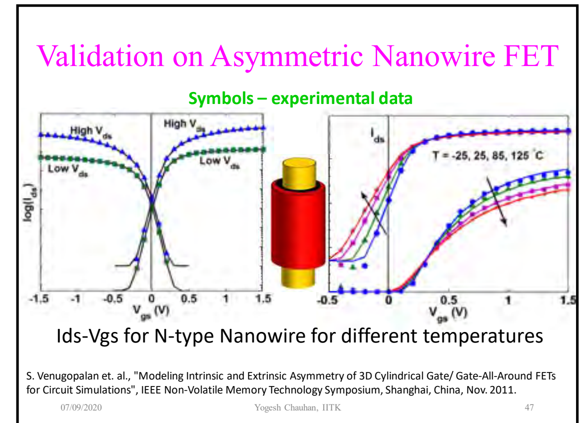
Validation on Asymmetric Nanowire FET
Symbols – experimental data
T = -25, 25, 85, 125 °C
Ids-Vgs for N-type Nanowire for different temperatures
S. Venugopalan et. al., "Modeling Intrinsic and Extrinsic Asymmetry of 3D Cylindrical Gate/ Gate-All-Around FETs for Circuit Simulations", IEEE Non-Volatile Memory Technology Symposium, Shanghai, China, Nov. 2011.
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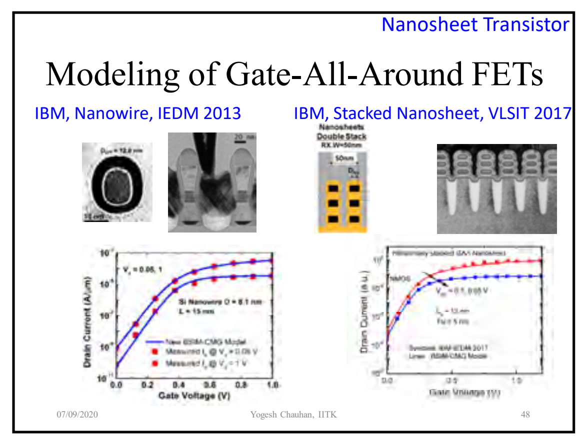
Nanosheet Transistor
Modeling of Gate-All-Around FETs
IBM, Nanowire, IEDM 2013
IBM, Stacked Nanosheet, VLSIT 2017
Drain Current (A/μm)
Gate Voltage (V)
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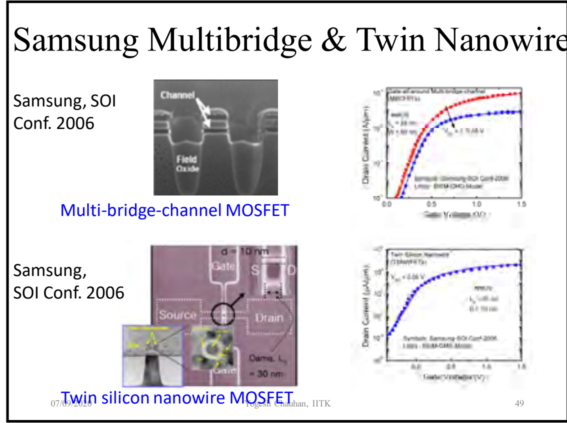
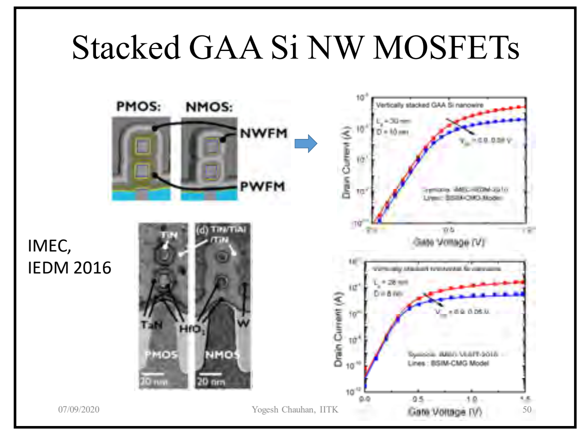
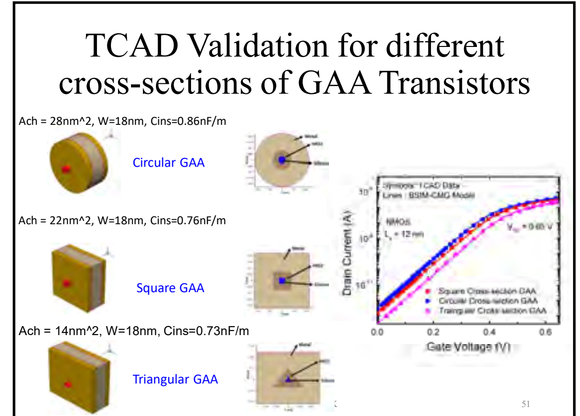


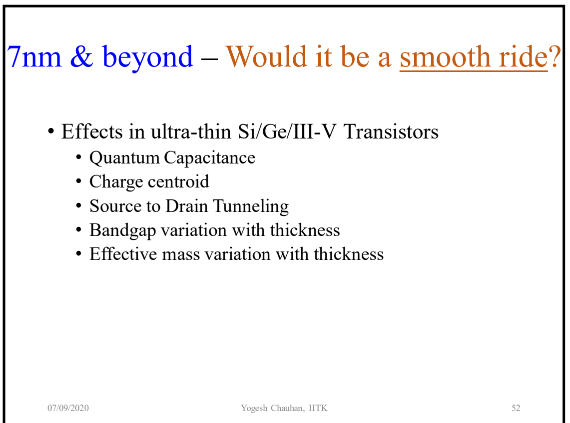
Samsung Multibridge & Twin Nanowire
Samsung, SOI Conf. 2006
Multi-bridge-channel MOSFET
Samsung, SOI Conf. 2006
Twin silicon nanowire MOSFET



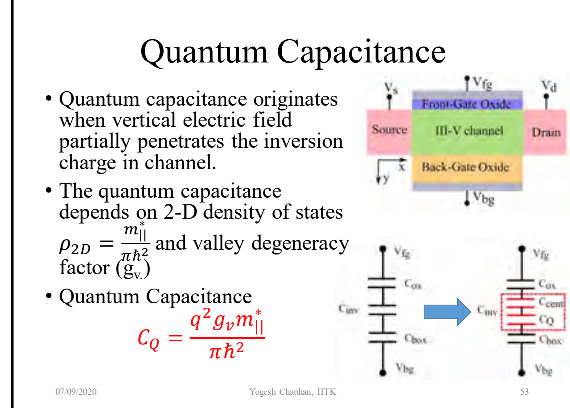
Stacked GAA Si NW MOSFETs
PMOS:
NMOS:
NWFM
PWFM
IMEC, IEDM 2016
Gate Voltage (V)



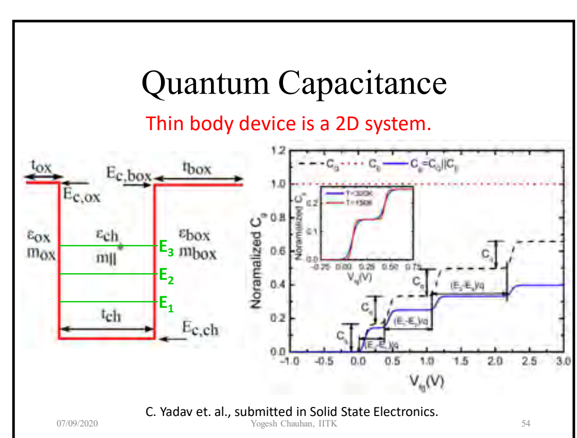
TCAD Validation for different cross-sections of GAA Transistors
Ach = 28nm^2, W=18nm, Cins=0.86nF/m
Circular GAA
Ach = 22nm^2, W=18nm, Cins=0.76nF/m
Square GAA
Ach = 14nm^2, W=18nm, Cins=0.73nF/m
Triangular GAA
Drain Current (A)
Gate Voltage (V)



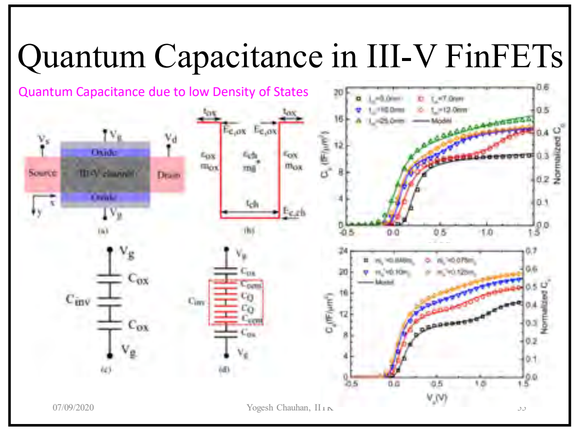
7nm & beyond – Would it be a smooth ride?
Effects in ultra-thin Si/Ge/III-V Transistors
Quantum Capacitance
Charge centroid
Source to Drain Tunneling
Bandgap variation with thickness
Effective mass variation with thickness



Quantum Capacitance
Quantum capacitance originates when vertical electric field partially penetrates the inversion charge in channel.
The quantum capacitance depends on 2-D density of states $\rho_{2D} = \frac{m_{||}^*}{\pi\hbar^2}$ and valley degeneracy factor (g_v)
Quantum Capacitance
$C_Q = \frac{q^2 g_v m_{||}^*}{\pi\hbar^2}$
Source
Front-Gate Oxide
III-V channel
Back-Gate Oxide
Drain



Quantum Capacitance
Thin body device is a 2D system.
Noramalized C_g
V_g(V)
C. Yadav et. al., submitted in Solid State Electronics.


Quantum Capacitance in III-V FinFETs
Quantum Capacitance due to low Density of States
Source
Oxide
III-V channel
Oxide
Drain
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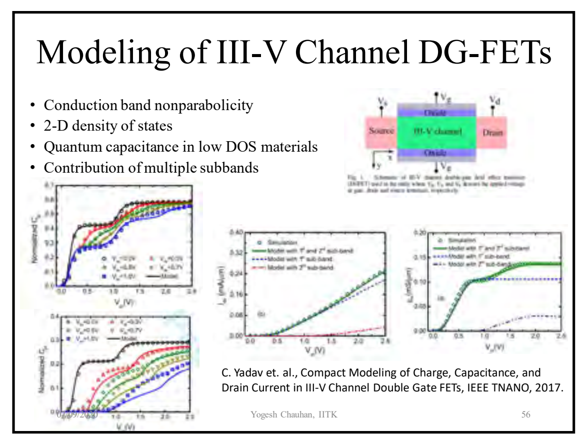
Modeling of III-V Channel DG-FETs
• Conduction band nonparabolicity
• 2-D density of states
• Quantum capacitance in low DOS materials
• Contribution of multiple subbands
Source
III-V channel
Drain
C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.
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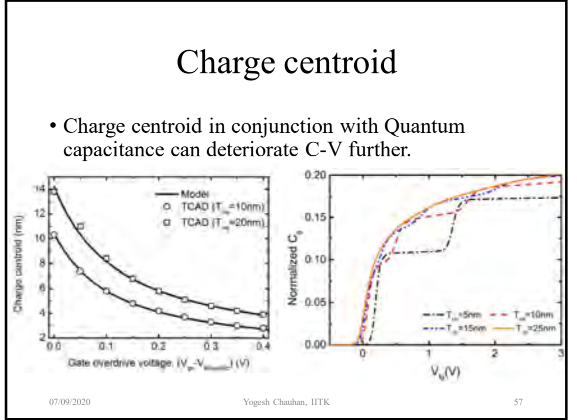
Charge centroid
• Charge centroid in conjunction with Quantum capacitance can deteriorate C-V further.
Model
Charge centroid (nm)
Normalized C_g
V_g(V)
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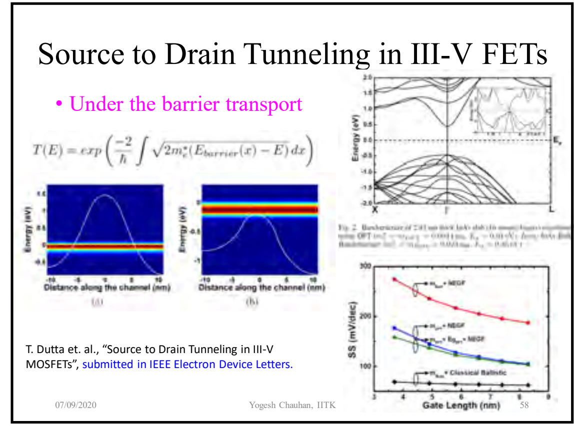
Source to Drain Tunneling in III-V FETs
• Under the barrier transport
$$T(E) = exp\left(\frac{-2}{\hbar}\int\sqrt{2m_t^*(E_{barrier}(x) - E)}\,dx\right)$$
Distance along the channel (nm)
Energy (eV)
SS (mV/dec)
Gate Length (nm)
T. Dutta et. al., "Source to Drain Tunneling in III-V MOSFETs", submitted in IEEE Electron Device Letters.
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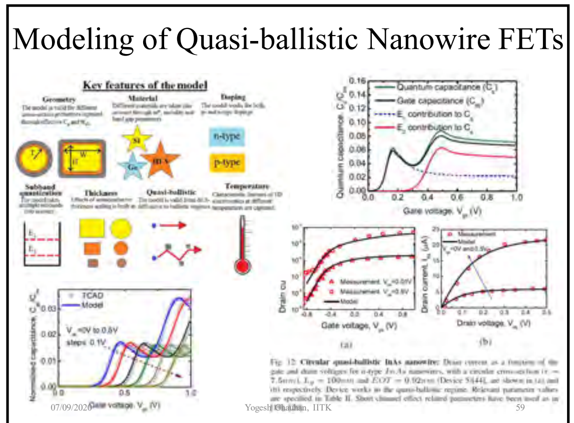
Modeling of Quasi-ballistic Nanowire FETs
Key features of the model
Geometry
Material
Doping
n-type
p-type
Thickness
Quasi-ballistic
Temperature
Quantum capacitance
Gate voltage, V_g (V)
Drain voltage, V_d (V)
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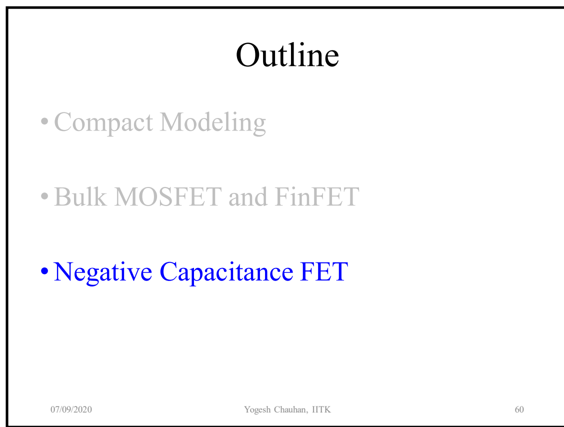
Outline
• Compact Modeling
• Bulk MOSFET and FinFET
• Negative Capacitance FET
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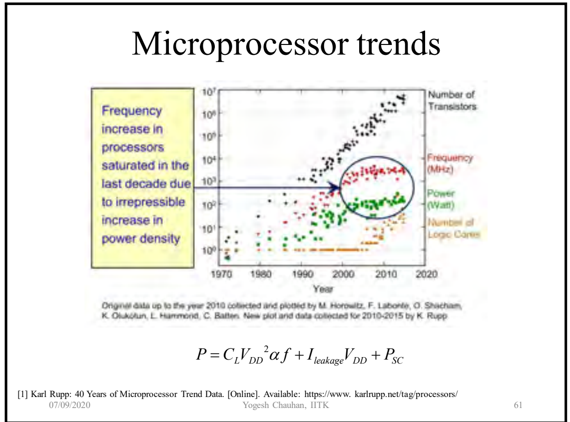
Microprocessor trends
Frequency increase in processors saturated in the last decade due to irrepressible increase in power density
Number of Transistors
Frequency (MHz)
Power (Watt)
Number of Logic Cores
Year
$P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC}$
[1] Karl Rupp: 40 Years of Microprocessor Trend Data. [Online]. Available: https://www. karlrupp.net/tag/processors/
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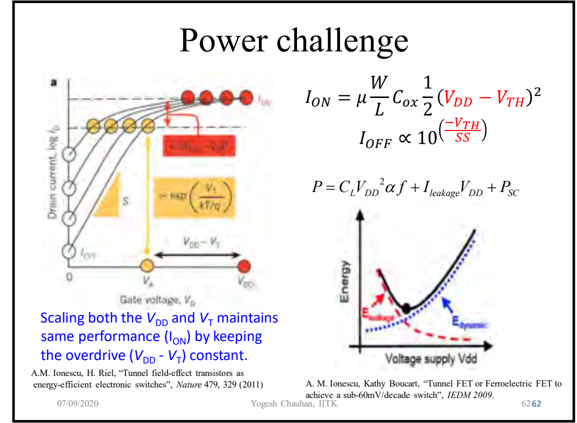
Power challenge
$I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$
$I_{OFF} \propto 10^{\left(\frac{-V_{TH}}{SS}\right)}$
$P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC}$
Scaling both the V_{DD} and V_T maintains same performance (I_{ON}) by keeping the overdrive (V_{DD} - V_T) constant.
Gate voltage, V_G
Energy
Voltage supply Vdd
A.M. Ionescu, H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", Nature 479, 329 (2011)
A. M. Ionescu, Kathy Boucart, "Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch", IEDM 2009.
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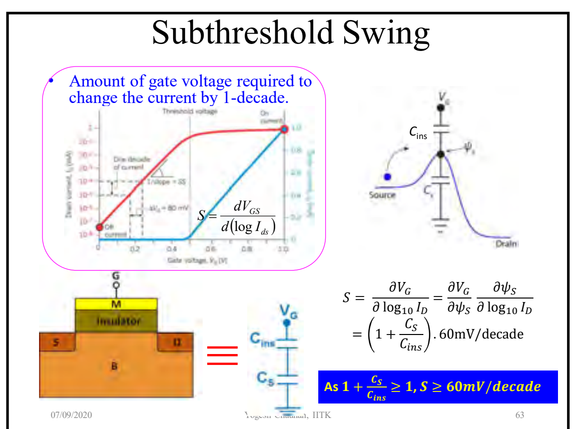
Subthreshold Swing
Amount of gate voltage required to change the current by 1-decade.
$S = \frac{dV_{GS}}{d(\log I_{ds})}$
$S = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial \psi_S} \frac{\partial \psi_S}{\partial \log_{10} I_D}$
$= \left(1 + \frac{C_S}{C_{ins}}\right)$. 60mV/decade
As $1 + \frac{C_S}{C_{ins}} \geq 1, S \geq 60mV/decade$
M
Insulator
S
D
B
C_{ins}
C_S
V_G
Source
Drain
07/09/2020
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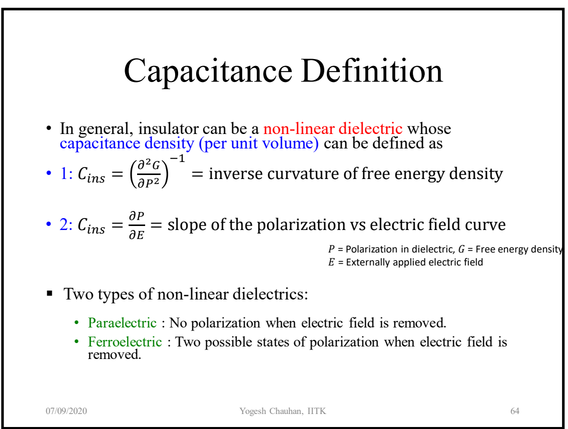
Capacitance Definition
In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as
1: $C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1}$ = inverse curvature of free energy density
2: $C_{ins} = \frac{\partial P}{\partial E}$ = slope of the polarization vs electric field curve
P = Polarization in dielectric, G = Free energy density
E = Externally applied electric field
Two types of non-linear dielectrics:
Paraelectric : No polarization when electric field is removed.
Ferroelectric : Two possible states of polarization when electric field is removed.
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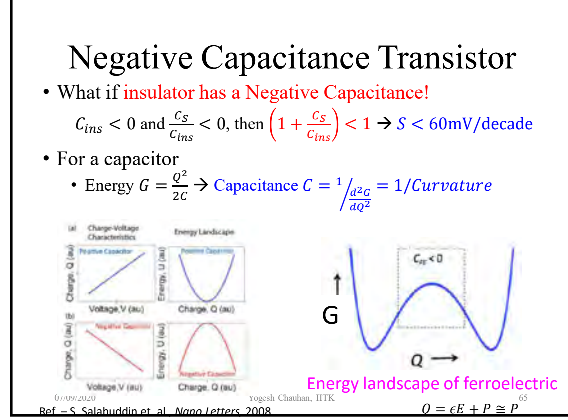
Negative Capacitance Transistor
What if insulator has a Negative Capacitance!
$C_{ins} < 0$ and $\frac{C_S}{C_{ins}} < 0$, then $\left(1 + \frac{C_S}{C_{ins}}\right) < 1 \rightarrow S < 60mV/decade$
For a capacitor
Energy $G = \frac{Q^2}{2C} \rightarrow$ Capacitance $C = 1 / \frac{d^2G}{dQ^2} = 1/Curvature$
G
Q
Energy landscape of ferroelectric
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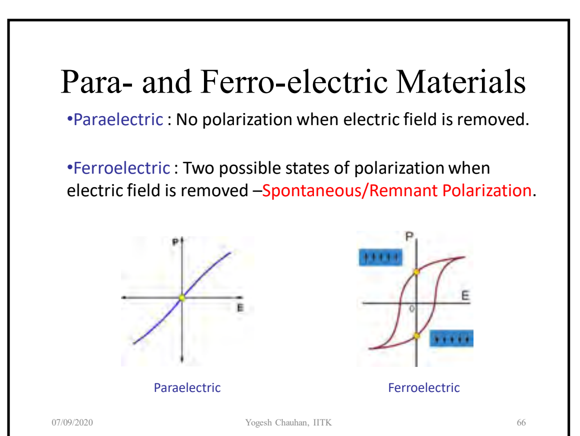
Ref – S. Salahuddin et. al, Nano Letters, 2008
$Q = \epsilon E + P \cong P$


Para- and Ferro-electric Materials
Paraelectric : No polarization when electric field is removed.
Ferroelectric : Two possible states of polarization when electric field is removed –Spontaneous/Remnant Polarization.
P
E
Paraelectric
Ferroelectric
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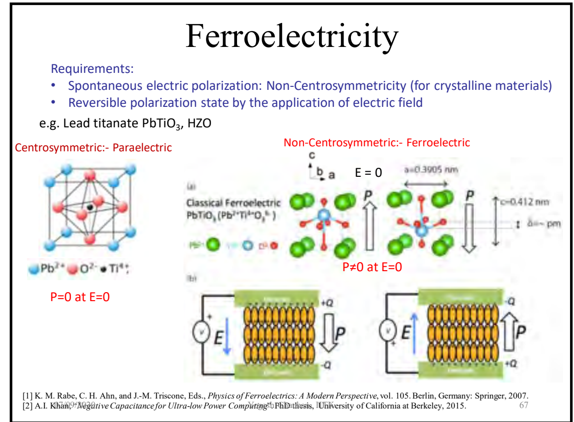

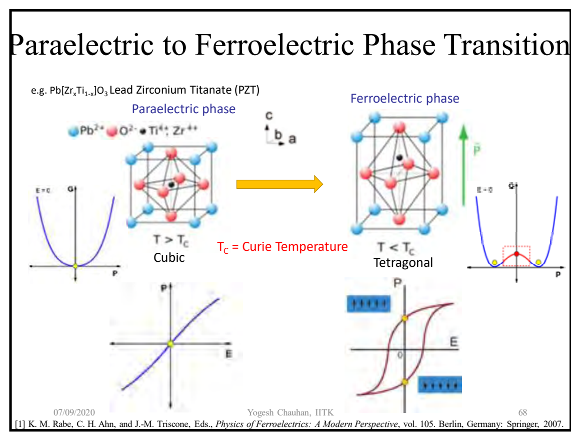

Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as
  $$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$
- α and β can be +ve or –ve but γ is always +ve for stability reasons.
- Dynamics of G is given by $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$ — δ = Polarization damping factor
- In the steady state, $\frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

For $\alpha > 0$ and at $E = 0$, there exist only one real root $P = 0$
A Paraelectric Material

For $\alpha < 0$ and at $E = 0$, there exit three real roots $P = 0, \pm P_r$ where $P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$
A Ferroelectric Material has a non-zero P at zero E.

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Assumptions

Free energy of a non-linear dielectric
$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- Polarization and Electric field are uniaxial. (perpendicular to electrodes)
- Polarization and Electric field magnitudes are uniform throughout the ferroelectric.
- Piezo-electricity is ignored.

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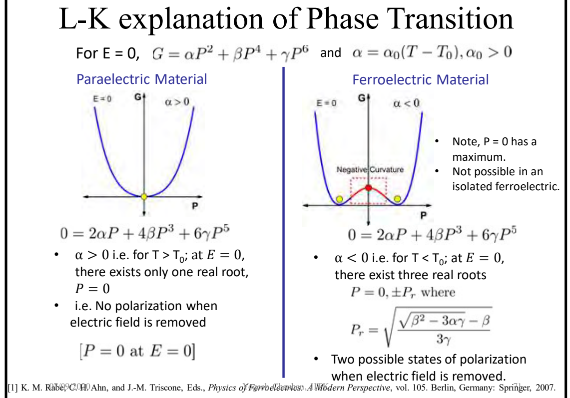

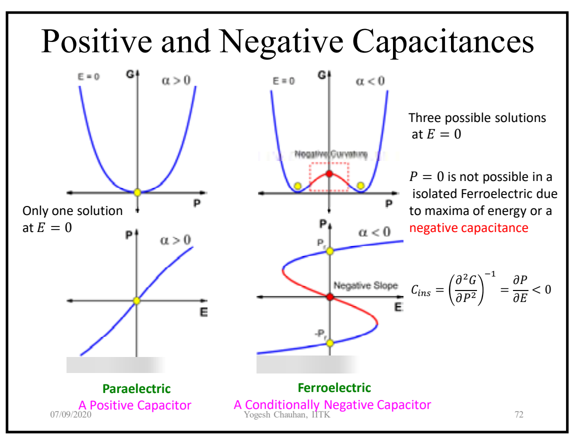

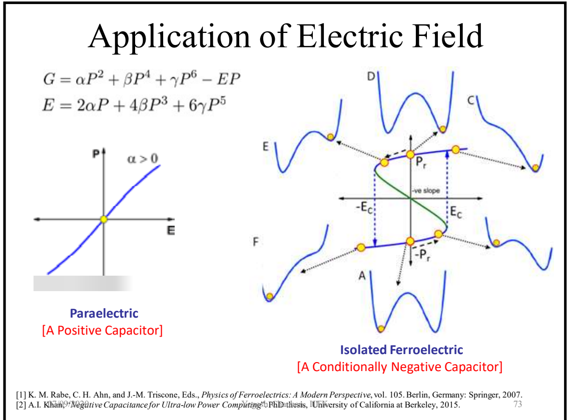
Application of Electric Field
$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$
$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$
Paraelectric
[A Positive Capacitor]
Isolated Ferroelectric
[A Conditionally Negative Capacitor]
[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., Physics of Ferroelectrics: A Modern Perspective, vol. 105. Berlin, Germany: Springer, 2007.
[2] A.I. Khan, "Negative Capacitance for Ultra-low Power Computing", PhD thesis, University of California at Berkeley, 2015.
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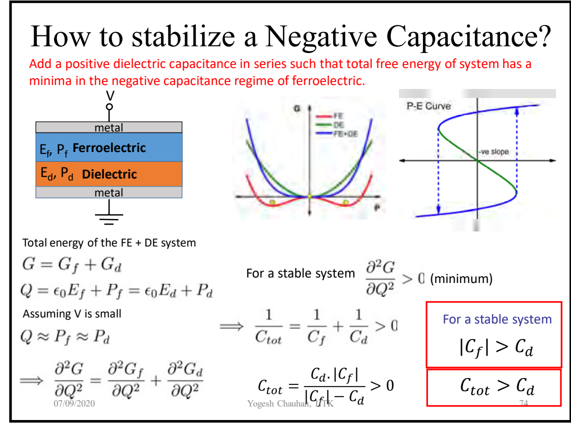
How to stabilize a Negative Capacitance?
Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.
metal
E_f, P_f Ferroelectric
E_d, P_d Dielectric
metal
P-E Curve
Total energy of the FE + DE system
$G = G_f + G_d$
$Q = \epsilon_0 E_f + P_f = \epsilon_0 E_d + P_d$
Assuming V is small
$Q \approx P_f \approx P_d$
$\implies \frac{\partial^2 G}{\partial Q^2} = \frac{\partial^2 G_f}{\partial Q^2} + \frac{\partial^2 G_d}{\partial Q^2}$
For a stable system $\frac{\partial^2 G}{\partial Q^2} > 0$ (minimum)
$\implies \frac{1}{C_{tot}} = \frac{1}{C_f} + \frac{1}{C_d} > 0$
$C_{tot} = \frac{C_d \cdot |C_f|}{|C_f| - C_d} > 0$
For a stable system
$|C_f| > C_d$
$C_{tot} > C_d$
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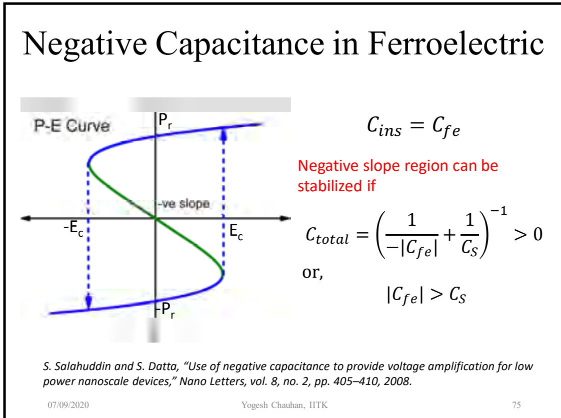
Negative Capacitance in Ferroelectric
P-E Curve
-ve slope
$C_{ins} = C_{fe}$
Negative slope region can be stabilized if
$C_{total} = \left(\frac{1}{-|C_{fe}|} + \frac{1}{C_S}\right)^{-1} > 0$
or,
$|C_{fe}| > C_S$
S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008.
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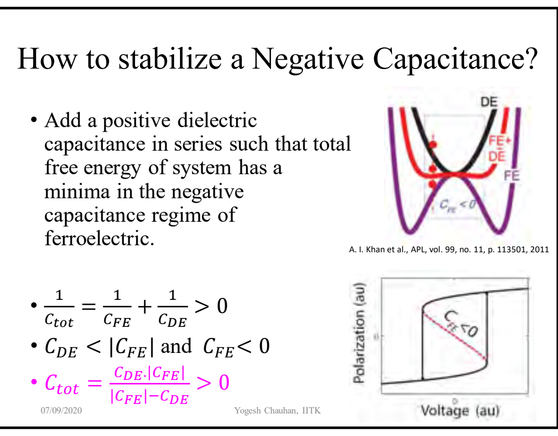
How to stabilize a Negative Capacitance?
Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.
A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011
$\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0$
$C_{DE} < |C_{FE}|$ and $C_{FE} < 0$
$C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0$
Polarization (au)
Voltage (au)
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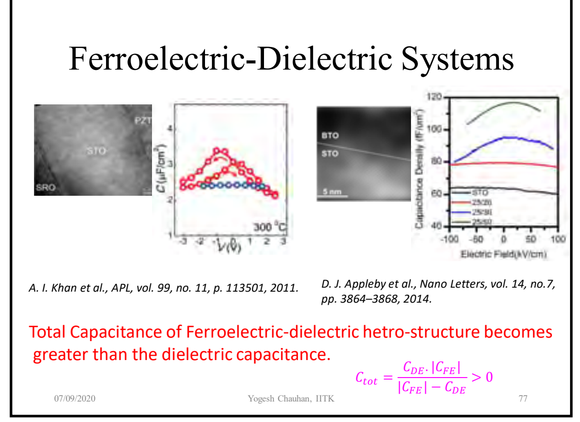
Ferroelectric-Dielectric Systems
A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011.
D. J. Appleby et al., Nano Letters, vol. 14, no.7, pp. 3864–3868, 2014.
Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.
$C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0$
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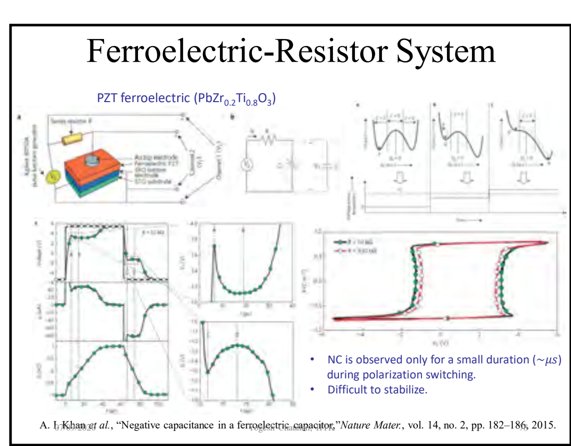
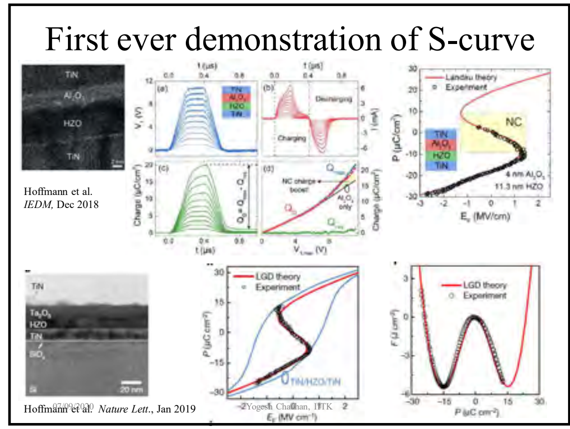
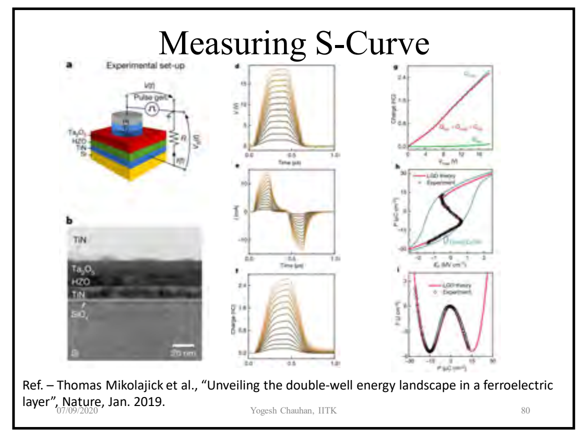

Ferroelectric-Resistor System
PZT ferroelectric ($PbZr_{0.2}Ti_{0.8}O_3$)
NC is observed only for a small duration (~μs) during polarization switching.
Difficult to stabilize.
A. I. Khan et al., "Negative capacitance in a ferroelectric capacitor," Nature Mater., vol. 14, no. 2, pp. 182–186, 2015.


First ever demonstration of S-curve
Hoffmann et al.
IEDM, Dec 2018
Hoffmann et al. Nature Lett., Jan 2019


Measuring S-Curve
Ref. – Thomas Mikolajick et al., "Unveiling the double-well energy landscape in a ferroelectric layer", Nature, Jan. 2019.
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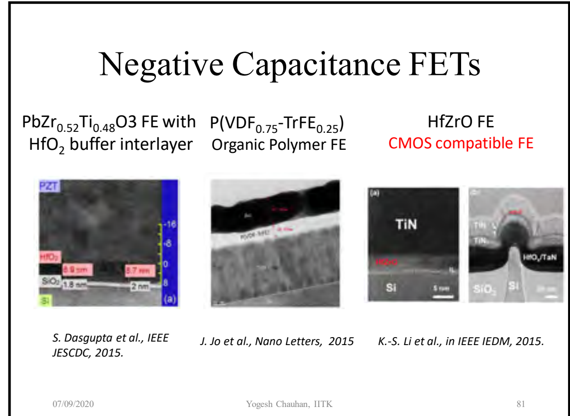
Negative Capacitance FETs
PbZr0.52Ti0.48O3 FE with HfO2 buffer interlayer
P(VDF0.75-TrFE0.25) Organic Polymer FE
HfZrO FE
CMOS compatible FE
S. Dasgupta et al., IEEE JESCDC, 2015.
J. Jo et al., Nano Letters, 2015
K.-S. Li et al., in IEEE IEDM, 2015.
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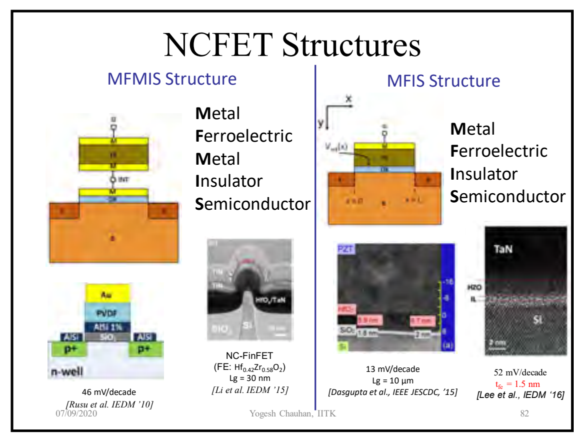
NCFET Structures
MFMIS Structure
MFIS Structure
Metal
Ferroelectric
Metal
Insulator
Semiconductor
Metal
Ferroelectric
Insulator
Semiconductor
46 mV/decade
[Rusu et al. IEDM '10]
NC-FinFET
Lg = 30 nm
[Li et al. IEDM '15]
13 mV/decade
Lg = 10 μm
[Dasgupta et al., IEEE JESCDC, '15]
52 mV/decade
[Lee et al., IEDM '16]
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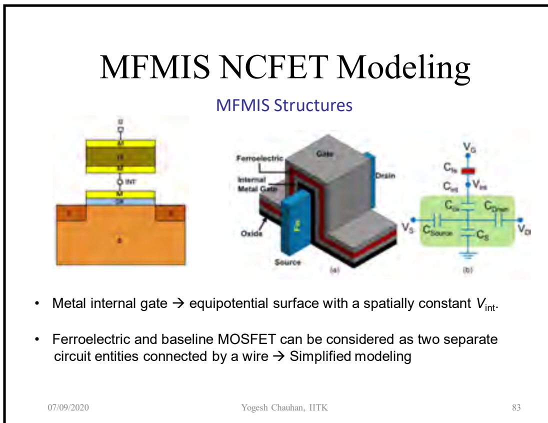
MFMIS NCFET Modeling
MFMIS Structures
Ferroelectric
Gate
Internal Metal Gate
Drain
Oxide
Source
Metal internal gate → equipotential surface with a spatially constant Vint.
Ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire → Simplified modeling
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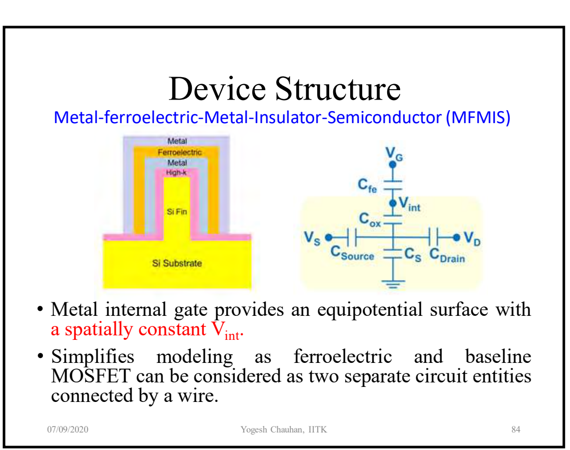
Device Structure
Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)
Metal
Ferroelectric
Metal
High-k
Si Fin
Si Substrate
Metal internal gate provides an equipotential surface with a spatially constant Vint.
Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.
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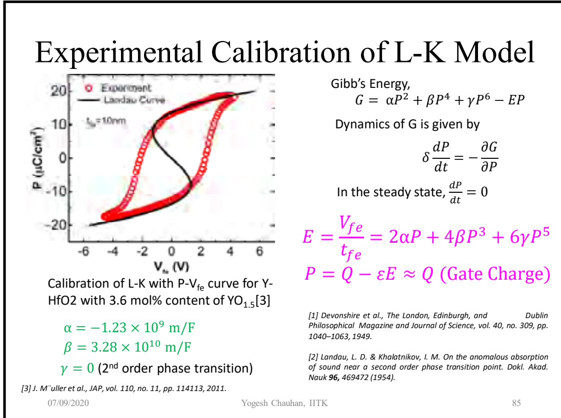

Experimental Calibration of L-K Model
Experiment
Landau Curve
P (μC/cm²)
V_fe (V)
Calibration of L-K with P-V_fe curve for Y-HfO2 with 3.6 mol% content of YO1.5[3]
α = −1.23 × 10⁹ m/F
β = 3.28 × 10¹⁰ m/F
γ = 0 (2nd order phase transition)
[3] J. M¨uller et al., JAP, vol. 110, no. 11, pp. 114113, 2011.
Gibb's Energy,
G = αP² + βP⁴ + γP⁶ − EP
Dynamics of G is given by
δ dP/dt = −∂G/∂P
In the steady state, dP/dt = 0
E = V_fe/t_fe = 2αP + 4βP³ + 6γP⁵
P = Q − εE ≈ Q (Gate Charge)
[1] Devonshire et al., The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 40, no. 309, pp. 1040–1063, 1949.
[2] Landau, L. D. & Khalatnikov, I. M. On the anomalous absorption of sound near a second order phase transition point. Dokl. Akad. Nauk 96, 469472 (1954).
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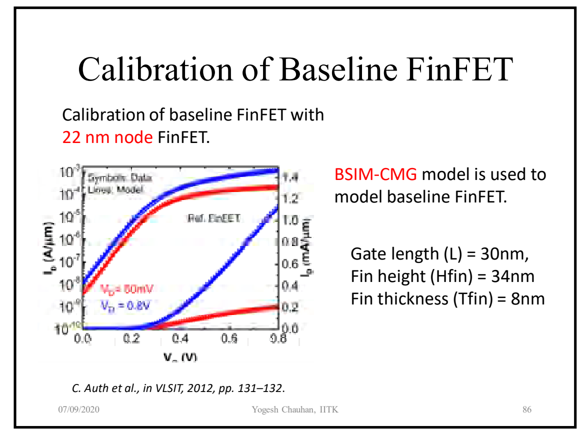

Calibration of Baseline FinFET
Calibration of baseline FinFET with
22 nm node FinFET.
Symbols: Data
Lines: Model
Ref. FinFET
V_D = 50mV
V_D = 0.8V
I_D (A/μm)
I_D (mA/μm)
V_G (V)
BSIM-CMG model is used to model baseline FinFET.
Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm
C. Auth et al., in VLSIT, 2012, pp. 131–132.
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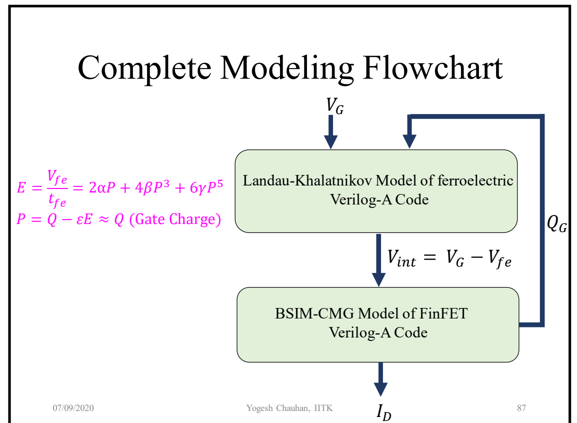

Complete Modeling Flowchart
V_G
E = V_fe/t_fe = 2αP + 4βP³ + 6γP⁵
P = Q − εE ≈ Q (Gate Charge)
Landau-Khalatnikov Model of ferroelectric
Verilog-A Code
Q_G
V_int = V_G − V_fe
BSIM-CMG Model of FinFET
Verilog-A Code
I_D
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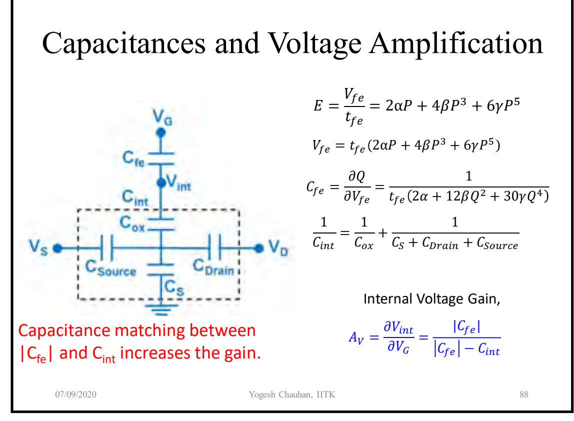

Capacitances and Voltage Amplification
V_G
C_fe
V_int
C_int
C_ox
V_S
V_D
C_Source
C_Drain
C_S
E = V_fe/t_fe = 2αP + 4βP³ + 6γP⁵
V_fe = t_fe(2αP + 4βP³ + 6γP⁵)
C_fe = ∂Q/∂V_fe = 1/(t_fe(2α + 12βQ² + 30γQ⁴))
1/C_int = 1/C_ox + 1/(C_S + C_Drain + C_Source)
Internal Voltage Gain,
A_V = ∂V_int/∂V_G = |C_fe|/(|C_fe| − C_int)
Capacitance matching between |C_fe| and C_int increases the gain.
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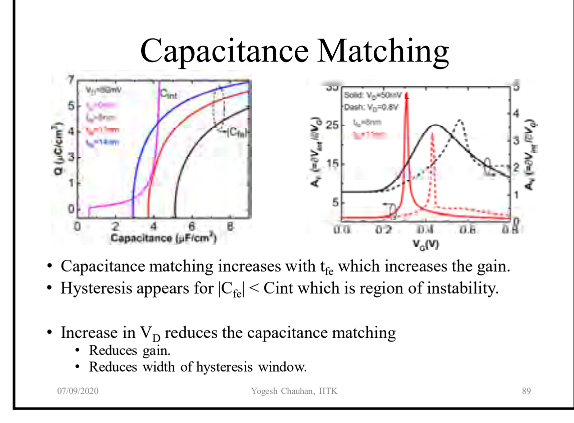

Capacitance Matching
V_D=50mV
C_int
|C_fe|
Q (μC/cm²)
Capacitance (μF/cm²)
Solid: V_D=50mV
Dash: V_D=0.8V
V_G(V)
• Capacitance matching increases with t_fe which increases the gain.
• Hysteresis appears for |C_fe| < Cint which is region of instability.
• Increase in V_D reduces the capacitance matching
• Reduces gain.
• Reduces width of hysteresis window.
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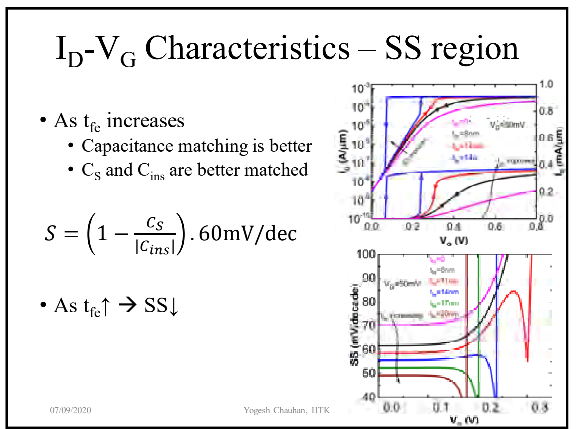

I_D-V_G Characteristics – SS region
• As t_fe increases
• Capacitance matching is better
• C_S and C_ins are better matched
S = (1 − C_S/|C_ins|) . 60mV/dec
• As t_fe↑ → SS↓
I_D (A/μm)
I_D (mA/μm)
V_G (V)
SS (mV/decade)
V_G (V)
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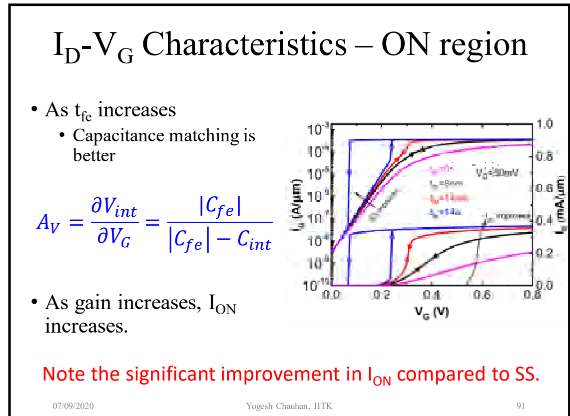
ID-VG Characteristics – ON region
• As tfe increases
• Capacitance matching is better
$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$
• As gain increases, ION increases.
Note the significant improvement in ION compared to SS.
VG (V)
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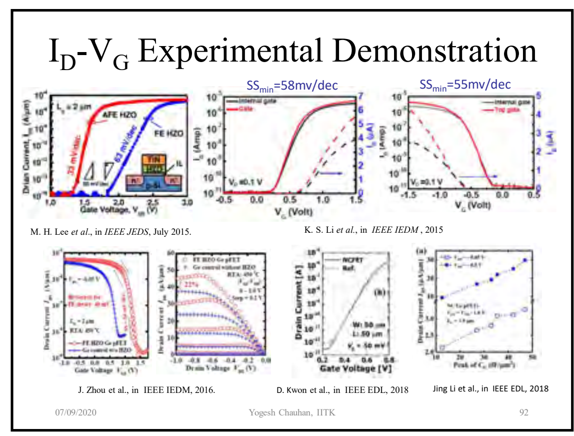
ID-VG Experimental Demonstration
SSmin=58mv/dec
SSmin=55mv/dec
M. H. Lee et al., in IEEE JEDS, July 2015.
K. S. Li et al., in IEEE IEDM, 2015
J. Zhou et al., in IEEE IEDM, 2016.
D. Kwon et al., in IEEE EDL, 2018
Jing Li et al., in IEEE EDL, 2018
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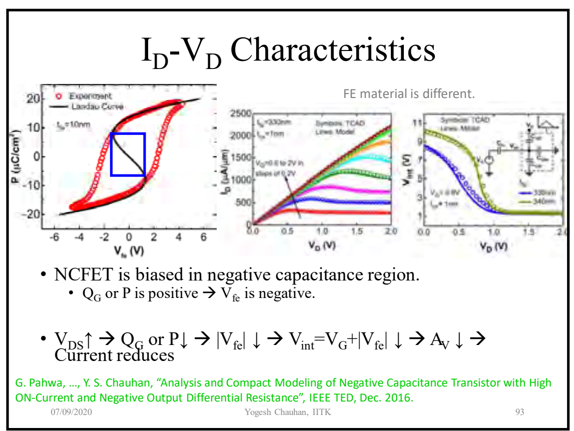
ID-VD Characteristics
FE material is different.
VD (V)
• NCFET is biased in negative capacitance region.
• QG or P is positive → Vfe is negative.
• VDS↑ → QG or P↓ → |Vfe| ↓ → Vint=VG+|Vfe| ↓ → AV ↓ → Current reduces
G. Pahwa, ..., Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance", IEEE TED, Dec. 2016.
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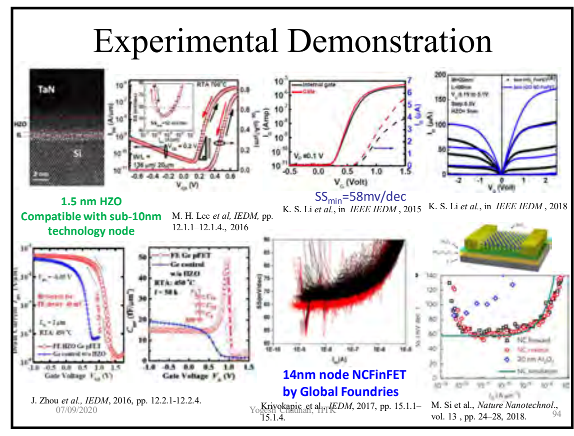
Experimental Demonstration
1.5 nm HZO
Compatible with sub-10nm technology node
M. H. Lee et al, IEDM, pp. 12.1.1–12.1.4., 2016
SSmin=58mv/dec
K. S. Li et al., in IEEE IEDM, 2015
K. S. Li et al., in IEEE IEDM, 2018
14nm node NCFinFET by Global Foundries
J. Zhou et al., IEDM, 2016, pp. 12.2.1-12.2.4.
Krivokapic et al., IEDM, 2017, pp. 15.1.1–15.1.4.
M. Si et al., Nature Nanotechnol., vol. 13, pp. 24–28, 2018.
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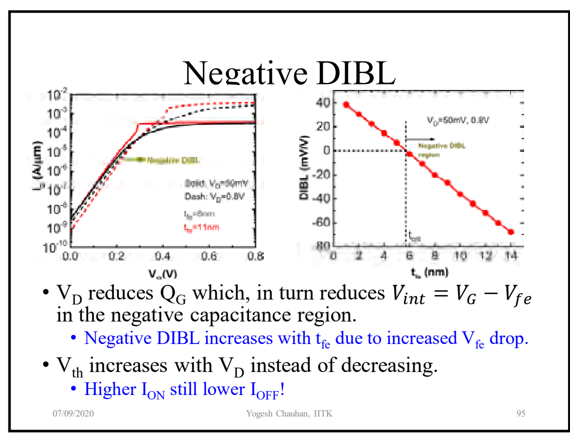
Negative DIBL
Negative DIBL
Solid: VD=50mV
Dash: VD=0.8V
VD=50mV, 0.8V
Negative DIBL region
tfe (nm)
• VD reduces QG which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
• Negative DIBL increases with tfe due to increased Vfe drop.
• Vth increases with VD instead of decreasing.
• Higher ION still lower IOFF!
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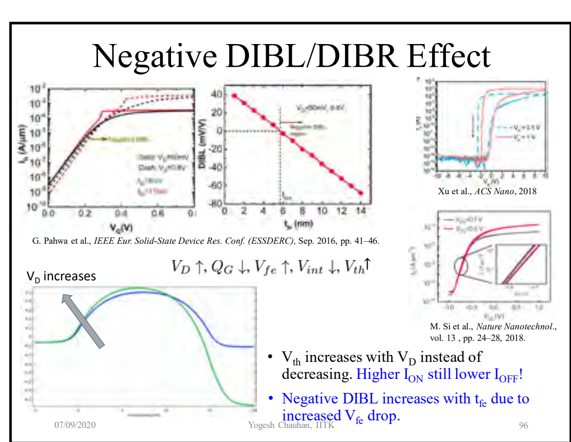
Negative DIBL/DIBR Effect
G. Pahwa et al., IEEE Eur. Solid-State Device Res. Conf. (ESSDERC), Sep. 2016, pp. 41–46.
Xu et al., ACS Nano, 2018
$V_D \uparrow, Q_G \downarrow, V_{fe} \uparrow, V_{int} \downarrow, V_{th} \uparrow$
VD increases
M. Si et al., Nature Nanotechnol., vol. 13, pp. 24–28, 2018.
• Vth increases with VD instead of decreasing. Higher ION still lower IOFF!
• Negative DIBL increases with tfe due to increased Vfe drop.
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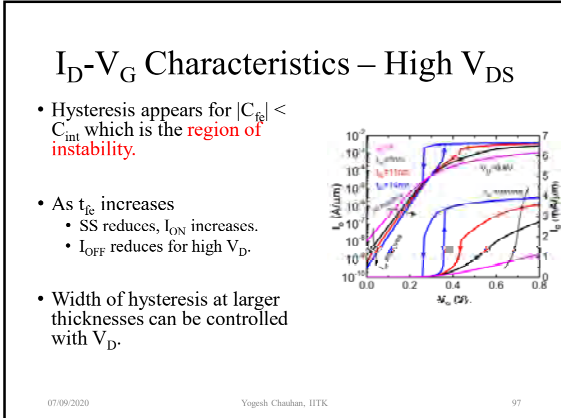
ID-VG Characteristics – High VDS
Hysteresis appears for |Cfe| < Cint which is the region of instability.
As tfe increases
SS reduces, ION increases.
IOFF reduces for high VD.
Width of hysteresis at larger thicknesses can be controlled with VD.
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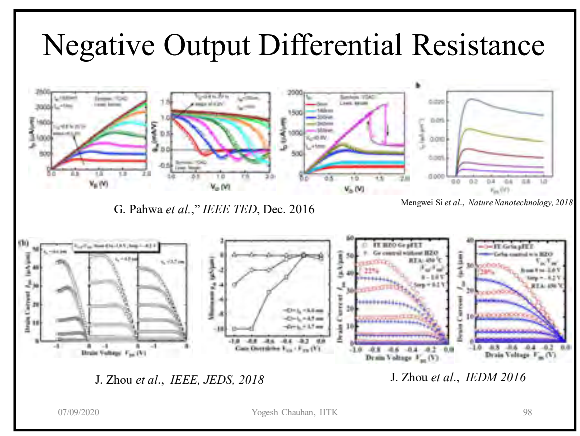
Negative Output Differential Resistance
G. Pahwa et al.," IEEE TED, Dec. 2016
Mengwei Si et al., Nature Nanotechnology, 2018
J. Zhou et al., IEEE, JEDS, 2018
J. Zhou et al., IEDM 2016
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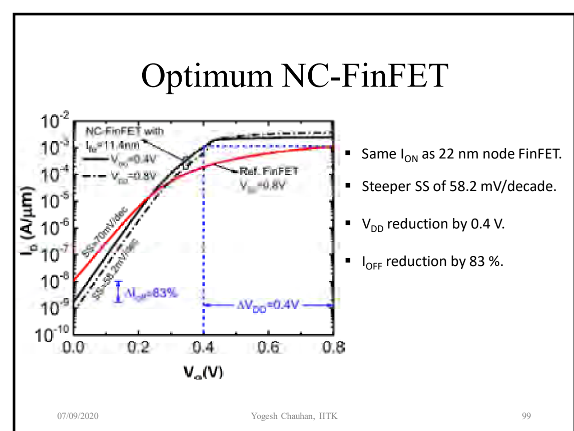
Optimum NC-FinFET
Same ION as 22 nm node FinFET.
Steeper SS of 58.2 mV/decade.
VDD reduction by 0.4 V.
IOFF reduction by 83 %.
NC-FinFET with
Ref. FinFET
VG(V)
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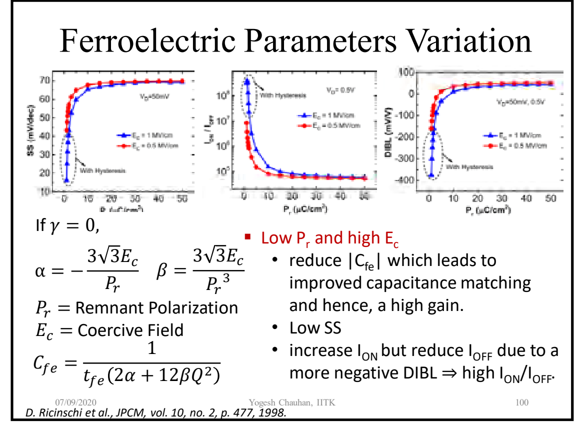
Ferroelectric Parameters Variation
If γ = 0,
Pr = Remnant Polarization
Ec = Coercive Field
Low Pr and high Ec
reduce |Cfe| which leads to improved capacitance matching and hence, a high gain.
Low SS
increase ION but reduce IOFF due to a more negative DIBL ⇒ high ION/IOFF.
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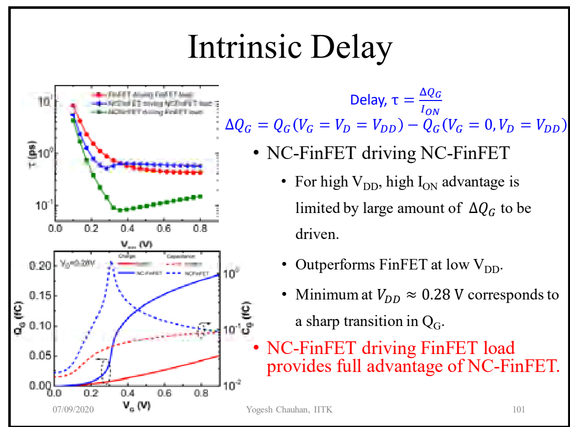
D. Ricinschi et al., JPCM, vol. 10, no. 2, p. 477, 1998.


Intrinsic Delay
NC-FinFET driving NC-FinFET
For high VDD, high ION advantage is limited by large amount of ΔQG to be driven.
Outperforms FinFET at low VDD.
Minimum at VDD ≈ 0.28 V corresponds to a sharp transition in QG.
NC-FinFET driving FinFET load provides full advantage of NC-FinFET.
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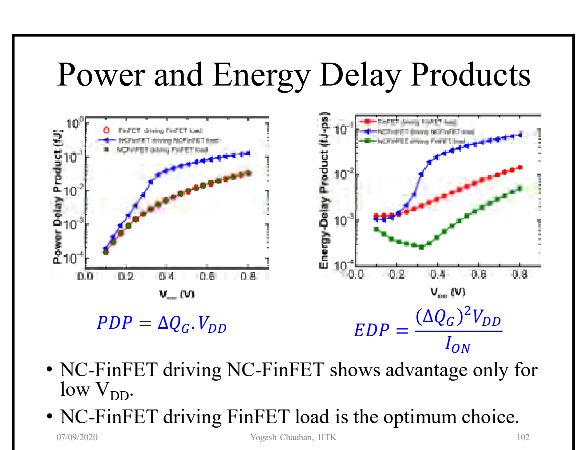
Power and Energy Delay Products
NC-FinFET driving NC-FinFET shows advantage only for low VDD.
NC-FinFET driving FinFET load is the optimum choice.
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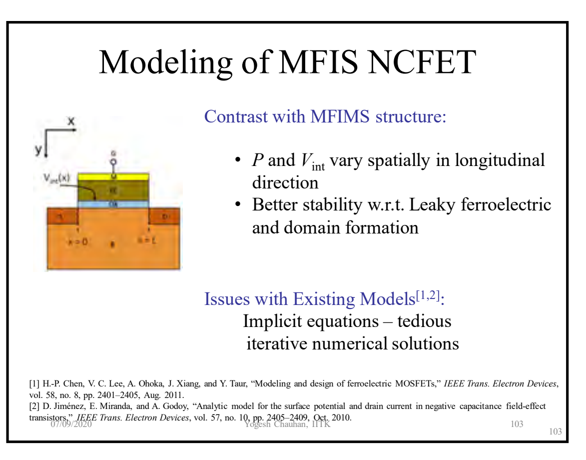
Modeling of MFIS NCFET
Contrast with MFIMS structure:
• P and V_int vary spatially in longitudinal direction
• Better stability w.r.t. Leaky ferroelectric and domain formation
Issues with Existing Models[1,2]:
Implicit equations – tedious iterative numerical solutions
[1] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.
[2] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," IEEE Trans. Electron Devices, vol. 57, no. 10, pp. 2405–2409, Oct. 2010.
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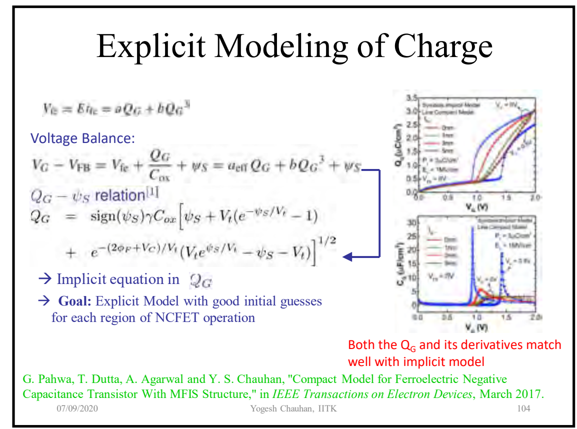
Explicit Modeling of Charge
Voltage Balance:
Q_G – ψ_S relation[1]
→ Implicit equation in Q_G
→ Goal: Explicit Model with good initial guesses for each region of NCFET operation
Both the Q_G and its derivatives match well with implicit model
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," in IEEE Transactions on Electron Devices, March 2017.
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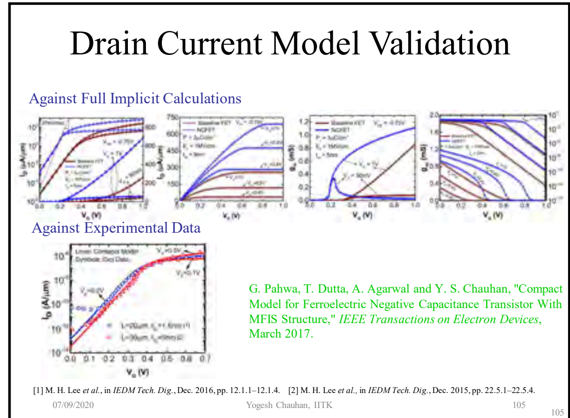
Drain Current Model Validation
Against Full Implicit Calculations
Against Experimental Data
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," IEEE Transactions on Electron Devices, March 2017.
[1] M. H. Lee et al., in IEDM Tech. Dig., Dec. 2016, pp. 12.1.1–12.1.4. [2] M. H. Lee et al., in IEDM Tech. Dig., Dec. 2015, pp. 22.5.1–22.5.4.
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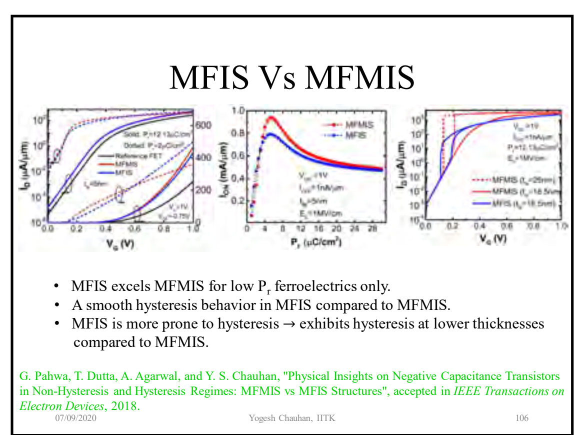
MFIS Vs MFMIS
• MFIS excels MFMIS for low P_r ferroelectrics only.
• A smooth hysteresis behavior in MFIS compared to MFMIS.
• MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", accepted in IEEE Transactions on Electron Devices, 2018.
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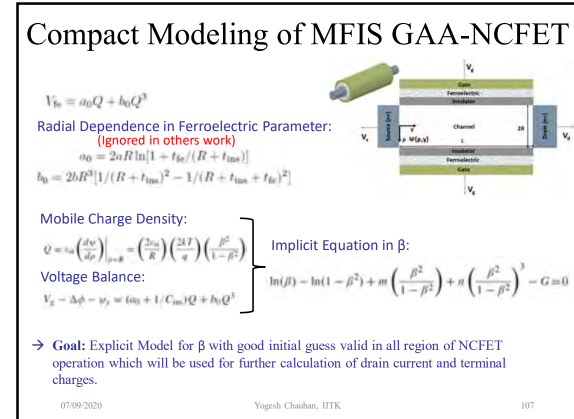
Compact Modeling of MFIS GAA-NCFET
Radial Dependence in Ferroelectric Parameter:
(Ignored in others work)
Mobile Charge Density:
Voltage Balance:
Implicit Equation in β:
→ Goal: Explicit Model for β with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.
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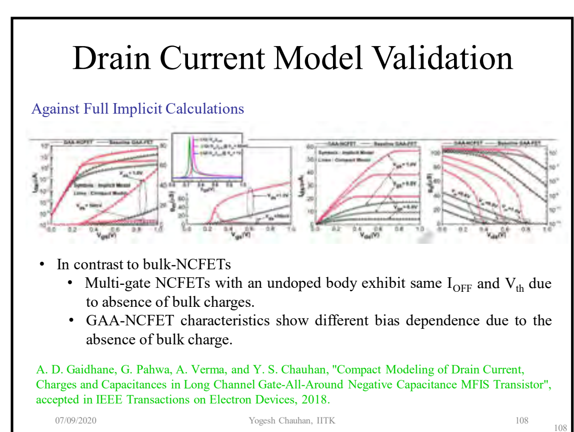
Drain Current Model Validation
Against Full Implicit Calculations
• In contrast to bulk-NCFETs
• Multi-gate NCFETs with an undoped body exhibit same I_OFF and V_th due to absence of bulk charges.
• GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.
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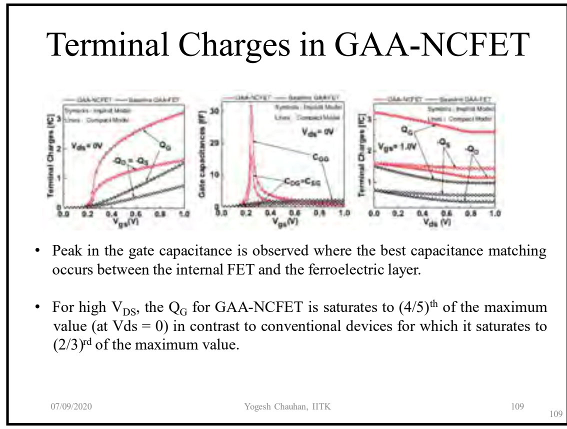
Terminal Charges in GAA-NCFET
Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
For high V_{DS}, the Q_G for GAA-NCFET is saturates to $(4/5)^{th}$ of the maximum value (at Vds = 0) in contrast to conventional devices for which it saturates to $(2/3)^{rd}$ of the maximum value.
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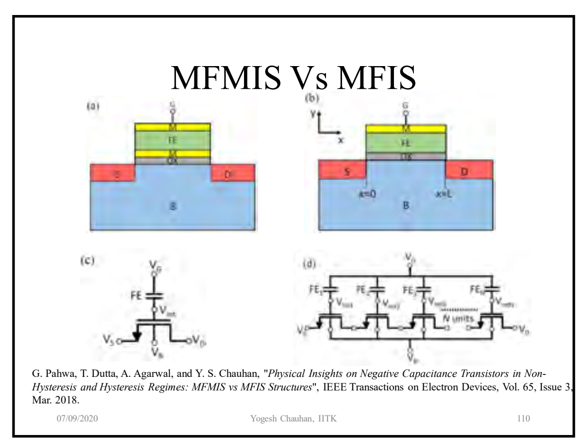
MFMIS Vs MFIS
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.
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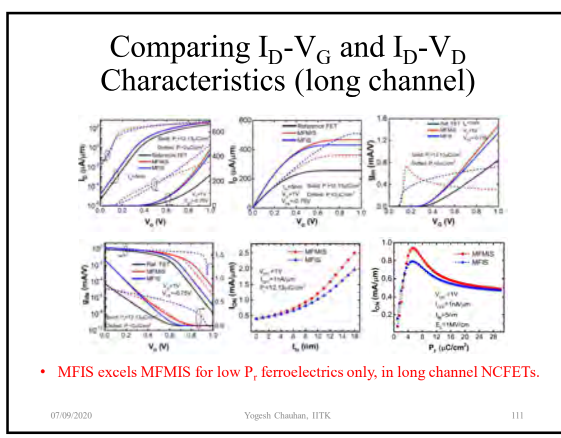
Comparing I_D-V_G and I_D-V_D Characteristics (long channel)
MFIS excels MFMIS for low P_r ferroelectrics only, in long channel NCFETs.
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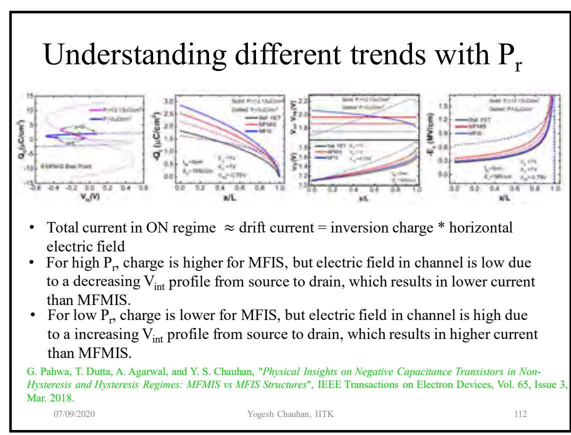
Understanding different trends with P_r
Total current in ON regime ≈ drift current = inversion charge * horizontal electric field
For high P_r, charge is higher for MFIS, but electric field in channel is low due to a decreasing V_{int} profile from source to drain, which results in lower current than MFMIS.
For low P_r, charge is lower for MFIS, but electric field in channel is high due to a increasing V_{int} profile from source to drain, which results in higher current than MFMIS.
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.
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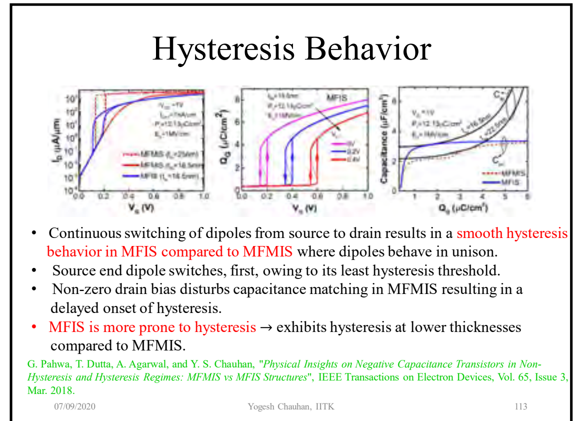
Hysteresis Behavior
Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
Source end dipole switches, first, owing to its least hysteresis threshold.
Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.
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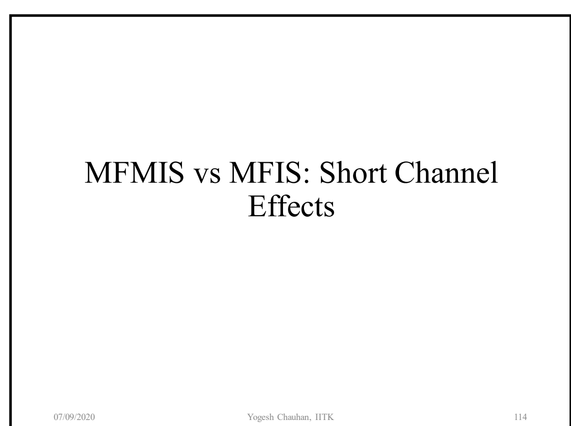
MFMIS vs MFIS: Short Channel Effects
07/09/2020
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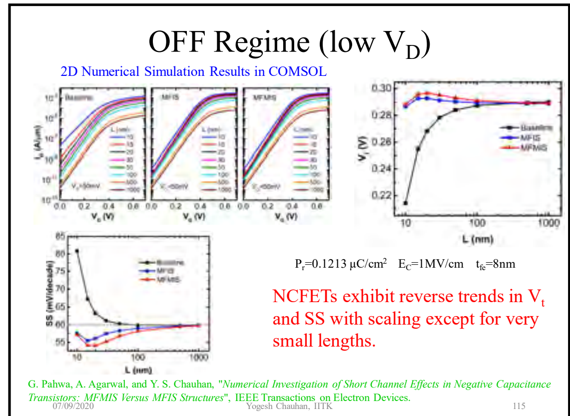
OFF Regime (low V_D)
2D Numerical Simulation Results in COMSOL
P_r=0.1213 μC/cm² E_C=1MV/cm t_{fe}=8nm
NCFETs exhibit reverse trends in V_t and SS with scaling except for very small lengths.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures", IEEE Transactions on Electron Devices.
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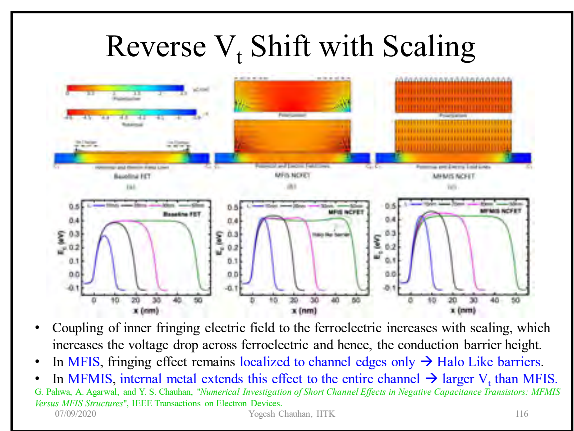
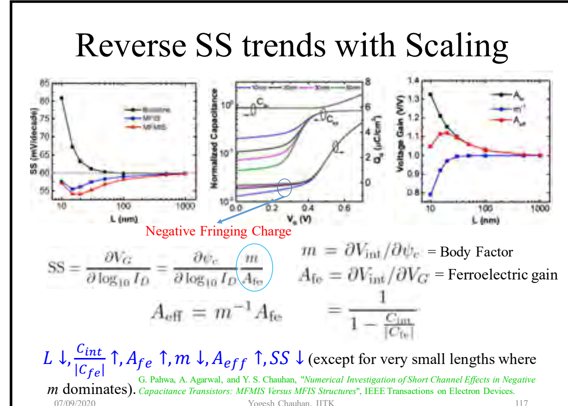
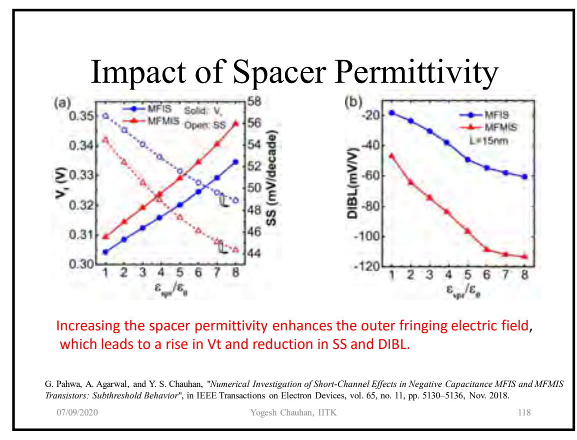

Reverse V_t Shift with Scaling
Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.
In MFIS, fringing effect remains localized to channel edges only → Halo Like barriers.
In MFMIS, internal metal extends this effect to the entire channel → larger V_t than MFIS.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures", IEEE Transactions on Electron Devices.
07/09/2020 Yogesh Chauhan, IITK 116


Reverse SS trends with Scaling
Negative Fringing Charge
$SS = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial \psi_c}{\partial \log_{10} I_D} \frac{m}{A_{fe}}$
$m = \partial V_{int}/\partial \psi_c$ = Body Factor
$A_{fe} = \partial V_{int}/\partial V_G$ = Ferroelectric gain
$A_{eff} = m^{-1} A_{fe} = \frac{1}{1 - \frac{C_{int}}{|C_{fe}|}}$
$L \downarrow, \frac{C_{int}}{|C_{fe}|} \uparrow, A_{fe} \uparrow, m \downarrow, A_{eff} \uparrow, SS \downarrow$ (except for very small lengths where m dominates).
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures", IEEE Transactions on Electron Devices.
07/09/2020 Yogesh Chauhan, IITK 117


Impact of Spacer Permittivity
Increasing the spacer permittivity enhances the outer fringing electric field, which leads to a rise in Vt and reduction in SS and DIBL.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130-5136, Nov. 2018.
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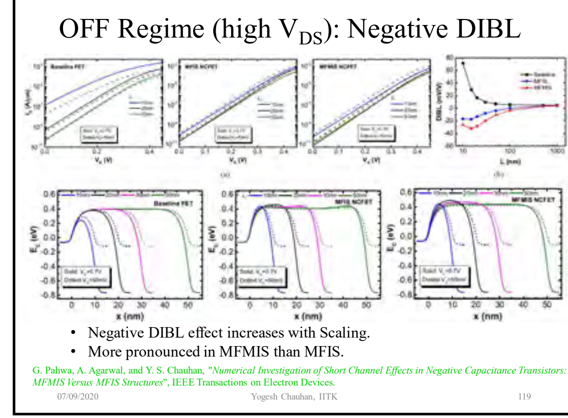
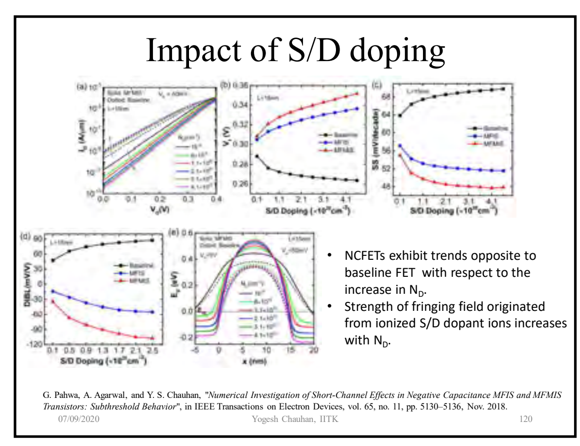

OFF Regime (high V_{DS}): Negative DIBL
Negative DIBL effect increases with Scaling.
More pronounced in MFMIS than MFIS.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance Transistors: MFMIS Versus MFIS Structures", IEEE Transactions on Electron Devices.
07/09/2020 Yogesh Chauhan, IITK 119


Impact of S/D doping
NCFETs exhibit trends opposite to baseline FET with respect to the increase in N_D.
Strength of fringing field originated from ionized S/D dopant ions increases with N_D.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130-5136, Nov. 2018.
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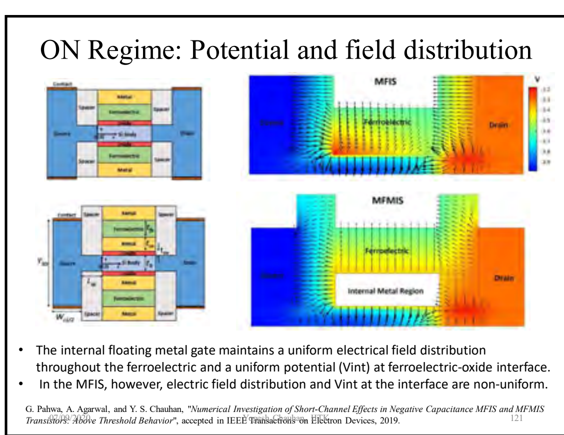
ON Regime: Potential and field distribution
MFIS
MFMIS
Ferroelectric
Drain
Internal Metal Region
• The internal floating metal gate maintains a uniform electrical field distribution throughout the ferroelectric and a uniform potential (Vint) at ferroelectric-oxide interface.
• In the MFIS, however, electric field distribution and Vint at the interface are non-uniform.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior", accepted in IEEE Transactions on Electron Devices, 2019.
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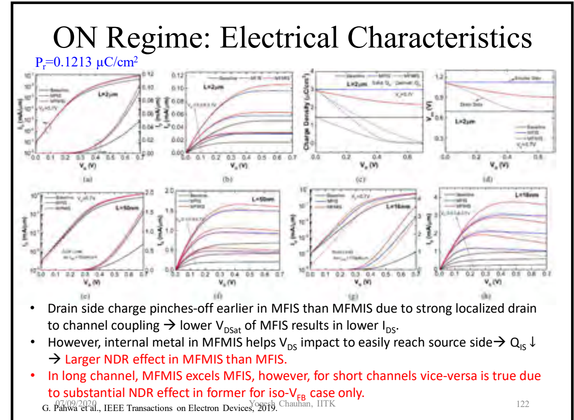
ON Regime: Electrical Characteristics
Pr=0.1213 µC/cm2
• Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling → lower VDSat of MFIS results in lower IDS.
• However, internal metal in MFMIS helps VDS impact to easily reach source side→ QIS ↓ → Larger NDR effect in MFMIS than MFIS.
• In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former for iso-VFB case only.
G. Pahwa et al., IEEE Transactions on Electron Devices, 2019.
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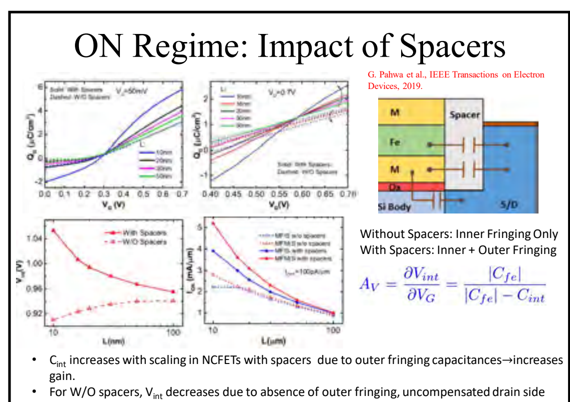
ON Regime: Impact of Spacers
G. Pahwa et al., IEEE Transactions on Electron Devices, 2019.
Spacer
Si Body
S/D
Without Spacers: Inner Fringing Only
With Spacers: Inner + Outer Fringing
$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$
• Cint increases with scaling in NCFETs with spacers due to outer fringing capacitances→increases gain.
• For W/O spacers, Vint decreases due to absence of outer fringing, uncompensated drain side inner fringing, and increased drain to channel coupling.
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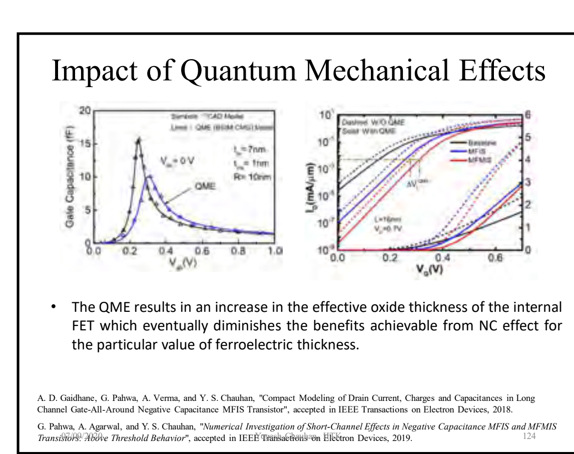
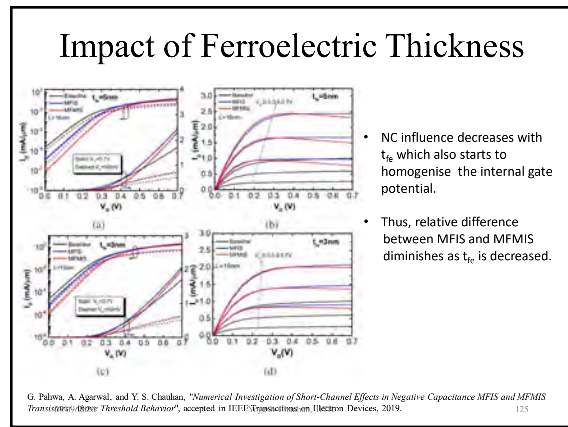
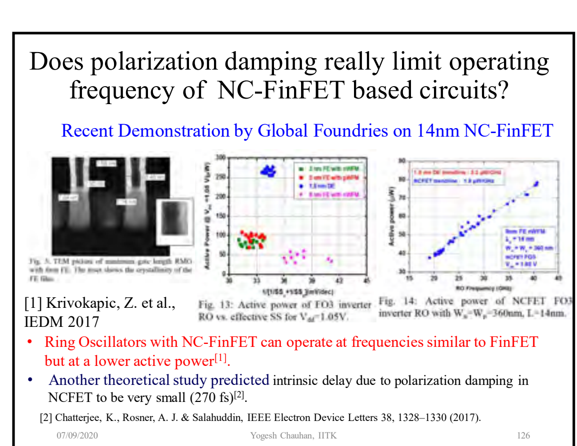

Impact of Quantum Mechanical Effects
Gate Capacitance (fF)
QME
• The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", accepted in IEEE Transactions on Electron Devices, 2018.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior", accepted in IEEE Transactions on Electron Devices, 2019.
124


Impact of Ferroelectric Thickness
• NC influence decreases with tfe which also starts to homogenise the internal gate potential.
• Thus, relative difference between MFIS and MFMIS diminishes as tfe is decreased.
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior", accepted in IEEE Transactions on Electron Devices, 2019.
125


Does polarization damping really limit operating frequency of NC-FinFET based circuits?
Recent Demonstration by Global Foundries on 14nm NC-FinFET
[1] Krivokapic, Z. et al., IEDM 2017
Fig. 13: Active power of FO3 inverter RO vs. effective SS for Vdd=1.05V.
Fig. 14: Active power of NCFET FO3 inverter RO with Wn=Wp=360nm, L=14nm.
• Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power[1].
• Another theoretical study predicted intrinsic delay due to polarization damping in NCFET to be very small (270 fs)[2].
[2] Chatterjee, K., Rosner, A. J. & Salahuddin, IEEE Electron Device Letters 38, 1328–1330 (2017).
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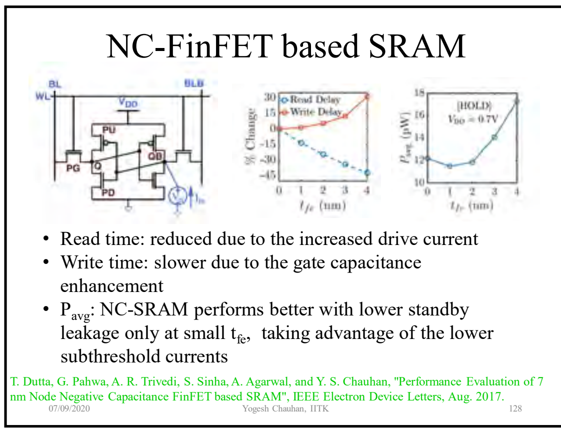
NC-FinFET based inverters

- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

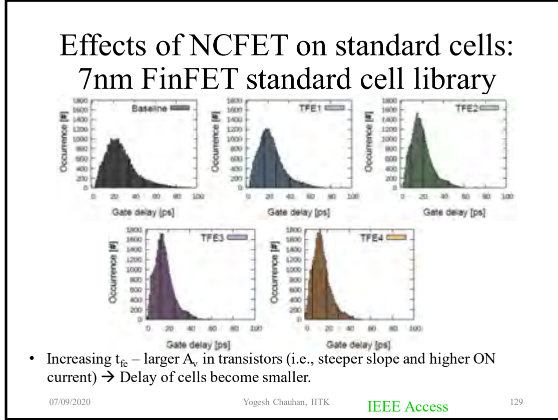
NC-FinFET based SRAM



- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- P_{avg}: NC-SRAM performs better with lower standby leakage only at small t_{fe}, taking advantage of the lower subthreshold currents

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

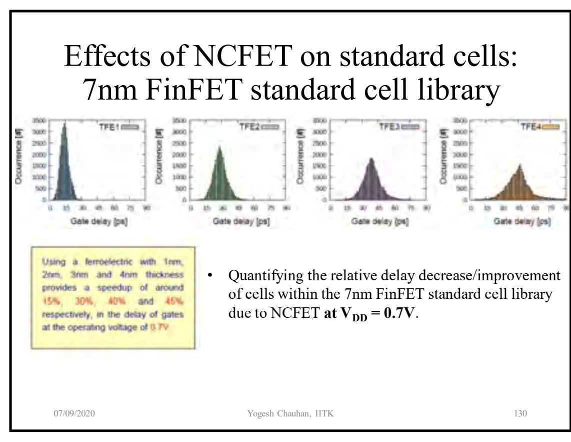
Effects of NCFET on standard cells: 7nm FinFET standard cell library



- Increasing t_{fe} – larger A_v in transistors (i.e., steeper slope and higher ON current) → Delay of cells become smaller.

IEEE Access

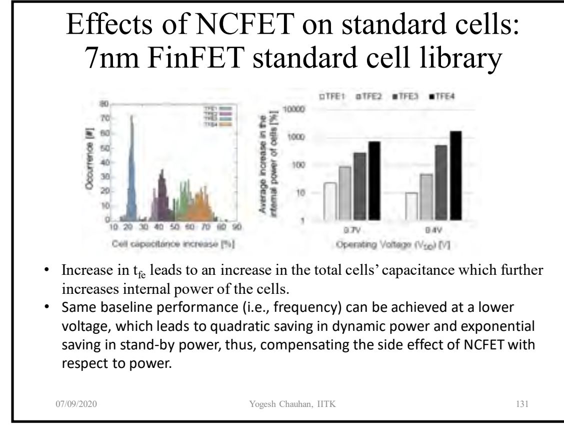
Effects of NCFET on standard cells: 7nm FinFET standard cell library



Using a ferroelectric with 1nm, 2nm, 3nm and 4nm thickness provides a speedup of around 15%, 30%, 40% and 45% respectively, in the delay of gates at the operating voltage of 0.7V

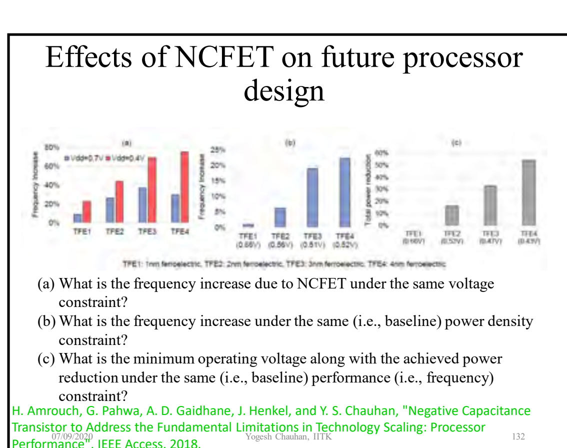
- Quantifying the relative delay decrease/improvement of cells within the 7nm FinFET standard cell library due to NCFET **at V_{DD} = 0.7V**.

Effects of NCFET on standard cells: 7nm FinFET standard cell library



- Increase in t_{fe} leads to an increase in the total cells' capacitance which further increases internal power of the cells.
- Same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.

Effects of NCFET on future processor design



(a) What is the frequency increase due to NCFET under the same voltage constraint?

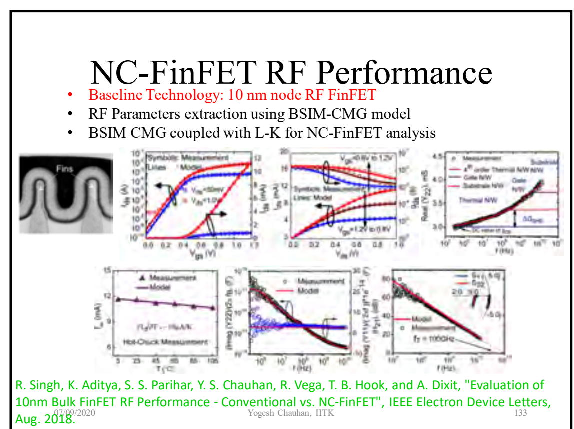
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?

(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance", IEEE Access, 2018.

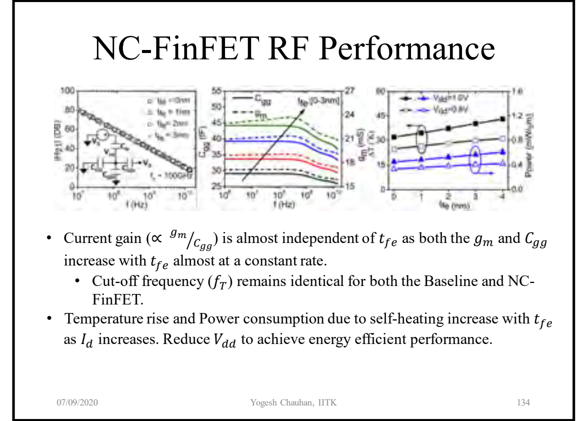
NC-FinFET RF Performance

- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis



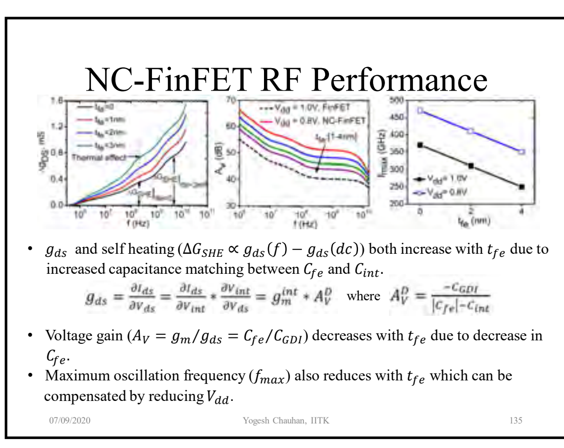
R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook, and A. Dixit, "Evaluation of 10nm Bulk FinFET RF Performance - Conventional vs. NC-FinFET", IEEE Electron Device Letters, Aug. 2018.

NC-FinFET RF Performance



- Current gain ($\propto {}^{g_m}/_{C_{gg}}$) is almost independent of t_{fe} as both the g_m and C_{gg} increase with t_{fe} almost at a constant rate.
  - Cut-off frequency (f_T) remains identical for both the Baseline and NC-FinFET.
- Temperature rise and Power consumption due to self-heating increase with t_{fe} as I_d increases. Reduce V_{dd} to achieve energy efficient performance.

NC-FinFET RF Performance

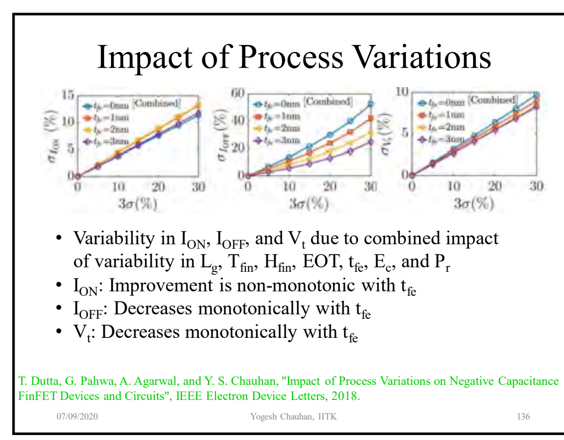


- g_{ds} and self heating ($\Delta G_{SHE} \propto g_{ds}(f) - g_{ds}(dc)$) both increase with t_{fe} due to increased capacitance matching between C_{fe} and C_{int}.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\partial I_{ds}}{\partial V_{int}} * \frac{\partial V_{int}}{\partial V_{ds}} = g_m^{int} * A_V^D \quad \text{where} \quad A_V^D = \frac{-C_{GDI}}{|C_{fe}| - C_{int}}$$

- Voltage gain ($A_V = g_m/g_{ds} = C_{fe}/C_{GDI}$) decreases with t_{fe} due to decrease in C_{fe}.
- Maximum oscillation frequency (f_{max}) also reduces with t_{fe} which can be compensated by reducing V_{dd}.

Impact of Process Variations



- Variability in I_{ON}, I_{OFF}, and V_t due to combined impact of variability in L_g, T_{fin}, H_{fin}, EOT, t_{fe}, E_c, and P_r
- I_{ON}: Improvement is non-monotonic with t_{fe}
- I_{OFF}: Decreases monotonically with t_{fe}
- V_t: Decreases monotonically with t_{fe}

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, 2018.

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.

11-stage Ring-Oscillator: Variation in τ due to combined variation

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, 2018.

Open Questions

- Is NC a static or transient phenomenon?
- Physical explanation of NC effect
- Second order effects
  - Impact of grain boundaries and their sizes
  - Impact of multi-domain effects
  - Impact of traps
  - Impact of FE thickness
  - Reliability, Variability
- Impact of NDR/NDIBL on circuits

Relevant Publications

- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior," in IEEE Transactions on Electron Devices, 2019.
- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Modeling of Inner Fringing Charges and Short Channel Effects in Negative Capacitance MFIS Transistor", accepted in Electron Devices Technology and Manufacturing (EDTM), 2019.
- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior," in IEEE Transactions on Electron Devices, Nov. 2018.
- Karishma Qureshi, G. Pahwa and Y.S. Chauhan, "Impact of Linear Intergranular Variation in Remnant Polarization on Negative Capacitance Field Effect Transistor", ICEE, 2018.
- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Compact Modeling of Drain Current in Double Gate Negative Capacitance MFIS Transistor", ICEE, 2018.
- H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance," IEEE Access, Sep. 2018.
- A.D. Gaidhane, G. Pahwa, A. Verma, Y. S. Chauhan, "Compact Modeling of Drain Current, Charges, and Capacitances in Long-Channel Gate-All-Around Negative Capacitance MFIS Transistor," IEEE Transactions on Electron Devices, May 2018.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Mar. 2018.
- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, Jan. 2018.

Relevant Publications

- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan,"Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS Structure", IEEE Transactions on Electron Devices, Mar. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part I, Model description", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part II, Model validation", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", IEEE ICEE, Dec. 2016. (Best Paper Award)
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE ESSDERC, Switzerland, Sept. 2016. (Invited)
- G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Compact Modeling of Negative Capacitance Transistor with Experimental Validation", IWPSD, Dec. 2015.

Summary

- Industry standard model development @ IITK
- All models are implemented in the **Verilog - A** code
  - Tested on commercial **simulators**
  - Validated with real device data
- Working with major semiconductor and EDA companies