BSIM-BULK: Industry Standard SPICE Model for Analog, RF & High Voltage Applications

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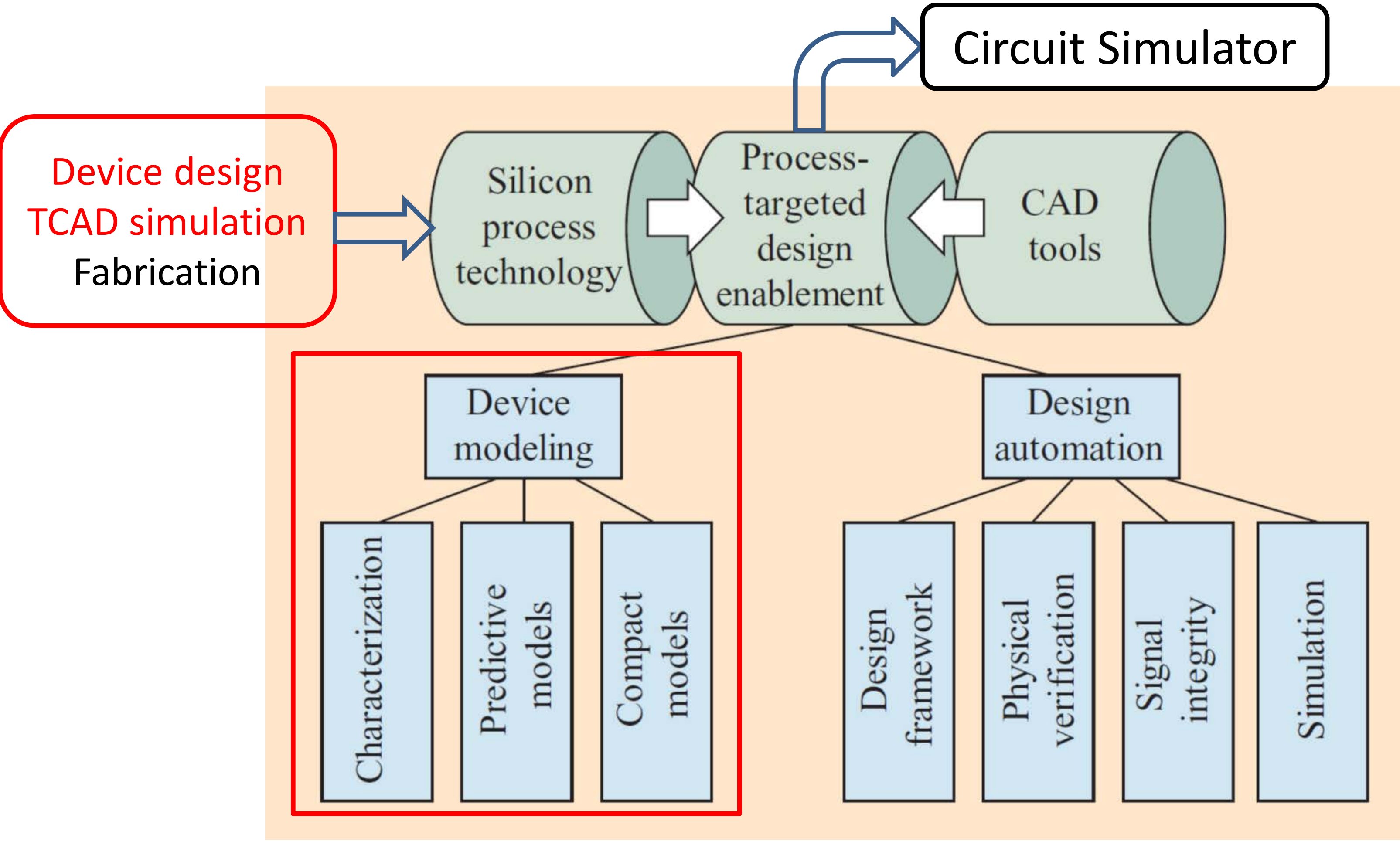
Components required for successful IC design



D. L. Harame et. al.,"Design automation methodology and rf/analog modeling for rf CMOS and SiGe BiCMOS technologies", IBM Journal of Research and Development, Vol. 47, No. 2/3, March/May 2003.

SPICE and Device Compact Models

Prof. at UCB – SPICE designer (1925-2004)

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tion and its negative side effec

Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.

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Prof. at UCB/Emeritus Prof. at CMU – CANCER designer which later led to SPICE development

Ron Rohrer

Special Issue on 40th Anniversary of SPICE

SPRING 2011 *IEEE SOLID-STATE CIRCUITS MAGAZINE*

Compact Model

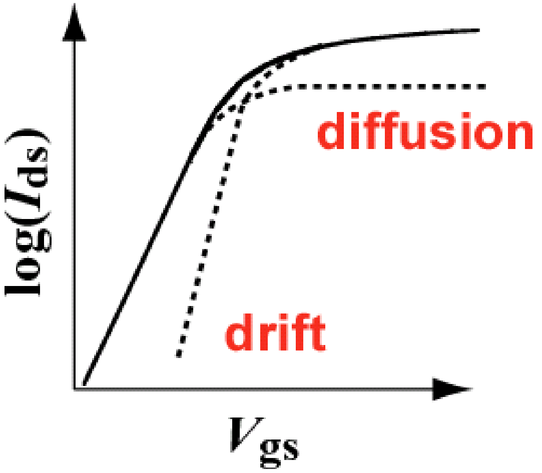
- Compact Model is the medium of information exchange between foundry and designer.

- Compact Model must have
  - Convergence on variety of conditions
  - Fast
  - Accuracy

Compact Model Approaches for MOSFET

- Threshold Voltage based Models (e.g. BSIM3, BSIM4)
  - Fully Analytical solution (easy to implement) – Fast
  - Currents expressed as functions of Voltages

$$I_{ds} = \mu \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_{th} \right) V_{ds} - \frac{1}{2} V_{ds}^{2} \right]$$



  - Different equations for
    - Sub-threshold and above-threshold
    - Linear/saturation regions
    - Use interpolation function to get smooth current

Compact Model Approaches for MOSFET

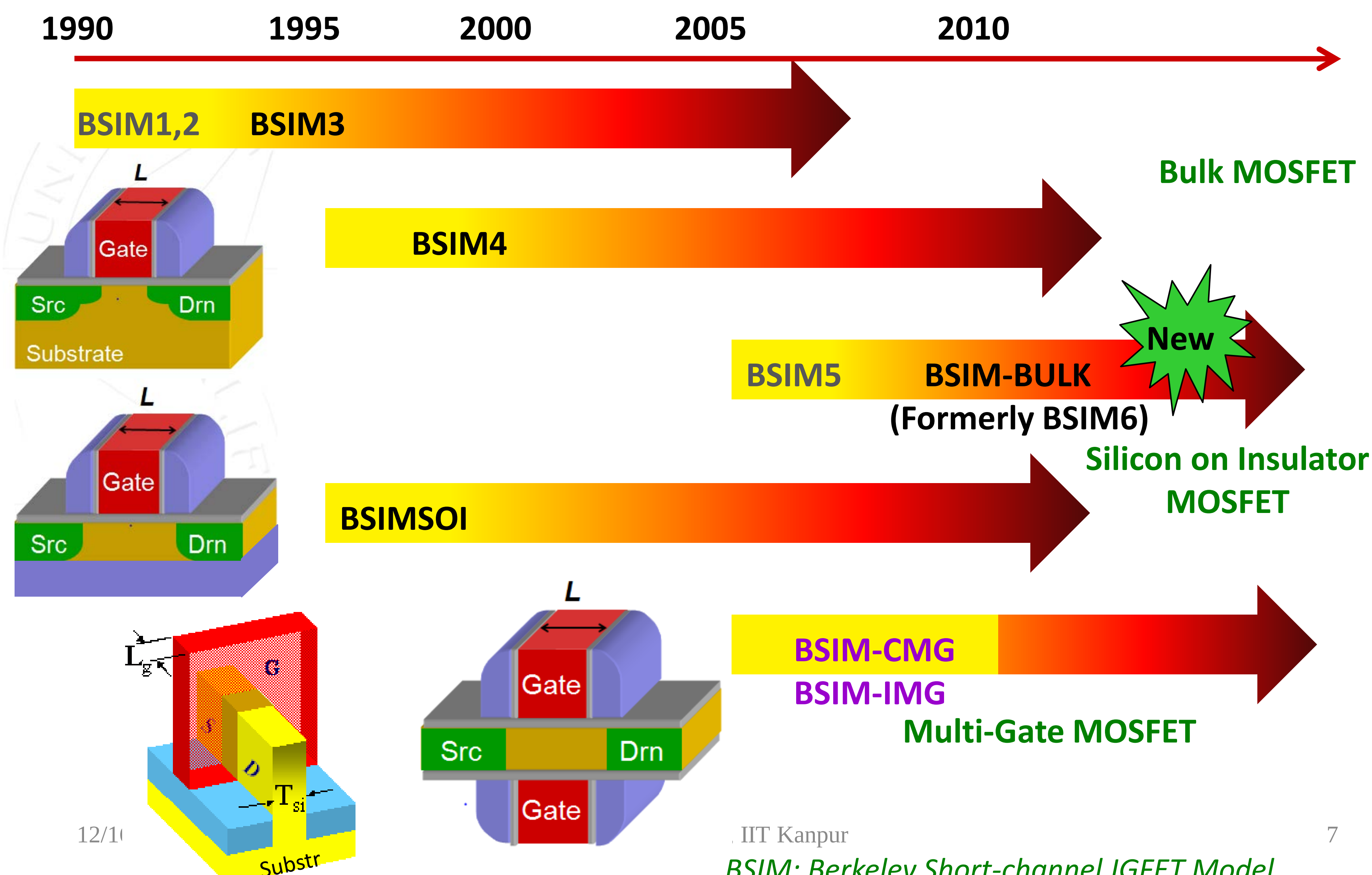
- Surface Potential based Models (e.g. ASM-HEMT, PSP, HiSim)

$$V_G - V_{FB} - \Psi_S = -\frac{Q_{si}}{C_{ox}}, Q_{si} = -sign(\Psi_S)\Gamma C_{ox}\sqrt{V_t\left(e^{-\frac{\Psi_S}{V_t}} - 1\right) + V_t e^{-\frac{2\Phi_F + V_{CH}}{V_t}}\left(e^{\frac{\Psi_S}{V_t}} - 1\right) + \Psi_S}$$

  – Implicit equation is solved either iteratively or analytically
  – Might be slower than threshold voltage based models

- Charge based Models (e.g. BSIM-BULK, BSIM-CMG)
  – Solve for charge instead of surface potential
  – No iterations
  – Faster than Surface Potential based approach with similar accuracy in charge/current

BSIM Family of Compact Device Models



BSIM: Berkeley Short-channel IGFET Model

BSIM-BULK Description

BSIM-BULK Developers

- Students –
  - Ravi Goel, IIT Kanpur
  - Chetan Gupta, IIT Kanpur
  - Harshit Agarwal, IIT Kanpur
  - S. Venugopalan, UCB
  - M. A. Karim, UCB
- Professors –
  - Yogesh S. Chauhan, IIT Kanpur
  - Chenming Hu, UCB

Charge based MOSFET model

- Next generation BSIM Bulk MOSFET model
- Charge based core derived from Poisson's solution
- Physical effects (SCE, CLM etc.) taken from BSIM4
- Parameter names matched to BSIM4 parameters
- Gummel Symmetry (symmetric @ V_{DS}=0)
- AC Symmetry
  - Capacitances/derivatives are symmetric @V_{DS}=0
- Continuous
  - From accumulation to strong inversion
  - From linear to saturation
- Physical Capacitance model
  - Short channel CV–Velocity saturation & other effects
- No glitches – smooth current and capacitance behavior

BSIM-BULK flow

1. Calculate **pinch-off potential** Ψp (function of Vg)

2. Calculate source and drain **inversion charge density**

3. Calculate **drain current**
   - Noise is calculated after inversion charge densities and i_{ds} is obtained

4. Calculate **total gate drain source and body charge**

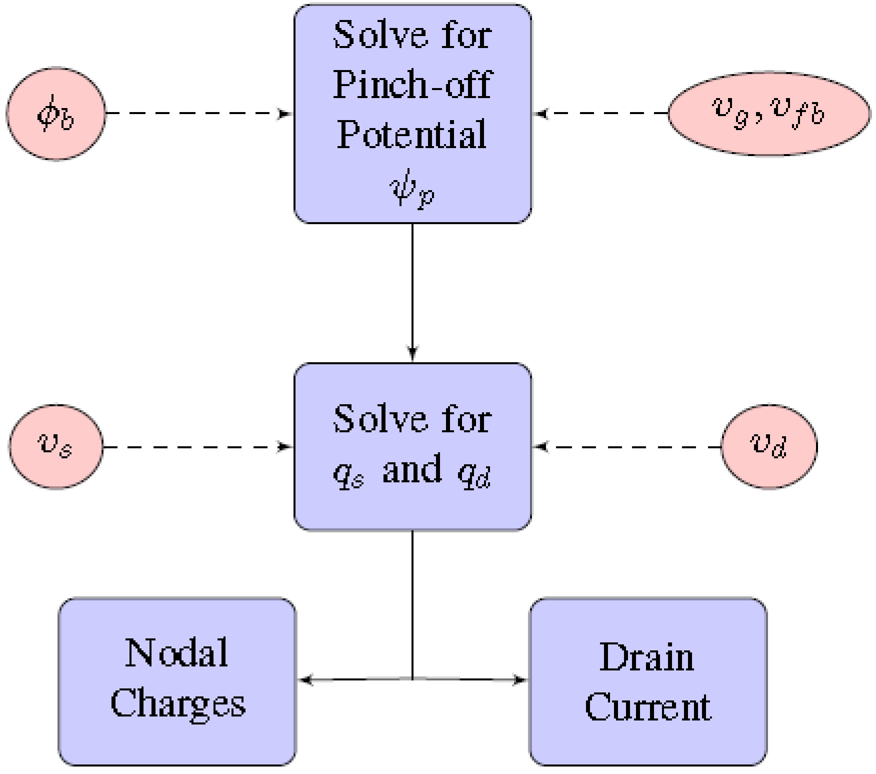
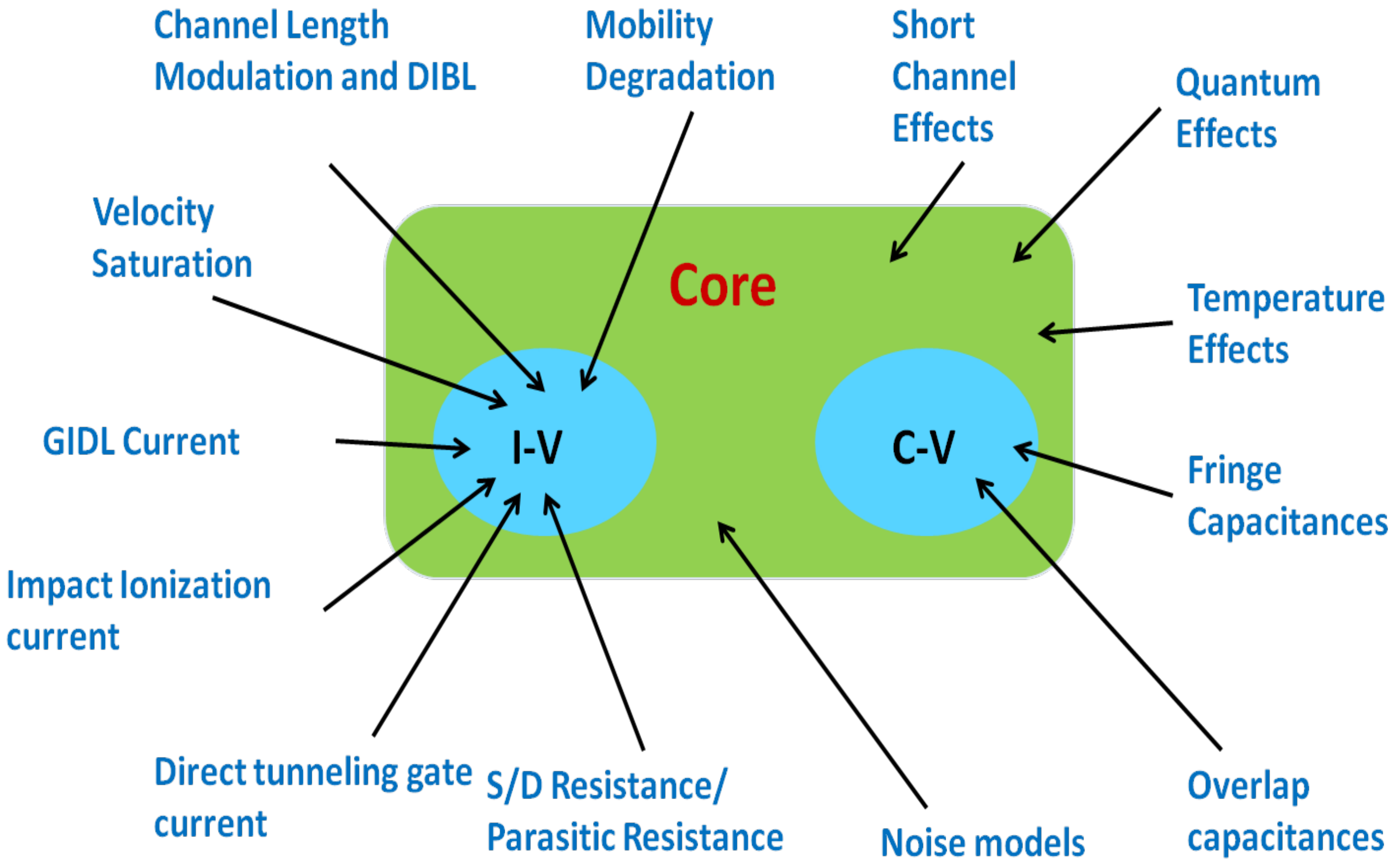


Fig: Solution of the core model

Core Model + Real effects



Y. S. Chauhan et al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET", IEEE Transactions on Electron Devices, Vol. 61, Issue 2, pp. 234-244, Feb. 2014. (Invited)

Physics of BSIM6 Model

- Poisson's solution for long channel MOSFET

$$V_G - V_{FB} - \Psi_S = -\frac{Q_i + Q_b}{C_{ox}} = -\frac{Q_i}{C_{ox}} + sign(\Psi_S)\Gamma C_{ox}\sqrt{V_t\left(e^{-\frac{\Psi_S}{V_t}} - 1\right) + \Psi_S}$$

- Inversion Charge linearization $-\frac{Q_i}{C_{ox}} = n_q(\Psi_P - \Psi_S)$

Ψ_{s0} is linearization point

- n_q is the slope factor

$$n_q = 1 + \frac{\Gamma}{\sqrt{\Psi_{S0}} + \sqrt{\Psi_P}}$$

$$V_G - V_{FB} - \Psi_P = sign(\Psi_P)\Gamma C_{ox}\sqrt{V_t\left(e^{-\frac{\Psi_P}{V_t}} - 1\right) + \Psi_P}$$

Ψ_P is evaluated from implicit equation

- $\Psi_P = \Psi_S$, when Q_i=0

n_q is made bias dependent to improve accuracy

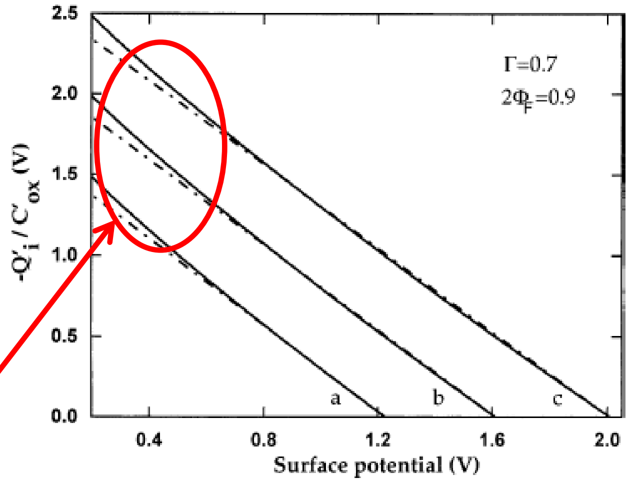


Fig. 1. Inversion charge density as a function of the surface potential for three values of the gate voltage (curve a: $V_g = 2$ V, curve b: $V_g = 2.5$ V, curve c: $V_g = 3$ V). Full line: exact model, dash-dotted: linearisation with the charge linearization factor calculated from relation (6).

*Ref.: Tsividis book & J.M. Sallese et al., Solid State Electronics

Physics of BSIM6 Model

- Using linearization approach and normalization

Other models ignored circled terms

$$2q_i + \ln(q_i) + \ln\left[\frac{2n_q}{\gamma}\left(\frac{2n_q}{\gamma}q_i + 2\sqrt{-2q_i + \psi_p}\right)\right] = \psi_p - 2\phi_f - v_{ch}$$

- No approximation to solve the charge equation

- Solved the charge equation using first & second order Newton-Raphson technique to obtain analytical expression of q_i

Analytical expression of q_i

$$n_{q0} = 1 + \frac{\gamma}{2\sqrt{\psi_p}} \quad (3.42)$$

$$T2 = \psi_p - 2\phi - v_{ch} - ln\left(4.0 \cdot \frac{n_{q0}}{\gamma} \cdot \sqrt{\psi_p}\right) \quad (3.43)$$

$$ln_{q0} = \frac{1}{2}\left[T2 - 0.201491 - \sqrt{T2 \cdot (T2 + 0.402982) + 2.446562}\right] \quad (3.44)$$

$$q_0 = e^{ln_{q0}} \quad (3.45)$$

Guess for q_i

if $ln_{q0} <= -80.0$

$$q_{s/d} = q_0 \cdot \left[1 + \psi_p - 2\phi - v_{ch} - ln_{q0} - \ln\left(2 \cdot \frac{n_{q0}}{\gamma}\left(2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0}-1)}\right)\right)\right] \quad (3.46)$$

Simplified expression for $q_i <= e^{-80}$

else

$$T_4 = 2 \cdot q_0 + \ln\left[2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma}\left(2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0}-1)}\right)\right] - \psi_p - 2\phi - v_{ch} \quad (3.47)$$

$$T_5 = 2 + \frac{1}{q_0} + \frac{\frac{n_{q0}}{\gamma} - \frac{2(n_{q0}-1)}{\gamma}}{\frac{n_{q0}}{\gamma} \cdot q_0 + \frac{\gamma}{2(n_{q0}-1)}} \quad (3.48)$$

$$q_1 = q_0 - \frac{T_4}{T_5} \quad (3.49)$$

First order Newton-raphson

$$T_4 = 2 \cdot q_1 + \ln\left[2 \cdot q_1 \cdot \frac{n_{q0}}{\gamma}\left(2 \cdot q_1 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0}-1)}\right)\right] - \psi_p - 2\phi - v_{ch} \quad (3.50)$$

$$T_5 = 2 + \frac{1}{q_1} + \frac{\frac{n_{q0}}{\gamma} - \frac{2(n_{q0}-1)}{\gamma}}{\frac{n_{q0}}{\gamma} \cdot q_1 + \frac{\gamma}{2(n_{q0}-1)}} \quad (3.51)$$

$$T_7 = -\frac{1}{q_1^2} - \frac{1}{\left[\frac{\gamma}{2(n_{q0}-1)}\right]^3 \cdot \left[\frac{n_{q0}}{\gamma} \cdot q_1 + \frac{\gamma}{2(n_{q0}-1)}\right]} - \left[\frac{\frac{n_{q0}}{\gamma} - \frac{2(n_{q0}-1)}{\gamma}}{\frac{n_{q0}}{\gamma} \cdot q_1 + \frac{\gamma}{2(n_{q0}-1)}}\right]^2 \quad (3.52)$$

$$q_{s/d} = q_1 - \frac{T_4}{T_5} \cdot \left(1 + \frac{T_4 \cdot T_7}{2 \cdot T_5^2}\right) \quad (3.53)$$

Second order Newton-raphson

Drain Current including Current saturation

- Drain-Source current
  - Mobility model
  - Current saturation

$$I_D = \frac{\mu_v}{\sqrt{1+\left(\frac{\mu_v}{v_{sat}}\left|\frac{d\Psi_S}{dx}\right|\right)^2}} W\left(-Q_i\frac{d\Psi_S}{dx}+V_T\frac{dQ_i}{dx}\right)$$

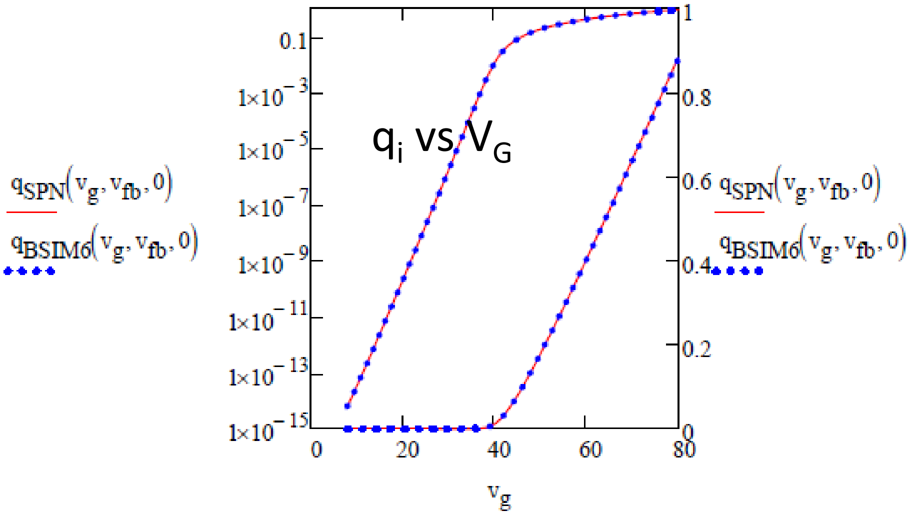
$$-\frac{Q_i}{C_{ox}} = n_q(\Psi_P-\Psi_S), q = \frac{-Q_i}{2n_qC_{ox}V_T}, i_d = \frac{I_D}{2n_q\frac{W}{L}\mu_vC_{ox}V_t^2}, \lambda_c = \frac{2\mu_vV_t}{v_{sat}L}$$

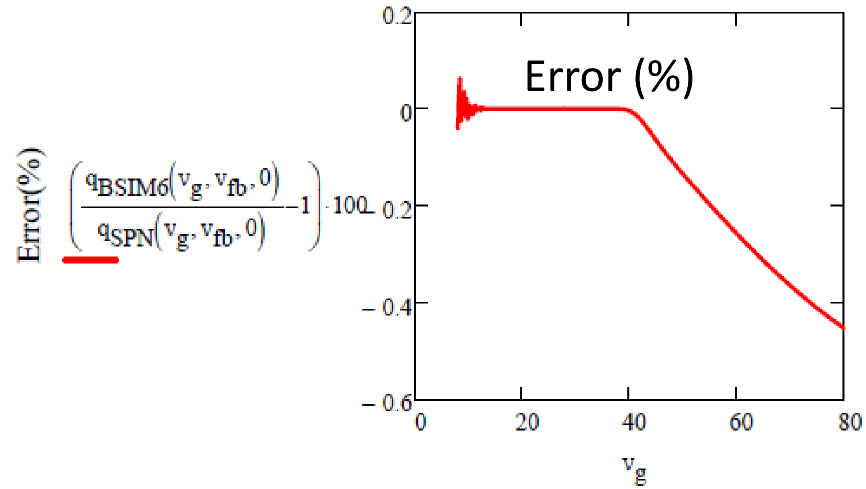
- Using charge linearization & normalization

$$i_{ds} = \frac{\left(q_s^2+q_s\right)-\left(q_d^2+q_d\right)}{\frac{1}{2}\left[\sqrt{1+\Gamma^2}+\frac{1}{\Gamma}\ln\left(\Gamma+\sqrt{1+\Gamma^2}\right)\right]}$$

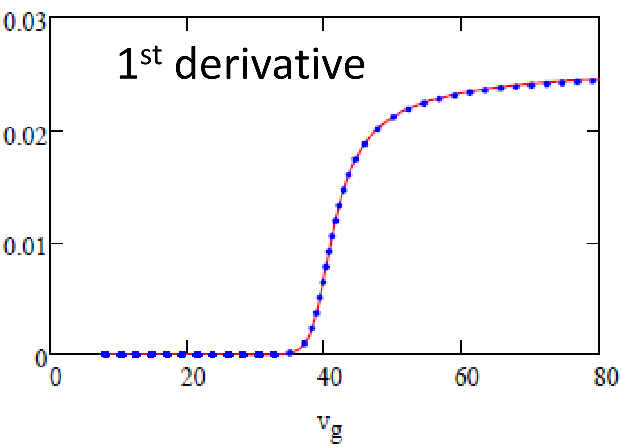
$$\Gamma = 2\lambda_c(q_s-q_d)$$

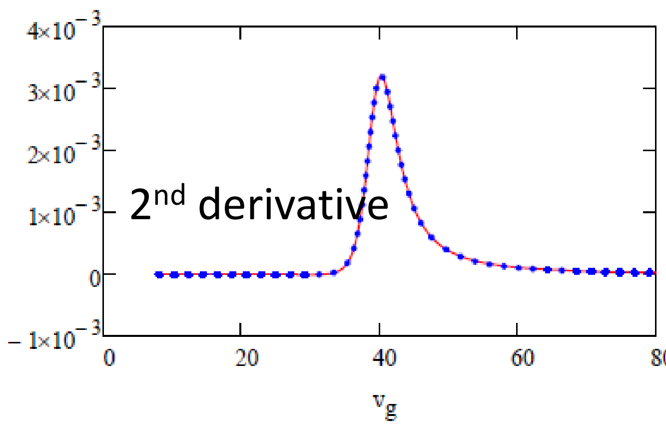
Normalized Q_i-V_G & derivatives

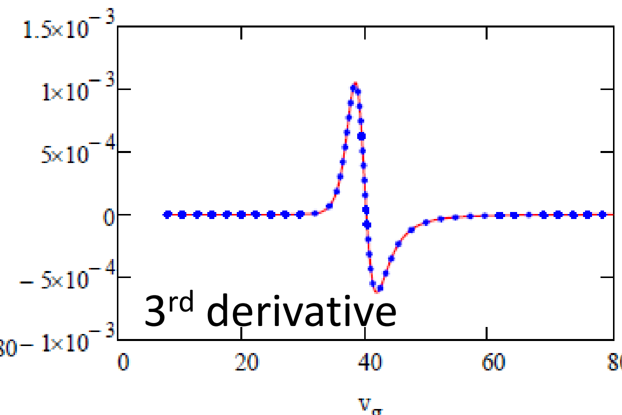




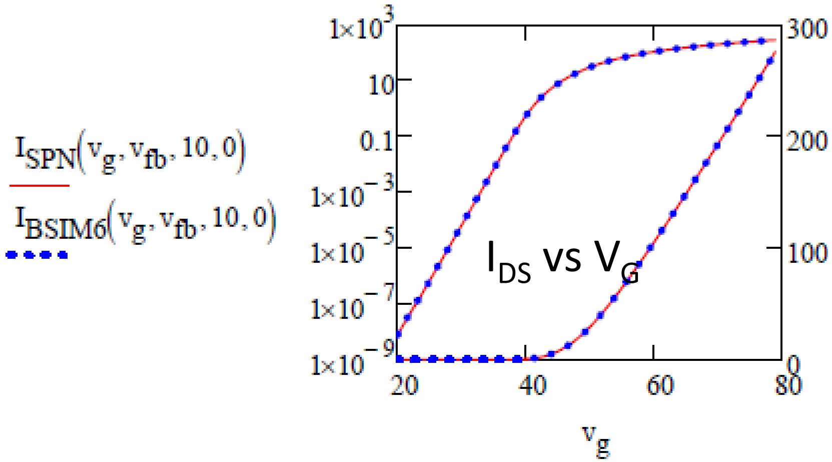
Red – Numerical Surf. Pot. model
Blue – BSIM6 model

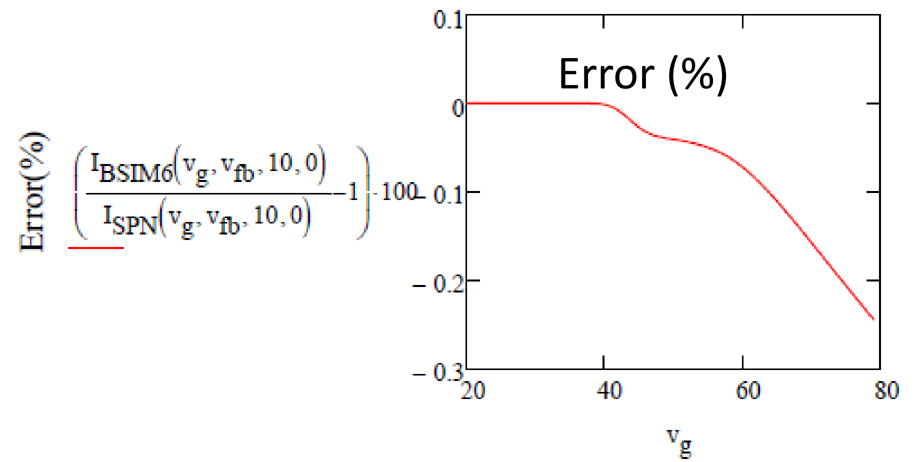






Normalized I_{DS}-V_{GS} & derivatives





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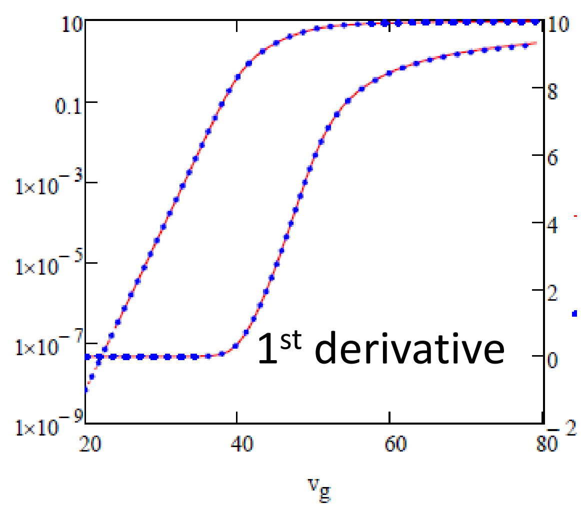
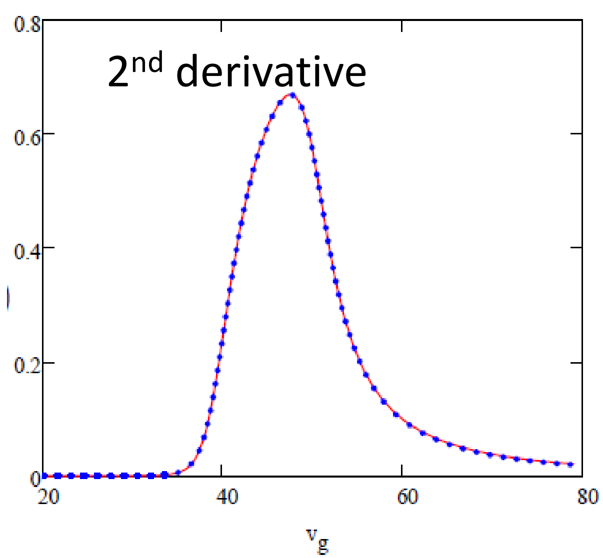
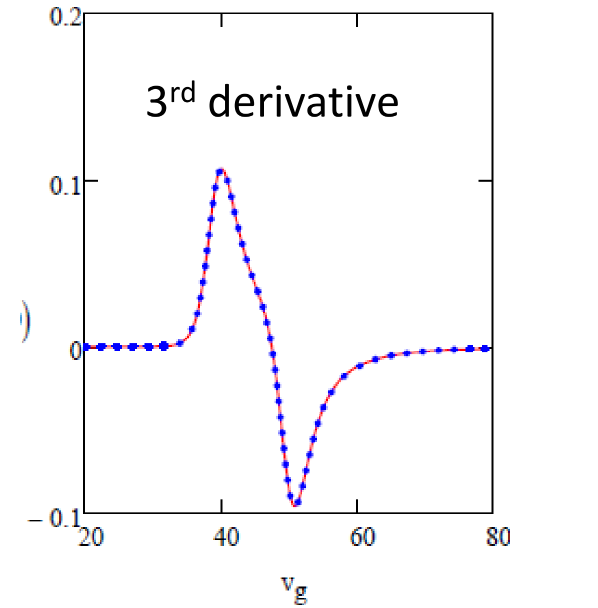






Short Channel Effects

- Many of the short channel effects are included using threshold voltage shift (same as BSIM4)

$$\Delta V_{th,VDNUD} = K1 \cdot (\sqrt{PhistVbs} - \sqrt{\psi_{st}}) \cdot \left(1 + \left(\frac{LPEB}{L_{eff}}\right)^{LPEBEXP}\right) - K2 \cdot V_{bsx} \tag{3.76}$$

$$\Delta V_{th,SCE} = -\theta_{SCE} \cdot DVT0 \cdot (V_{bi} - \psi_{st}) \tag{3.77}$$

$$\Delta V_{th,DIBL} = -(ETA0 + ETAB \cdot V_{bsx}) \cdot \theta_{DIBL} \cdot V_{dsx} \tag{3.78}$$

$$\Delta V_{th,RSCE} = K1 \cdot \theta_{RSCE} \cdot \sqrt{\psi_{st}} \tag{3.79}$$

$$\Delta V_{th,NW1} = (K3 + K3B \cdot V_{bsx}) \cdot \left(\frac{T_{ox}}{W_{eff} \cdot W0}\right) \tag{3.80}$$

$$\Delta V_{th,NW2} = -\theta_{NW2} \cdot (V_{bi} - \psi_{st}) \tag{3.81}$$

$$\Delta V_{th,DITS} = -n\frac{KT}{q} \cdot \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + \exp(-DVTP1 \cdot V_{ds}))}\right) \tag{3.82}$$

$$\Delta V_{th,all} = \Delta V_{th,VNUD} + \Delta V_{th,SCE} + \Delta V_{th,DIBL} + \Delta V_{th,RSCE} + \Delta V_{th,NW1} + \Delta V_{th,NW2} + \Delta V_{th,DITS} \tag{3.83}$$

$$V_{gfb} = V_g - V_{fb} - \Delta V_{th,all} \tag{3.84}$$

Mobility Model

- Mobility model adopted from BSIM4

BSIM4

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1+(UA+UC \cdot V_{bseff})\left[\frac{V_{gsteff}+C_0 \cdot (VTHO-VFB-\Phi_s)}{TOXE}\right]^{EU} + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff}+2\sqrt{V_{th}^2+0.0001}}\right)}$$

BSIM-BULK

$$\mu_{eff} = \frac{U0}{1+(UA+UC \cdot V_{bsx}) \cdot E_{eff}^{EU} + \frac{UD}{\left[\frac{1}{2}\left(1+\frac{q_{is}}{q_{bs}}\right)\right]^{UCS}}}$$

where

$$\eta = \begin{cases} \frac{1}{2} \cdot ETAMOB & \text{for NMOS} \\ \frac{1}{3} \cdot ETAMOB & \text{for PMOS} \end{cases}$$

$$E_{effs} = 10^{-8} \cdot \left(\frac{q_{bs}+\eta \cdot q_{is}}{\epsilon_{ratio} \cdot Tox}\right)$$ MV/cm

$$V_{dsx} = \sqrt{V_{ds}^2+0.01} - 0.1$$

$$V_{bsx} = -\left[V_s + \frac{1}{2}(V_{ds} - V_{dsx})\right]$$

Saturation Voltage V_{dsat}

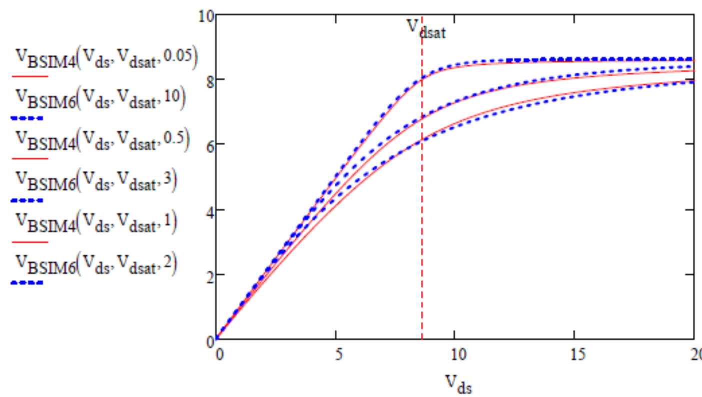
$$V_{BSIM4}(V_{ds}, V_{dsat}, \delta_0) := V_{dsat} - \frac{1}{2}\cdot\left[(V_{dsat} - V_{ds} - \delta_0) + \sqrt{(V_{dsat} - V_{ds} - \delta_0)^2 + 4\cdot\delta_0\cdot V_{dsat}}\right]$$

- V_{ds} to V_{dsat} – BSIM4 formulation causes asymmetry in higher order derivatives
- New V_{dsat} evaluation:

$$\lambda_c = \frac{2\mu_{effs}V_t}{VSAT \bullet L_{eff}} \quad \Rightarrow \quad q_{dsat} = \frac{1}{2}KSATIV \bullet \lambda_c \bullet \frac{q_s^{\;2} + q_s}{1 + \frac{1}{2}\lambda_c(1+q_s)}$$

$$v_{dsat} = \frac{V_{dsat}}{V_t} = \psi_p - 2\varphi_f - 2q_{dsat} - \ln\left[\frac{2q_{dsat}\cdot n_q}{\gamma}\left(\frac{2q_{dsat}\cdot n_q}{\gamma} + \frac{\gamma}{n_q - 1}\right)\right]$$

$$V_{dseff} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{dsat} - V_s}\right)^{1/DELTA}\right]^{DELTA}}$$



Output conductance – CLM

Adopted from BSIM4

$$E_{sat} = \frac{2 \cdot VSAT}{U0 \cdot Dmobs}$$

$$F = \begin{cases} 1 & \text{for } FPROUT \leq 0 \\ \frac{1}{1+\frac{FPROUT \cdot \sqrt{L_{eff}}}{qia+2 \cdot nV_t}} & \text{for } FPROUT > 0 \end{cases}$$

$$C_{clm} = \begin{cases} \frac{F \cdot \left(1+PCLMG \cdot \frac{q_{ia}}{E_{sat} \cdot L_{eff}}\right)}{PCLM} & \text{for } PCLMG > 0 \\ \frac{F \cdot \left(1-PCLMG \cdot \frac{q_{ia}}{E_{sat} \cdot L_{eff}}\right)}{PCLM} & \text{for } PCLMG < 0 \end{cases}$$

$$V_{asat} = V_{dsat} + E_{satL}$$

$$M_{CLM} = 1 + \frac{1}{C_{clm}} \ln\left[1 + \frac{V_{ds} - V_{dseff}}{V_{asat}} \cdot C_{clm}\right]$$

Output conductance – DIBL Effect

Adopted from BSIM4

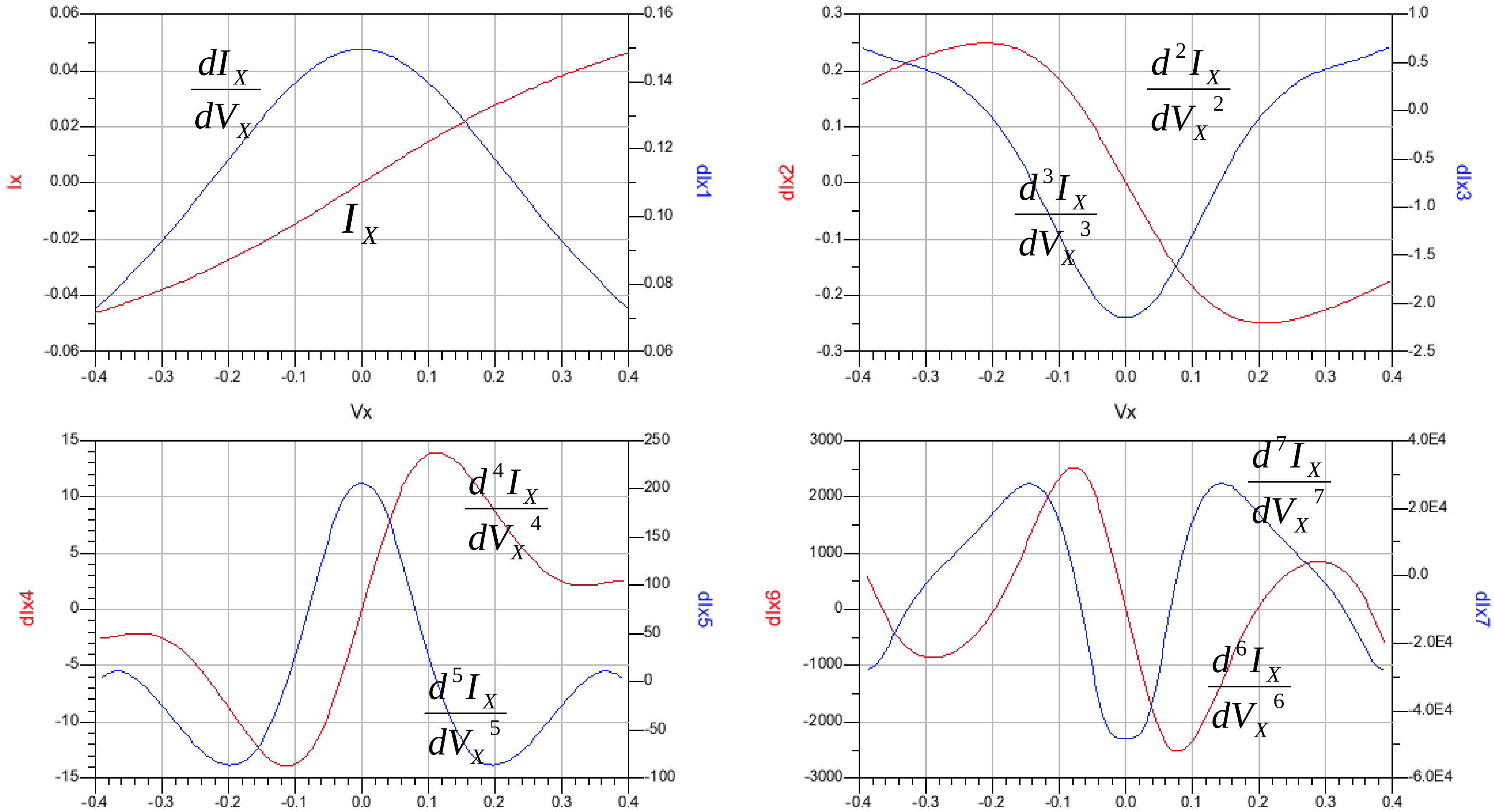
$$PVAGfactor = \begin{cases} 1 + PVAG \cdot \frac{q_{im}}{E_{sat} L_{eff}} & \text{for } PVAG > 0 \\ \frac{1}{1 - PVAG \cdot \frac{q_{im}}{E_{sat} L_{eff}}} & \text{for } PVAG < 0 \end{cases} \tag{3.104}$$

$$\theta_{rout} = \frac{0.5 \cdot PDIBL1}{cosh\left(DROUT \cdot \frac{L_{eff}}{L_{t0}}\right) - 1} + PDIBL2 \tag{3.105}$$

$$V_{ADIBL} = \frac{q_{ia} + 2kT/q}{\theta_{rout}} \cdot \left(1 - \frac{V_{dsat}}{V_{dsat} + q_{ia} + 2kT/q}\right) \cdot PVAGfactor \cdot \frac{1}{1 + PDIBLCB \cdot V_{bsx}} \tag{3.106}$$

$$M_{DIBL} = \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \tag{3.107}$$

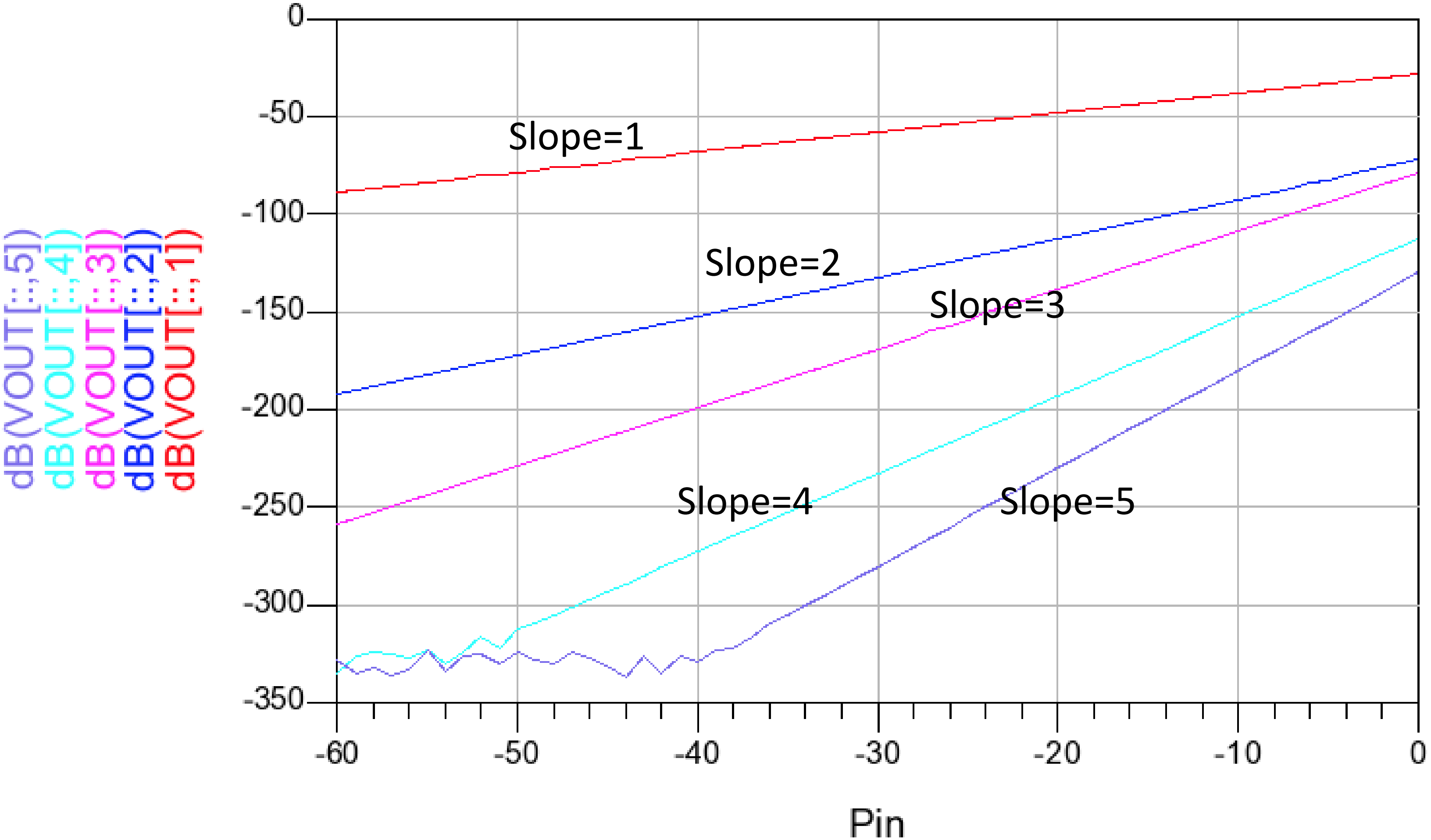
I_{DS}-V_X Gummel Symmetry



All derivatives are continuous at V_{DS}=0
(N+1 derivatives exist, where N=DELTA)

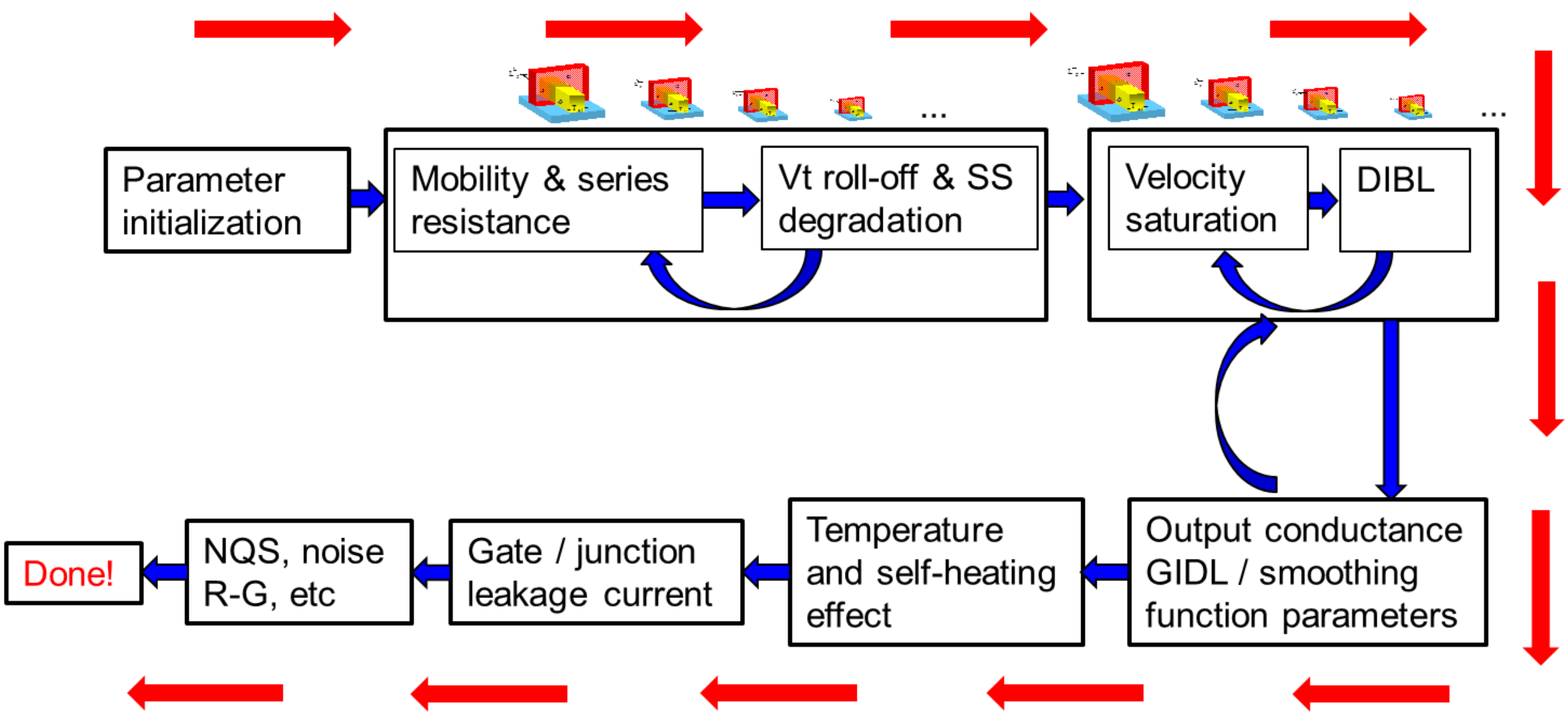
Harmonic Balance Simulation

- Accurate value of slope for all harmonics

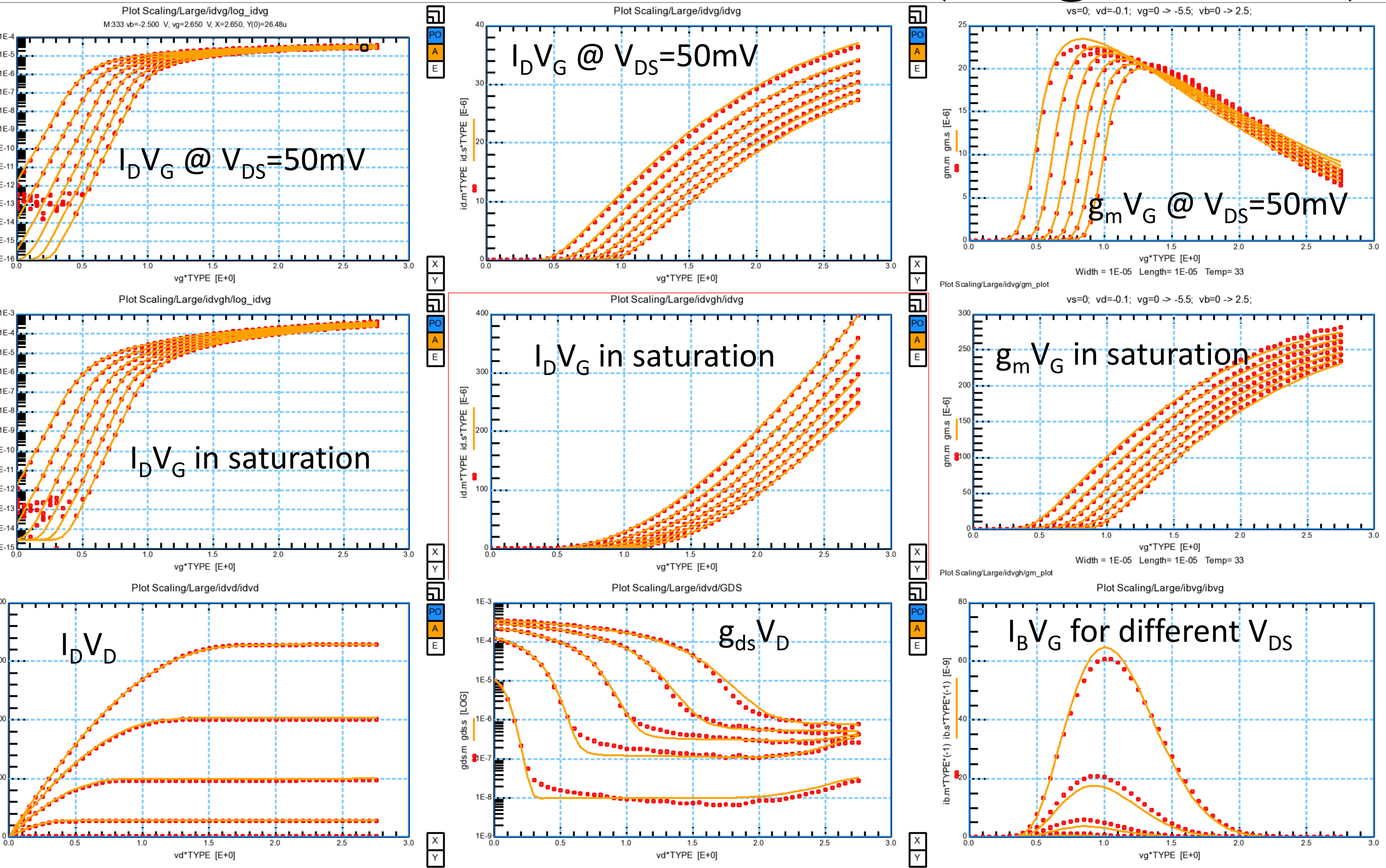


Global Extraction Procedure

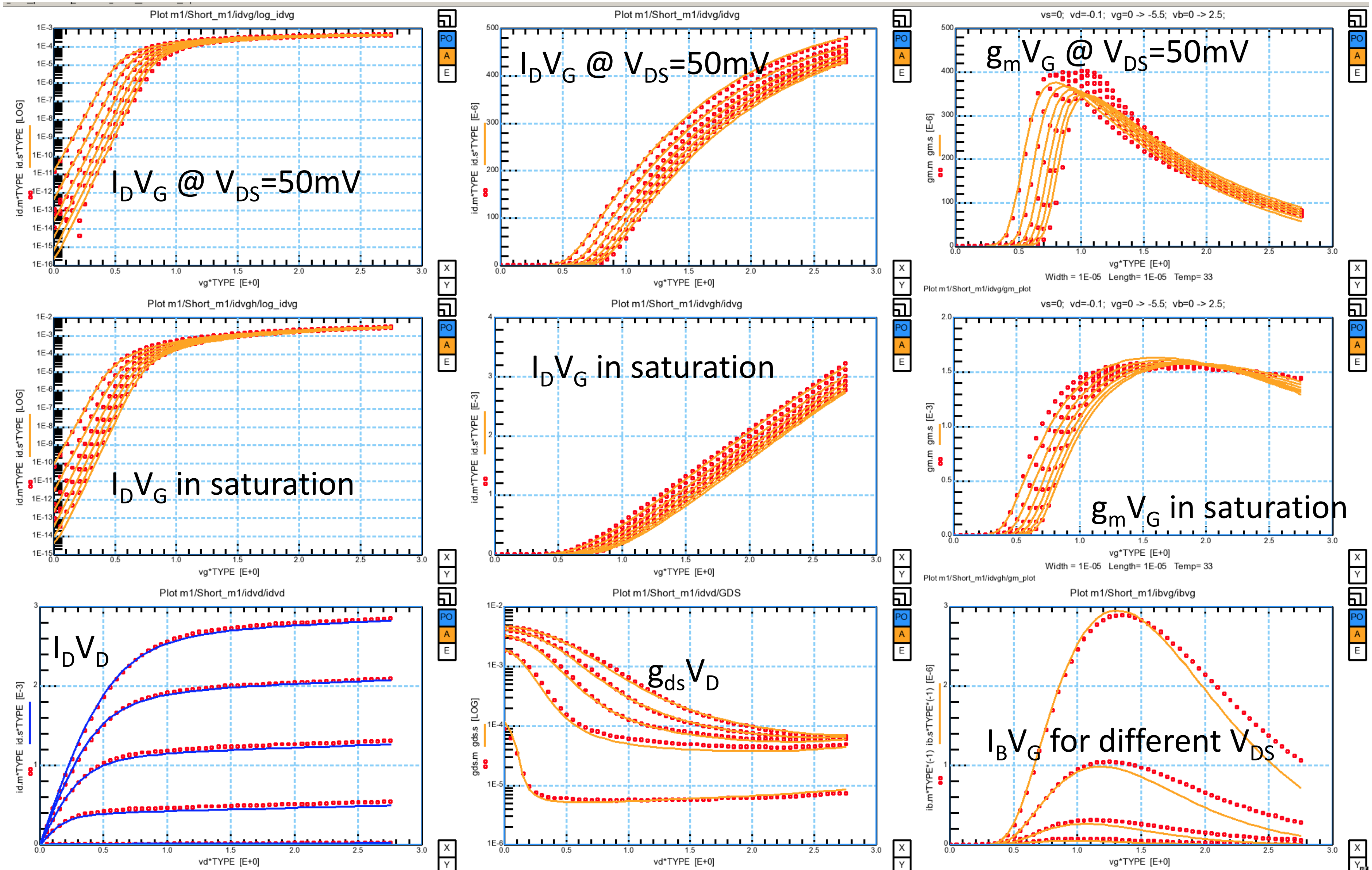
- Single set of parameters for geometrical scaling
- Step by step approach needed



Validation on Measured Data (Large device)

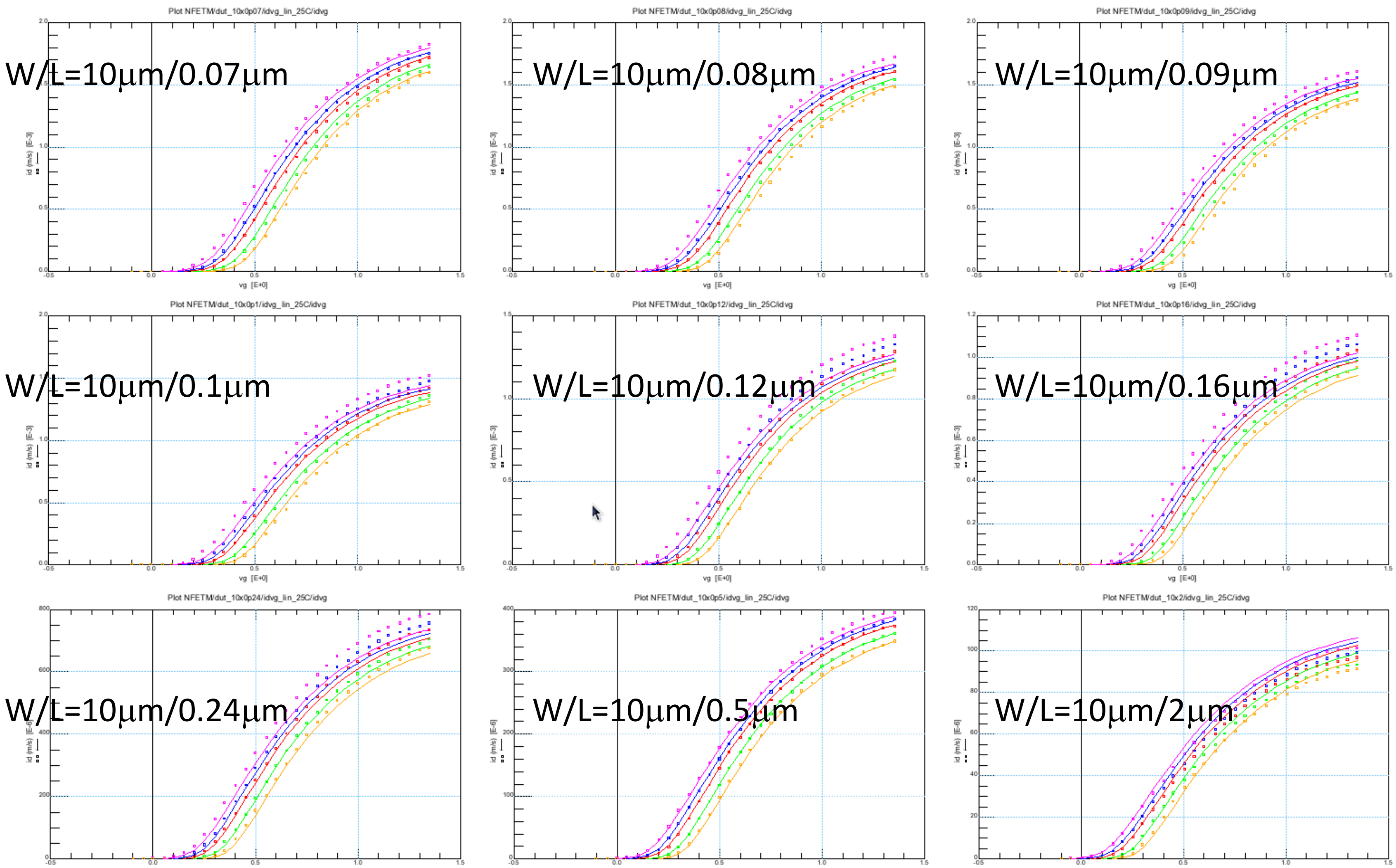


Validation on Measured Data (Short device)



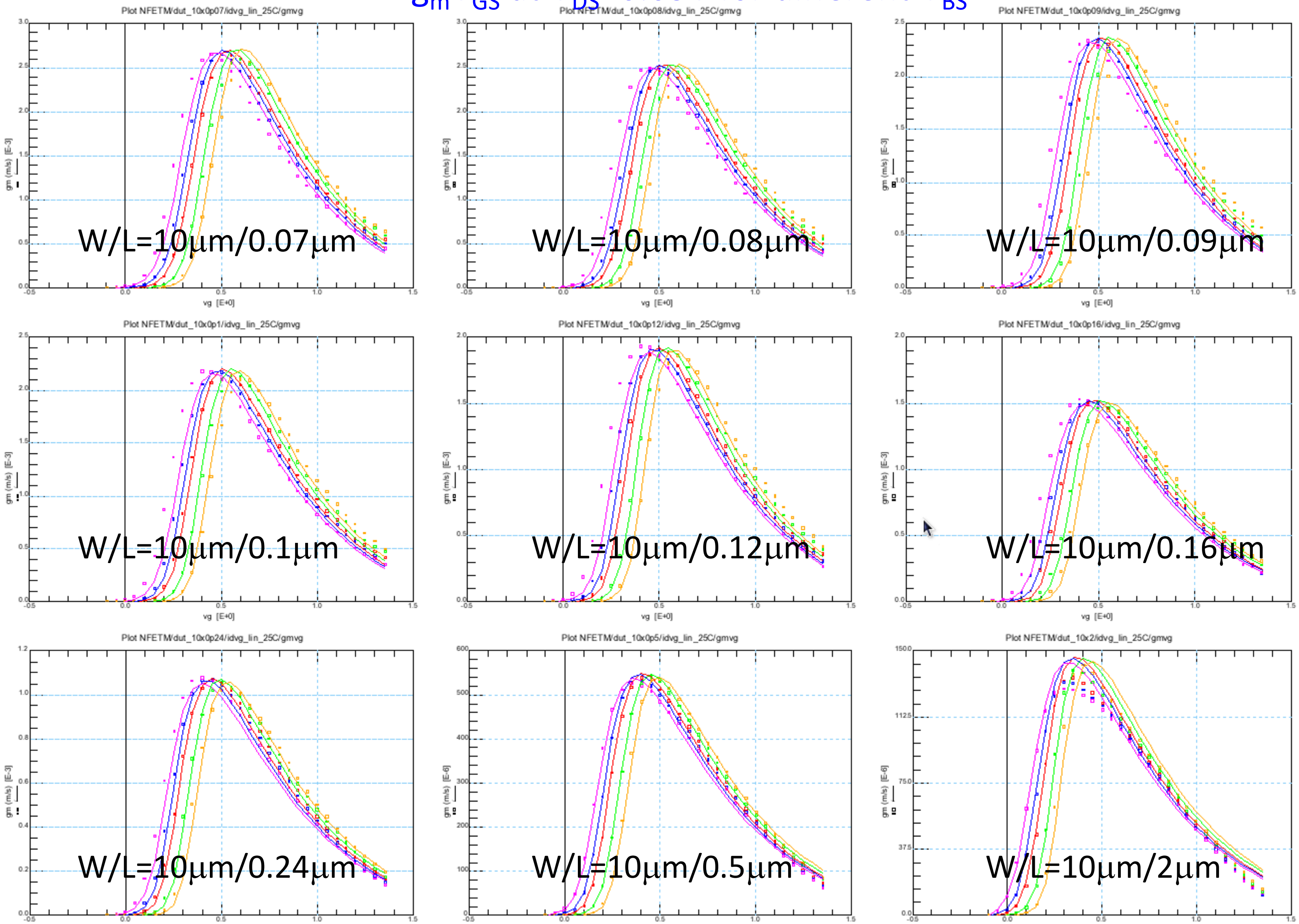
Model Validation on Measurements

$I_{DS}V_{GS}$ at V_{DS}=0.05V for different V_{BS}



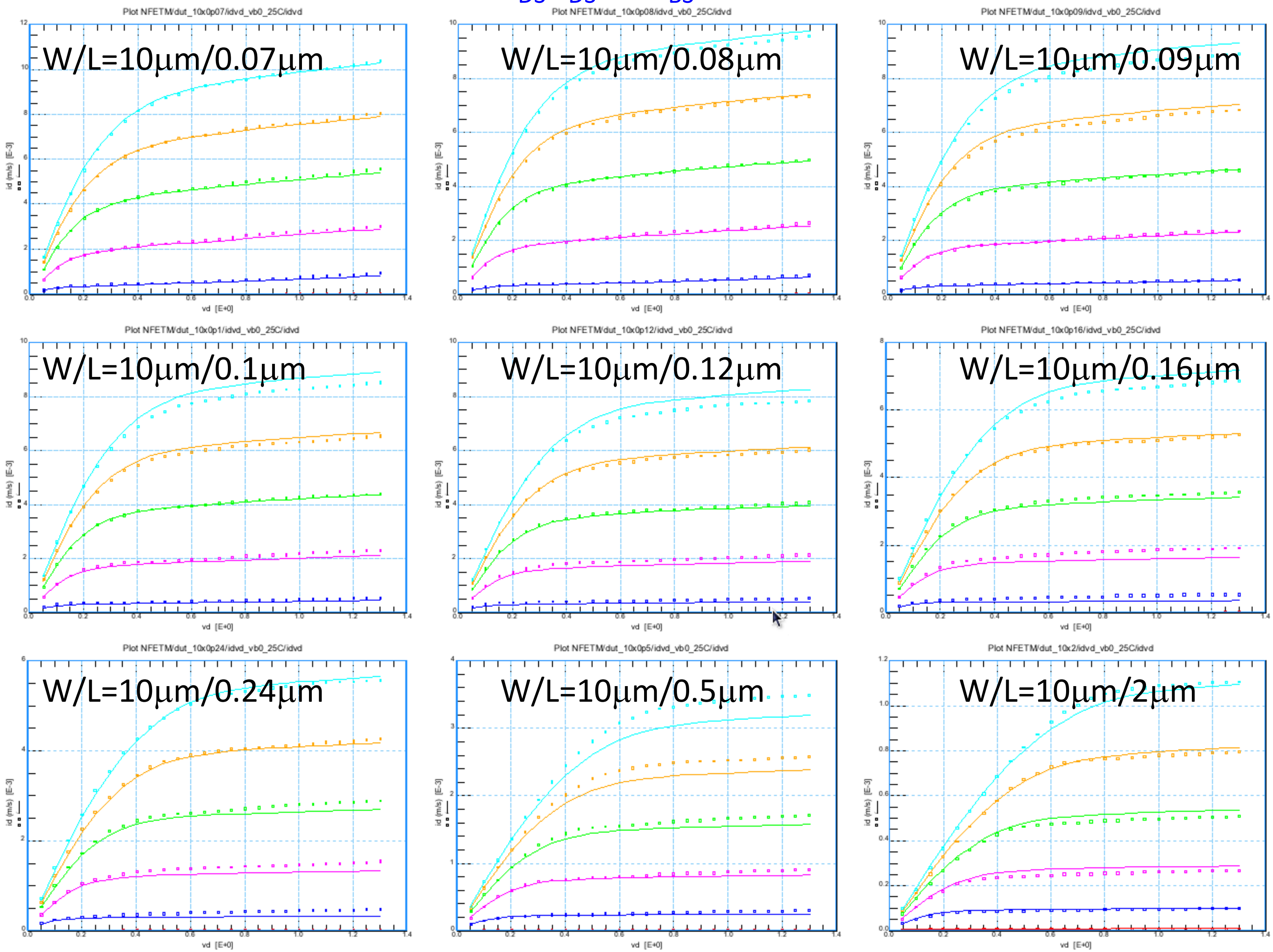
Model Validation on Measurements

$g_m V_{GS}$ at V_{DS}=0.05V for different V_{BS}



Model Validation on Measurements:

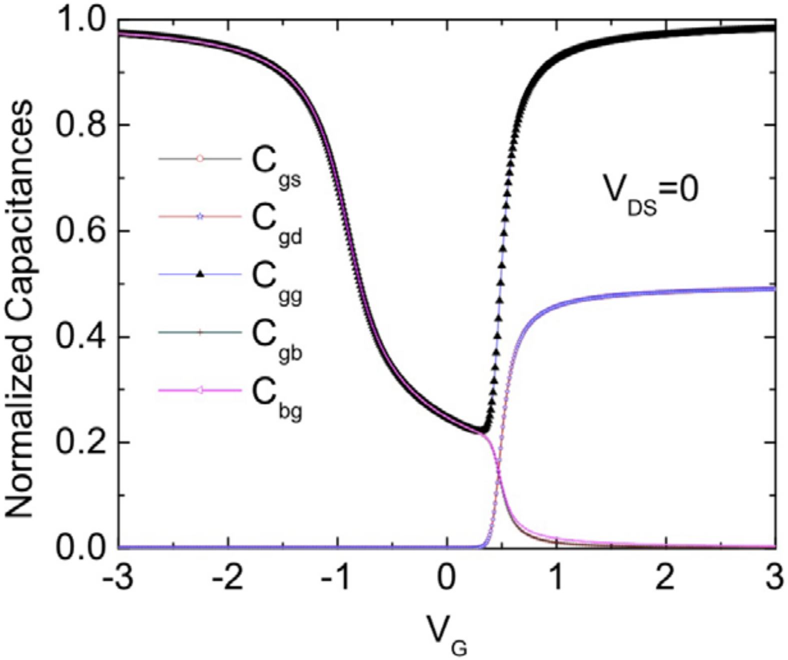
$I_{DS}V_{DS}$ at V_{BS}=0V



CV Model

- Physical Capacitance Model
- Poly-depletion & *Quantum Mechanical Effect*
- Channel Length Modulation
- *Velocity Saturation Effect*

- Charge conservation



Physical Capacitance Model

$$T_1 = \frac{v_{gpqm} + 2 \cdot q_s}{1 + 2 \cdot \chi_s}$$

$$T_2 = \frac{v_{gpqm} + 2 \cdot q_{deff}}{1 + 2 \cdot \chi_d}$$

$$T_4 = \frac{(q_s - q_{deff})^2}{3(\chi_s + \chi_d)^3}$$

$$T_7 = \frac{0.8 \cdot \left[(\chi_s + \chi_d)^2 + \chi_s \cdot \chi_d\right]}{1 + q_s + q_{deff}} + \frac{2}{\gamma_g^2}$$

$$v_{gpqm} = v_g - v_{fb} - \psi_p$$

$$\chi_s = \sqrt{0.25 + \frac{v_{gpqm} + 2 \cdot q_s}{\gamma_g^2}}$$

$$\chi_d = \sqrt{0.25 + \frac{v_{gpqm} + 2 \cdot q_{deff}}{\gamma_g^2}}$$

Also available in CV Model

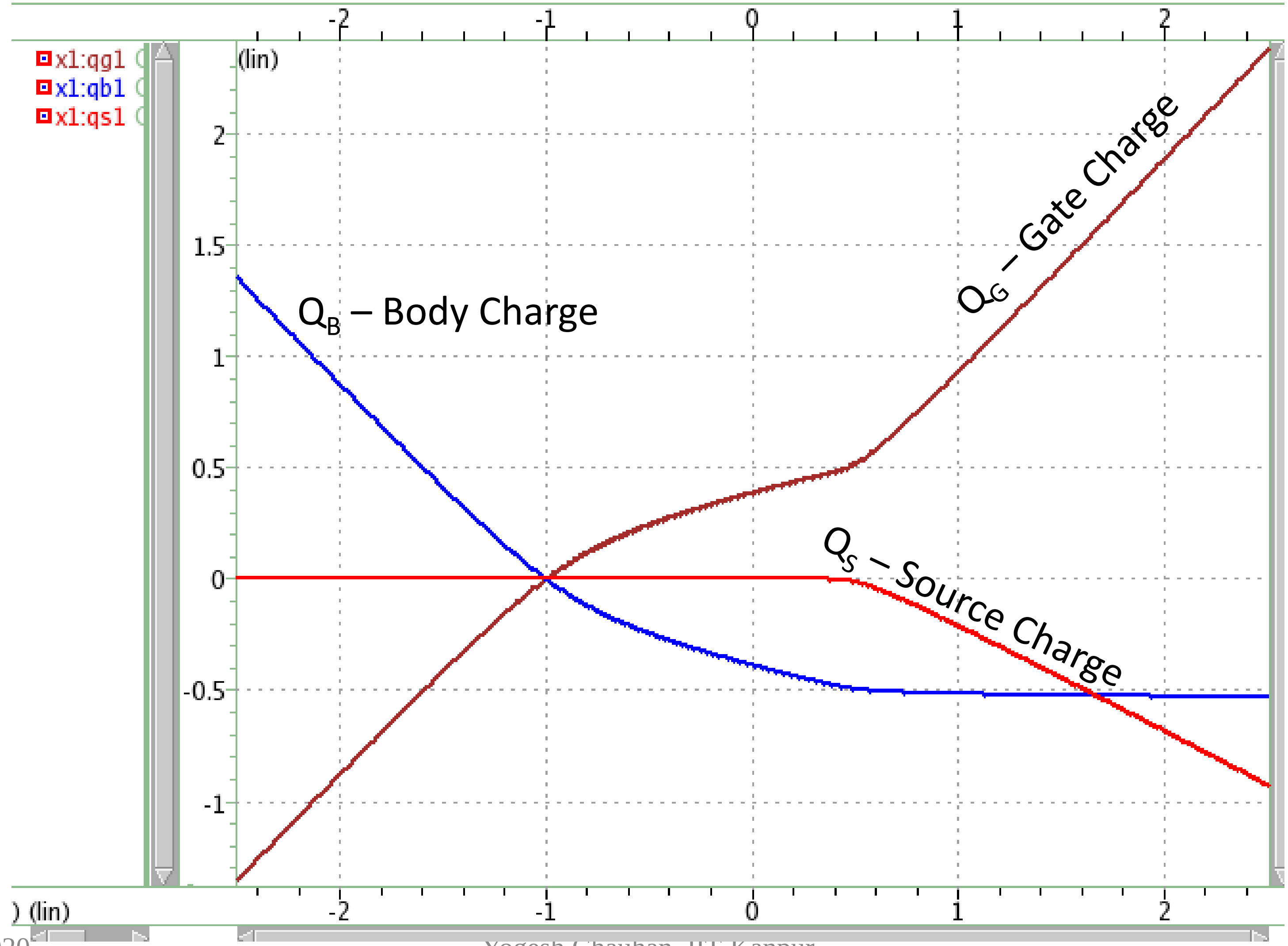
- PDE
- QME
- SCE

Bulk terminal
$$Q_b = T_1 + T_2 + \left[T_4 \cdot T_7 - n_q \cdot \left(q_s + q_{deff} + \frac{(q_s - q_{deff})^2}{3(1 + q_s + q_{deff})}\right)\right]$$

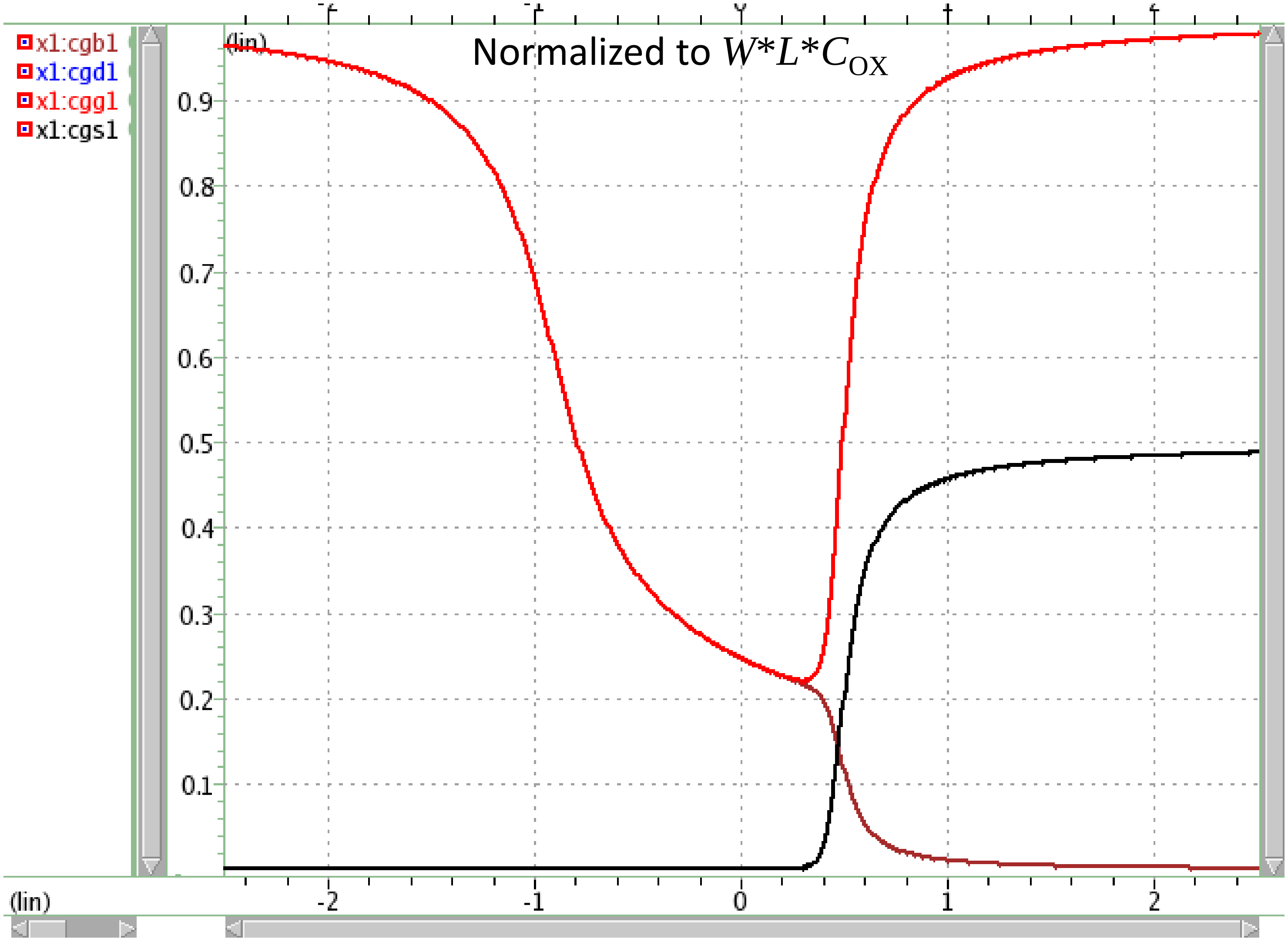
Source terminal
$$Q_s = \frac{n_q}{3}\left[2 \cdot q_s + q_{deff} + \frac{1 + 0.8 \cdot q_s + 1.2 \cdot q_{deff}}{2}\left(\frac{q_s - q_{deff}}{1 + q_s + q_{deff}}\right)^2\right]$$

Drain terminal
$$Q_d = \frac{n_q}{3}\left[q_s + 2 \cdot q_{deff} + \frac{1 + 1.2 \cdot q_s + 0.8 \cdot q_{deff}}{2}\left(\frac{q_s - q_{deff}}{1 + q_s + q_{deff}}\right)^2\right]$$

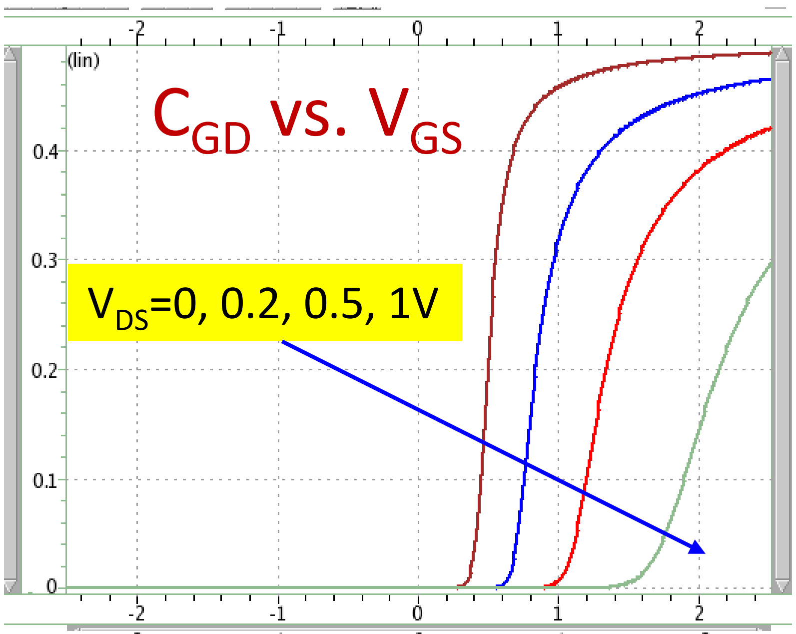
Normalized Q_G, Q_B and Q_S vs. V_{GS}

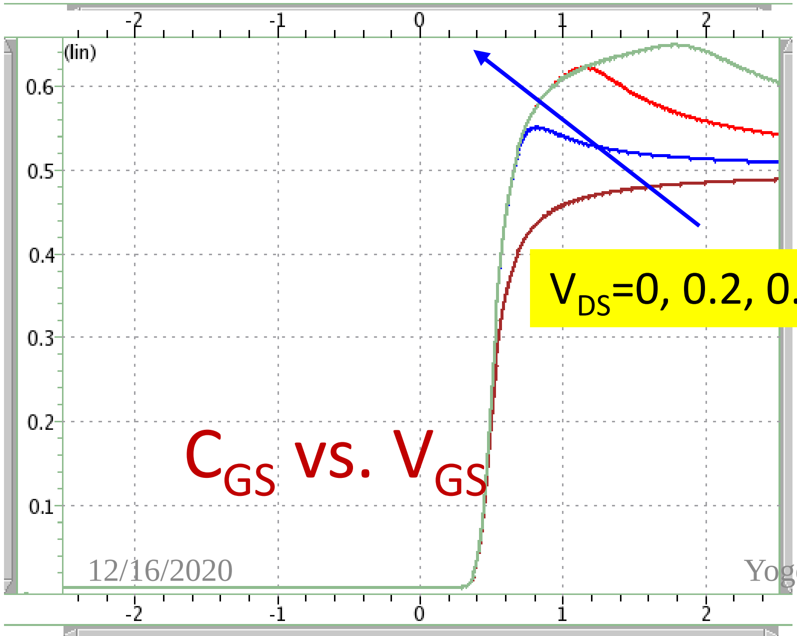


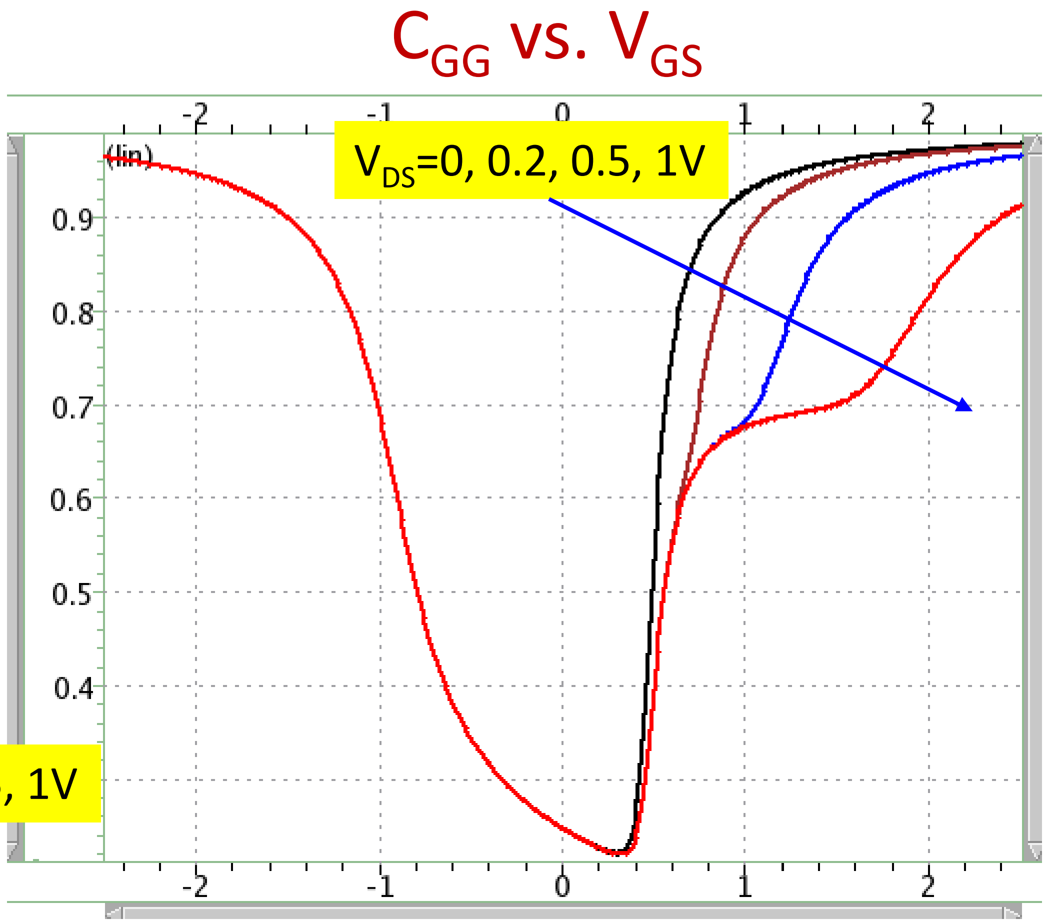
Normalized Capacitance



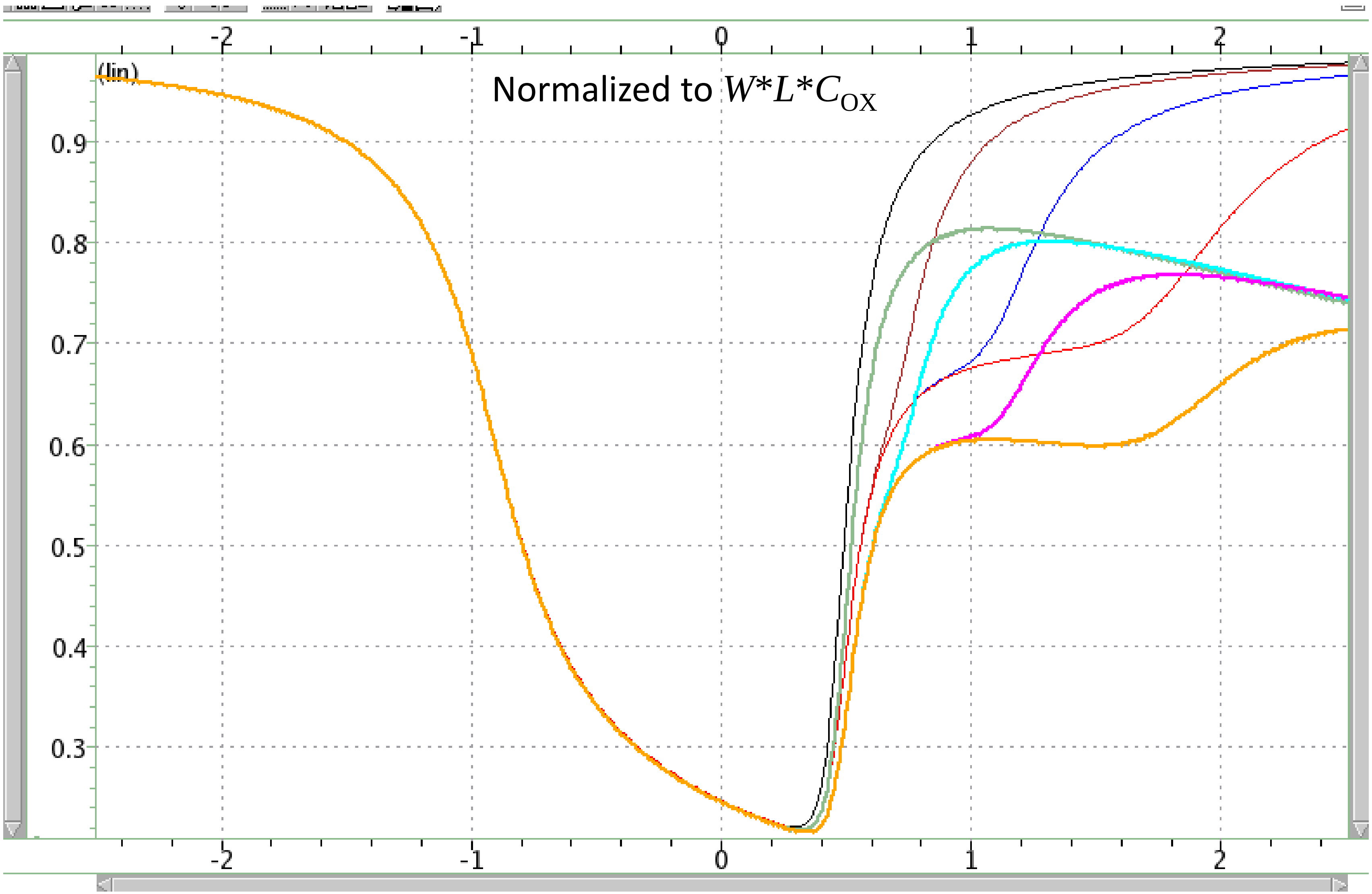
Normalized Capacitance (No QME & PDE)







Normalized C_{GG} vs. V_{GS} (with PDE only)



QME model for Capacitance

Charge centroid

$$X_{DC}^{inv} = \frac{ADOS \cdot (1.9 \cdot 10^{-9})}{1 + \left[\frac{Q_i + ETAQM \cdot Q_B}{QM0}\right]^{0.7*BDOS}}$$

$$C_{ox}^{inv} = \frac{3.9 \cdot \epsilon_0}{TOXP \cdot \frac{3.9}{EPSROX} + \frac{X_{DC}^{inv}}{\epsilon_{ratio}}}$$

Intrinsic Charge expressions:

$$WLCOXVt_{inv} = NF \cdot Wact \cdot Lact \cdot C_{ox}^{inv} \cdot nVt$$

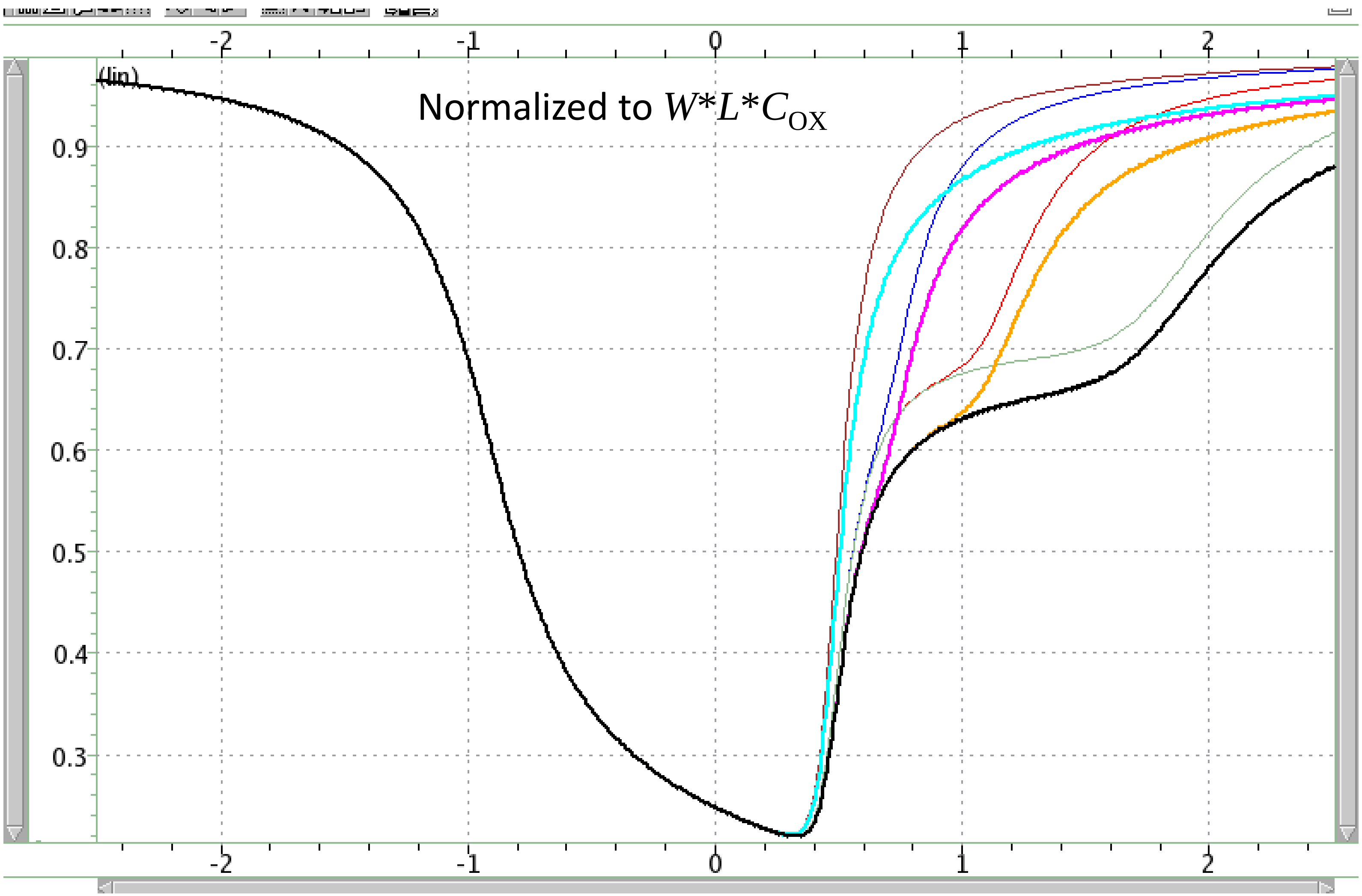
$$QBi = -NF \cdot Wact \cdot Lact \cdot \left(\frac{\epsilon_0 \cdot EPSROX}{TOXP}\right) \cdot nVt \cdot Qb$$

$$QSi = -WLCOXVt_{inv} \cdot Qs$$

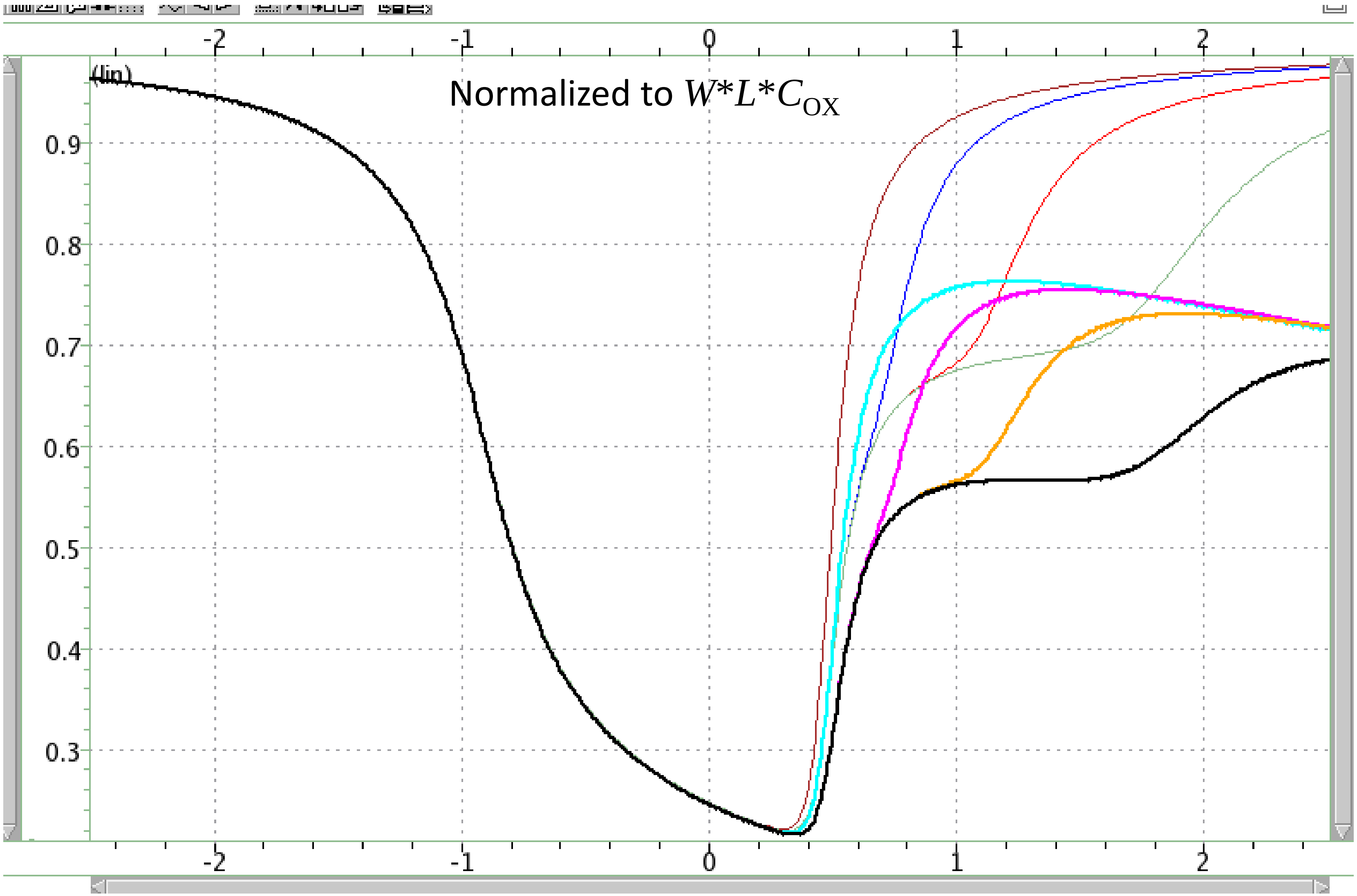
$$QDi = -WLCOXVt_{inv} \cdot Qd$$

$$QGi = QSi + QDi + QBi$$

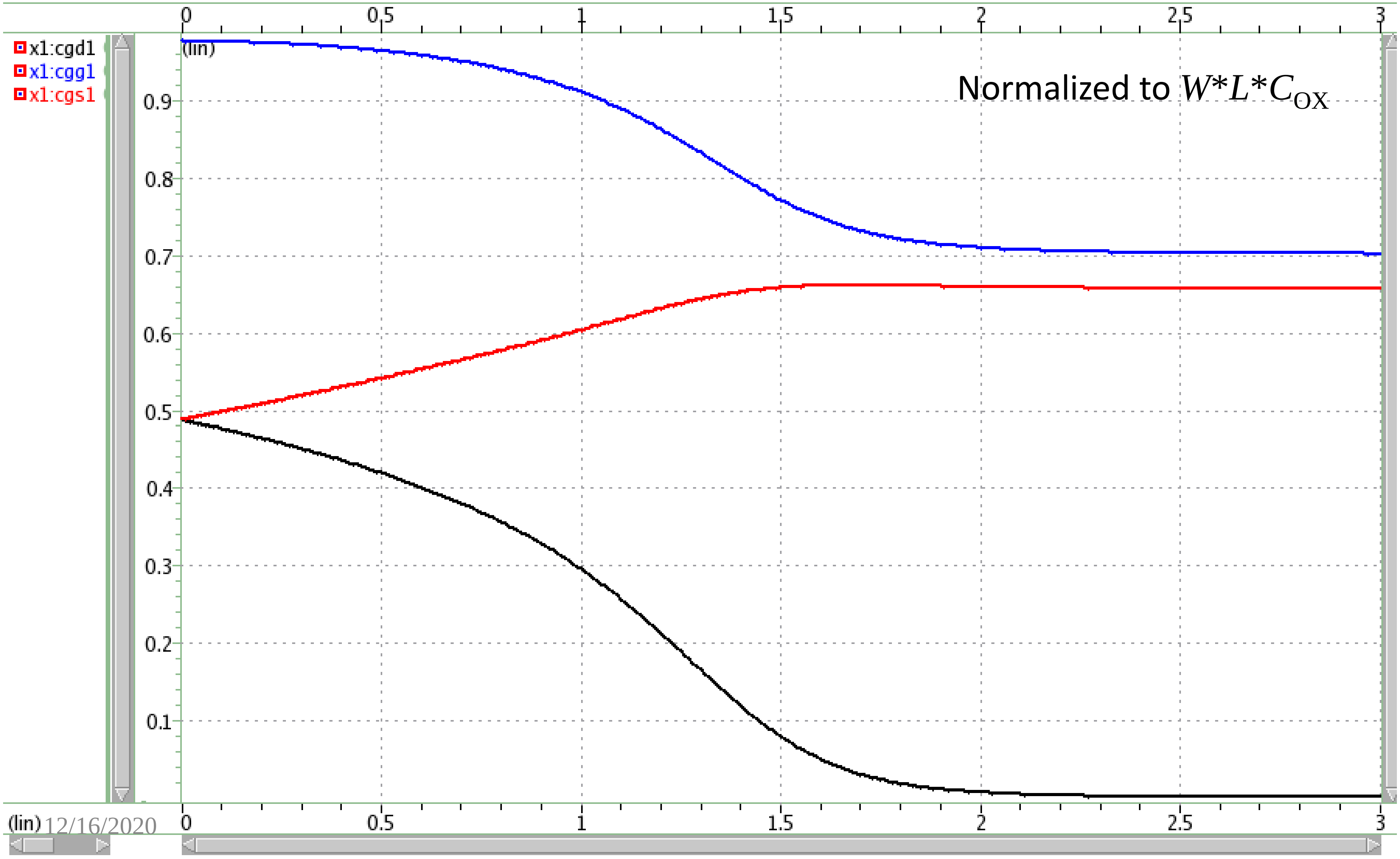
Normalized C_{GG} vs. V_{GS} (with QME only)



Normalized C_{GG} vs. V_{GS} (QME and PDE)

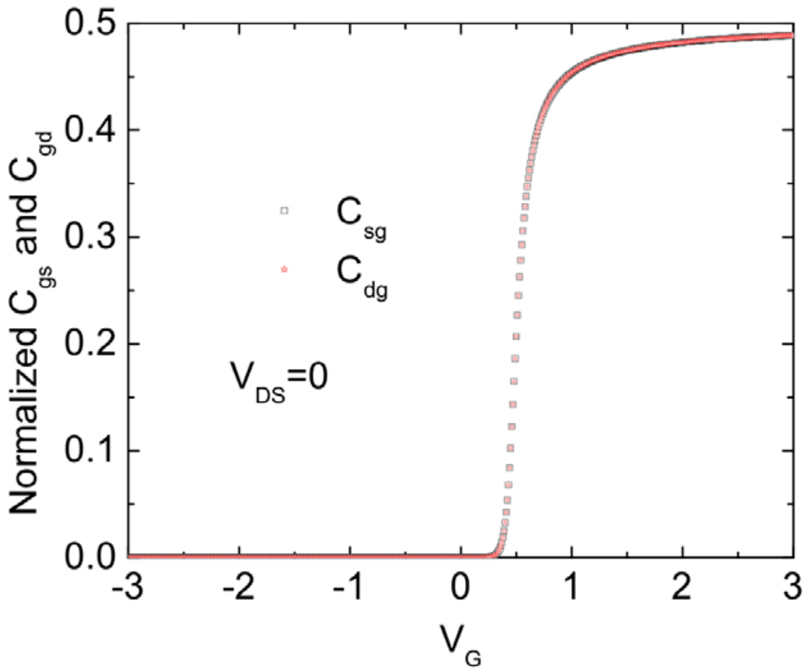


Normalized Caps vs. V_{DS}

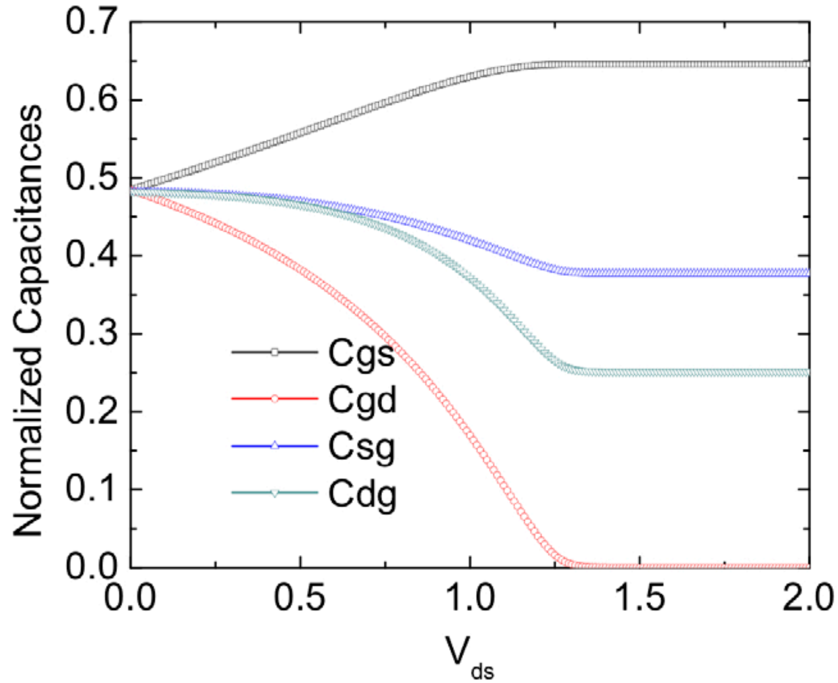


Capacitance Quality Test

$C_{SG}=C_{DG}$ @$V_{DS}=0$



$C_{GD}=C_{GS}$ @$V_{DS}=0$



Junction capacitance model

- BSIM4 junction capacitance model causes asymmetry
- Updated junction capacitance model for AC symmetry

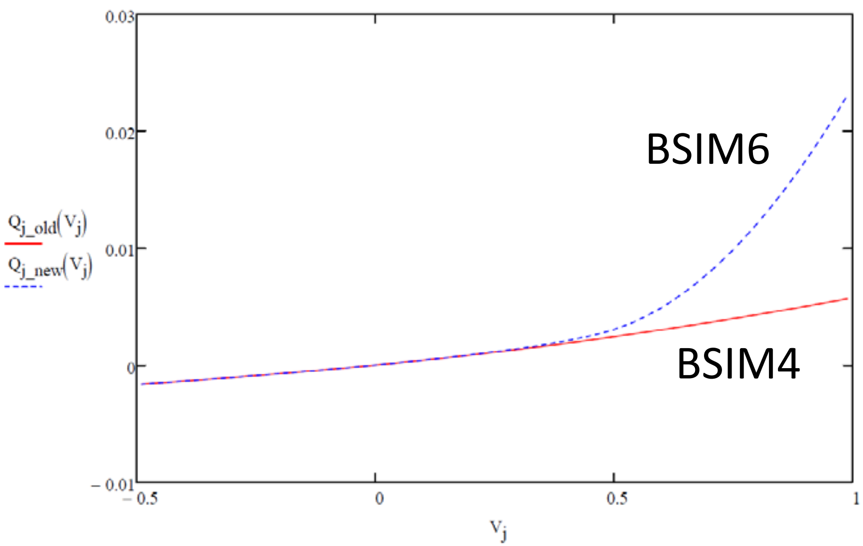
$$Q_{j\_old}(V_j) := \begin{cases} C_j \cdot PBS \cdot \dfrac{1 - \left(1 - \dfrac{V_j}{PBS}\right)^{1-MJS}}{1 - MJS} & \text{if } V_j < 0 \\ 0 & \text{if } V_j = 0 \\ V_j \cdot C_j + V_j^{2} \cdot \dfrac{MJS \cdot C_j}{2 \cdot PBS} & \text{if } V_j > 0 \end{cases}$$

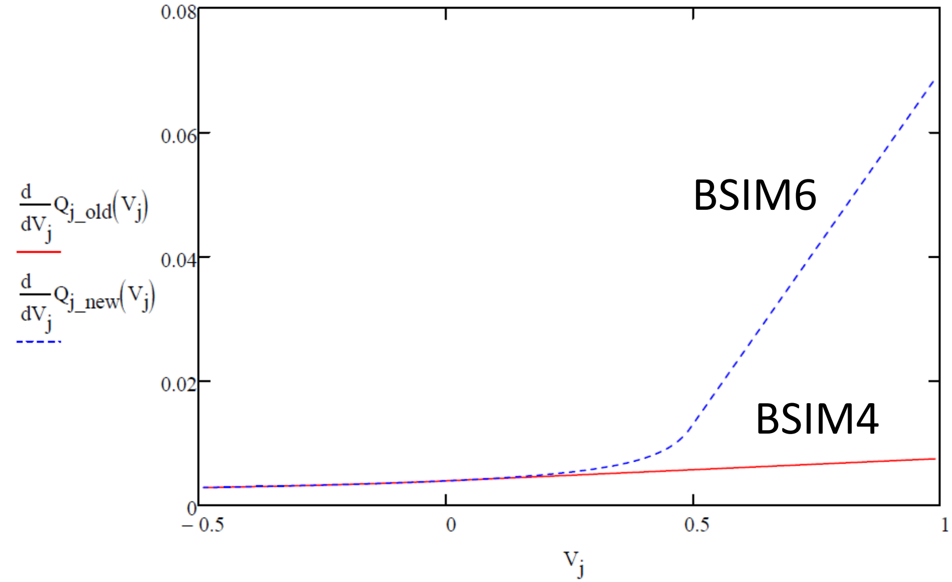
Transition point is at V_j=0

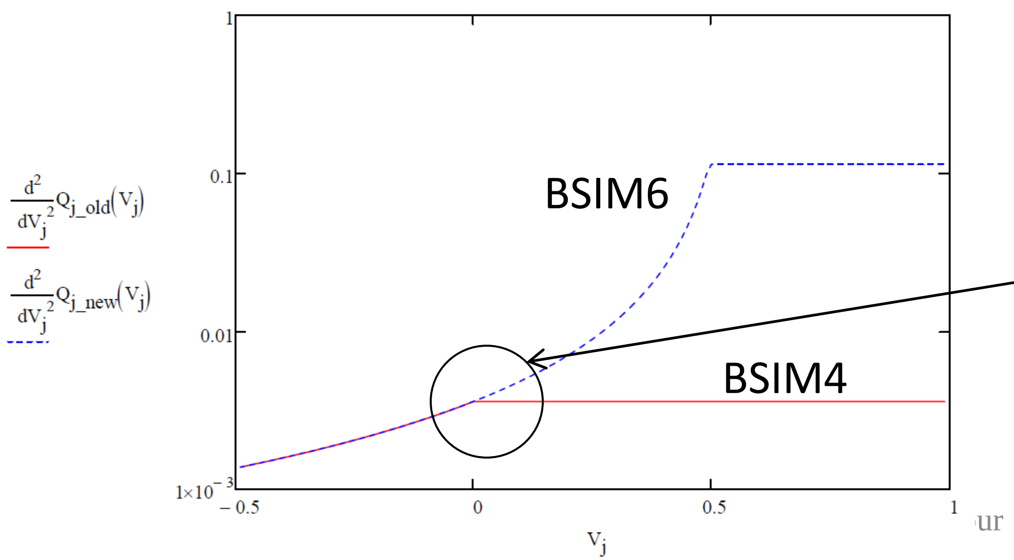
$$Q_{j\_new}(V_j) := \begin{array}{l} x_0 \leftarrow 0.9 \\ C_j \cdot PBS \cdot \dfrac{1 - \left(1 - \dfrac{V_j}{PBS}\right)^{1-MJS}}{1 - MJS} \quad \text{if } \dfrac{V_j}{PBS} < x_0 \\ C_j \cdot PBS \cdot \dfrac{1}{(1 - x_0)^{MJS}} \cdot \left(1 - \dfrac{V_j}{PBS}\right) \cdot \left[\dfrac{1}{2} \cdot MJS \cdot \dfrac{1}{(1 - x_0)} \cdot \left(1 - \dfrac{V_j}{PBS}\right) - (1 + MJS)\right] + C_j \cdot \dfrac{PBS}{1 - MJS} \cdot \left[1 - \dfrac{MJS}{2} \cdot (1 + MJS) \cdot (1 - x_0)^{1-MJS}\right] \quad \text{otherwise} \end{array}$$

Transition point is at V_j=0.9V

Junction capacitance model

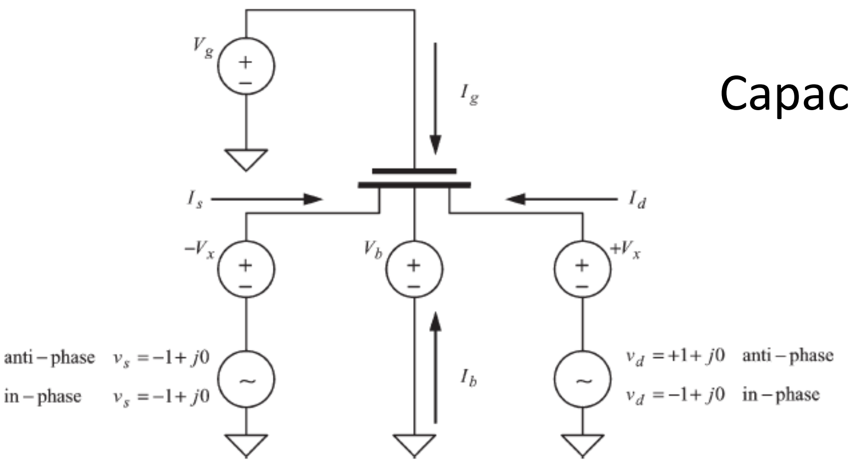




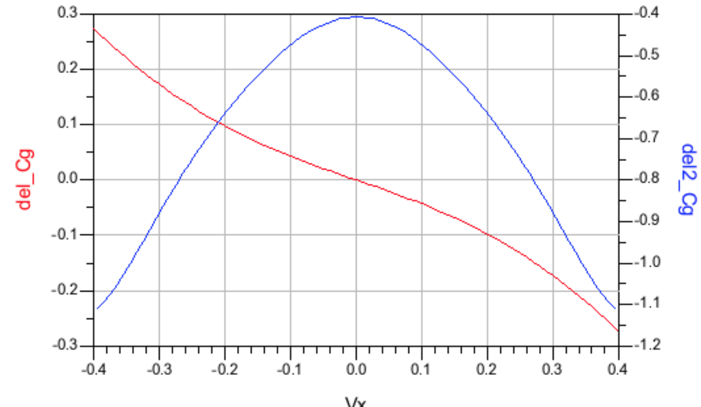


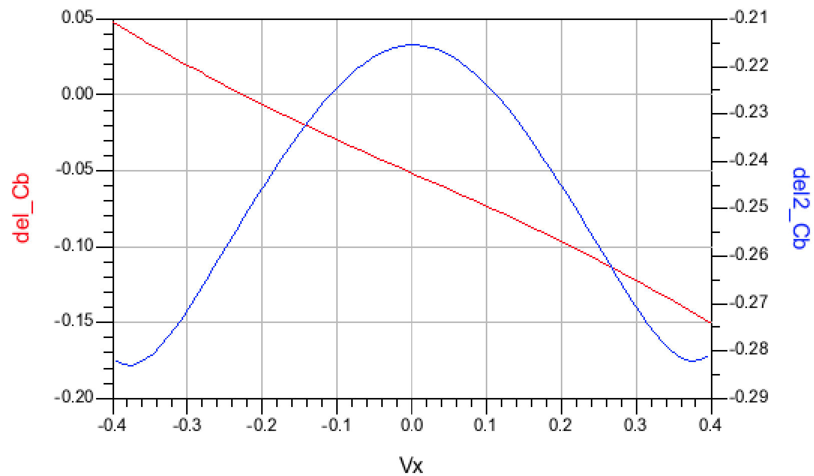
- Symmetry problem using old Q_j
- New model is infinitely differentiable @ V_{DS}=0

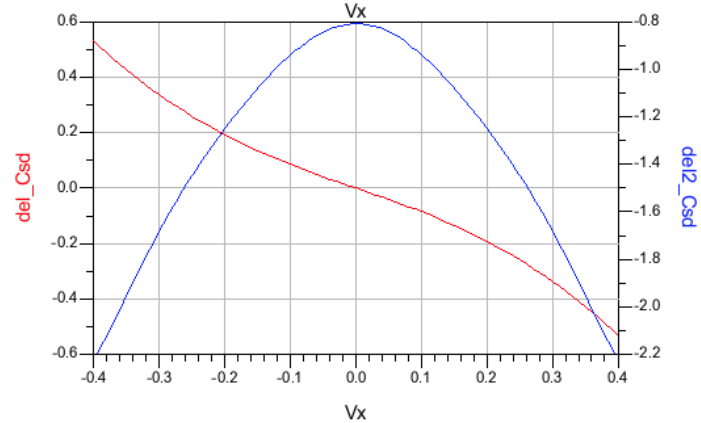
AC Symmetry test



Capacitance & derivatives are symmetric



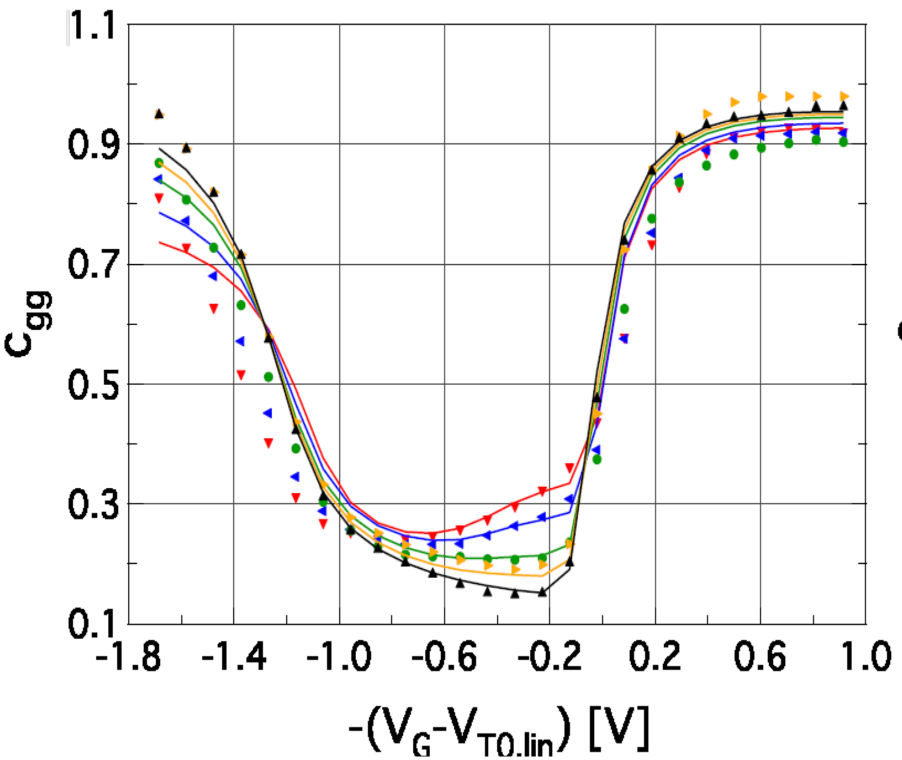




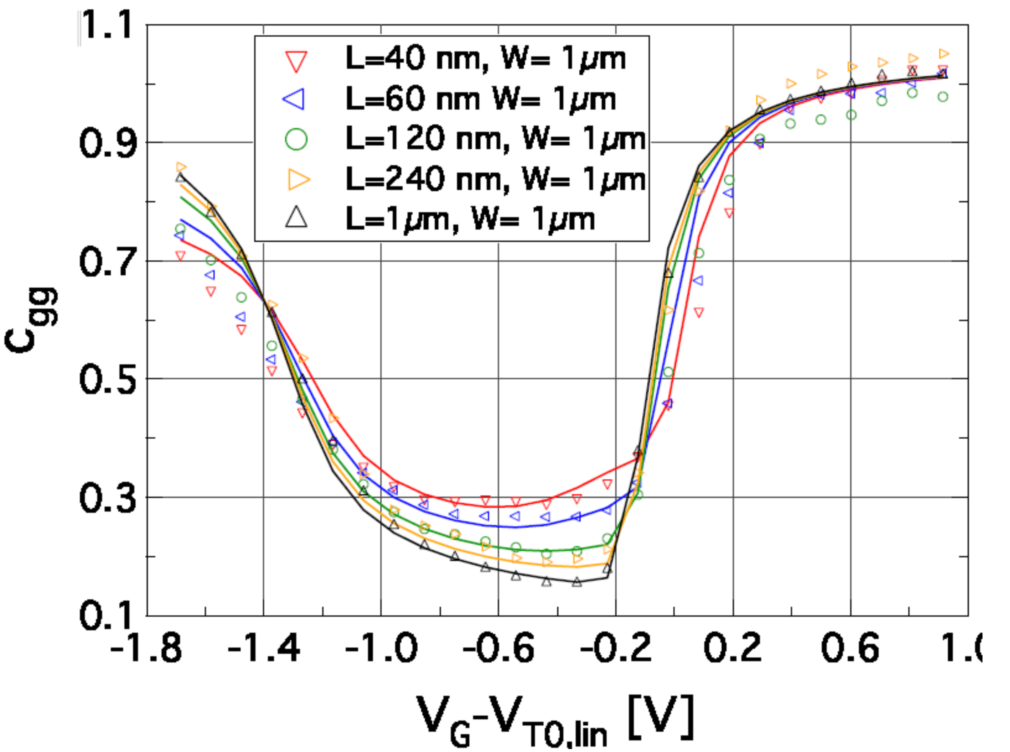
Ref. - C. McAndrew, IEEE TED, 2006

BSIM6 Validation – Gate Capacitance

PMOS



NMOS



C_{gg} normalized to C_{ox}.WL

RF Validation

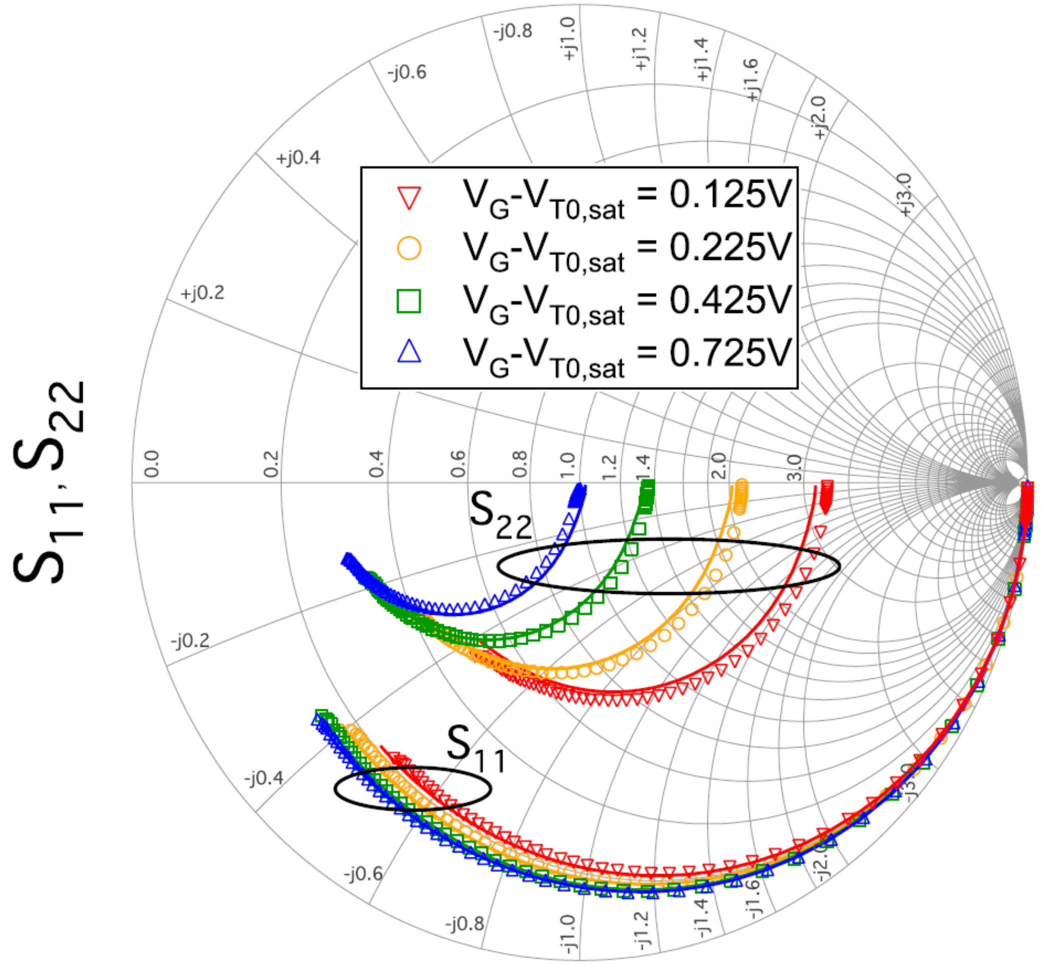
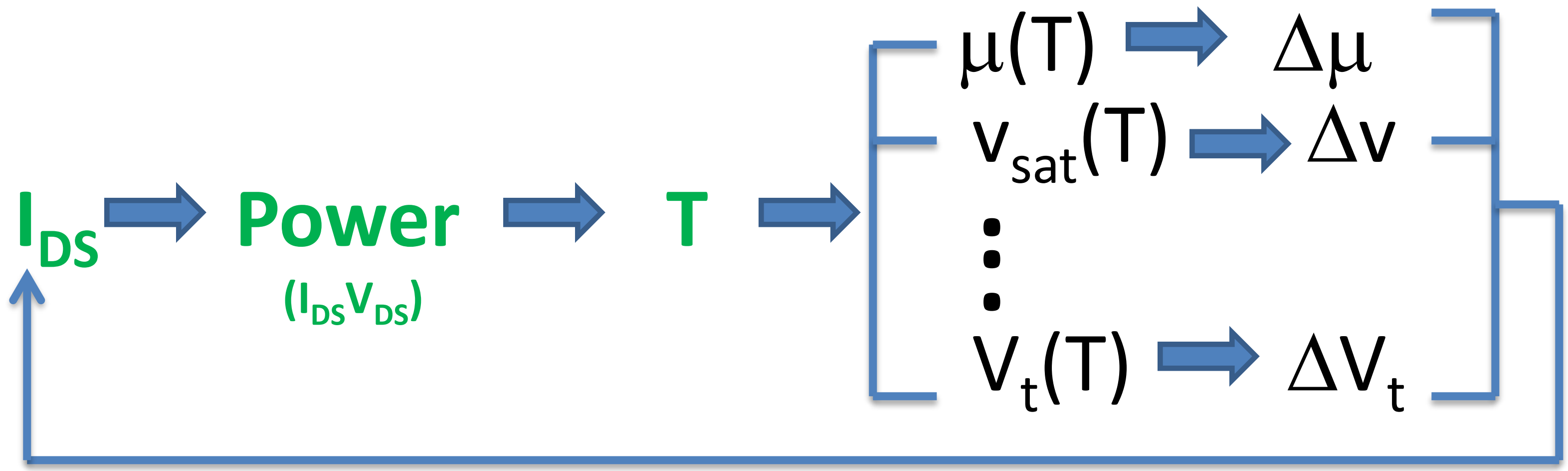
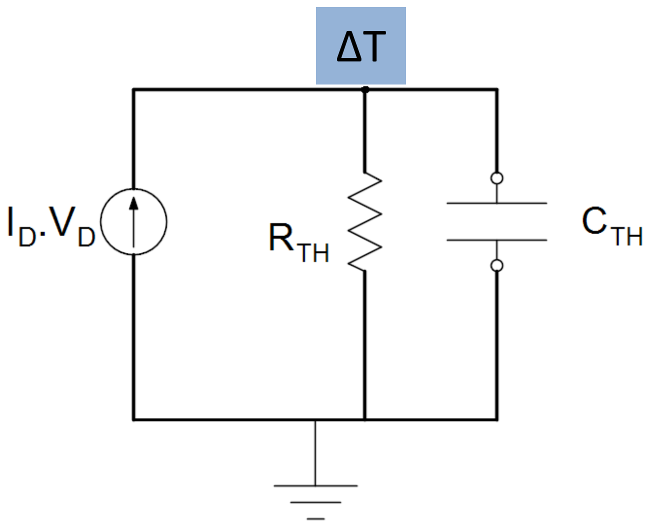


Fig. 12. Smith chart of S_{11} and S_{22} parameters at $V_G - V_{T0,sat} =$ [0.125, 0.225, 0.425, 0.725] V and $V_D = 1.1$ V.

Modeling of Self-Heating Effect



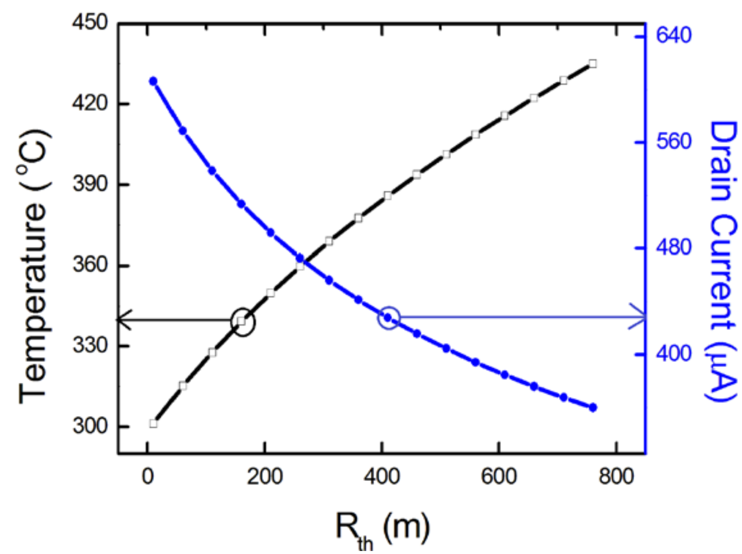
- Self Heating Effect is modeled by using Thermal Network
- Voltage at thermal node 'ΔT' is rise in temperature.
- This Voltage (ΔT) is added to the temperature variable in the model.



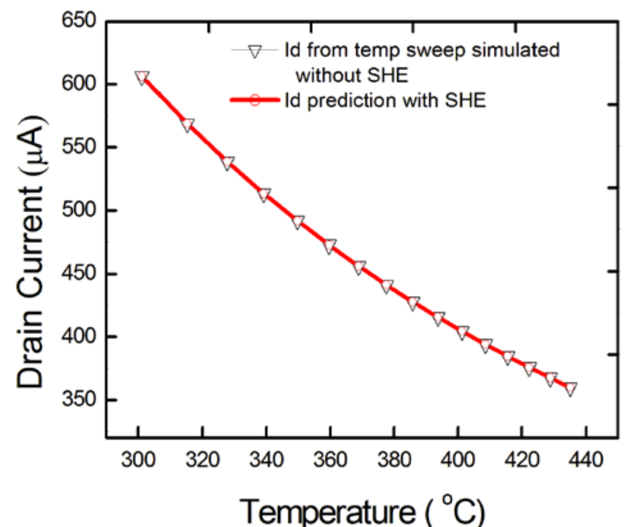
Ref.: BSIM-SOI Model

Self Heating Model – Quality Test

- **Step 1**: For transistor biased in saturation, sweep R_{TH} (thermal resistance) with self heating ON, observe current and temperature.



- Step 2: Switch off self heating model, simulate the same circuit for temperature range obtained in step 1.

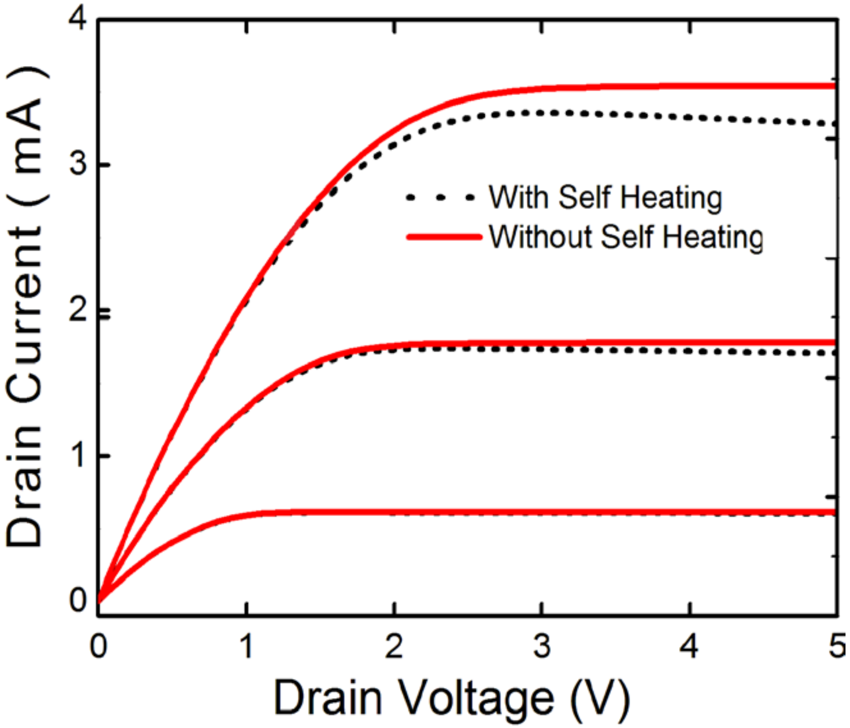


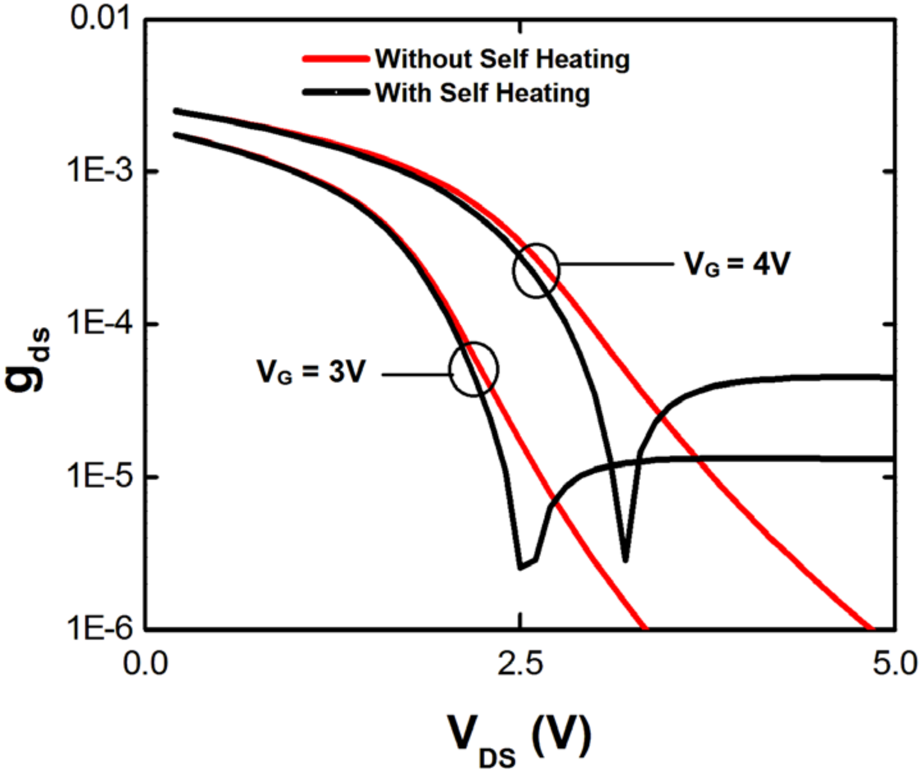
- *Drain current obtained from both the steps should be same.*

Ref: G. Gildenblat, Compact Modeling: Principles, Techniques and Applications, Springer, 2010.

Self Heating Effect: Output Characteristics

- Drain current reduces in high power region.
  - Negative 'gds'





Modeling of Gate Resistance and NQS in BSIM-BULK Model

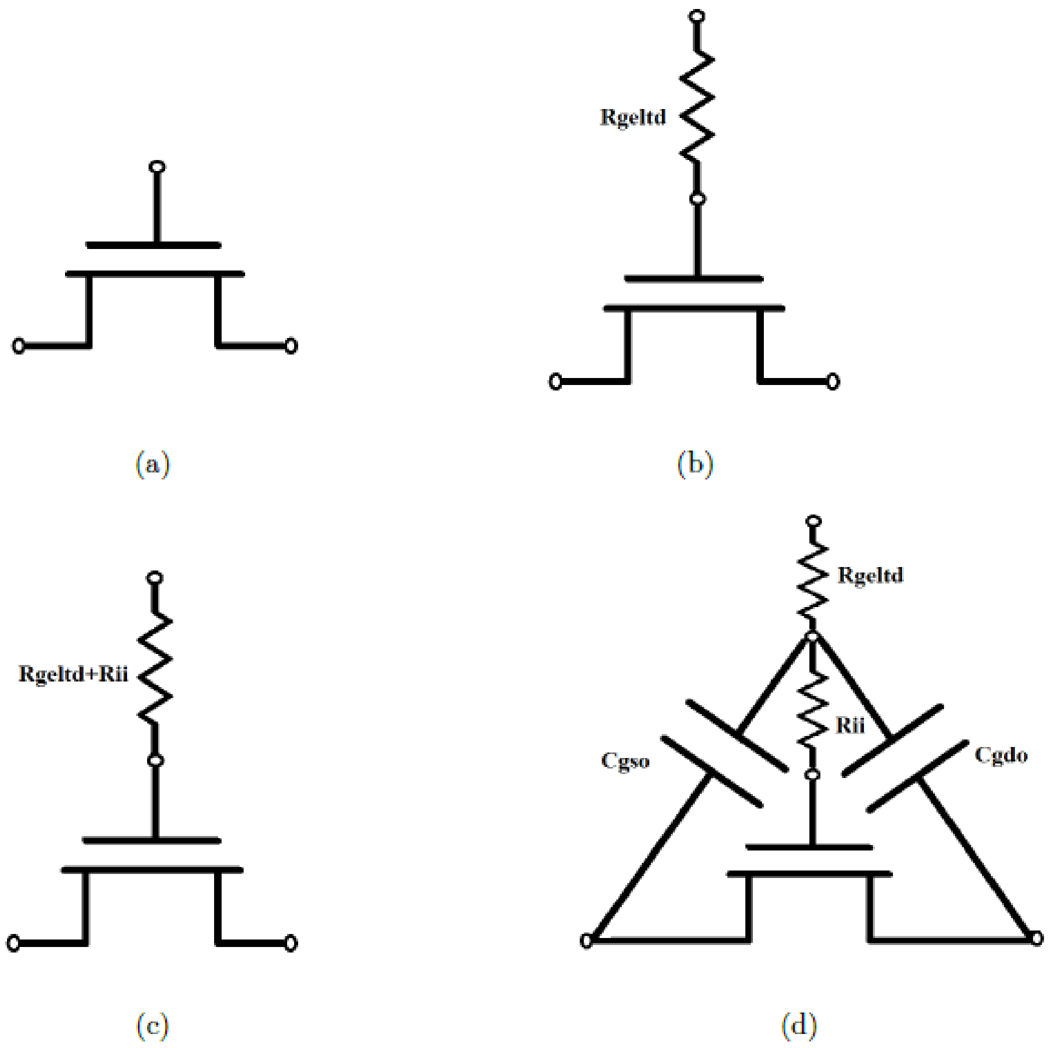


Figure 2: Gate resistance network for (a) $RGATEMOD = 0$ (b) $RGATEMOD = 1$ (b) $RGATEMOD = 2$ (d) $RGATEMOD = 3$.

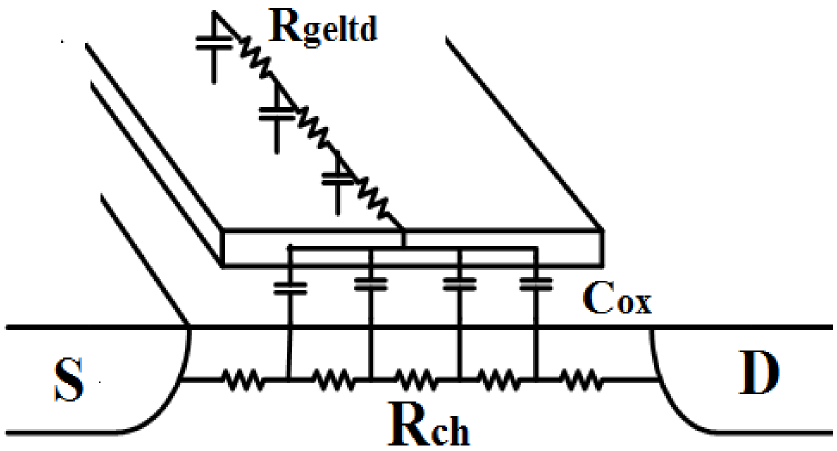
NQS(Non-Quasi-Static) Effect

In QS modeling: charge is a function of terminal voltages only.

$$Q(t) = Q(V_G(t), V_D(t), V_S(t), V_B(t))$$

In NQS modeling: charge is a not only a function of terminal voltages but also an explicit function of time.

$$Q(t) = Q(V_G(t), V_D(t), V_S(t), V_B(t), t)$$

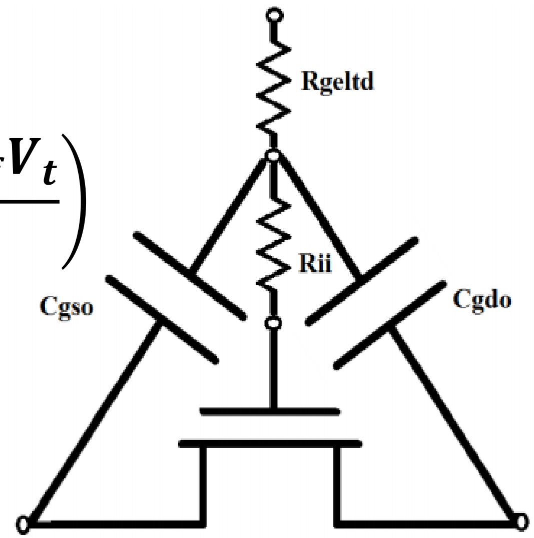


- The onset frequency of NQS (f_{nqs}) is typically around $\approx \frac{f_t}{3}$.

NQS(Non-Quasi-Static) Effect

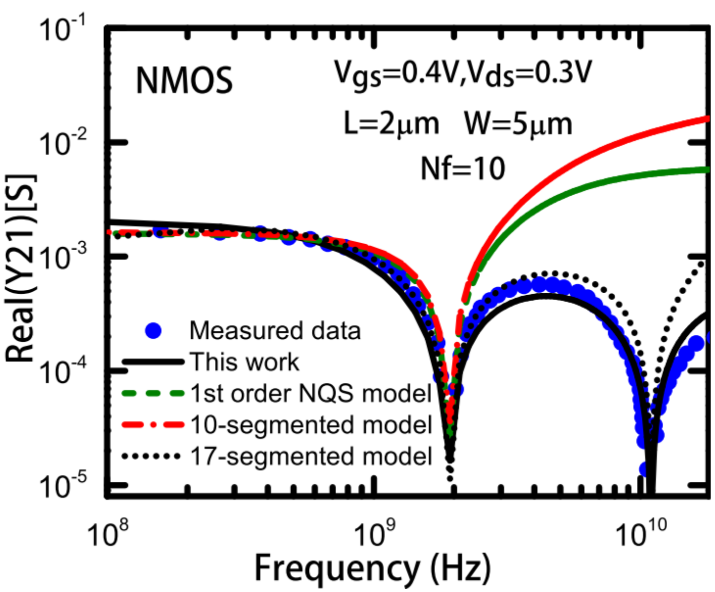
This is first order NQS model

$$\frac{1}{R_{ii}} = \mathbf{XRCRG1} \cdot \mathbf{NF} \cdot \left(\frac{\mathbf{I}_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff}\mu_{eff}C_{oxeff}V_t}{L_{eff}} \right)$$



R_{ii} is the channel reflected NQS resistance

R_{geltd} is used as the Gate Electrode Resistance



- Segmentation model with segments ≥ 17 can capture the NQS trend
- Increases the computational time

This approach has been there in the present BSIM-BULK model

NQS: Improved Model

✓ **Modeling of Channel RC Network**

✓ **Modeling of Gate Electrode RC Network**

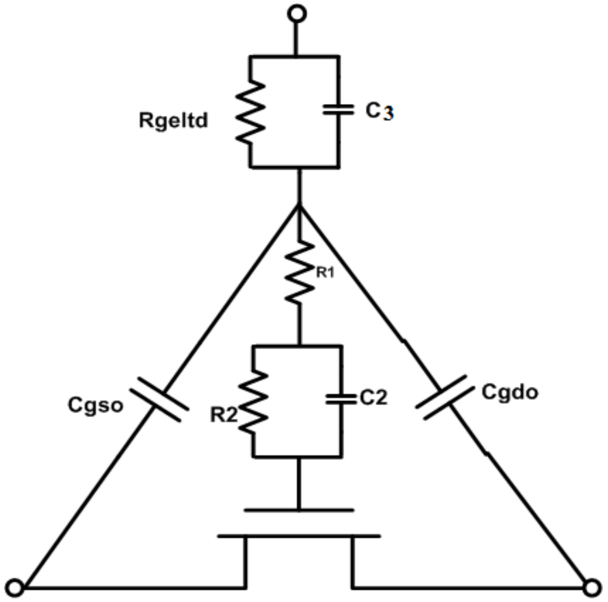
$R_1 = \frac{R_{ch}}{40}, R_2 = \frac{7R_{ch}}{120}, R3 = \frac{R_g}{3}, \mathrm{C}_2 = \frac{20\mathrm{C_{OX}}}{49}$ and $\mathrm{C}_3 = \frac{6C_{OX}}{5}$

$$\frac{1}{R_1} = XRCRG1.\frac{1}{R_{ch}} \quad \frac{1}{R_2} = XRCRG2.\frac{1}{R_{ch}}$$

$$\mathrm{C}_2 = XRCCG.CGGI$$

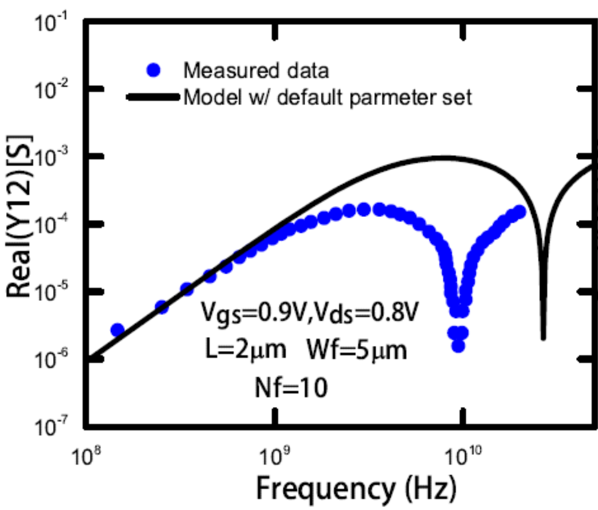
$$R_3 = R_{geltd}\ and\ C_3 = XGCCG.C_{GG}$$

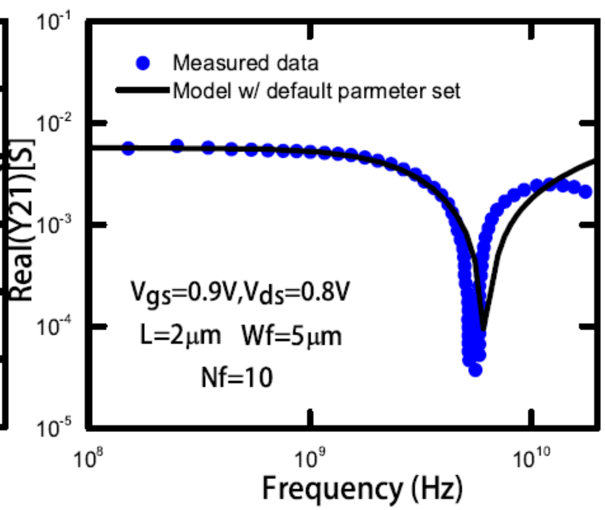
where, $\boldsymbol{XRCRG1 = 40, XRCRG2 = \frac{120}{7},}$
$\boldsymbol{XRCCG = \frac{49}{20}}$ **and** $\boldsymbol{XGCCG = \frac{6}{5}}$

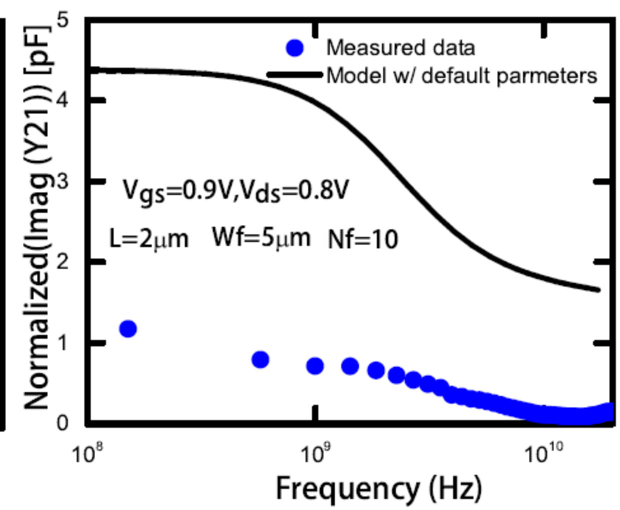


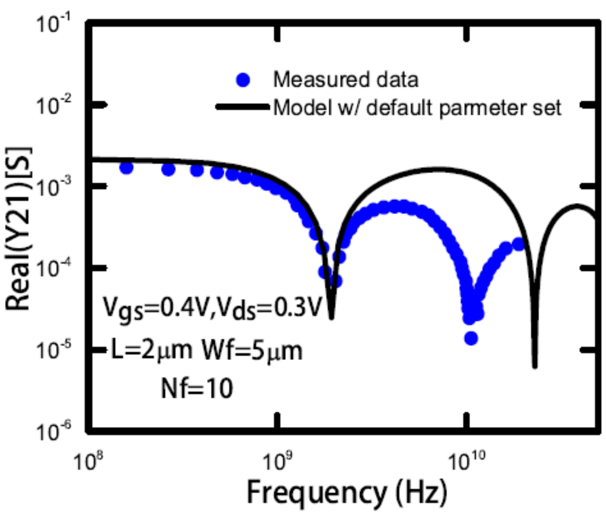
C. Gupta, N. Mohamed, H. Agarwal, R. Goel, C. Hu, and Y. S. Chauhan, "Accurate and Computationally Efficient Modeling of Nonquasi Static Effects in MOSFETs for Millimeter Wave Applications", IEEE Transactions on Electron Devices, Vol. 66, Issue 1, pp. 44-51, Jan. 2019.

NQS: Improved Model







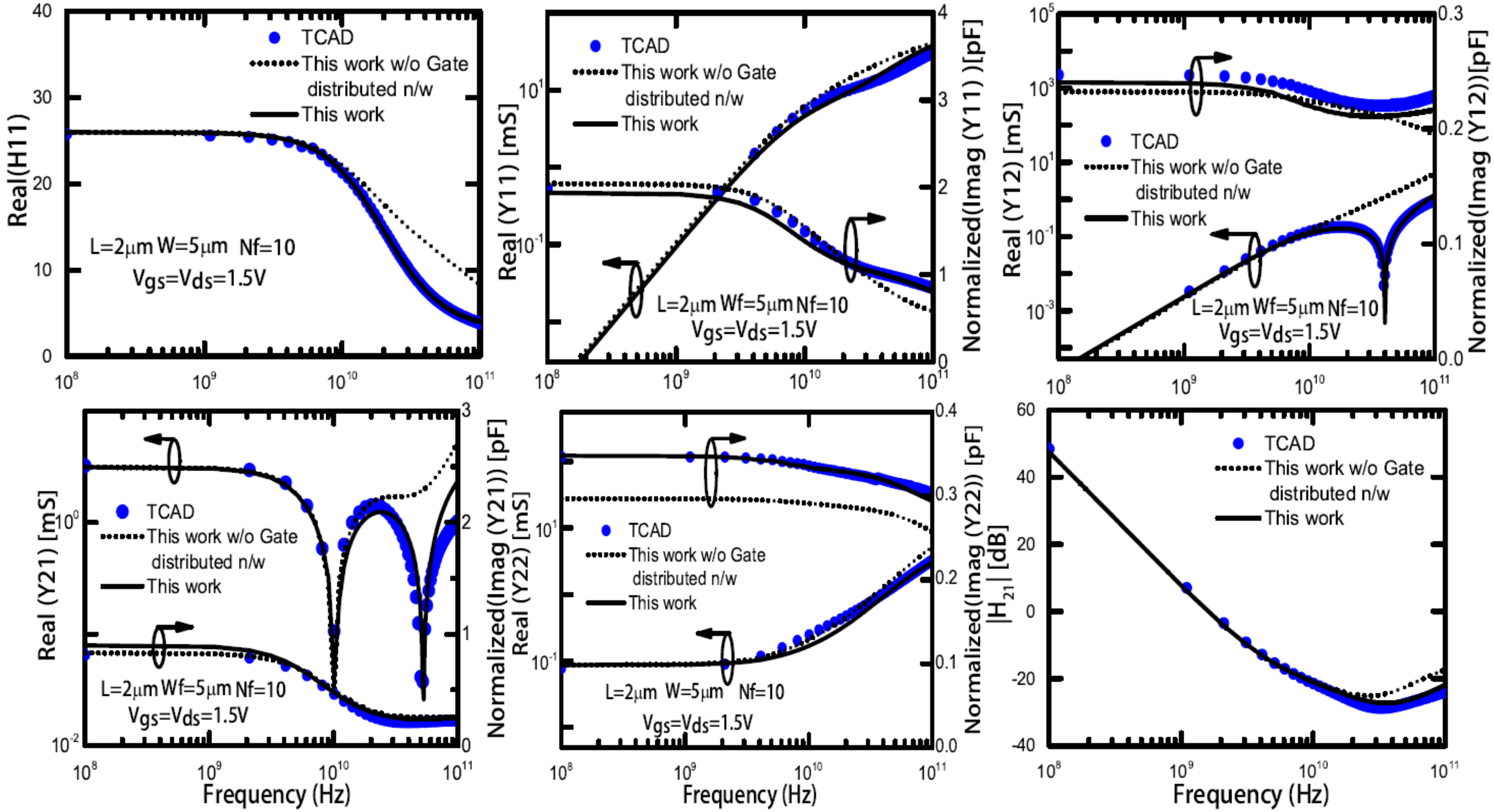


If we use $XRCRG1 = 40, XRCRG2 = \frac{120}{7}, XRCCG = \frac{49}{20}$ and $XGCCG = \frac{6}{5}$

- Gives the required NQS trend.
- Cannot give a good fitting at high frequency
- For $V_{DS} \neq 0$ channel is tapered from source to drain
- Also have some layout effects in the actual fabricated device
- Fitting parameters can provide more flexibility

NQS: Improved Model

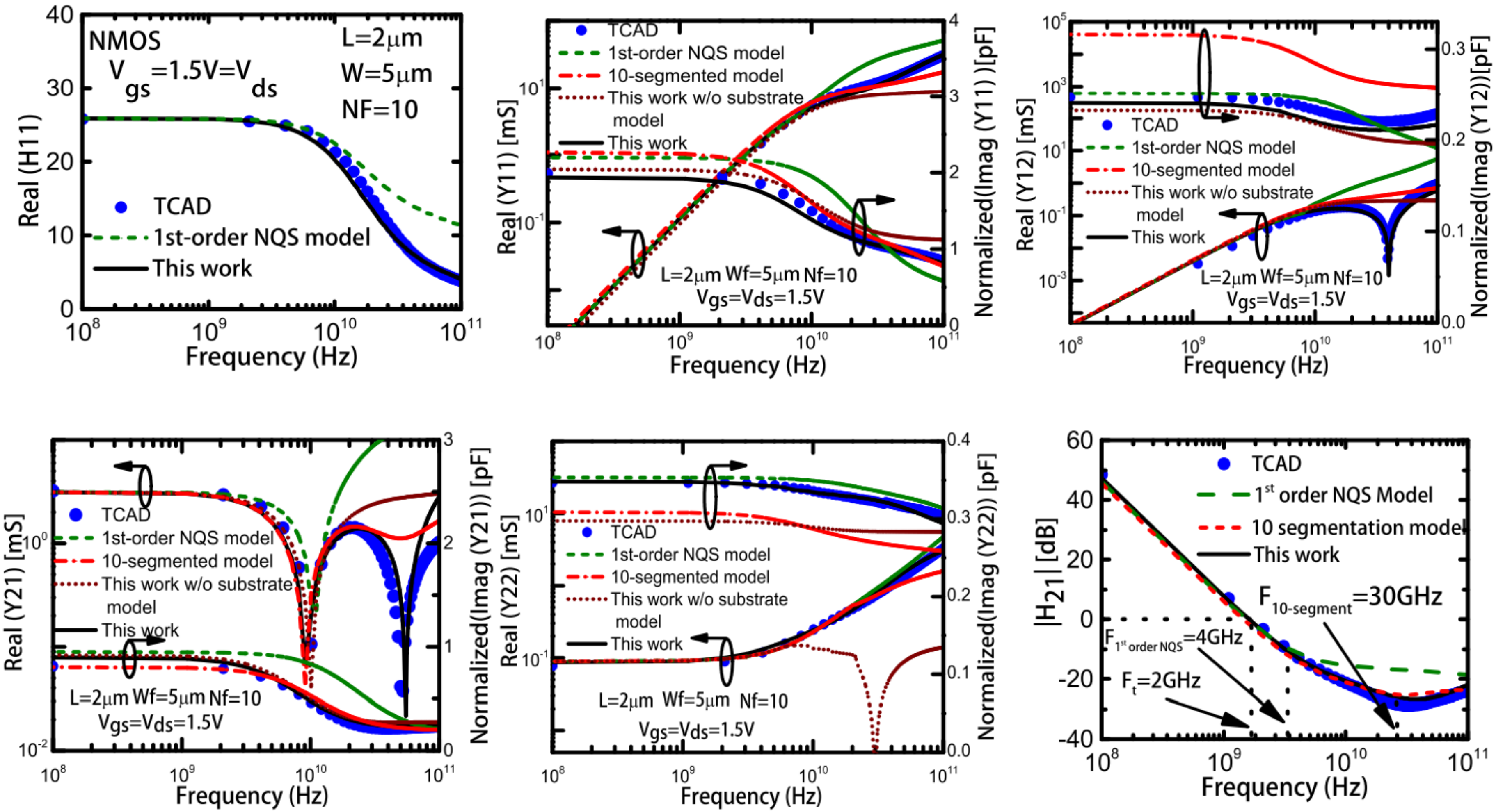
2D TCAD does not consider the impact of gate electrode distributed network on NQS



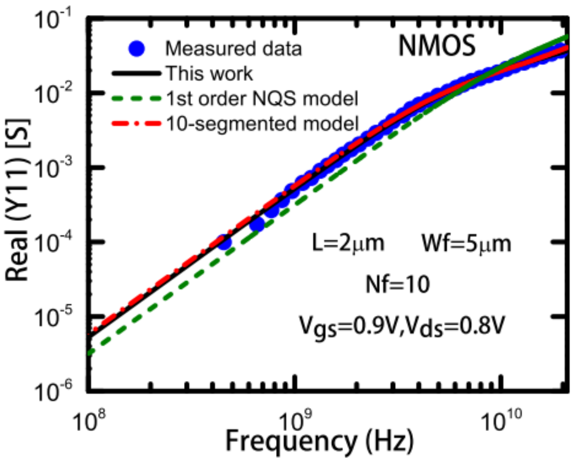
- Increases the fitting flexibility
- Developed model involves assumptions

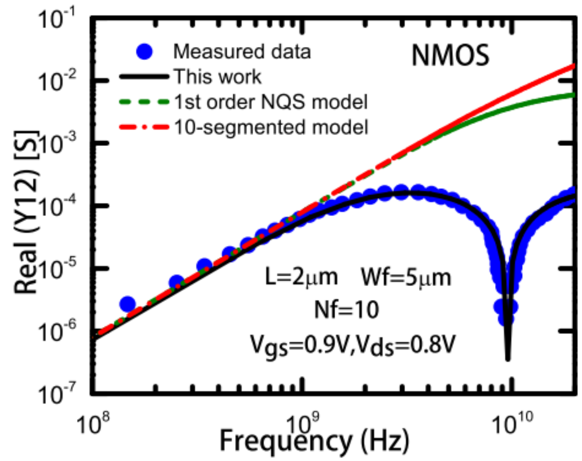
Improved Complete Model: TCAD Validation

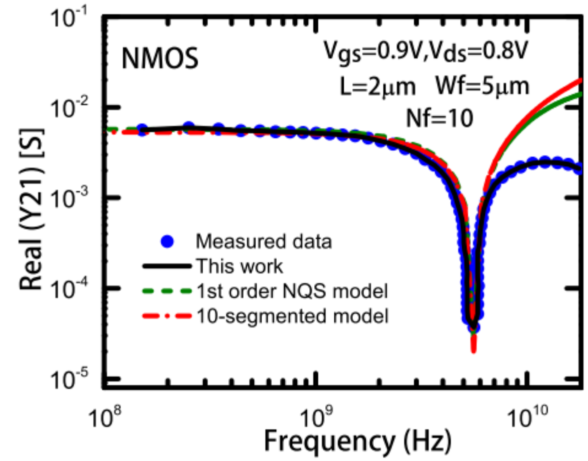
2D TCAD does not consider the impact of gate electrode distributed network on NQS

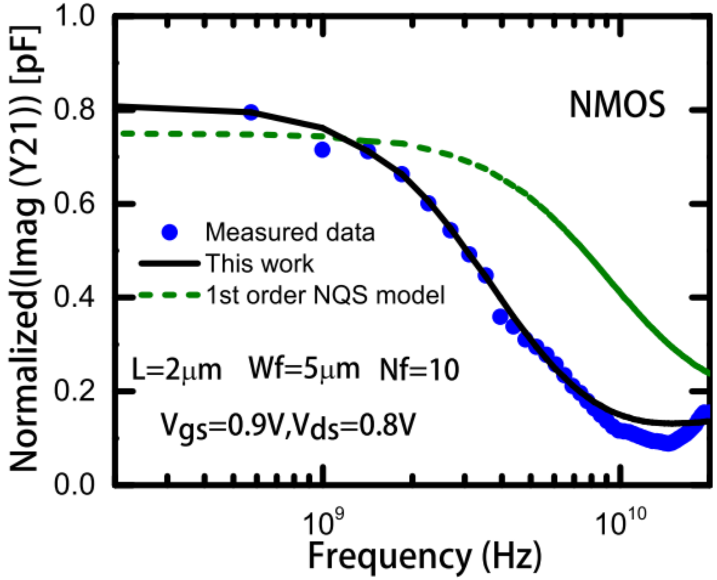


Improved Complete Model: Validation on Measured Data

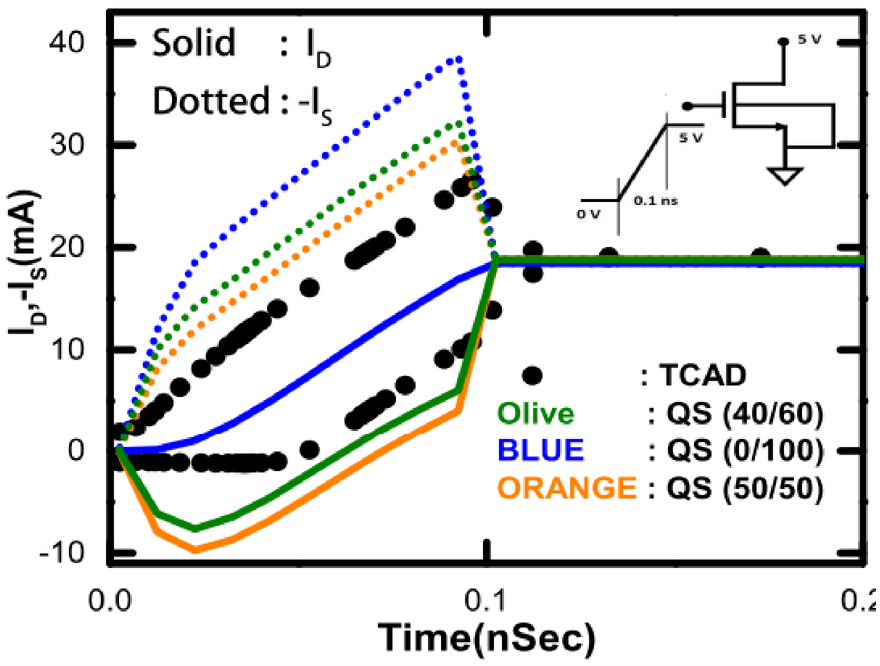


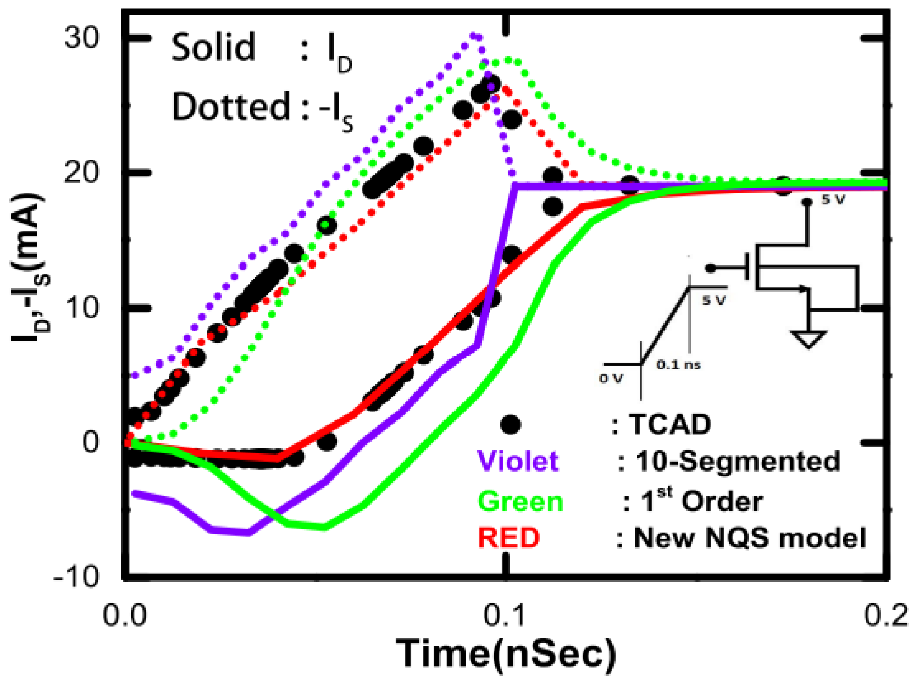






Large Signal Analysis





Summary of BSIM-BULK

- Charge based physical compact model
  - Physical effects & Parameter names matched to BSIM4 → No new training required for engineers
  - Smooth charge/current/capacitance & derivatives
- Model is symmetric and continuous around $V_{DS}=0$
  - Fulfills Gummel symmetry and AC symmetry
  - Shows accurate slope for harmonic balance simulation
- BSIM4's extraction methodology can be easily used for BSIM6 → fast deployment & lower cost
- Rapid development
  - From scratch to production level in two years!

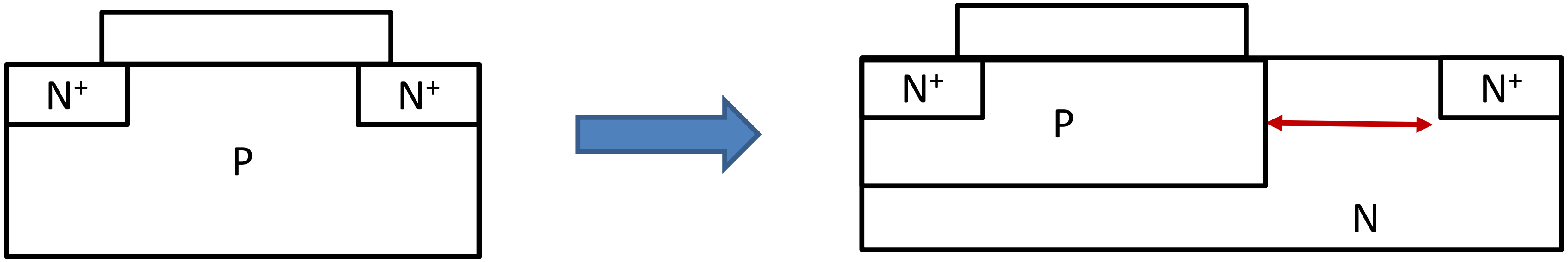
High Voltage MOSFET Modeling in BSIM-BULK

H. Agarwal, C. Gupta, R. Goel, P. Kushwaha, Y.-K. Lin, M.-Y. Kao, J.-P Duarte, H.-L. Chang, Y. S. Chauhan, S. Salahuddin, and C. Hu, "BSIM-HV: High Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect", IEEE Transactions on Electron Devices, Vol. 66, Issue 10, pp. 4258-4263, Oct. 2019.

High Voltage MOSFET Model

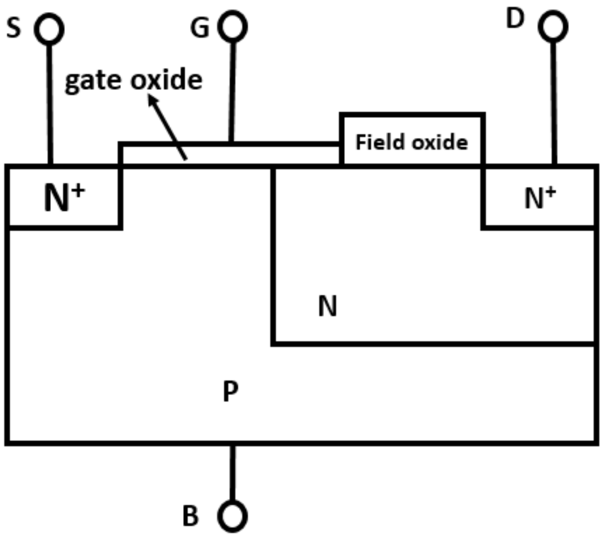
High Voltage Devices: Overview

- Wide application domain: Display, self-driving cars, etc.
- To withstand high voltage:
- Increase gate oxide thickness
- Add a drift region between drain/gate: prevents breakdown of gate oxide and breakdown of drain junction.



Physics of Drift Region

- Transport in the drift



$$I_{dr} = Q_{dr} * v_{dr}$$
$$I_{dr} = I_{ds}$$

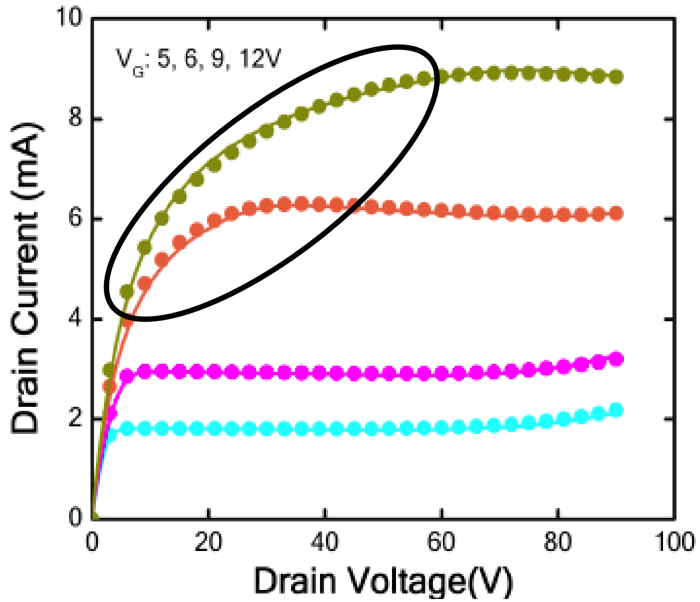
- To support higher current, carrier velocity in the drift region increases

$$V_g \uparrow \rightarrow I_{ds} \uparrow \rightarrow v_{dr} \uparrow$$

- As the carrier velocity reaches the saturation velocity limit, the resistance of the drift region increases

Physics of Drift Region

Ids-Vds of 90V transistor



$$I_{dr} = W * Q_{dr} * v$$

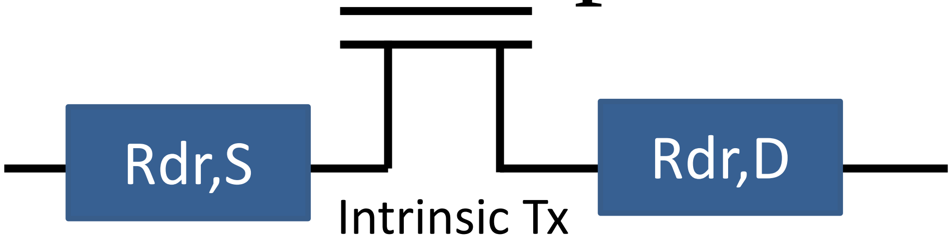
$$= W * Q_{dr} * \mu * \frac{E}{1 + E/ESAT}$$

On integration,

$$R_{dr} = \frac{V_{dr}}{I_{dr}} = \frac{R0}{1 - R0 * \frac{I_{drift}}{ESAT * L_{drift}}} = \frac{R0}{1 - \frac{I_{dr}}{I_{dr,max}}}$$

$$R0 = \frac{L_{dr}}{W * \mu * Q_{drift}} \qquad I_{drift,max} = Q_{dr} * W * VSAT$$

Compact Model Adoption



RDLCW: Resistance of the **D**rain side at **L**ow **C**urrent

MDRIFT: Smoothing parameter for velocity saturation

VDRIFT: Saturation Velocity in the drift

NDRIFTD: Charge Density in the drift

$$R_{dr,D} = \frac{RDLCW}{\left[1 - \delta_{HV}\left\{\frac{I_{ds}}{I_{dr,sat,D}}\right\}^{MDRIFT}\right]^{\frac{1}{MDRIFT}}}$$

$$I_{dr,sat,D} = q * NDRIFTD * W_{eff} * VDRIFT$$

δ_{HV} introduced for smoothness. Nominal value ~ 1

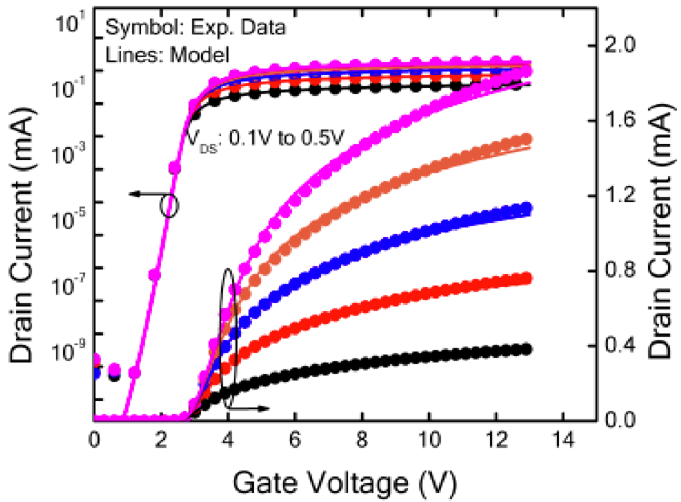
Source side parameters: RSLCW, NDRIFTS

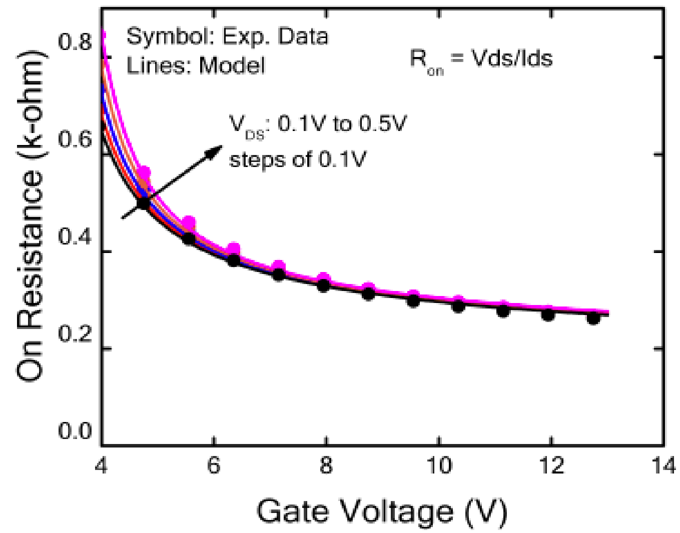
Implementation in BSIM-BULK

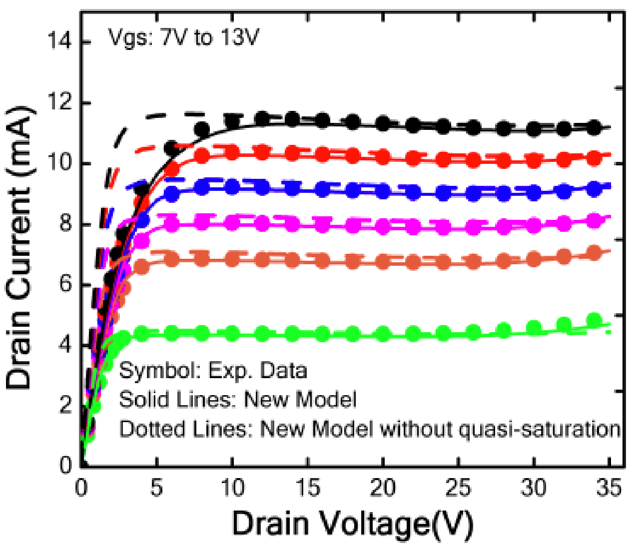
- Turn-key feature: Activates only when *switch HVMOD is set to 1*.
- Default value of HVMOD is 0 (HV feature turned-off)

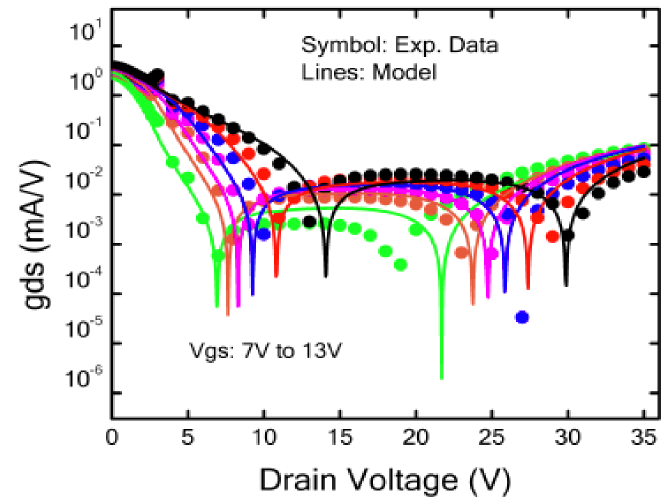
```
if (RDSMOD== 1 && HVMOD == 1) begin
    T4  = 1 + PDRWB * Vbsx;
    T0  = ids ;
    T11 = NF * Weff * `q  * VDRIFT_t ;
    if (RDLCW!=0) begin
        idrift sat d = T11 * NDRIFTD  ;


    rdrift d = rdstemphv * RDLCW * WeffWRFactor/T2D * T4;

     Rdrain  = Rdrain + rdrift_d;
     Rsource = Rsource + rdrift_s;
```

Experimental 35V LDMOS



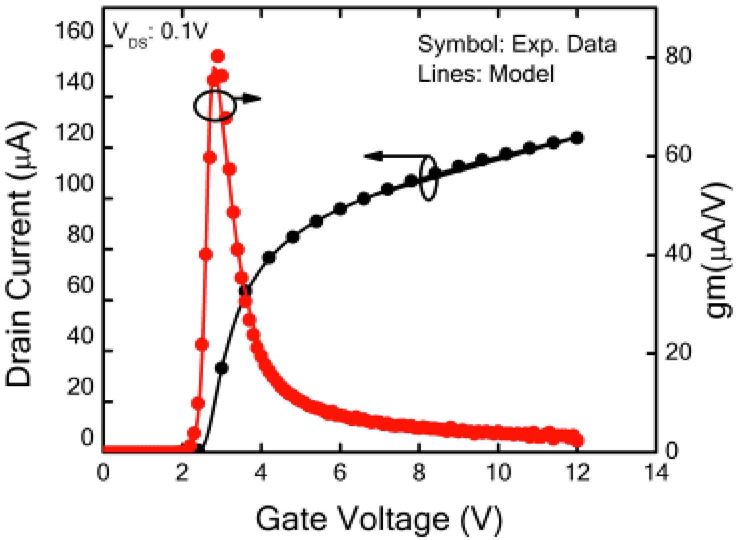


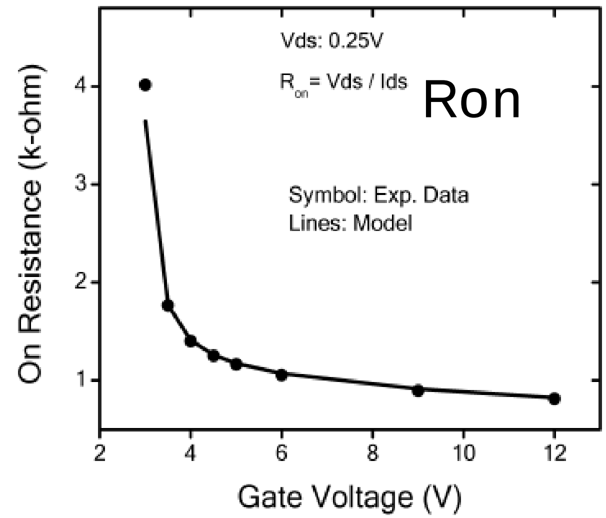


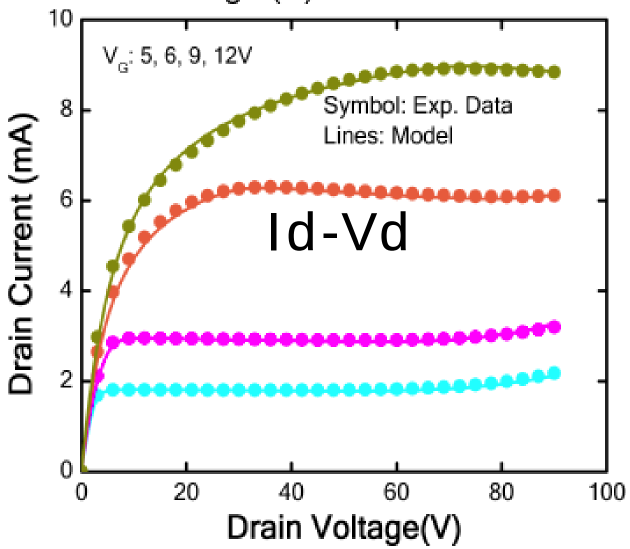


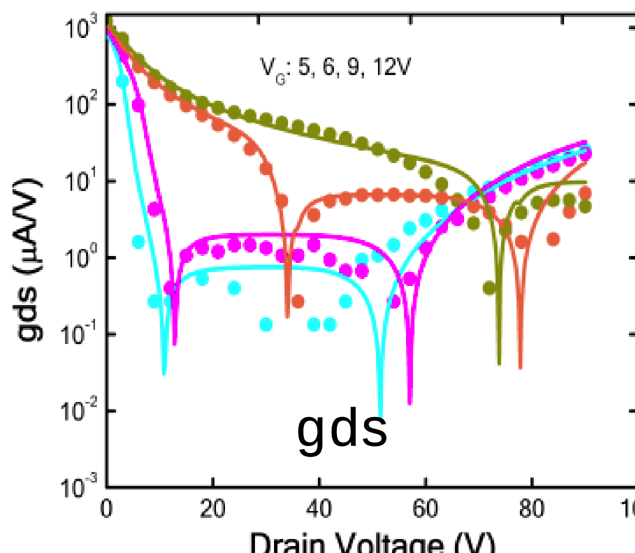
Experimental 90V LDMOS

Id-Vg gm-Vg







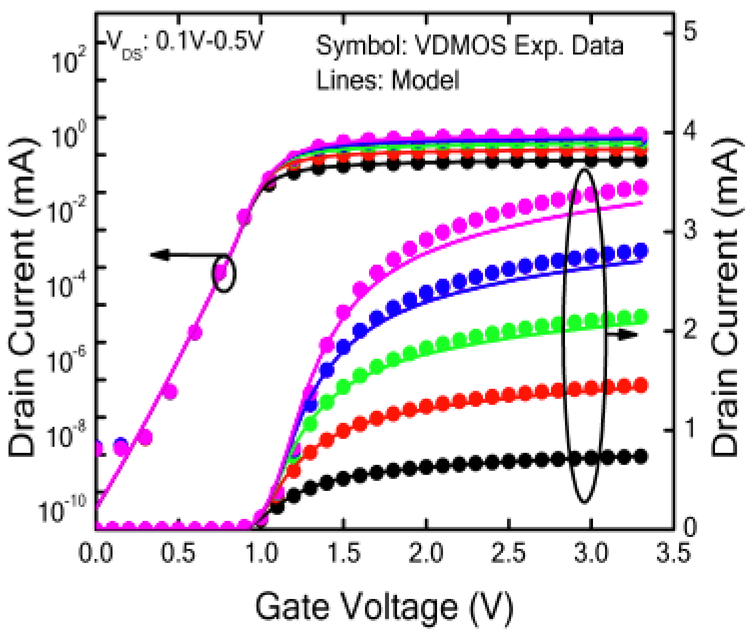


Experimental 40V VDMOS

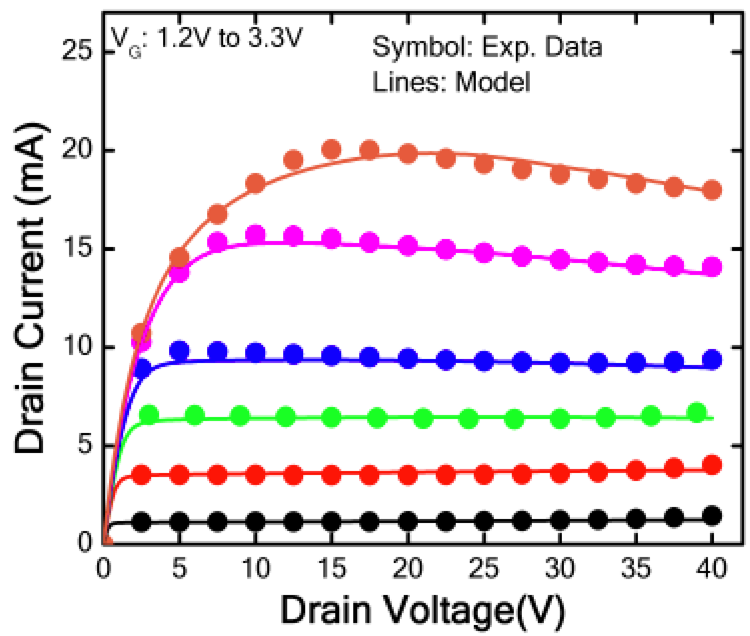
Lines: Model

Symbols: Exp. Data

Id-Vg

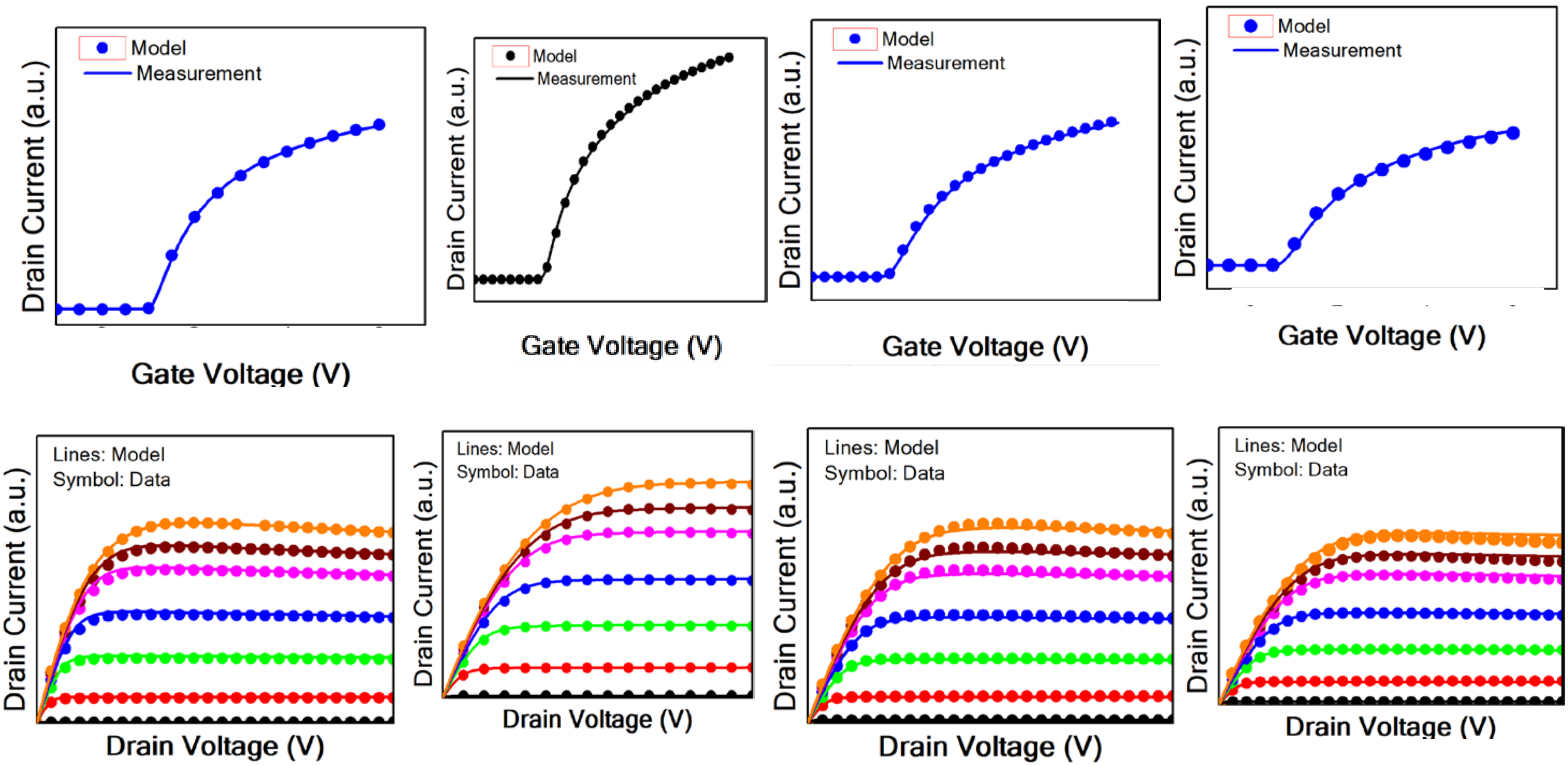


Id-Vd

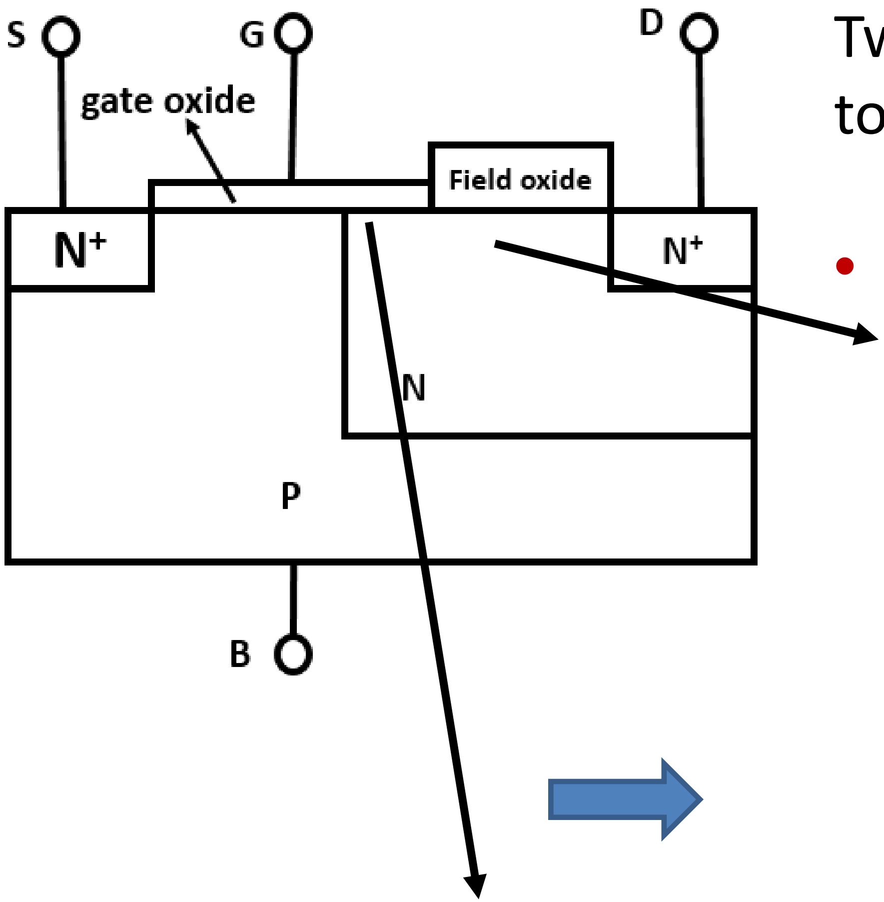


Temperature Dependence

T=-40C T=25C T=125C T=175C



Capacitances in HV Devices



Two important differences as compared to low voltage transistor

- **Presence of high series resistance**

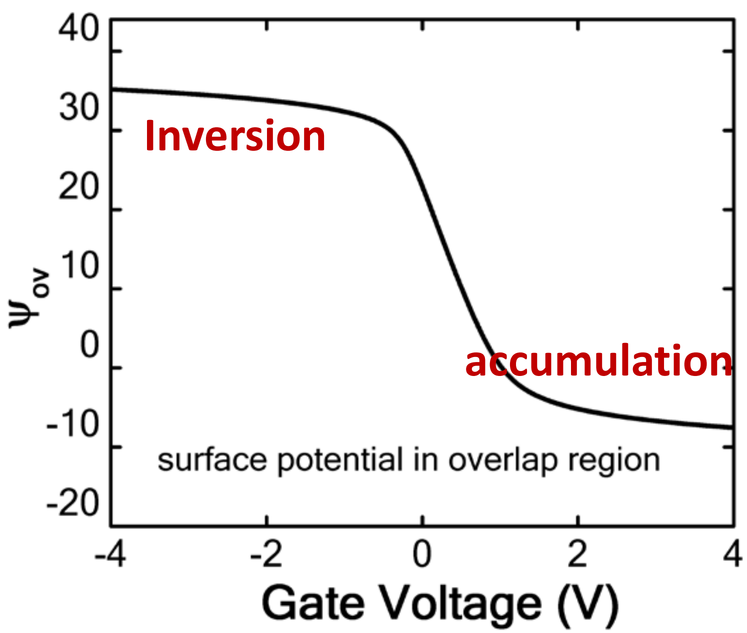
$$Q_g = f(V_g, V_{di}, V_s, V_b)$$

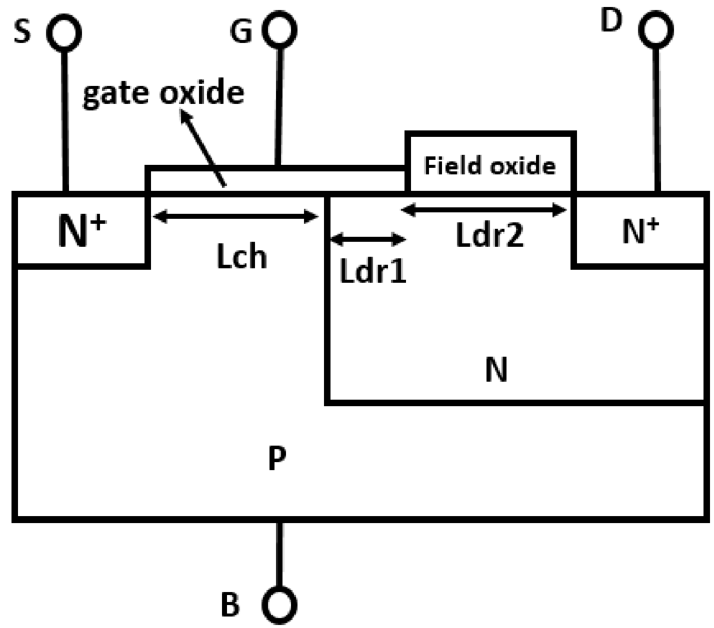
$$\frac{dQ_g}{dV_g} = \frac{\partial Q_g}{\partial V_g} + \frac{\partial Q_g}{\partial V_{di}} * \frac{dV_{di}}{dV_g}$$

$$C_{gg} = C_{gg,i} - C_{gd,i} * \frac{dV_{di}}{dV_g}$$

Presence of overlap region: Contributes bias dependent capacitance

Charge Model





$$V_{gdi} - V_{fb} = \psi_P + \gamma * \sqrt{e_P^{-\psi} + \psi_P - 1}$$

(Solved analytically)

$$Q_{I,dr} = W * L_{dr1} * 2n_q * C_{ox} * V_t * q_{dr}$$

$$Q_{B,dr} = W * L_{dr1} * 2n_q * C_{ox} * V_t * (V_{gdi} - V_{fb} - \psi_{s,ov} - 2n_q * q_{dr})$$

Model Implementation

- Activate the model: *Set HVCAP=1 along with HVMOD =1*
- Default value of HVCAP is 0

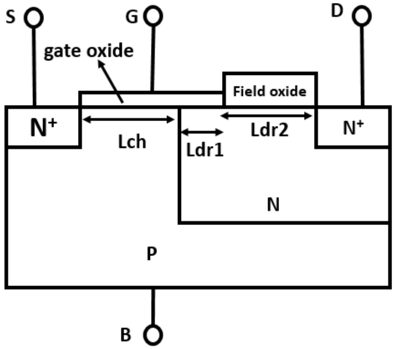
```
if (HVCAP == 1 && HVMOD == 1) begin

    // CV calculations

    vgfbdrift = -devsign * V(g,di) - VFBOV ;
    vgfbdrift = vgfbdrift/Vt;

    gamhv     = sqrt(2.0 * `q * epssi * NDR * inv_Vt) / Cox;
    phibHV    = lln(NDR / ni);

    `PO_psip(vgfbdrift,gamhv,0,phibHV,psip_k)
    `BSIM_q(psip_k, phibHV, devsign *V(di,b)/Vt, gamhv, q_k)

   QBOV = NF * Wact * LOVER * `EPS0 * EPSROX / BSIMBULKTOXP * Vt *
   QIOV = NF * Wact * LOVERACC * 2 * nq_hv * Vt * T0 * q_k ;

       Qovb = Qovb + QIOV;
       Qovd = Qovd + QBOV;
```

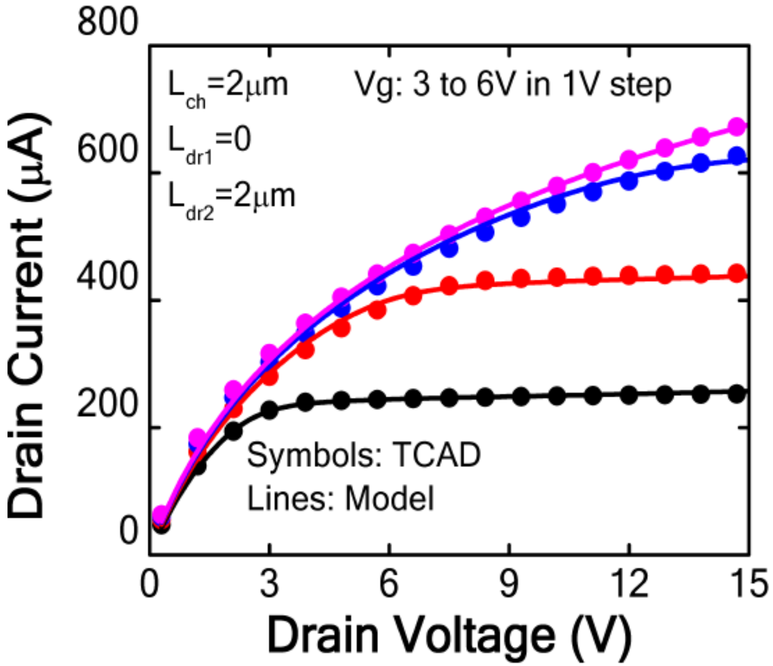
Model Implementation

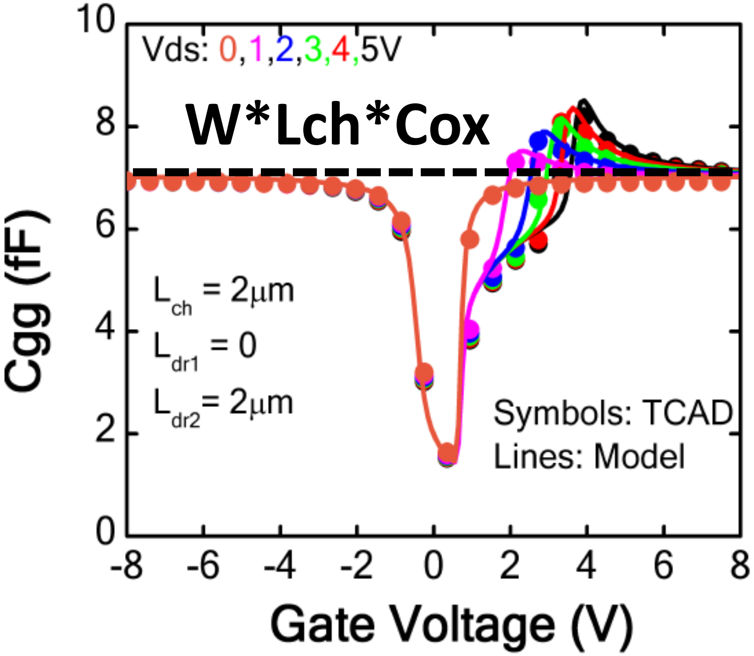
Parameters introduced for the charge model:

VFBOV: Flat-band voltage of the drift region
LOVER: Length of the drift region
LOVERACC: Effective length in accumulation
NDR: Doping of the drift region
SLHV: Parameter and Flag for smoothing the capacitance
SLHV1: Parameter for smoothing the capacitance

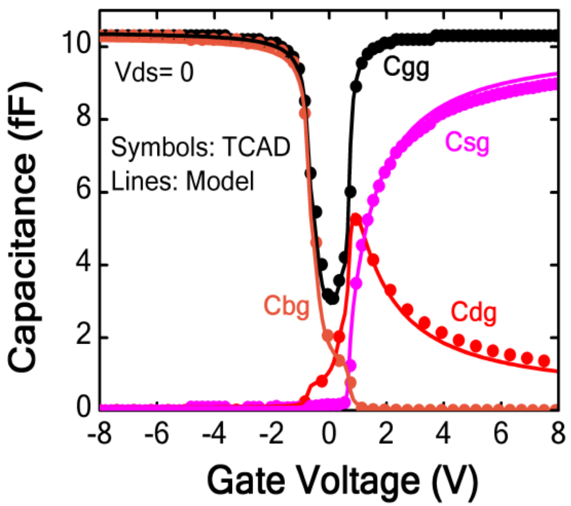
TCAD Validation

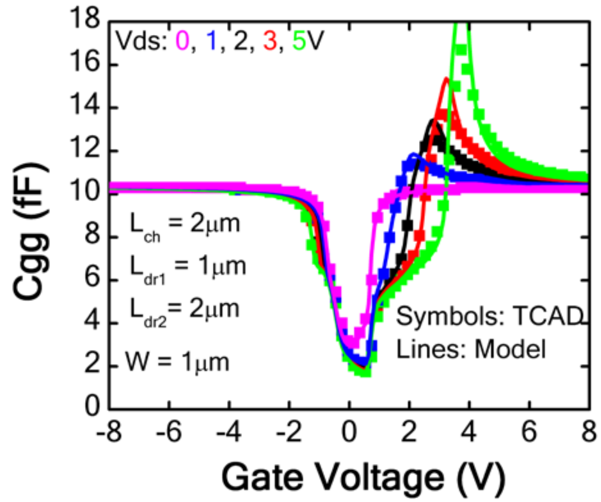


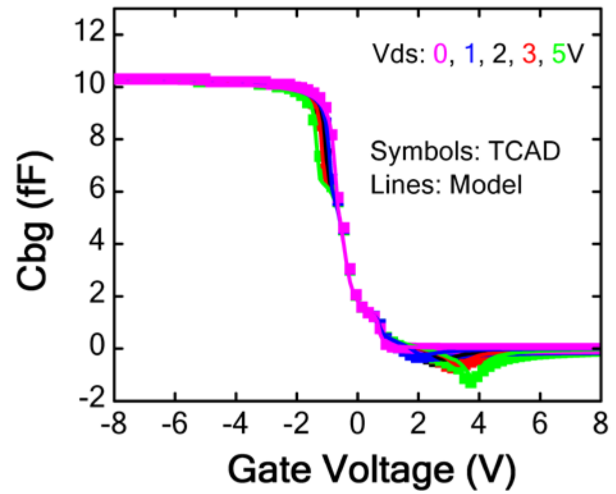




TCAD Validation



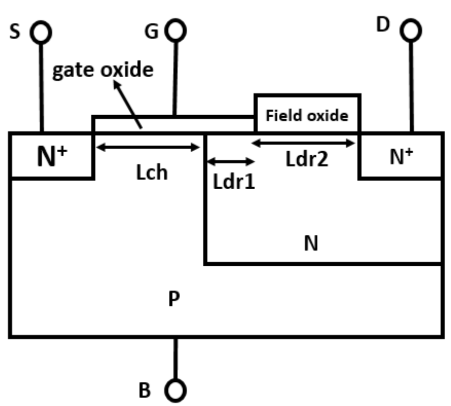


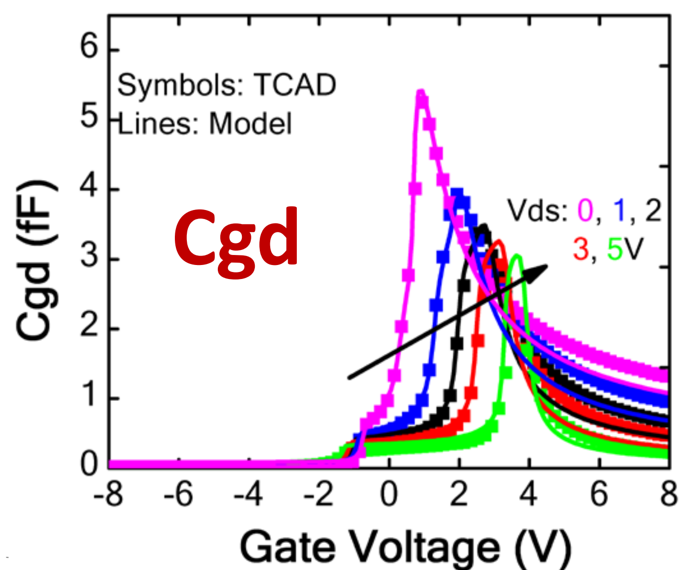


Ldr1 = 1um

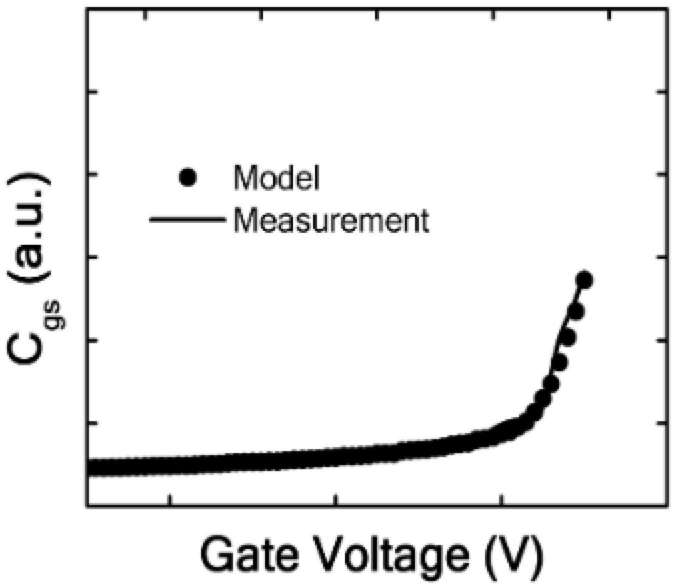
Ldr2 = 1um

Lch = 2um

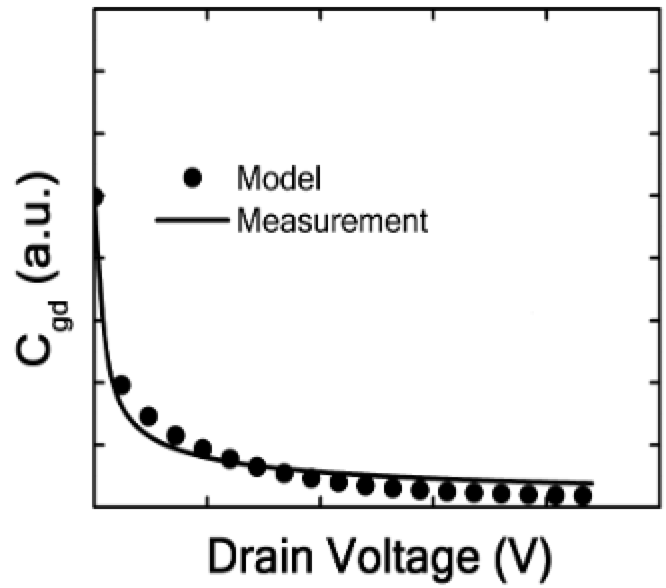




Validation with Experimental Data-1



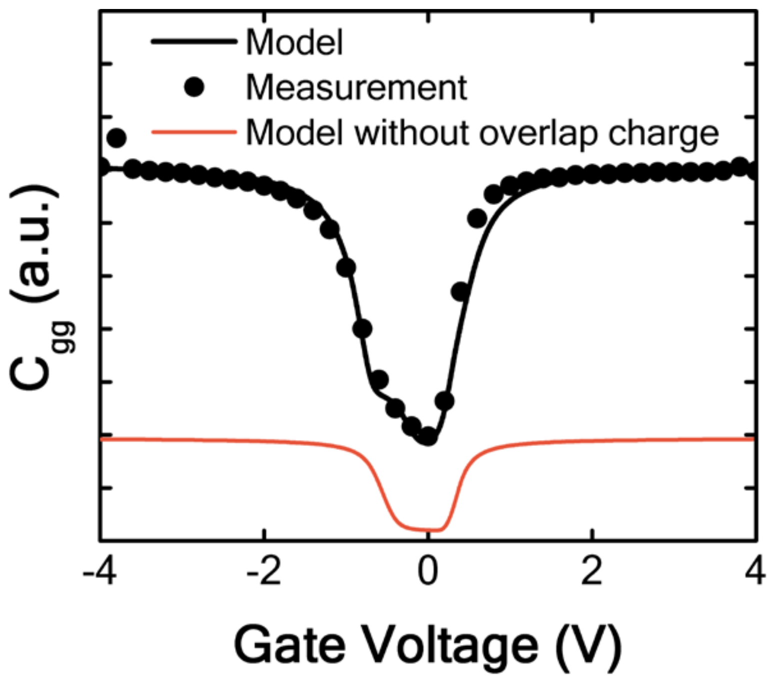
Cgs vs Vgs



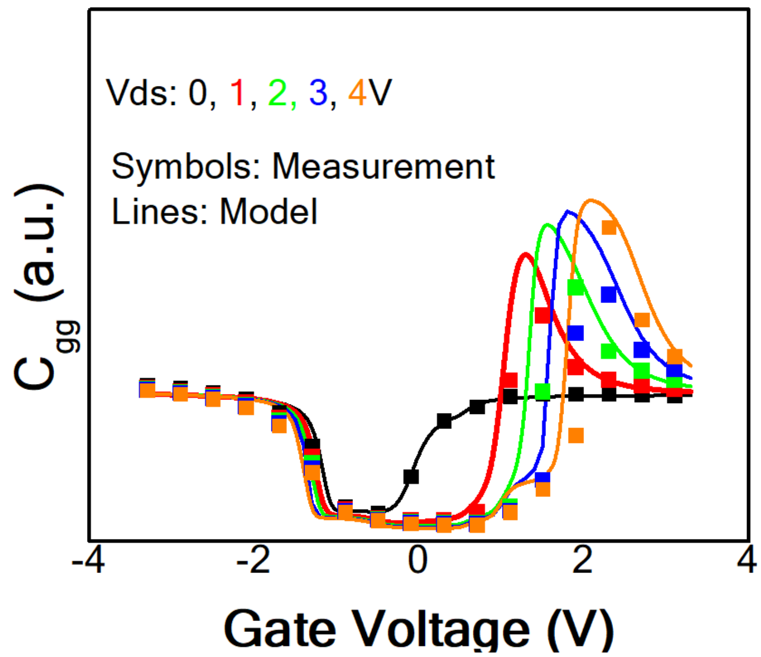
Cgd vs Vds

Validation with Experimental Data

Experimental data 2

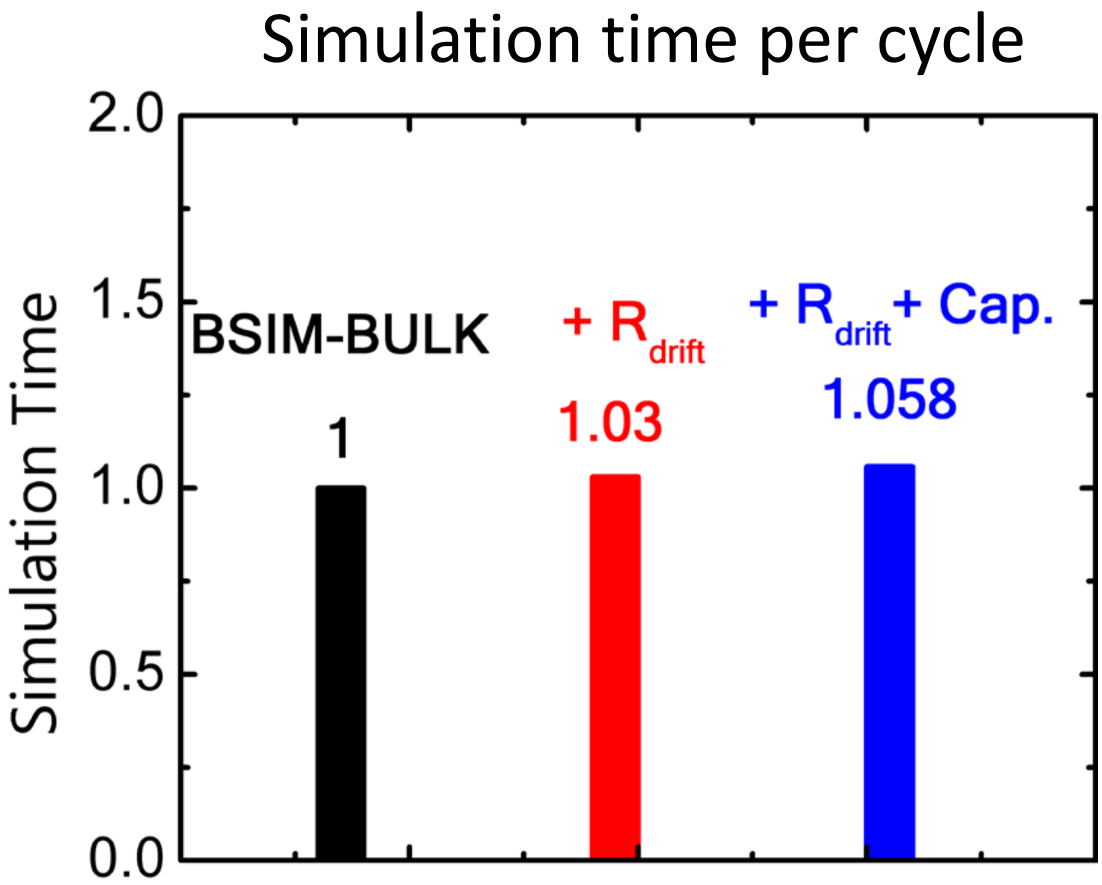


Experimental data 3



Speed Test

21 stage Ring Oscillator: 1000 cycles
100 points/cycle



Summary of High Voltage Model

- HV module is turned off-by default in BSIM-BULK model.
  - Default value of model selector HVMOD = 0
  - Activate the HV feature by setting HVMOD=1

- Model captures the physics of high-voltage devices
- Excellent convergence in large circuit simulations

Journal Publications

- C. Gupta, S. Dey, R. Goel, C. Hu, and Y. S. Chauhan, "Modeling of Current Mismatch and 1/f Noise for Halo Implanted Drain-Extended MOSFETs", IEEE Transactions on Electron Devices, Vol. 67, Issue 11, Nov. 2020.
- H. Agarwal, C. Gupta, R. Goel, P. Kushwaha, Y.-K. Lin, M.-Y. Kao, J.-P Duarte, H.-L. Chang, Y. S. Chauhan, S. Salahuddin, and C. Hu, "BSIM-HV: High Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect", IEEE Transactions on Electron Devices, Vol. 66, Issue 10, pp. 4258-4263, Oct. 2019.
- C. Gupta, H. Agarwal, R. Goel, C. Hu, and Y. S. Chauhan, "Improved Modeling of Bulk Charge Effect for BSIM-BULK Model", IEEE Transactions on Electron Devices, Vol. 66, Issue 6, pp. 2850-2853, June 2019.
- C. Gupta, N. Mohamed, H. Agarwal, R. Goel, C. Hu, and Y. S. Chauhan, "Accurate and Computationally Efficient Modeling of Nonquasi Static Effects in MOSFETs for Millimeter Wave Applications", IEEE Transactions on Electron Devices, Vol. 66, Issue 1, pp. 44-51, Jan. 2019.
- C. Gupta, R. Goel and Y. S. Chauhan, "Analysis and Modeling of Current Mismatch in Laterally Non-Uniform MOSFETs", IEEE Transactions on Electron Devices, Vol. 65, Issue 10, pp. 4254-4262, Oct. 2018.
- C. Gupta, S. Dey, H. Agarwal, R. Goel, C. Hu, and Y. S. Chauhan, "Analysis and Modeling of Temperature and Bias Dependence of Current Mismatch in Halo Implanted MOSFETs", IEEE Transactions on Electron Devices, Vol. 65, Issue 9, pp. 3608-3616, Sept. 2018.
- C. Gupta, H. Agarwal, Y. K. Lin, A. Ito, C. Hu and Y. S. Chauhan, "Analysis and Modeling of Zero-VTH Native Devices with Industry Standard BSIM6 Model", Japanese Journal of Applied Physics (Special Issue), Vol. 56, Issue 4S, pp. 04CD09(1-6), Apr. 2017.
- H. Agarwal, C. Gupta, S. Dey, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Anomalous Transconductance in Long Channel Halo Implanted MOSFETs: Analysis and Modeling", IEEE Transactions on Electron Devices, Vol. 64, Issue 2, pp. 376-383, Feb. 2017.
- Y.-K. Lin, S. Khandelwal, A. Medury, H. Agarwal, H.-L. Chang, Y. S. Chauhan, and C. Hu, "Modeling of Sub-surface Leakage Current in Low Vth Short Channel MOSFET at Accumulation Bias", IEEE Transactions on Electron Devices, Vol. 63, Issue 5, pp. 1840-1845, May 2016.
- H. Agarwal, P. Kushwaha, C. Gupta, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Analysis and Modeling of Flicker Noise in Lateral Asymmetric Channel MOSFETs", Solid State Electronics, Vol. 115, Part A, pp. 33-38, Jan. 2016.
- H. Agarwal, S. Khandelwal, S. Dey, C. Hu, and Y. S. Chauhan, "Analytical Modeling of Flicker Noise in Halo Implanted MOSFETs", IEEE Journal of Electron Devices Society, Vol. 3, Issue 4, pp. 355-360, April 2015.
- H. Agarwal, C. Gupta, P. Kushwaha, C. Yadav, J. P. Duarte, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Analytical Modeling and Experimental Validation of Threshold Voltage in BSIM6 MOSFET Model", IEEE Journal of the Electron Devices Society, Vol. 3, Issue 3, pp. 240,243, March 2015.
- Y. S. Chauhan, S. Venugopalan, M.-A. Chalkiadaki, M. A. Karim, H. Agarwal, S. Khandelwal, N. Paydavosi, J. P. Duarte, C. C. Enz, A. M. Niknejad, and C. Hu, "BSIM6: Analog and RF Compact Model for Bulk MOSFET", IEEE Transactions on Electron Devices, Vol. 61, Issue 2, pp. 234-244, Feb. 2014. (Invited)

Conference Publications-1

- A. Rathi, M. Kumar, J. K. Verma, H. S. Jatana, Y. S. Chauhan, and Abhisek Dixit, "Modeling of 0.18µm RF Bulk and SOI Planar MOSFETs using Industry Standard BSIM Models", IEEE International Conference on Emerging Electronics (ICEE), Delhi, Nov. 2020.
- J. K. Verma and Y. S. Chauhan, "Investigation of Standard and Enclosed Gate n-MOSFET Degradation due to Total Ionizing Dose Using BSIM-BULK", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Penang, Malaysia, Mar. 2020.
- R. Goel, C. Gupta, and Y. S. Chauhan, "Analysis and Compact Modeling of Thermal Noise in Halo Implanted MOSFETs", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Penang, Malaysia, Mar. 2020.
- C. Gupta, R. Goel, H. Agarwal, C. Hu, and Y. S. Chauhan, "BSIM-BULK: Accurate Compact Model for Analog and RF Circuit Design", IEEE Custom Integrated Circuits Conference (CICC), Austin, USA, April 2019. (Invited).
- J. K. Verma, S. Ghosh, A. Yadav and Y. S. Chauhan, "Simulation, Characterization and Parameter Extraction of Radiation Hardened MOSFET", IEEE International Conference on Modeling of Systems Circuits and Devices, Hyderabad, India, Feb. 2019.
- R. Goel, C. Gupta, and Y. S. Chauhan, "An Empirical Model to Enhance the Flexibility of gm/Id Tuning in BSIM-BULK Model", IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur, India, Nov. 2018.
- C. Gupta, H. Agarwal, C. Hu, and Y. S. Chauhan, "Analysis and Modeling of Capacitances in Halo-Implanted MOSFETs", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, Feb.-Mar. 2017.
- A. Dasgupta, C. Gupta, A. Dutta, Y.-K. Lin, S. Srihari, T. Ethirajan, C. Hu, and Y. S. Chauhan, "Modeling of Body-bias Dependence of Overlap Capacitances in Bulk MOSFETs", IEEE International Conference on VLSI Design, Hyderabad, India, Jan. 2017.
- N. Mohamed, H. Agarwal, C. Gupta, and Y. S. Chauhan, "Compact Modeling of NQS Effect in Bulk MOSFETs for RF Circuit Design in Sub-THz Regime", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
- H. Agarwal, C. Gupta, S. Khandelwal, C. Hu, S. Dey, K. Chan and Y. S. Chauhan, "Analysis and Modeling of Low Frequency Noise in Presence of Doping Non-Uniformity in MOSFETs", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
- C. Gupta, H. Agarwal, Y. K. Lin, S. Khandelwal, Akira Ito, C. Hu, and Y. S. Chauhan, "Analysis and Modeling of Zero-VTH Devices with Industry Standard BSIM6 Model", International Conference on Solid State Devices and Materials (SSDM2016), Tsukuba, Japan, September 2016.
- C. Gupta, H. Agarwal, R. Gillon, S. Khandelwal, Y.-K. Lin, C. Hu and Y. S. Chauhan, "Modeling of High Voltage LDMOSFET using Industry Standard BSIM6 MOS Model", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
- C. Gupta, H. Agarwal, Akira Ito, S. Ghosh, P. Khushwaha, C. Hu, and Y. S. Chauhan, "Modeling of Zero-Vth MOSFET with Industry Standard BSIM6 Model", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.

Conference Publications-2

- N. Mohamed, H. Agarwal, C. Gupta, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Scaling Capabilities of Industry-Standard BSIM6 MOSFET Model", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- H. Agarwal, S. Khandelwal, C. Hu, and Y. S. Chauhan, "Analysis and Modeling of Assymetric Channel MOSFET", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
- A. Dutta, S. Sirohi, T. Ethirajan, H. Agarwal, Y. S. Chauhan, and R. Q Williams, "BSIM6 - Benchmarking the Next Generation MOSFET Model for RF Applications", IEEE International Conference on VLSI Design, Mumbai, India, Jan. 2014.
- J. R. Sahoo, H. Agarwal, C. Yadav, P. Kushwah, S. Khandewal, R. Gillon, and Y. S. Chauhan, "High Voltage LDMOSFET Modeling using BSIM6 as Intrinsic-MOS Model", IEEE PrimeAsia, Visakhapatnam, Dec. 2013.
- H. Agarwal, S. Venugopalan, M. Chalkiadaki, N. Paydavosi, J. P. Duarte, S. Agnihotri, C. Yadav, P. Kushwaha, Y. S. Chauhan, C. C. Enz, A. Niknejad and C. Hu, "Recent Enhancements in BSIM6 Bulk MOSFET Model", IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Glasgow, Scotland, Sept. 2013.
- Y. S. Chauhan, S. Venugopalan, N. Paydavosi, P. Kushwaha, S. Jandhyala, J. P. Duarte, S. Agnihotri, C. Yadav, H. Agarwal, A. Niknejad, and C. Hu, "BSIM Compact MOSFET Models for SPICE Simulation", IEEE International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Gdynia, Poland, June 2013. (Invited)
- M.-A. Chalkiadaki, A. Mangla, C. C. Enz, Y. S. Chauhan, M. A. Karim, S. Venugopalan, A. Niknejad, and C. Hu, "Evaluation of the BSIM6 Compact MOSFET Model's Scalability in 40nm CMOS Technology", IEEE European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, Sept. 2012.
- Y. S. Chauhan, S. Venugopalan, M. A. Karim, S. Khandelwal, N. Paydavosi, P. Thakur, A. M. Niknejad, and C. C. Hu, "BSIM - Industry Standard Compact MOSFET Models", IEEE European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, Sept. 2012. Slides (Invited)
- Y. S. Chauhan, M. A. Karim, S. Venugopalan, S. Khandelwal, P. Thakur, N. Paydavosi, A. B. Sachid, A. Niknejad, and C. Hu, "BSIM6: Symmetric Bulk MOSFET Model", Workshop on Compact Modeling (WCM), Santa Clara, USA, June 2012. (Invited)
- S. Khandelwal, Y. S. Chauhan, M. A. Karim, S. Venugopalan, A. Sachid, A. Niknejad, and C. Hu, "Analysis and Modeling of Vertical Non-uniform Doping in Bulk MOSFETs for Circuit Simulations", IEEE International Caribbean Conference on Devices, Circuits and Systems (ICCDCS), Playa del Carmen, Mexico, March 2012.
- M. A. Karim, S. Venugopalan, Y. S. Chauhan, D. Lu, A. Niknejad, and C. Hu, "Drain Induced Barrier Lowering (DIBL) Effect on the Intrinsic Capacitances of Nano-Scale MOSFETs", Workshop on Compact Modeling (WCM), Boston, USA, June 2011.

Thank You