RF Wireless, 5G and GaN HEMT: Characterization and Modeling using ASM-HEMT

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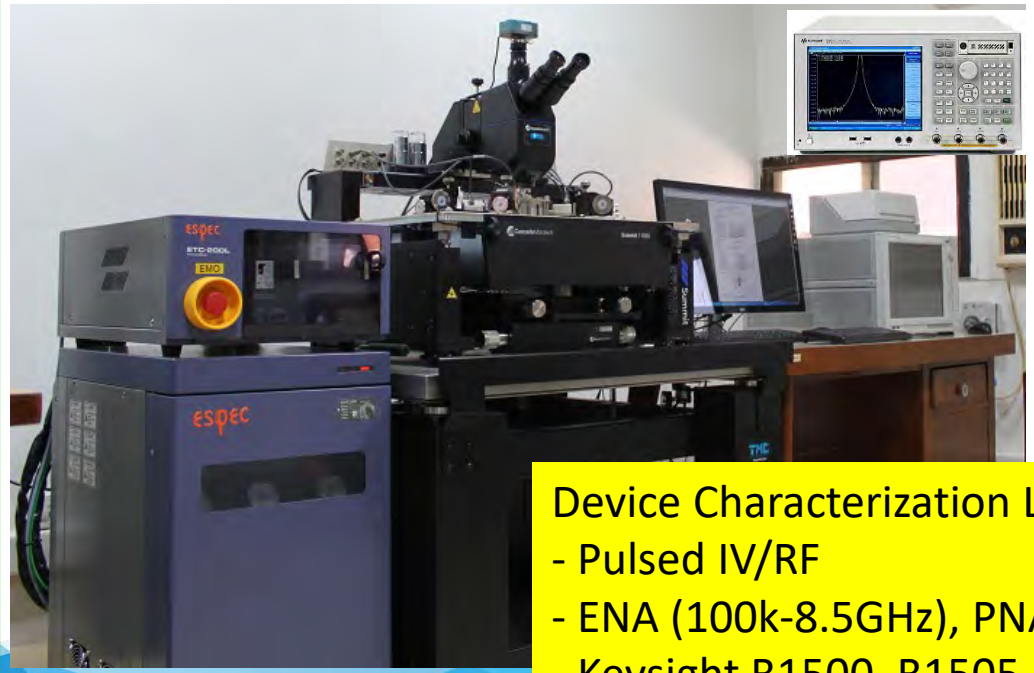
My Group and Nanolab

Current members – 38

- Postdoc – 5
- Ph.D. – 27
- PhD graduated – 10 + 2

	2020	2019	2018	2017	2016
Books		1			
Journal	16	14	20	19	18
Conference	11	15	19	11	30



Device Characterization Lab
- Pulsed IV/RF
- ENA (100k-8.5GHz), PNA-X 43.5GHz
- Keysight B1500, B1505
- Load Pull, NFA

Joint Development & Collaboration

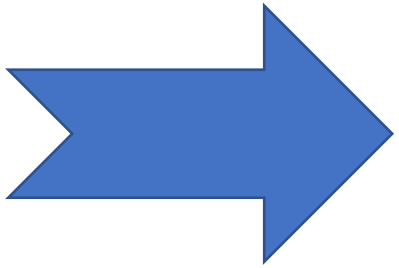
Alumni (PhD) of Nanolab

S. No.	Year	Name	Current Status
12.	2021*	Dinesh R.	Postdoc at UC Berkeley
11	2021*	Chetan Dabhi	Postdoc at UC Berkeley
10.	2020	Girish Pahwa	Postdoc at UC Berkeley
9.	2020	Shantanu Agnihotri	Asst. Prof. at Bennett University
8.	2020	Chetan Gupta	Micron Hyderabad
7.	2018	Priyank Rastogi	Intel Bangalore
6.	2018	Prateek Jain	Postdoc at IIT Bombay
5.	2018	Avirup Dasgupta	Asst. Prof. at IIT Roorkee
4.	2017	Sheikh Aamir Ahsan	Asst. Prof. at NIT Srinagar
3.	2017	Chandan Yadav	Asst. Prof. at NIT Calicut
2.	2017	Harshit Agarwal	Asst. Prof. at IIT Jodhpur
1.	2017	Pragya Kushwaha	SAC, ISRO

Nanolab@IITK: From Theory to Applications

Theory

Materials
Atomistic Sim.
Semiconductors
Transport



Applications

Fabrication
Characterization
SPICE Models
RF Circuit Design

Nanolab: Characterization and Modeling Capabilities

- *About Nanolab*
- *Hardware Capabilities*
- *EDA Capabilities*

About Nanolab: Areas of Research

Atomistic Simulation

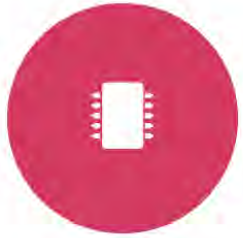
Strong compute and storage infrastructure for atomistic simulations - paving the way for first principle studies of materials. Research topics include materials like VO2, V2O5, black phosphoros, TMDs like MoS2, phosphorene, borophene among many others.

SPICE/Compact Modeling

Strong collaboration with the industry in terms of model development. Working closely with UC Berkeley to maintain and develop the BSIM standard models. Out ASM-HEMT model for GaN-HEMTs was recently recognized as an industry standard by the Compact Model Coalition (CMC)

DC and RF Device Characterization

State-of-the-art equipment for DC and RF characterization of packaged and on-wafer devices. High power measurement capabilities coupled with pulsed IV/RF and load pull systems allow for characterizations of higher level circuits like power amplifiers.



RF Circuit Design

Hardware and software capabilities to design and implement prototypes for RF circuits. Power Amplifier and Low Noise Amplifier design using advanced device technologies.

Hardware Capabilities I

Keysight Semiconductor Device Analyzer (B1500A) Measurement capabilities:

- IV, CV, pulse/ dynamic IV range of 0.1 fA - 1 A / 0.5 µV - 200 V
- Evaluation of devices, materials, semiconductors, active/ passive components
- AC capacitance measurement in multi frequency from 1 kHz to 5 MHz
- Pulsed IV measurement min 10 ns gate pulse width with 2 ns rise and fall times with 1 µs current measurement resolution

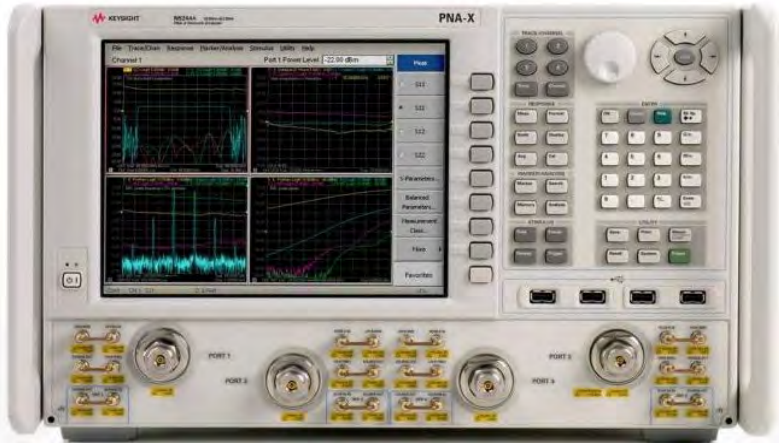
Maury Microwaves/ AMCAD AM3221

- Bipolar ±25V/ 1A (gate) and high-voltage 250V/ 30A (drain) models
- Pulse widths down to 200ns
- Synchronized pulsed S-parameter measurements
- Connect systems in series for synchronizing 3+pulsed channels
- Long pulses into the tens and hundreds of seconds for trapping and thermal characterization

Hardware Capabilities II

Keysight ENA (E5071C) 100KHz to 8.5 GHz

- 9 kHz to 4.5/ 6.5/ 8.5/ 14/ 20 GHz
- 2- or 4-port, 50-ohm, S-parameter test set
- Improve accuracy, yield and margins with wide dynamic range 130 dB, fast measurement speed 8ms and excellent temperature stability 0.005 dB/ °C



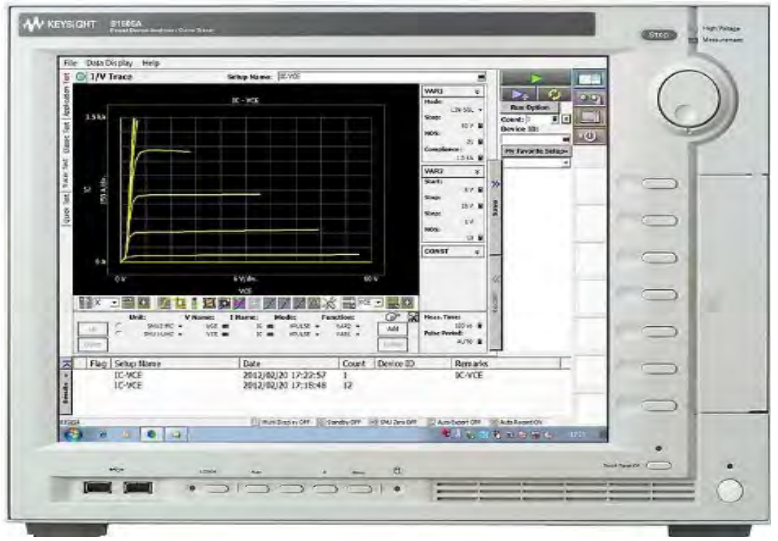
Keysight PNA-X (N5244A) 10 MHz to 43.5 GHz

- High Frequency Device Characterization (Microwave Network Analyzer)
- 100Khz to 8.5 GHz and 10 MHz to 43.5 GHz
- 2-port and 4-ports with two built-in sources
- High output power (+16 dBm)
- Best dynamic accuracy: 0.1 dB compression with +15 dBm input power at the receiver
- Low noise floor of -111 dBm at 10 Hz IF bandwidth

Hardware Capabilities III

Keysight Power Device Characterization System: B1505

- Power device characterization up to 1500 A & 10 kV
- Medium current measurement with high voltage bias (e.g. 500 mA at 1200 V)
- μΩ on-resistance measurement capability
- Accurate, sub-picoamp level, current measurement at high voltage bias
- Fully automated Capacitance measurement at up to 3000 V of DC bias
- High power pulsed measurements down to 10 μs
- High voltage/ high current fast switch option to characterize GaN current collapse effect
- Fully automated thermal testing from -50 °C to +250 °C



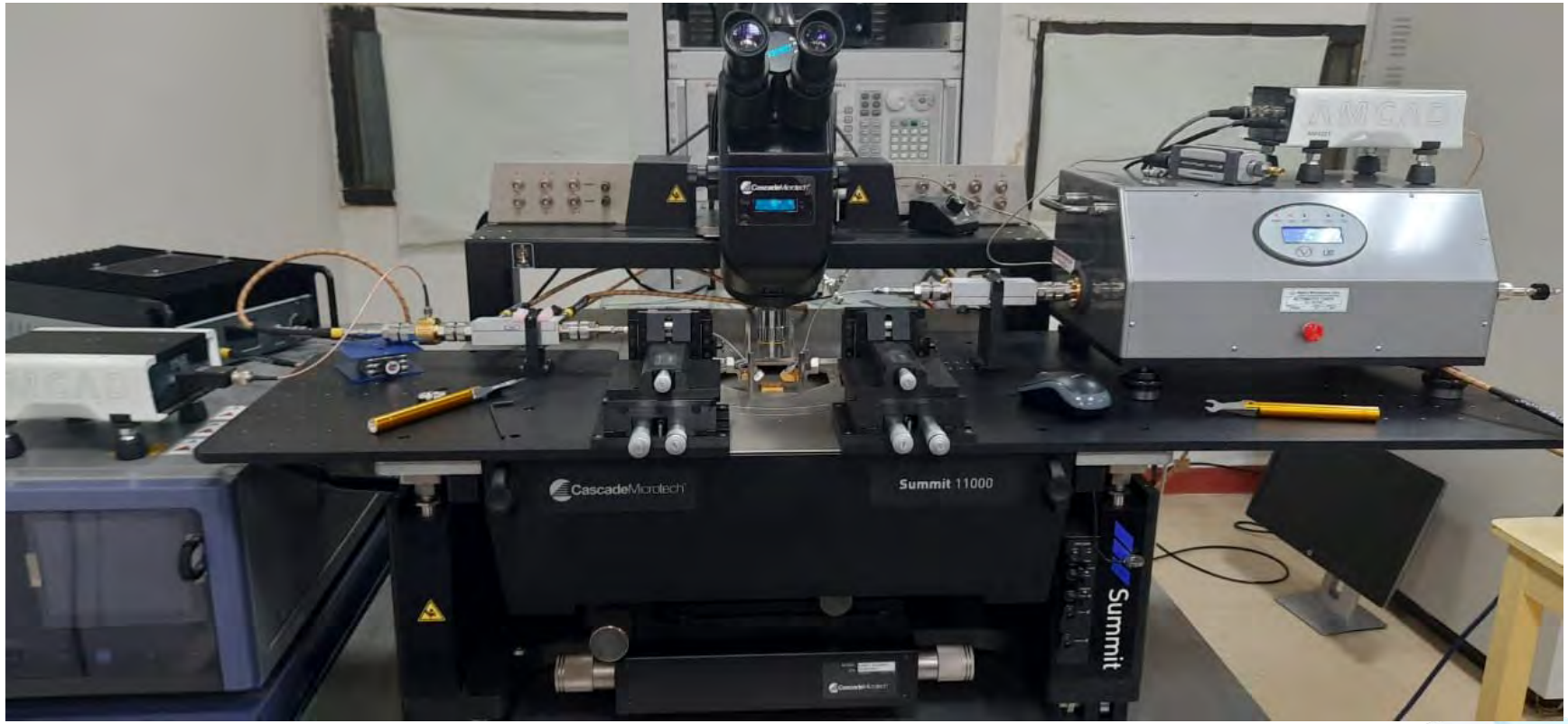
Keysight N8975B Noise Figure Analyzer

- Frequency range 10 MHz to 26.5 GHz in a one-box solution
- Includes Spectrum Analyzer and IQ Analyzer (Basic) modes
- SNS series noise source N4002A
- U7227C 100 MHz to 26.5 GHz External USB Preamplifier included

Load Pull Characterization

Maury Load Pull Characterization system

- A fundamental passive load pull system capable of performing load pull characterization up to 15W.
- XT982GL01– 0.6 to 18 GHz Load tuner
- Plan to expand to a 3 harmonic hybrid load pull system soon.



EDA Capabilities

SPICE SIMULATORS

SYNOPSYS HSPICE®

cadence Advanced Design System

cadence Advanced Design System

Microwave Office

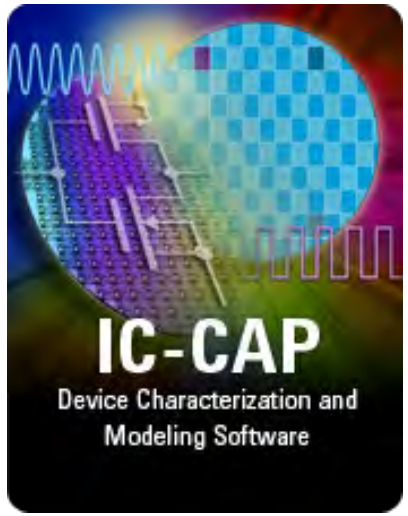
RF

TCAD

COMSOL

SILVACO

SYNOPSYS®

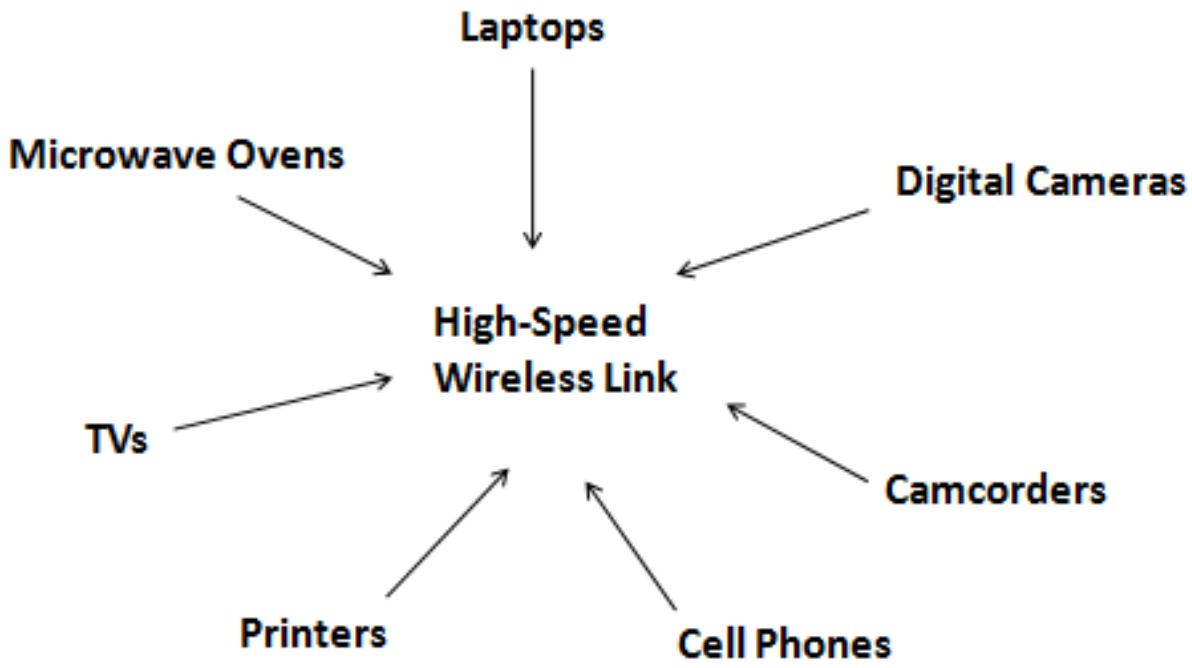


Atomistic Simulations

Quantum Wise

nextnano

A Wireless World

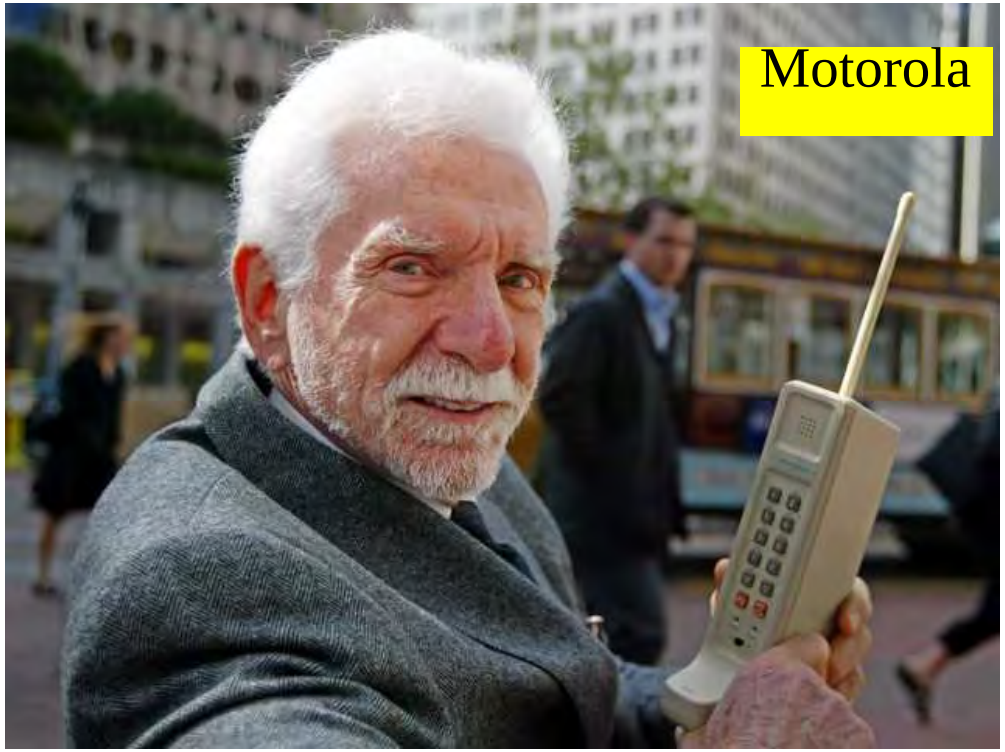


- High-speed wireless links (WiFi, Bluetooth) allow seamless connections among device and appliance.
- Although RF design always talks about wireless transmission, all concepts are valid for wired transmission.

Evolution of Mobile Wireless Communication

Early wireless devices

An old car phone (1940)

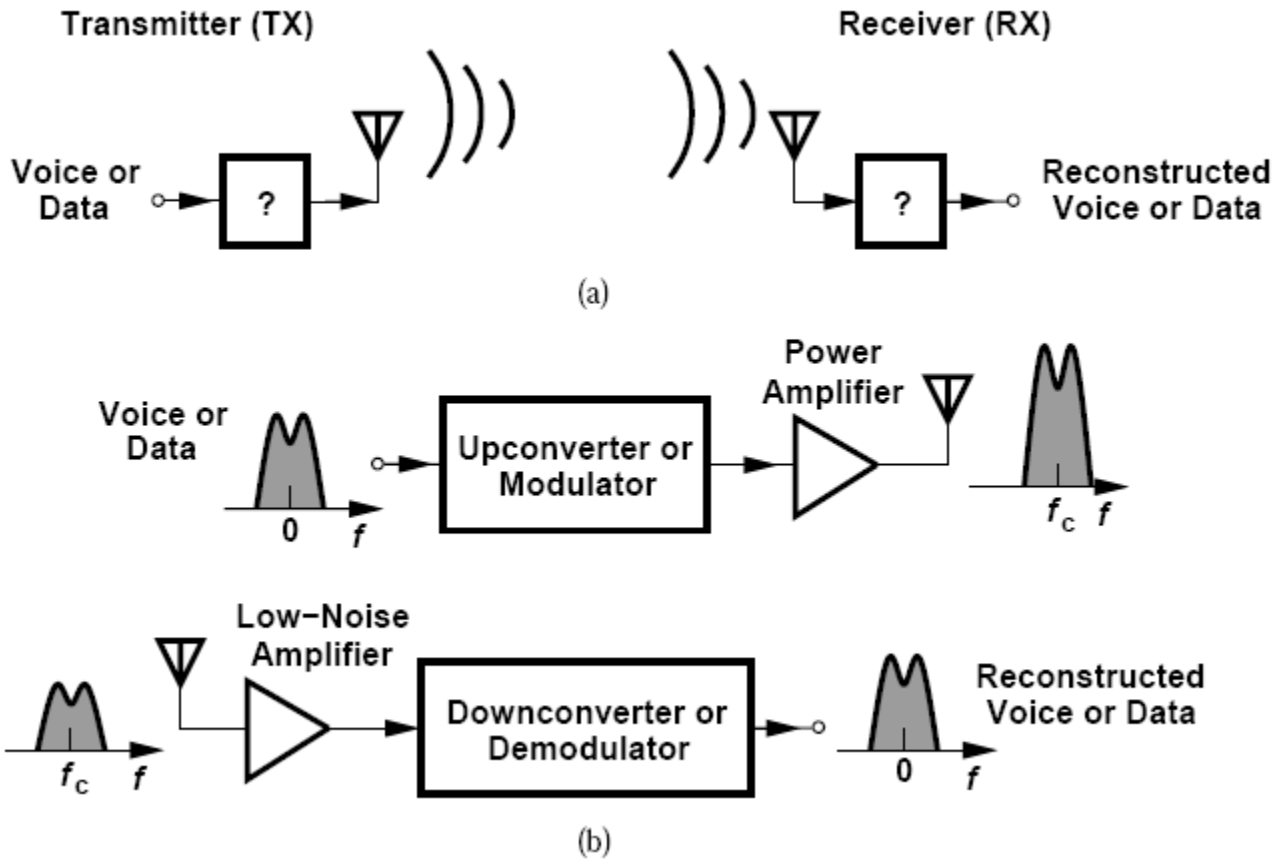


First Hand held cell phone (1973)

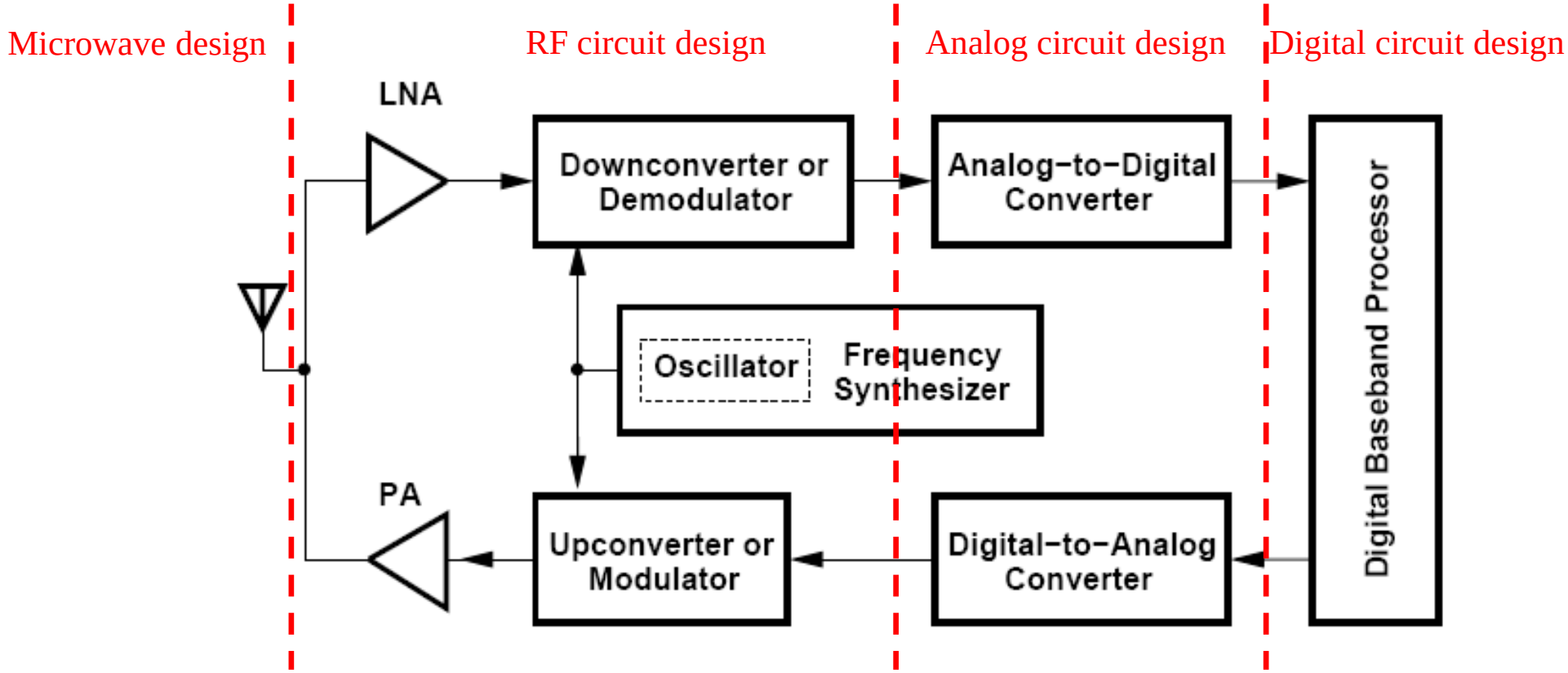
The Big Picture: RF Communication

TX: Drive antenna with high power level

RX: Sense small signal (amplify with low noise)



The Big Picture: Generic RF Transceiver



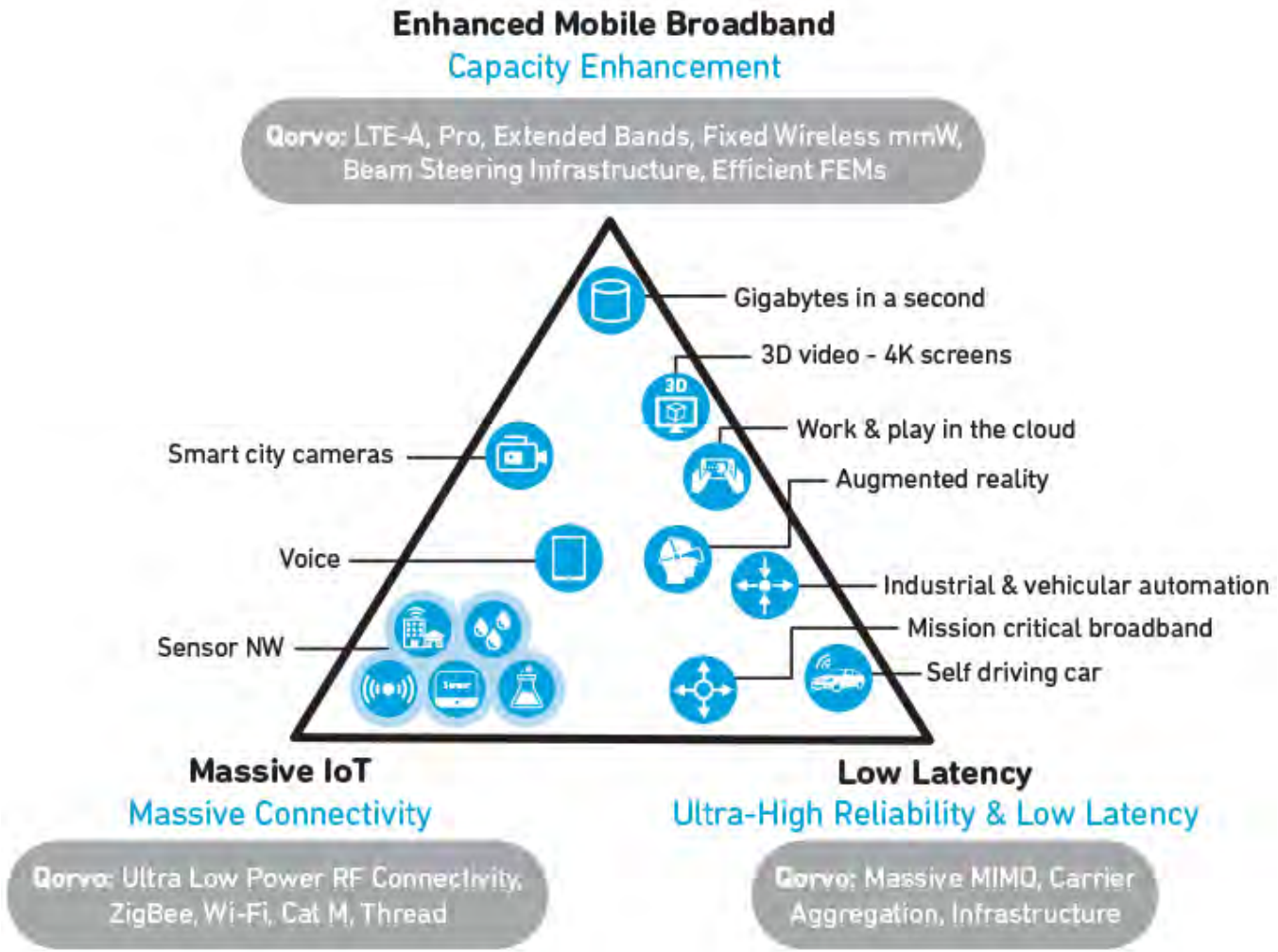
- Signals are upconverted/downconverted at TX/RX, by an oscillator controlled by a Frequency Synthesizer

Evolution of Mobile Wireless Communication

Generation	Speed	Technology	Key Features
1G (1970–1980s)	14.4 Kbps	AMPS,NMT, TACS	Voice only services
2G (1990 to 2000)	9.6/ 14.4 Kbps	TDMA,CDMA	Voice and Data services
2.5G to 2.75G (2001-2004)	171.2 Kbps 20-40 Kbps	GPRS	Voice, Data and web mobile internet, low speed streaming services and email services.
3G (2004-2005)	3.1 Mbps 500- 700 Kbps	CDMA2000 (1xRTT, EVDO) UMTS and EDGE	Voice, Data, Multimedia, support for smart phone applications, faster web browsing, video calling and TV streaming.
3.5G (2006-2010)	14.4 Mbps 1-3 Mbps	HSPA	All the services from 3G network with enhanced speed and more mobility.
4G (2010 onwards)	100-300 Mbps. 3-5 Mbps 100 Mbps (Wi-Fi)	WiMax, LTE and Wi-Fi	High speed, high quality voice over IP, HD multimedia streaming, 3D gamming, HD video conferencing and worldwide roaming.
5G (Expecting at the end of 2019)	1 to 10 Gbps	LTE advanced schemes, OMA and NOMA	Super fast mobile internet, low latency network for mission critical applications, Internet of Things, security and surveillance, HD multimedia streaming, autonomous driving, smart healthcare applications.

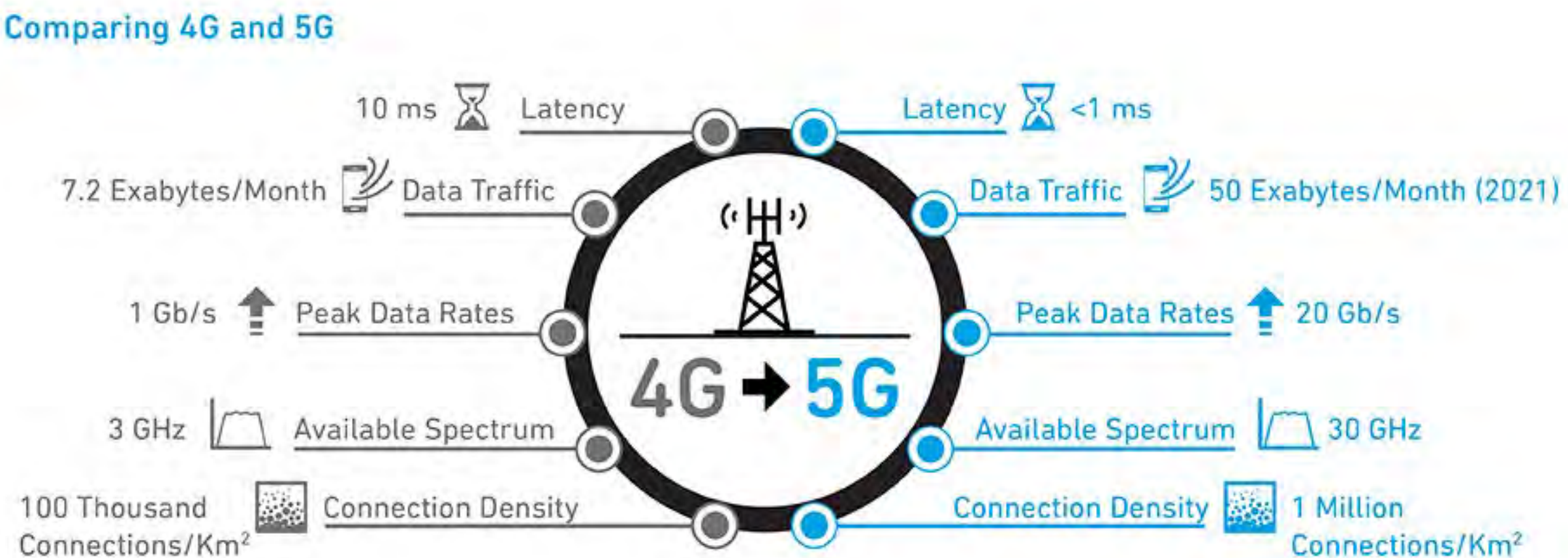
www.rfpage.com

5G - Promises



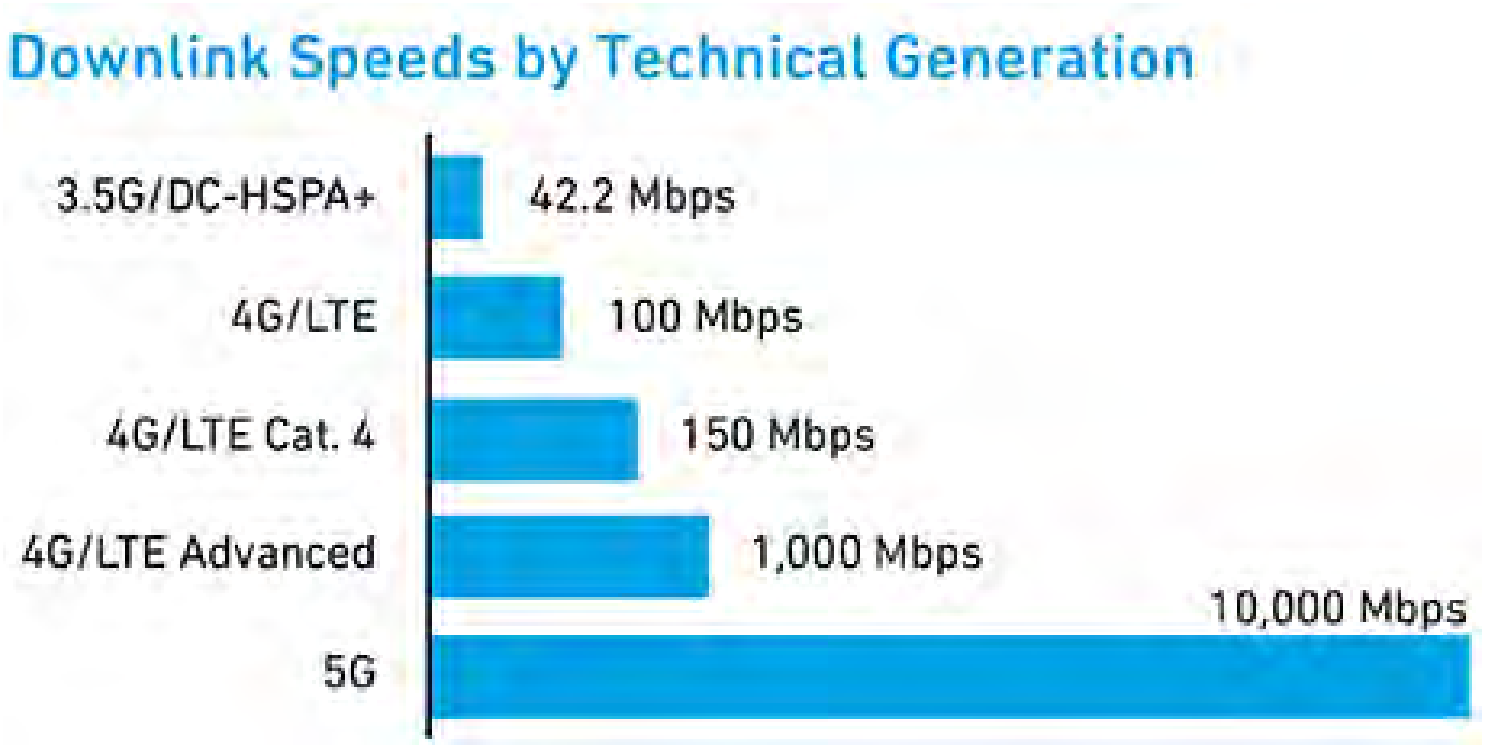
[1] Image Courtesy - Qorvo

5G vs 4G



[1] Image Courtesy - Qorvo

Speed



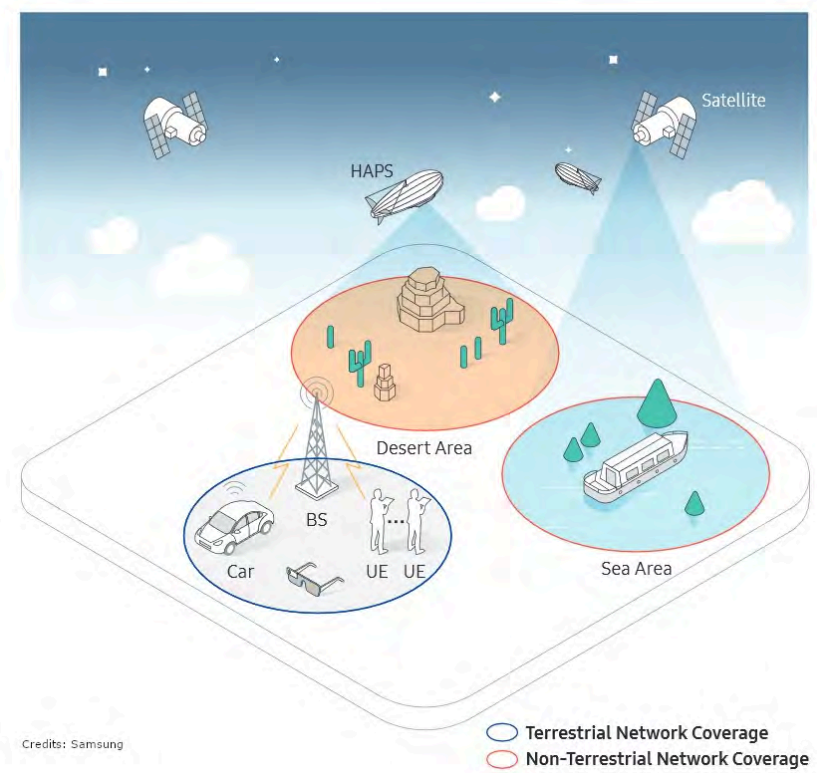
Requirements:

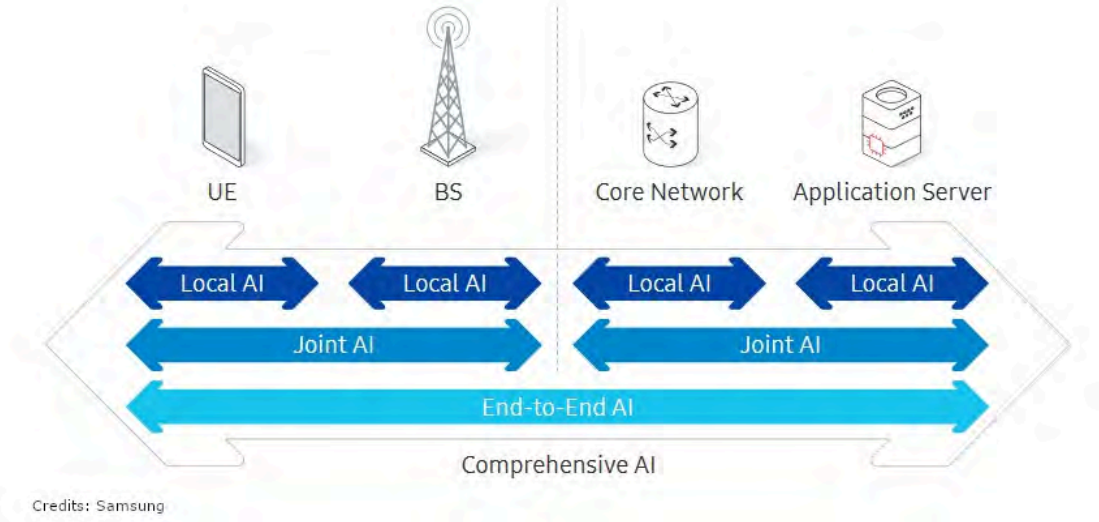
- High frequency operation
- High bandwidth

[1] Image Courtesy - Qorvo

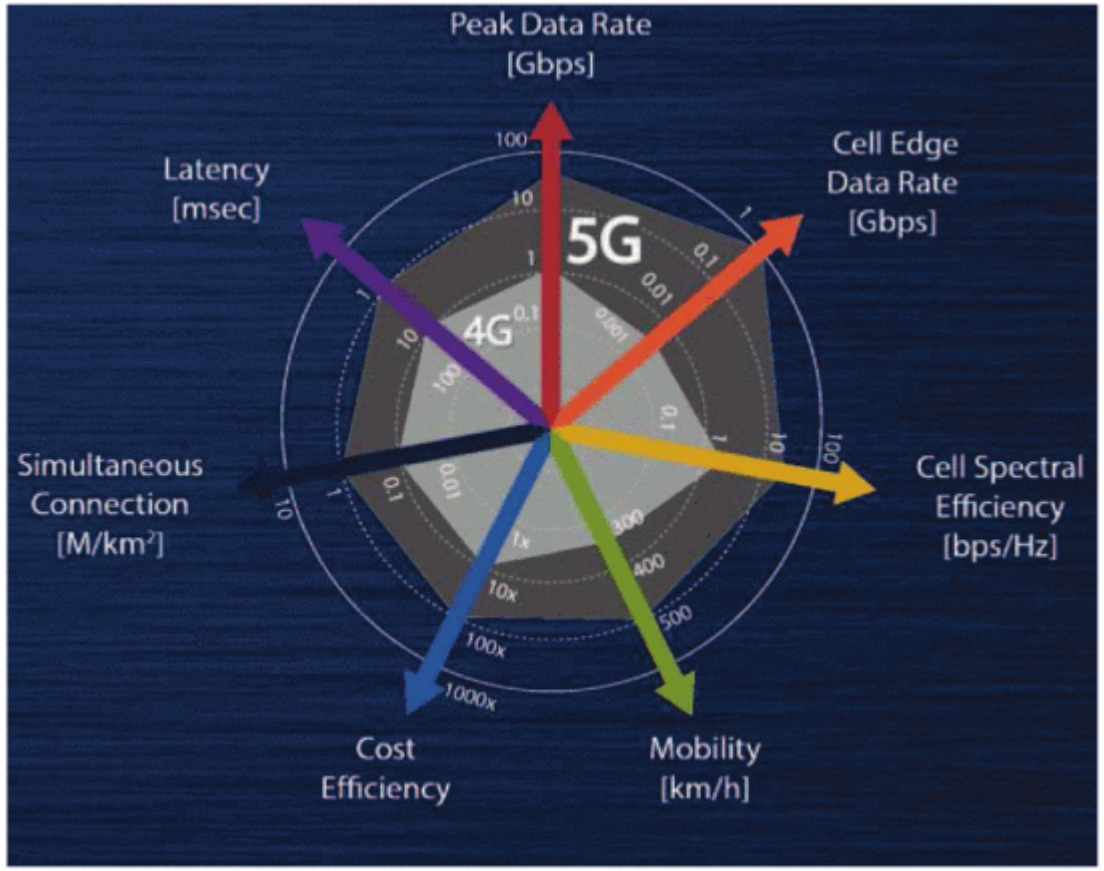
6G?

- Research on 6G
- Applications
  - Artificial Intelligence (AI)
  - Extended Reality (XR)
  - Automation
  - Robotics
- 6G requires massive performance improvements as compared to 5G.
- 5G speed - 20 Gbps and frequencies up to 100 GHz
- 6G - 1000 Gbps and may utilize frequencies up to 3 THz



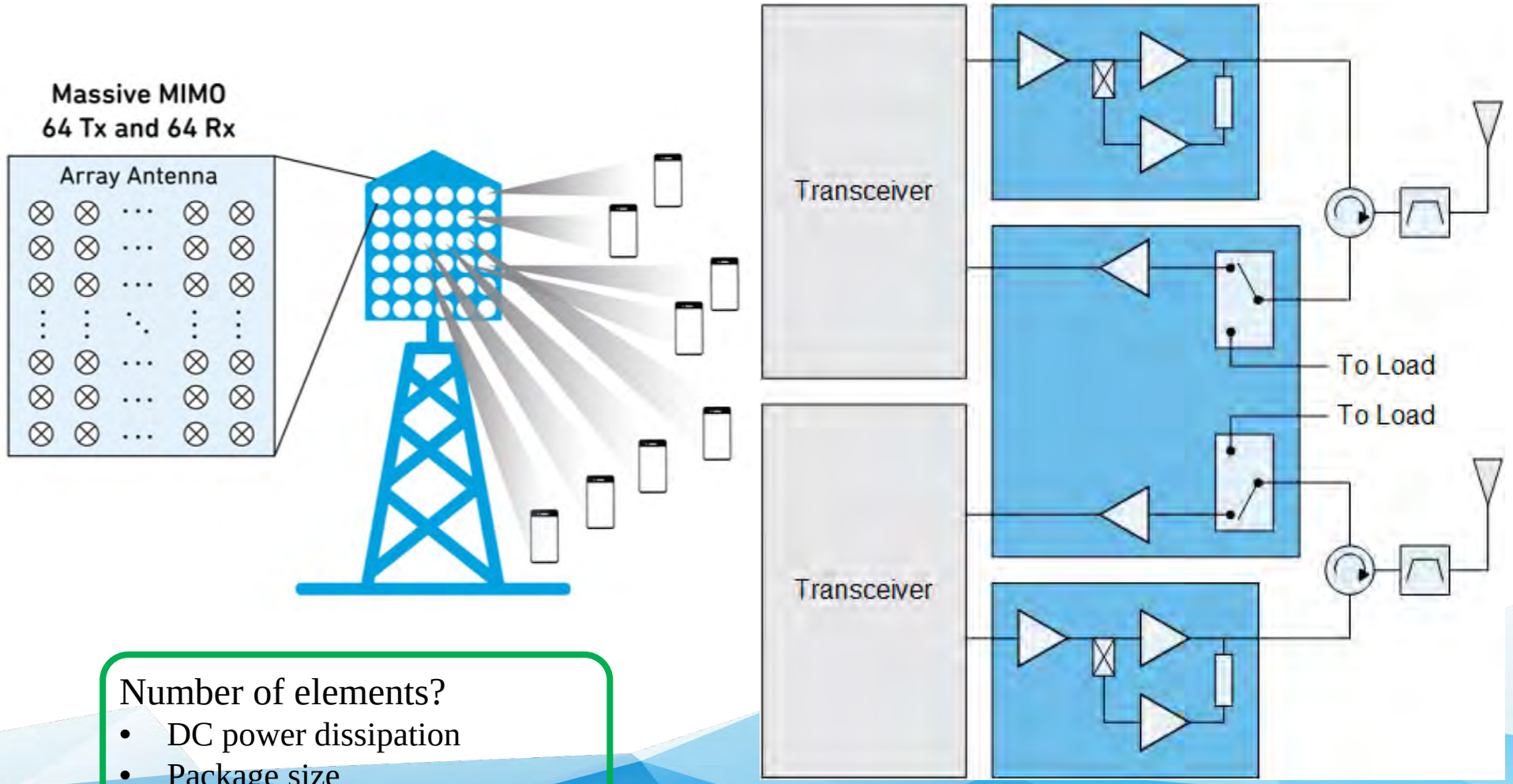


What's so special in 5G



- Frequency bands – sub-6GHz and 28GHz
- 5G small cell
  - Qorvo and Peregrine Semi are offering solutions using SOI technology.
    - Average power of 5-6 W
  - Lower power will limit the coverage area of small cells, restricting its use in cities.
- Solution – GaN technology
  - Enables high power modules for data transmission.

Massive MIMO



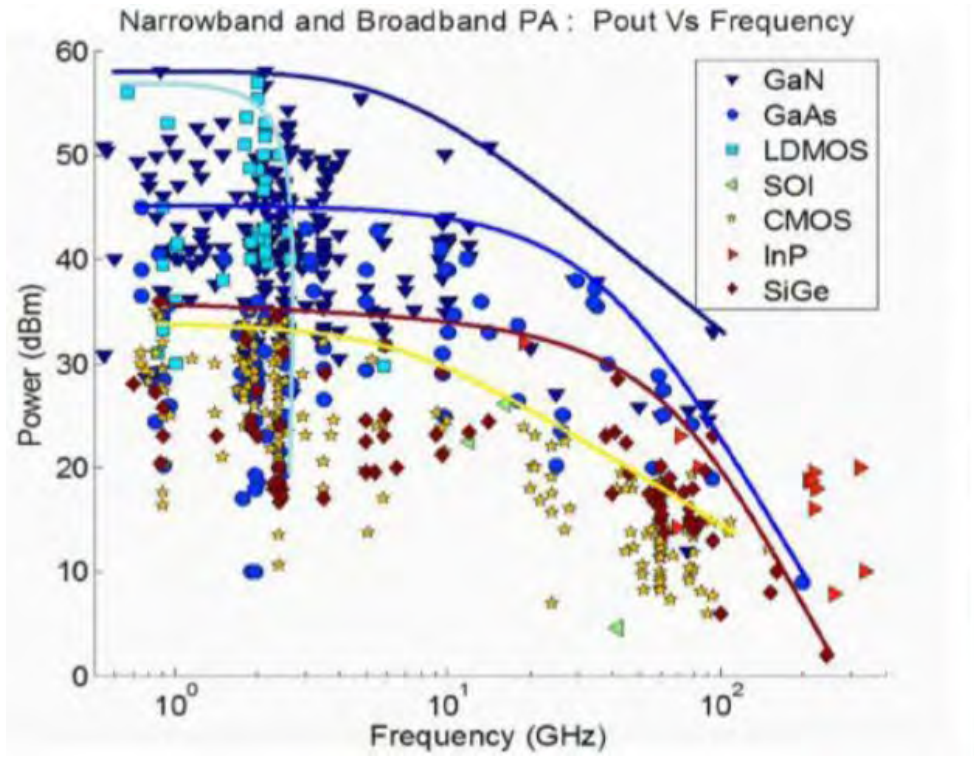
Number of elements?

- DC power dissipation
- Package size

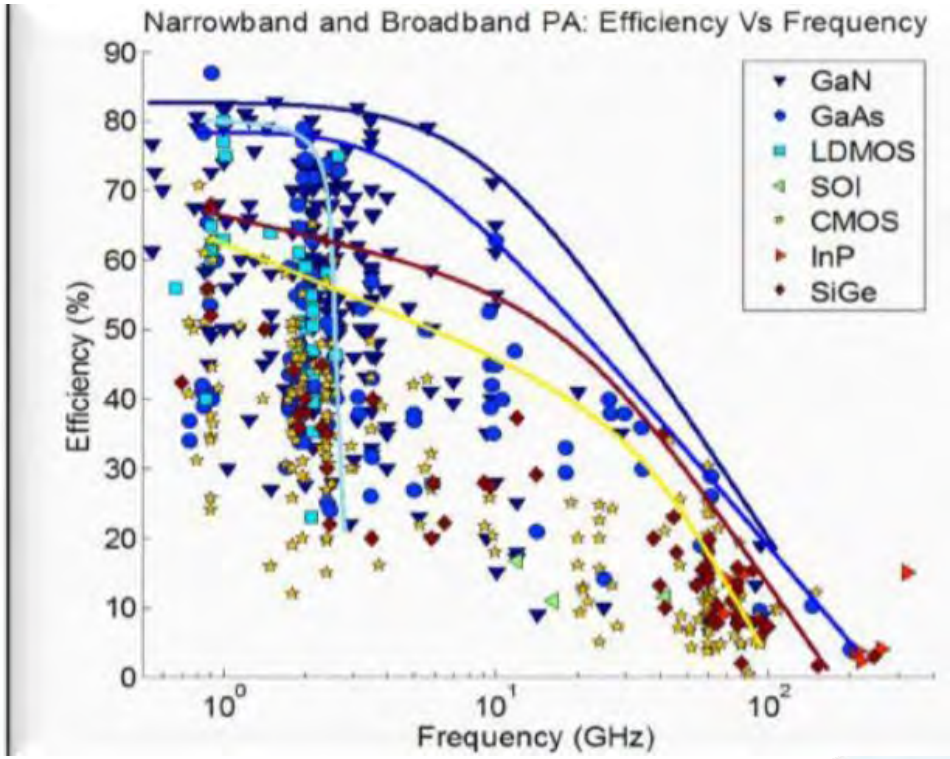
[1] Image Courtesy - Qorvo

Technologies - State-of-the-art

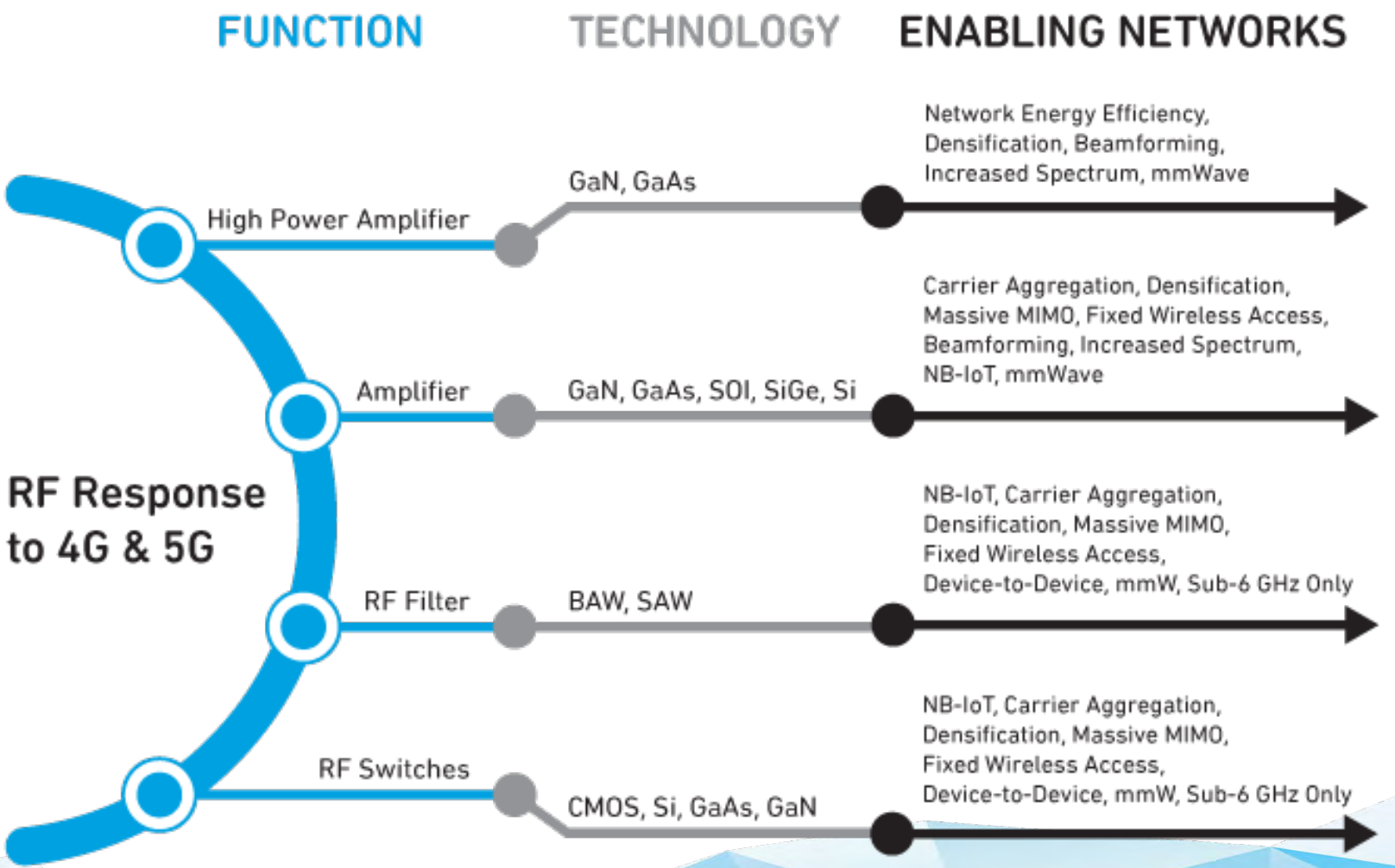
Power



Efficiency

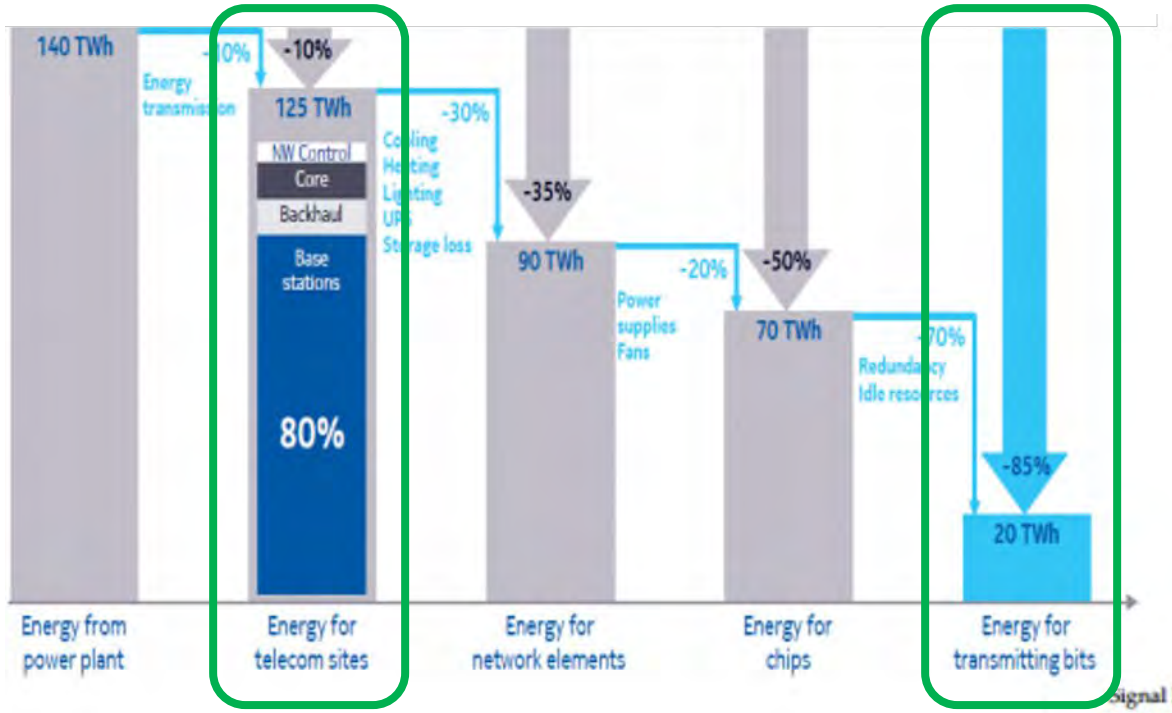


GaN dominance in RF

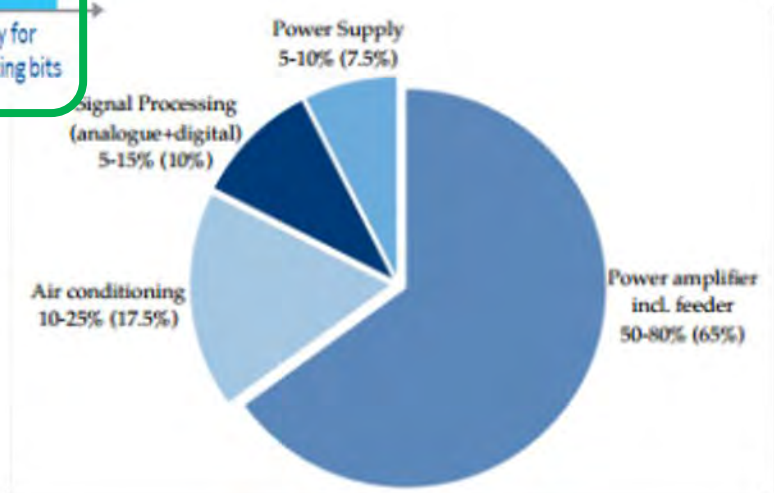


[1] Image Courtesy - Qorvo

Energy Budget and Loss



Base Station Energy Breakup



Efficiency Question:

- 50-60 % base station power taken by PA
- 15 % of total energy transmitted

[1] Image Courtesy - Nokia Networks

Efficiency - GaN vs LDMOS

Silicon LDMOS: NXP A2T18S160W31SR3

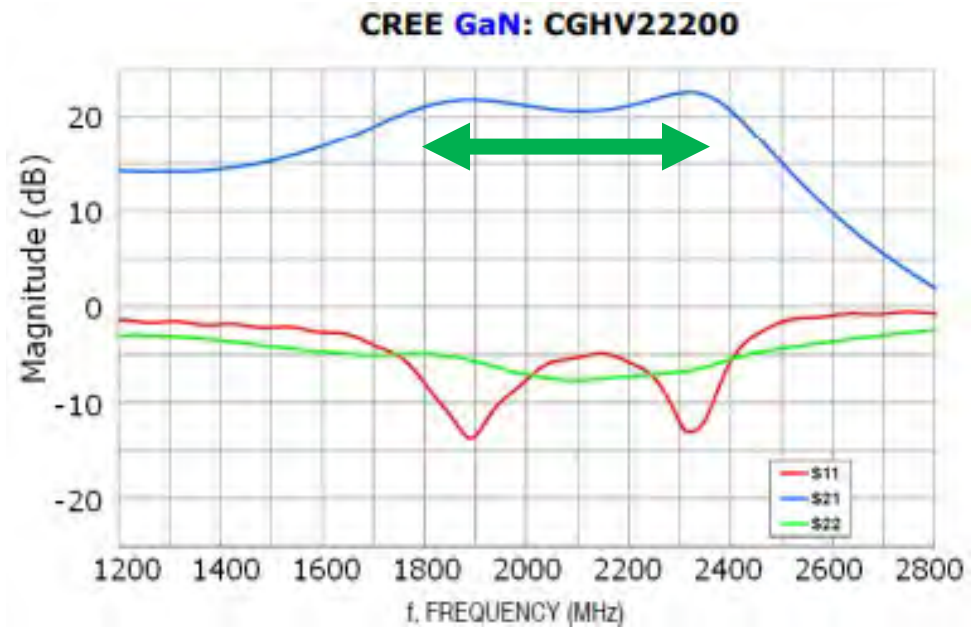
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	19.6	32.1	7.2	–34.7	–12
1840 MHz	20.1	32.1	7.2	–35.0	–17
1880 MHz	19.9	31.6	7.2	–35.4	–12

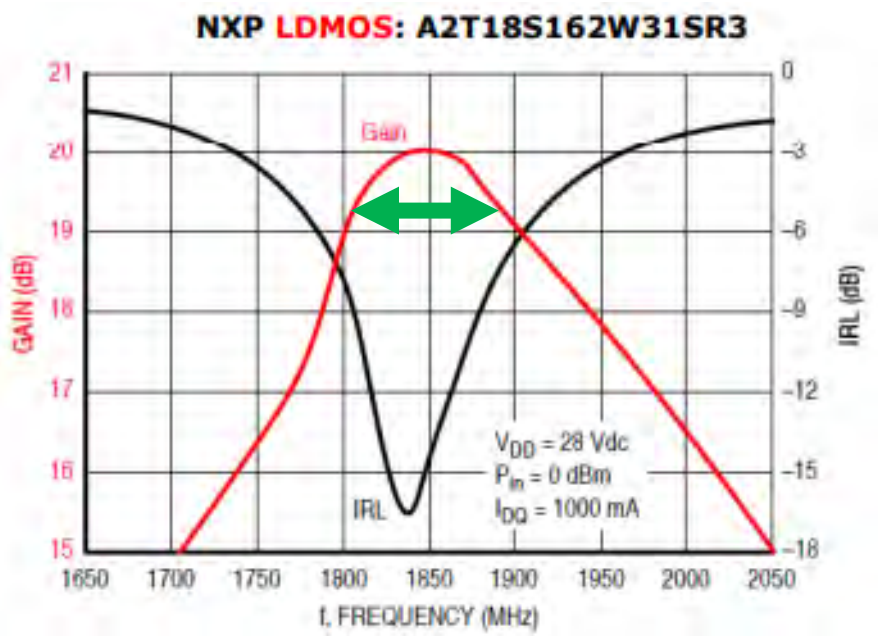
GaN: NXP A2G22S160-01SR3

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.2	36.9	7.1	–33.4	–11
1840 MHz	18.5	37.4	7.1	–33.0	–16
1880 MHz	18.6	38.2	7.0	–32.5	–16

[1] Image Courtesy - NXP Semiconductors

Bandwidth - GaN vs LDMOS





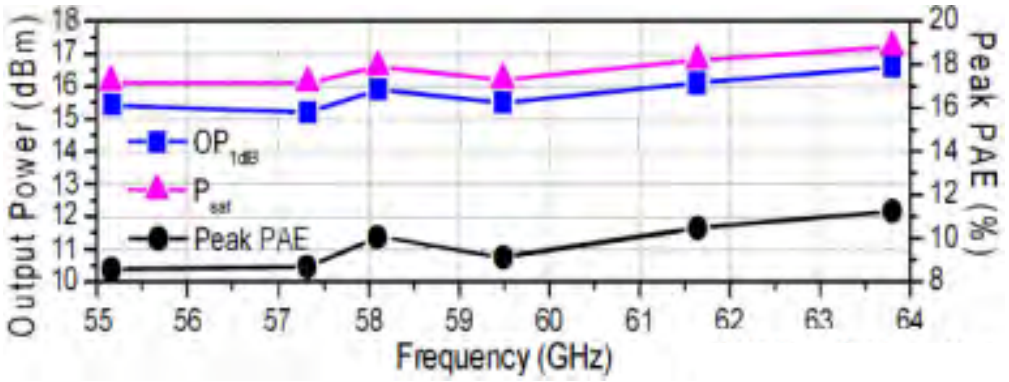
Inference:

- GaN Wideband Gain
- LDMOS would need 4 channel carrier aggregation → One GaN Carrier

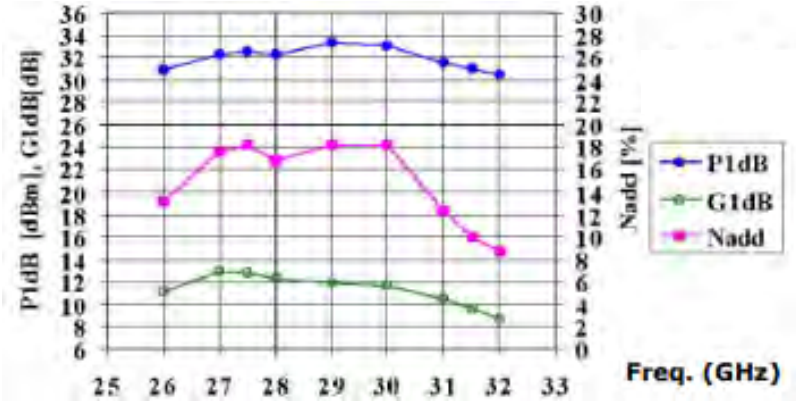
[1] Image Courtesy - Wolfspeed - Datasheets

[2] Image Courtesy - NXP Semiconductors - Datasheets

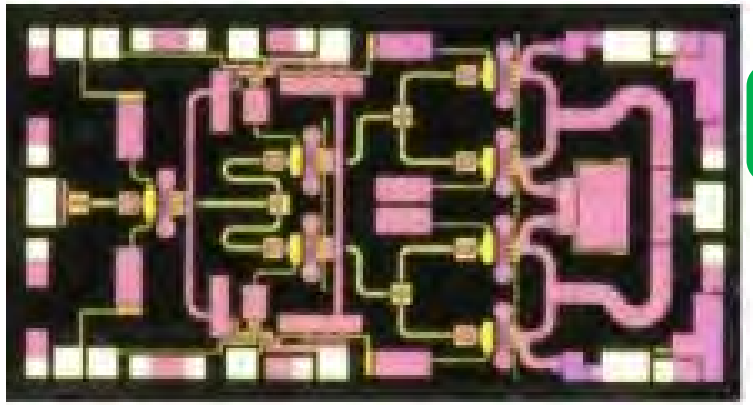
Comparison at mmWave



Si CMOS: 11% & 0.1W



GaAs: 14% & 2W



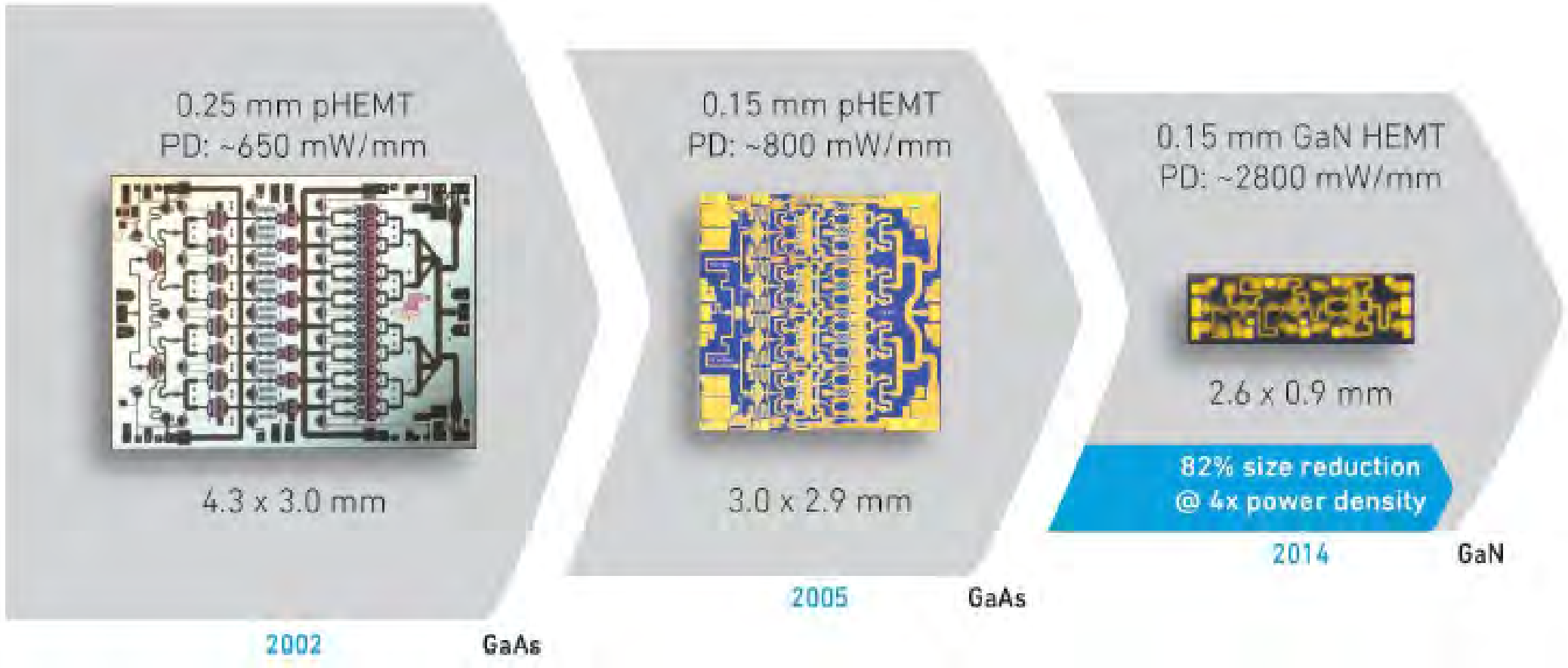
Product Features

- Frequency Range: 27 – 31GHz
- Psat: 37dBm (typical across frequency)
- PAE: 28%
- Small Signal Gain: 23dB
- Input Return Loss: 10dB
- IM3 @ 25dBm/tone: -36dBc
- IM5 @ 25dBm/tone: -45dBc
- Bias: V_D = 20V, I_{DQ} = 140mA, V_G = -3.0V Typical
- Chip Dimensions: 3.24 x 1.74 x 0.10mm

GaN MMIC: 28% & 5W

[1] Image Courtesy - IEEE Microw. Mag., 2017

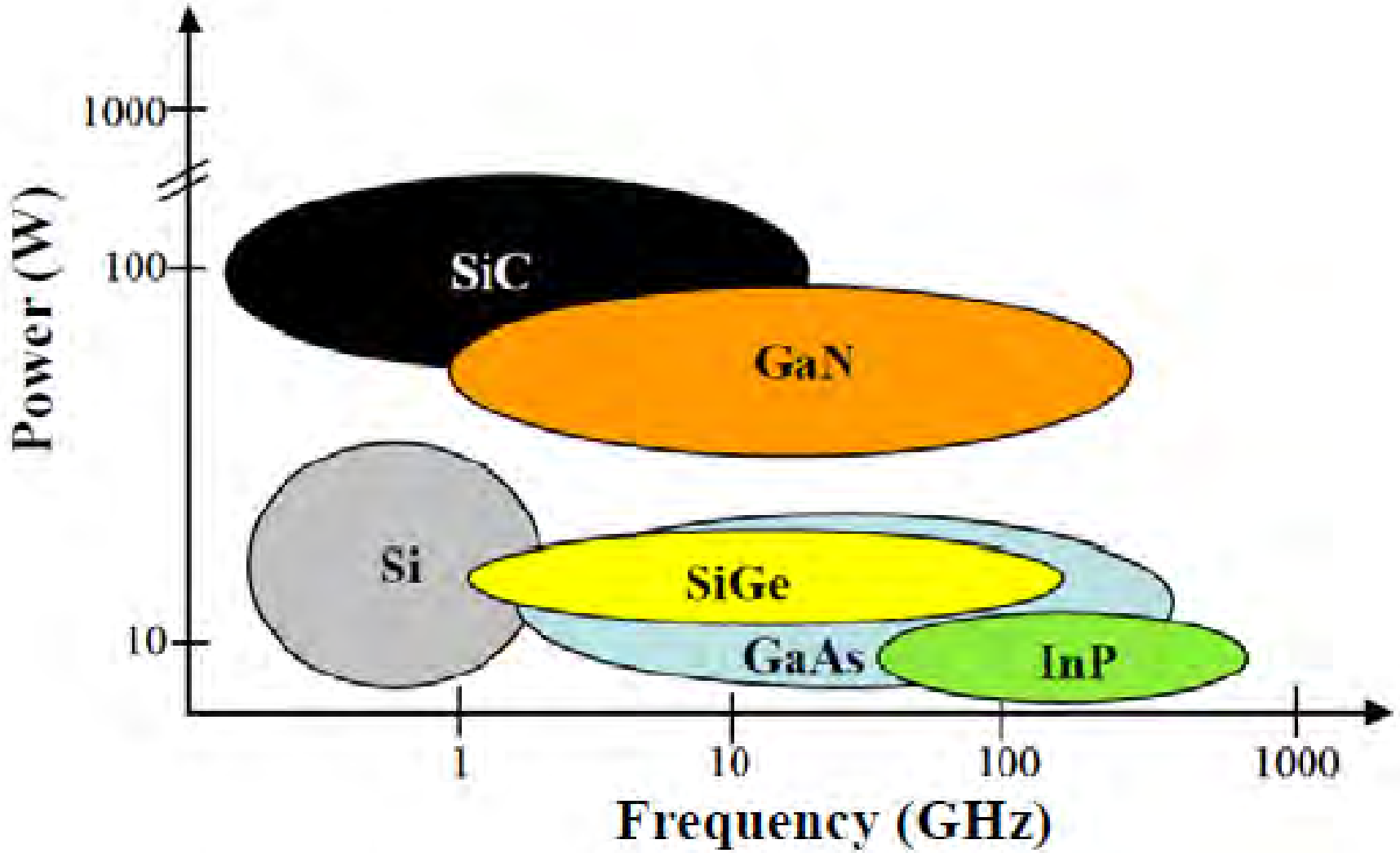
Size reduction



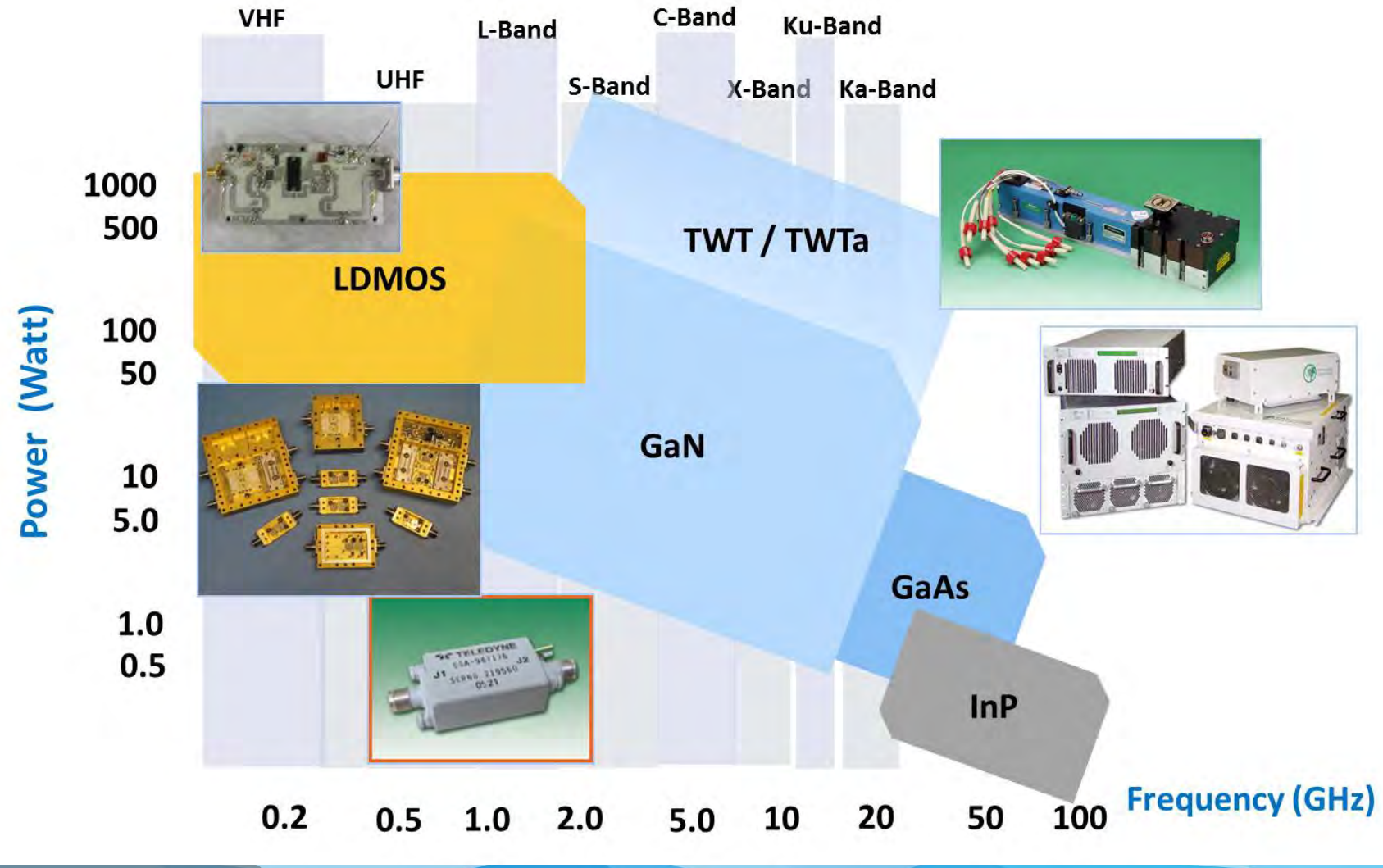
High Power Density → Small Size → Miniaturization & Easy Integration

[1] Image Courtesy - Qorvo

Application area of different semiconductor materials



RF Market


VHF
UHF
L-Band
S-Band
C-Band
X-Band
Ku-Band
Ka-Band
1000
500
100
50
10
5.0
1.0
0.5
Power (Watt)
LDMOS
TWT / TWTa
GaN
GaAs
InP
0.2
0.5
1.0
2.0
5.0
10
20
50
100
Frequency (GHz)

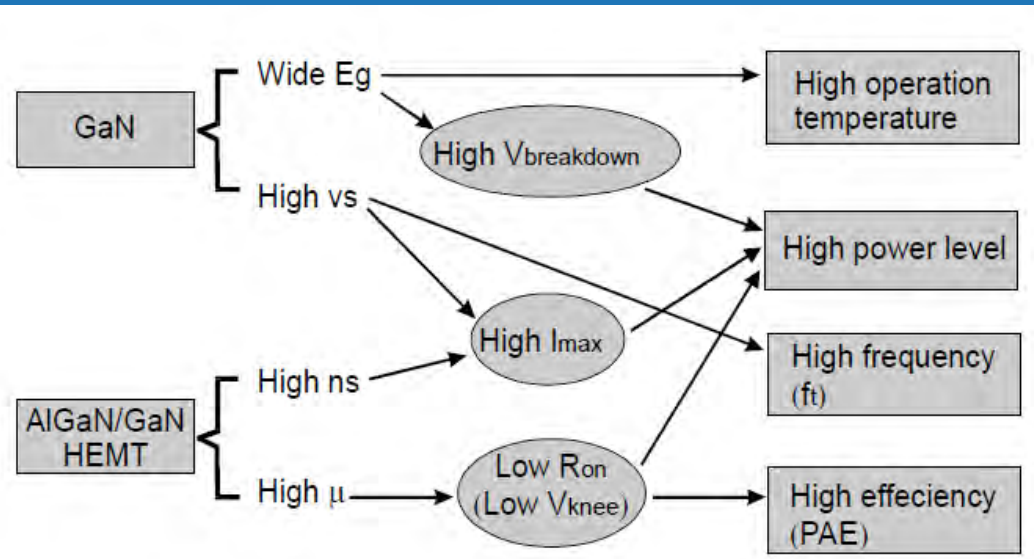
GaN Properties

Comparison of Material Properties & respective FoMs

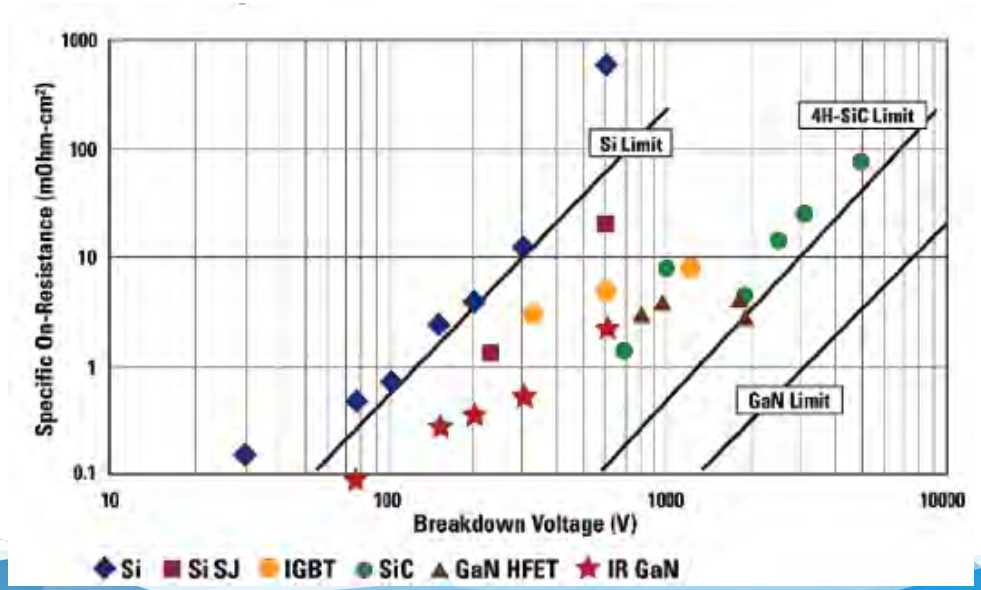
[1]

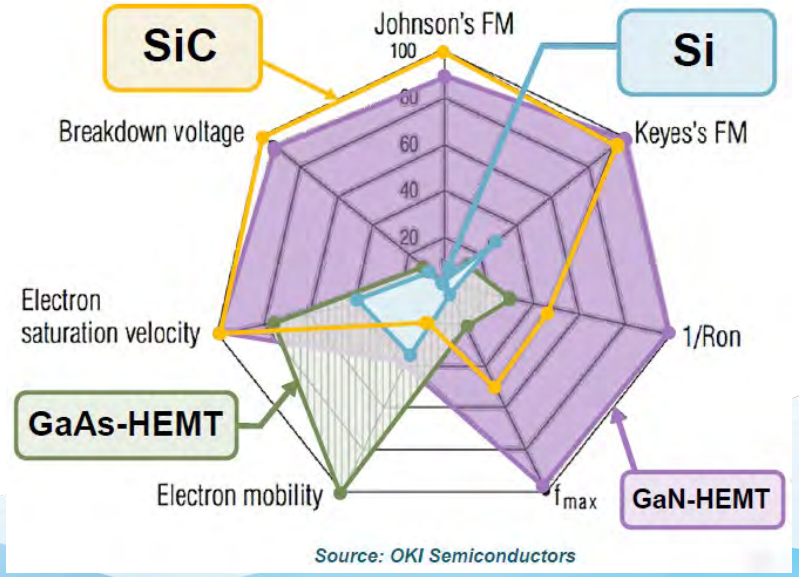
	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.1	1.42	3.26	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0
μ_n (cm^2/Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)
v_{sat} (10^7cm/s)	1.0	1.0	2.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5

Johnson's figure of merit (rel. to Si)



[2]

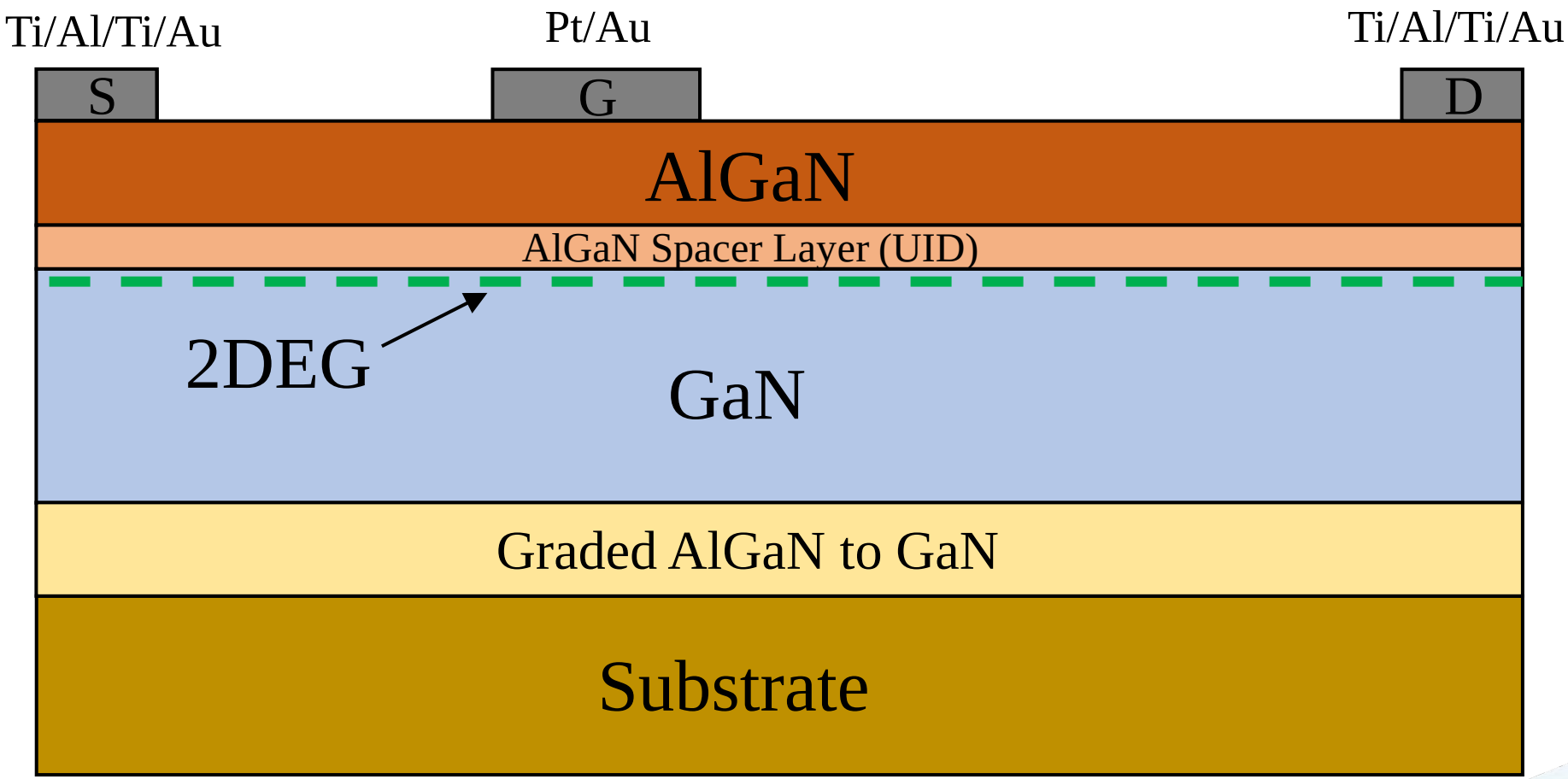




[1] U. K. Mishra *et al.*, *Proc. IEEE*, **96 (2),** [2008]

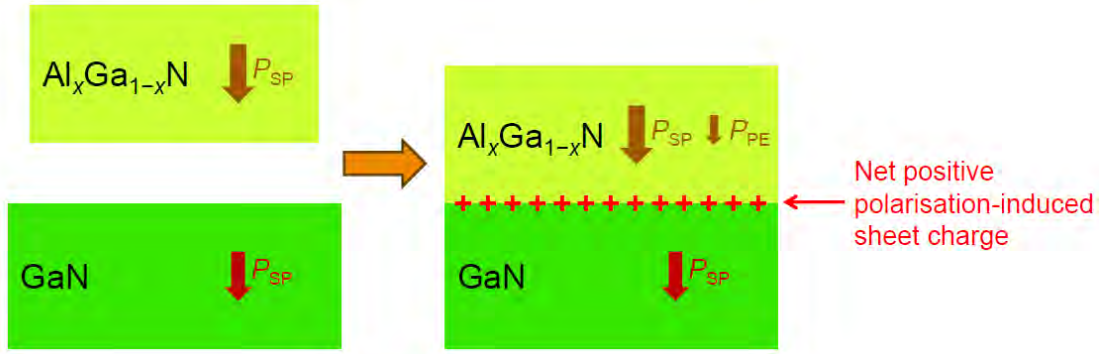
[2] M. A. Briere, Tech. Rep., International Rectifier, Dec. [2008]

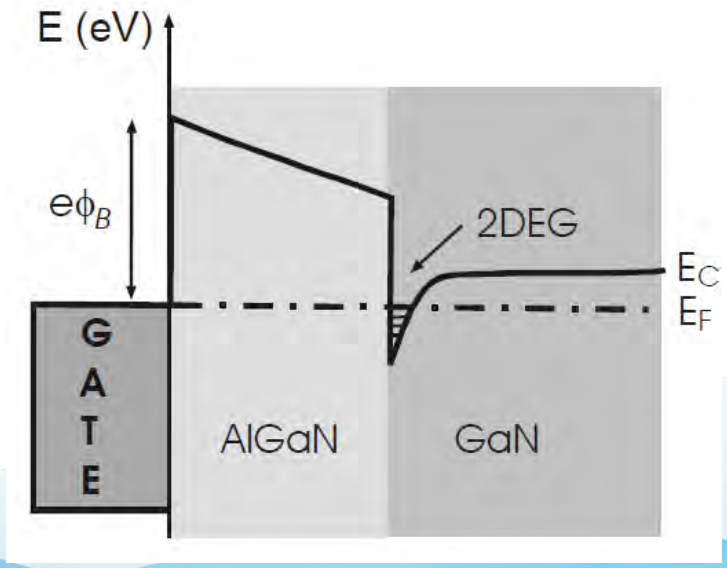
GaN HEMT Structure



AlGaN/ GaN Hetero-structure

- The AlGaN/GaN hetero-structure is used to take advantage of the two dimensional electron gas (2-DEG)
- AlGaN/GaN materials create piezoelectric and spontaneous polarization effects using an un-doped hetero-interface



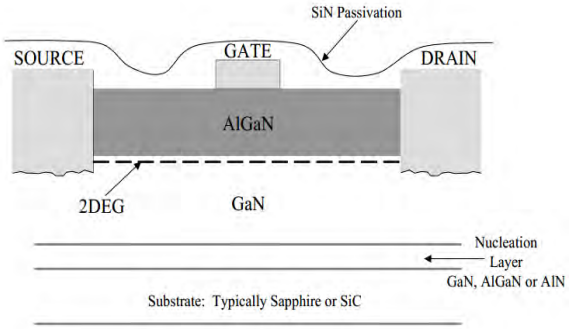


GaN HEMT

Some interesting features of III-nitride system:

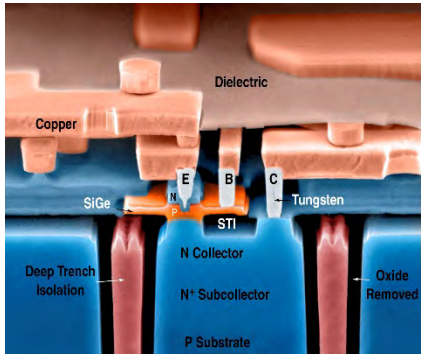
- Wide bandgap
- High 2-DEG charge density
- High electron mobility
- High breakdown voltage
- Excellent thermal conductivity
- High power density per mm of gate periphery

- GaN HEMTs are able to operate in high frequency, high power as well as high temperature device applications



Goal of a PDK – The output of Enablement

Technology Innovation

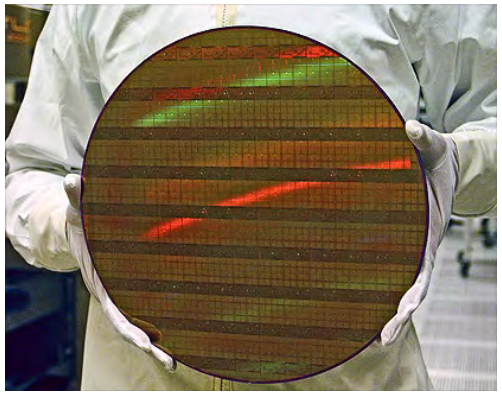


Enablement PDK
Key to Happy Designers!!

Circuit Designers

- Offer a circuit design environment that enables full exploitation of technology
  - Capture all device physics
  - Model impact of layout choices on device mean and variance
  - Accurate modeling of layout effects for simulation from layout

Compact Modeling or SPICE Modeling



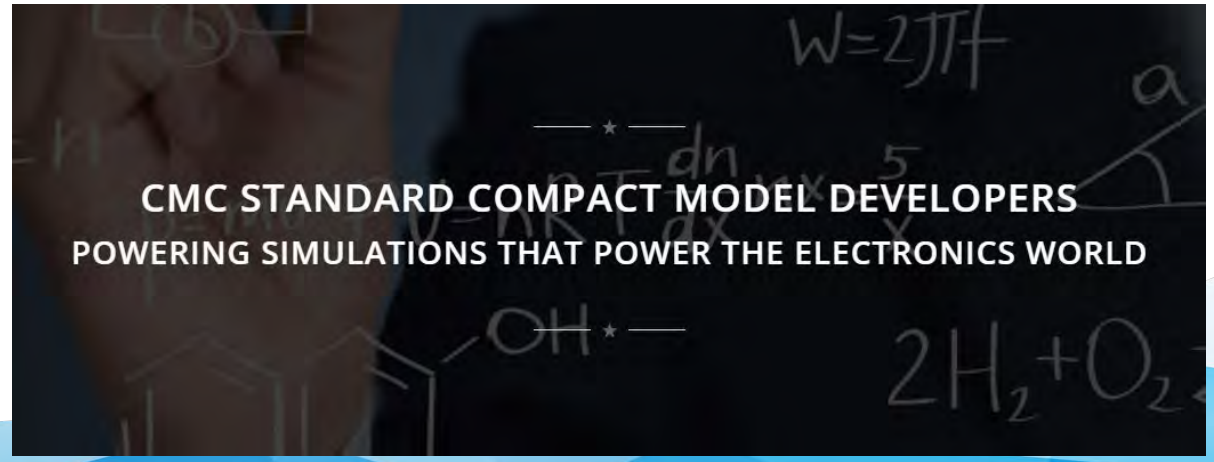
Medium of information exchange

- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~µ*sec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG, ASH-HEMT

Industry Standard Compact Models

- Standardization Body – Compact Model Coalition
  http://www.si2.org/cmc/
- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia
- CMC models are available in commercial SPICE simulators



News (March 14, 2018)

- Our ASM-GaN-HEMT Model is industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

Si Compact Models

Si2 Approves IC Design Simulation Standards for Gallium Nitride Devices

http://www.si2.org/cmc/

March 14, 2018 / 0 Comments / in Compact Model, Frontpage /

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

http://www.si2.org/2018/03/14/gallium-nitride-models/

Media Coverage (April 11, 2018)

आईआईटी में बना सिमुलेशन सॉफ्टवेयर

यह सॉफ्टवेयर तैयार करने वाला दुनिया का दूसरा संस्थान बना आईआईटी कानपुर, आसानी से टेस्ट कर पाएंगे इंटीग्रेटेड सर्किट का डिजाइन

अमर उजाला ब्यूरो

कानपुर। आईआईटी कानपुर के वैज्ञानिकों ने पांच साल की मेहनत के बाद आखिरकर इंटीग्रेटेड सर्किट डिजाइन सिमुलेशन सॉफ्टवेयर तैयार कर लिया। इस सॉफ्टवेयर को तैयार करने वाला आईआईटी कानपुर दुनिया का दूसरा संस्थान है। इसके पहले अमेरिका के मैचाच्यूट्स इंस्टीट्यूट ऑफ टेक्नोलॉजी के वैज्ञानिकों ने इसे तैयार किया था।

इस सॉफ्टवेयर को इलेक्ट्रॉनिक्स विभाग के प्रो. योगेश चौहान ने तैयार किया है। इस सॉफ्टवेयर के जरिए इंटीग्रेटेड सर्किट की डिजाइन को आसानी से टेस्ट किया जा सकेगा। मतलब कोई भी सर्किट डिजाइन करने से पहले इस सॉफ्टवेयर के जरिए कंप्यूटर पर ही चेक किया जा सकता है कि सर्किट में क्या-क्या कमी है सकता है। अभी तक लिए लाखों रुपये स

आईआईटी में तैयार किया गया सिमुलेशन सॉफ्टवेयर।

बिजली की होगी बचत 5जी में भी भूमिका

सॉफ्टवेयर के जरिए जैन सेमीकंडक्टर के डिजाइन का भी परीक्षण किया जा सकेगा। इस सेमीकंडक्टर का प्रयोग बिजली की बचत के लिए किया जाता है। अभी तक इसका परीक्षण महंगा होता था लेकिन अब सॉफ्टवेयर तैयार होने से यह भी सस्ता हो जाएगा। इसके अलावा इस सॉफ्टवेयर का प्रयोग 5 जी की तकनीक विकसित करने में भी की जा सकेगी।

आईआईटी के विशेषज्ञों ने खुद तैयार कर लिया है तो उम्मीद है कि आने वाले दिनों में देश के शिक्षण संस्थानों और देश की कंपनियों को इसके लिए कम कीमत चुकानी पड़े। प्रो. चौहान ने यह शोध अपने एक ऑस्ट्रेलियाई दोस्त के साथ मिलकर की है। अब इस रिसर्च को और बड़े स्तर पर पहुंचाने के लिए

सभी इलेक्ट्रॉनिक डिवाइस में प्रयोग होता है इंटीग्रेटेड सर्किट

इंटीग्रेटेड सर्किट का प्रयोग हर तरह के इलेक्ट्रॉनिक और इलेक्ट्रिकल डिवाइस में किया जाता है। इसलिए इसे तैयार करना मुश्किल होता था। पहले लोग प्रैक्टिकली इसे तैयार

'आईआईटीके' ने बनाया सर्किट सिम्यूलेशन सॉफ्टवेयर मॉडल

सहारा न्यूज ब्यूरो

कानपुर।

आईआईटी, कानपुर (आईआईटीके) संयुक्त राज्य अमरीका के मैसाच्यूट्स इंस्टीट्यूट ऑफ टेक्नालॉजी के वाद इंट्रीगेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार करने वाला दुनिया का दूसरा संस्थान वन गया है। यह सॉफ्टवेयर इंडस्ट्री के क्षेत्र में मील का पत्थर साबित होगा। कई सालों के कठोर परिश्रम के वाद संस्थान ने यह सफलता पायी है।

संस्थान के विद्युत अभियांत्रिकी विभाग के प्रो.योगेश सिंह चौहान की अगुवाई में डिजाइन सिम्यूलेशन तैयार किया गया है। प्रो.चौहान व उनके आस्ट्रेलियन सहयोगी सौरभ खंडेलवाल ने इस मॉडल को तैयार करने में कड़ी मेहनत की। अनुसंधान एवं विकास के लिए दोनों वैज्ञानिकों को सीएमसी द्वारा प्रतिवर्ष 70 हजार यूएस डॉलर का अनदान

प्रो. योगेश सिंह चौहान

संस्थान के प्रो.योगेश चौहान ने आस्ट्रेलियन सहयोगी संग मिल तैयार किया डिजाइन

'आईआईटीके' एमआईटी अमरीका के बाद सिम्यूलेशन बनाने वाला दूसरा संस्थान

आगे अनुसंधान के लिए सीएमएसी देगा 70 हजार यूएस डॉलर प्रति वर्ष

स्वीकृत किया गया है। इस परियोजना के तहत शोध कार्य लंबे समय 10-15 वर्षों तक चलने की संभावना है। प्रो.चौहान एवं उनकी टीम इसरो व डीआरडीओ के साथ मिलकर परीक्षण मॉडल तथा जीएएन उपकरणों के विकास के लिए भी कार्य कर रही है।

वताया जाता है कि जीएएन सेमी कंडक्टर उपकरण वनाने वाली कंपनियां इस टीम के द्वारा विकसित मॉडल से वास्तविक उत्पादन करने से पहले अपने सर्किट का परीक्षण कर पाएंगे। इसे जीएएन सेमीकंडक्टर उपकरणों की लागत में कमी लायी जा सकेगी। पावर डिवाइसेज में जीएएन सेमी कंडक्टर का उपयोग किये जाने से ऊर्जा की वचत होगी व उसकी क्षमता वढ़ेगी। वर्तमान में सिलिकान सेमीकंडक्टर का वहुत प्रचलन है, किन्तु शीघ्र ही जीएएन का उपयोग इसके विकल्प के रूप में कई एप्लीकेशन में होने में की उम्मीद जतायी जा रही है। इसके अलावा संस्थान के विद्युत शेष पेज 13

अंतरिक्ष, रक्षा व पावर क्षेत्र के लिए उपयोगी होगा सिम्यूलेशन

पूर्व में रामानुजन फेलो सहित कई सम्मानएवार्ड से सम्मानित प्रो.योगेश कुमार चौहान ने वताया कि संवंधित सेमी कंडक्टर व साफ्टवेयर पावर एम्प्लीफायर अंतरिक्ष अनुसंधान के लिए उपयोगी होगा। संवंधित उपकरणों की उत्पादन लागत कम की जा सकेगी व पावर उपकरणों की कार्यकुशलता एक्यूरेसी वढ़ेगी। भविष्य के 5 जी तकनीक के लिए भी यह काफी उपयोगी होगा। अंतरिक्ष अनुसंधान के क्षेत्र में काम आने वाले उपकरणों की कार्यकुशलता वढ़ाने में यह सहायक सिद्ध होगा।

अब झटपट बनेंगे इलेक्ट्रॉनिक उपकरण

जागरण संवाददाता, कानपुर : आइआइटी कानपुर के इलेक्ट्रिक इंजीनियरिंग विभाग के प्रो. योगेश चौहान की खोज से मजबूत और टिकाऊ इलेक्ट्रानिक उपकरण भी झटपट बन जाएंगे। उन्होंने ऐसा इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार किया है, जिसकी सहायता से चंद मिनटों में किसी भी इलेक्ट्रानिक गैजेट्स का कंप्यूटरीकृत डिजाइन बन सकेगा। इस खोज से आइआइटी कानपुर यूएसए के मैसाचुसेट्स इंस्टीट्यूट ऑफ टेक्नालाजी (एमआइटी) के बाद इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर तैयार करने वाला दुनिया का दूसरा संस्थान बन गया है।

अमेरिका में चुना गया सॉफ्टवेयर : अमेरिका में सेमी कंडक्टर इंडस्ट्री से संबंधित 40 से अधिक कंपनियों की संस्था (काम्पैक्ट मॉडल कोएलेशन) ने कई देशों के सॉफ्टवेयर का अवलोकन किया। जिसमें से एमआइटी और आइआइटी के सॉफ्टवेयर को चुना।

हर साल मिलेंगे 70 हजार

- आइआइटी प्रोफेसर ने वनाया इंटीग्रेटेड सर्किट डिजाइन सिम्यूलेशन सॉफ्टवेयर

प्रो. योगेश चौहान

यूएस डालर : प्रो. चौहान ने आस्ट्रेलिया के सहयोगी प्रो सौरभ खंडेलवाल के साथ पांच साल की कड़ी मेहनत के बाद साफ्टवेयर तैयार किया। अनुसंधान एवं विकास के लिए इन दोनों वैज्ञानिकों को हर साल 70 हजार यूएस डालर का अनुदान मिलेगा।

गणित और भौतिक विज्ञान के फार्मूले पर आधारित : साफ्टवेयर गणित और भौतिक विज्ञान के साधारण फार्मूले पर आधारित है। किसी भी इलेक्ट्रॉनिक उपकरण का कैसा डिजाइन तैयार किया जाना है, उसकी आसानी से गणना हो सकेगी।

रक्षा क्षेत्र और अंतरिक्ष कार्यक्रम में सहयोग

प्रो. चौहान के मुताबिक साफ्टवेयर से रक्षा क्षेत्र और अंतरिक्ष कार्यक्रम में काफी सहयोग मिलेगा। 5जी के हाई स्पीड एम्पलीफायर बनाने में मदद मिलेगी। चालकरहित कार, रिमोट सर्जरी आदि बनाना संभव हो जाएगा।

Contents

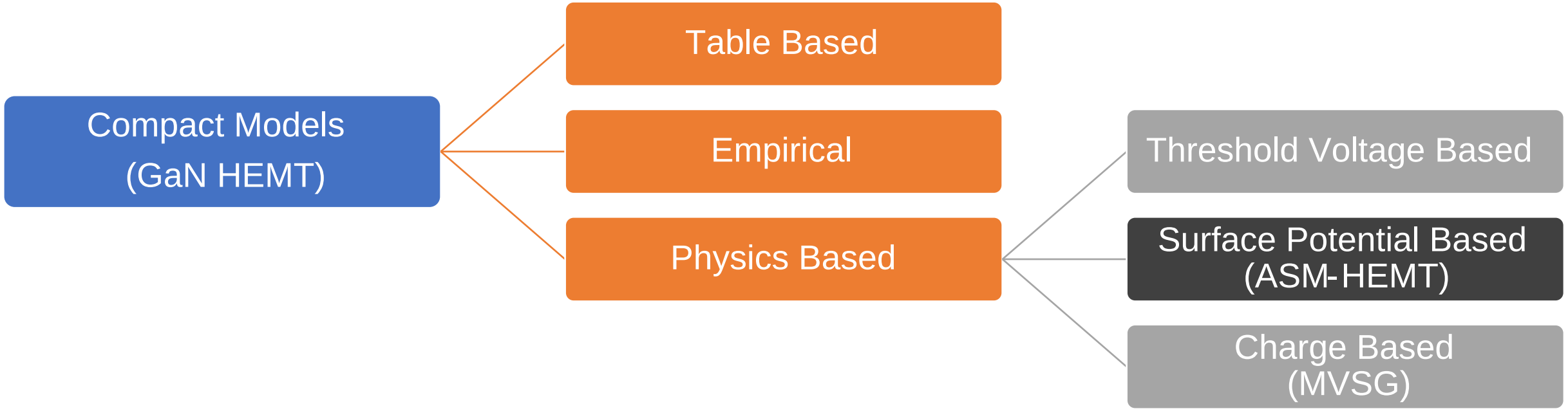
An introduction to ASM -HEMT

- *About ASM-HEMT and its core*
- *Extraction flow*
- *Other models incorporated into the core*
- *Geometric Scaling*

A brief history of HEMT models

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

Various classes of compact models



Advanced **S**PICE **M**odel for GaN **HEMT**s (**ASM-HEMT**)

www.iitk.ac.in/ asm

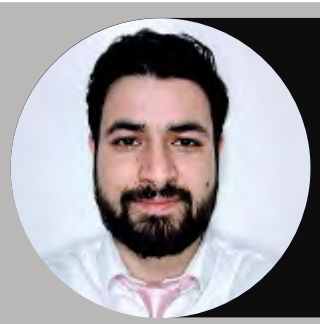
ASM-HEMT Team

Directors

Prof. Yogesh Singh Chauhan

Developers

Dr. Sudip Ghosh



Dr. Aamir Ahsan

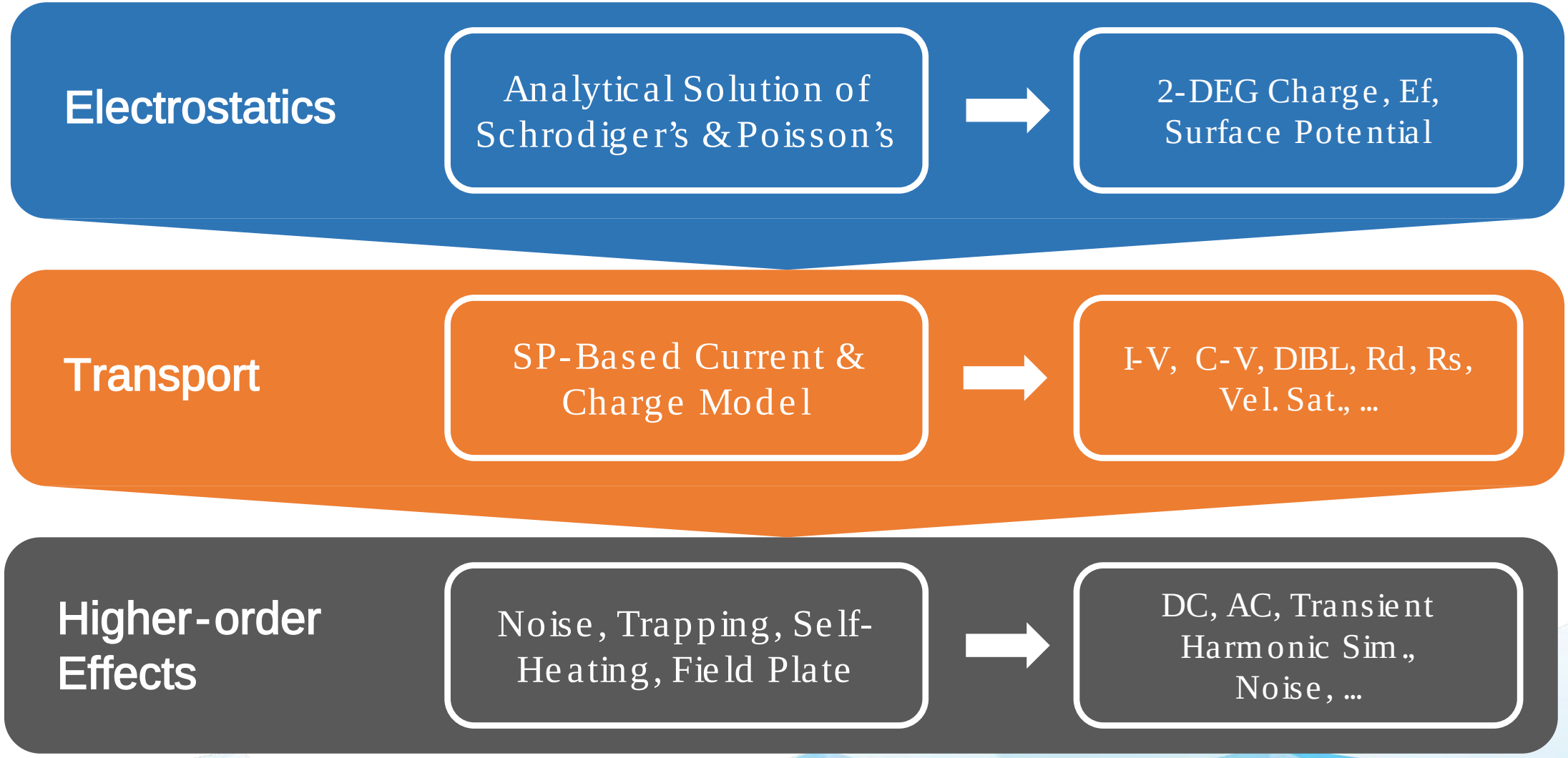
Dr. Avirup Dasgupta

Ahtisham Pampori

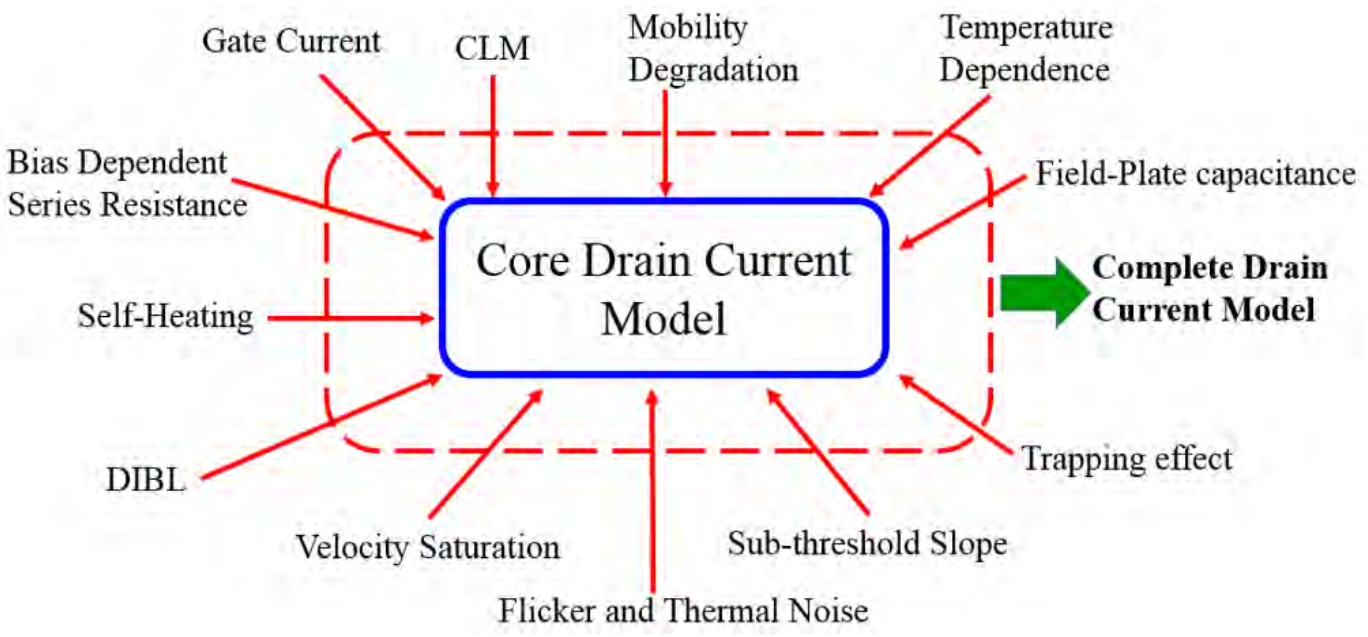
Raghvendra Dangi

Hasnain Ansari

ASM-HEMT: Summary



ASM-HEMT: Core Model



Real Device Effects Incorporated into the Model

Core Model Parameters

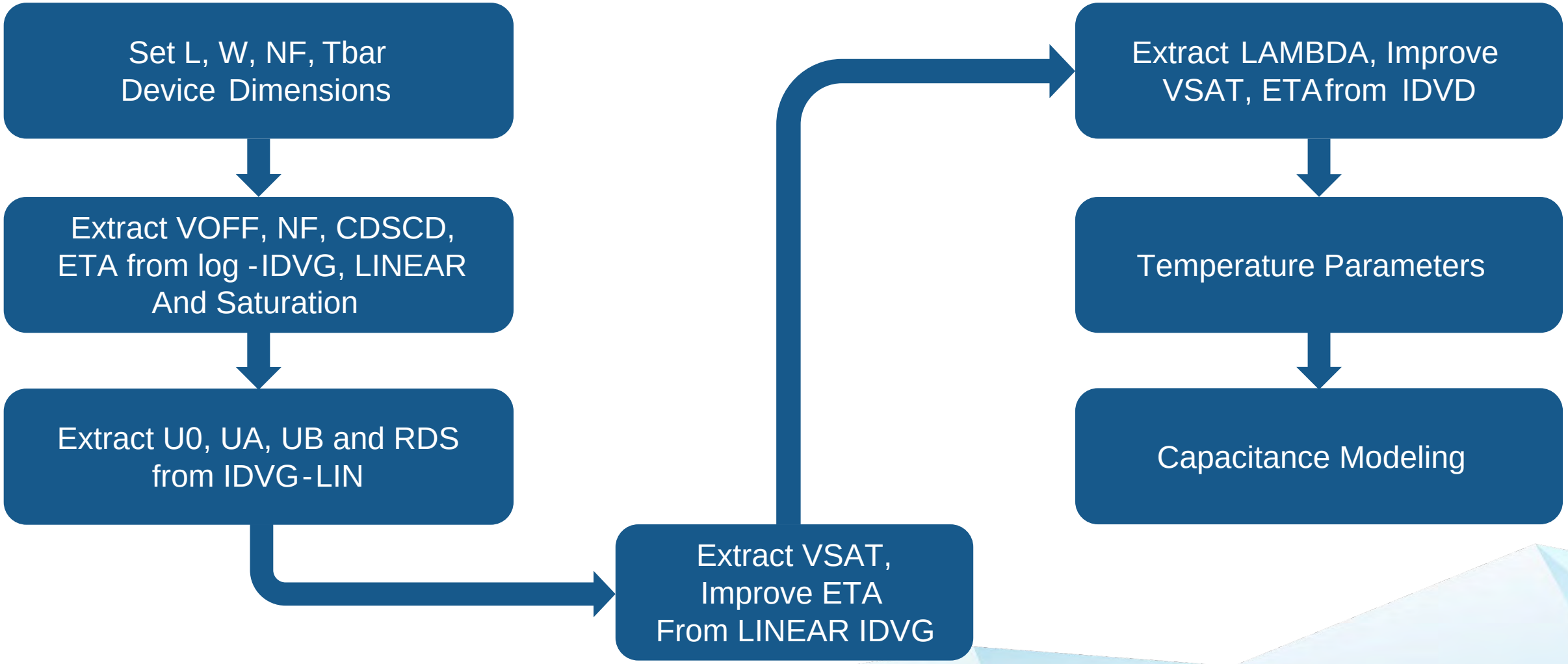
Parameter	Description	Extracted Value
V_{OFF}	Cutoff Voltage	$-2.86\ V$
N_{FACTOR}	Subthreshold Slope Factor	0.202
C_{DSCD}	SS Degradation Factor	$0.325\ V^{-1}$
η_0	DIBL Parameter	0.117
U_0	Low Field Mobility	$33.29\ mm^2/Vs$
N_{S0ACCS}	AR 2DEG Density	$1.9e+17\ /m^2$
$V_{SATACCS}$	AR saturation velocity	$157.6e+3\ cm/s$
R_{TH0}	Thermal Resistance	$22\ \Omega$

Core drain current expression

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}}\frac{W}{L}C_g N_f\left[V_{go} - \left(\frac{\psi_s+\psi_d}{2}\right) + V_{th}\right]\times\psi_{ds}$$

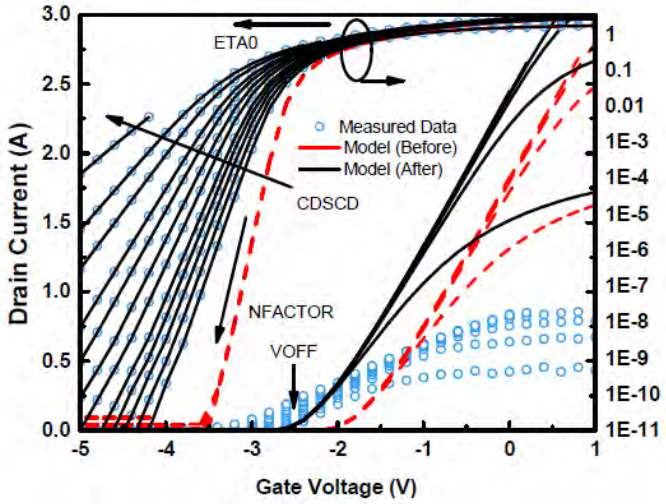
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Extraction Flow I

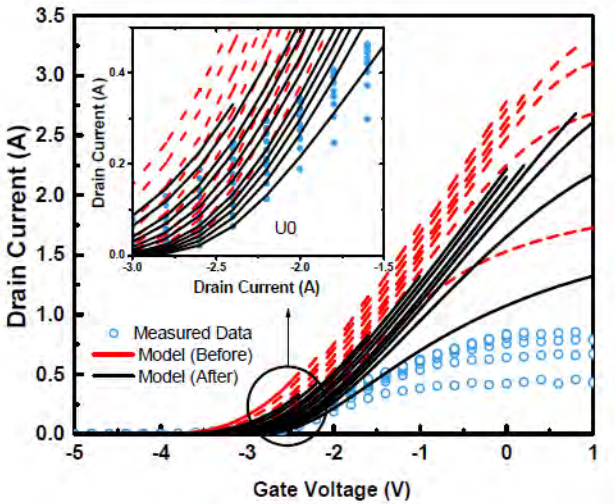


[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

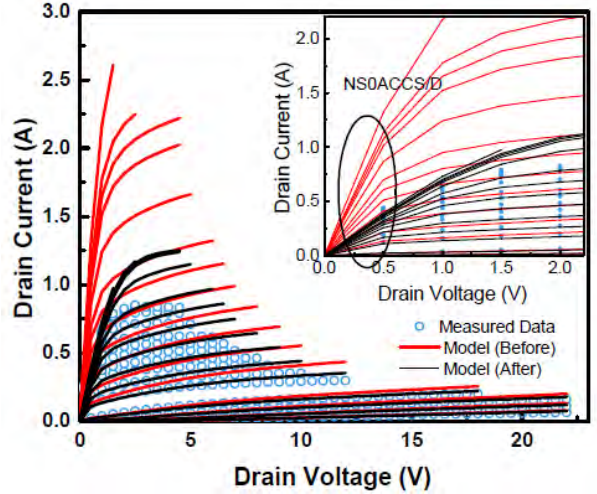
Extraction Flow II



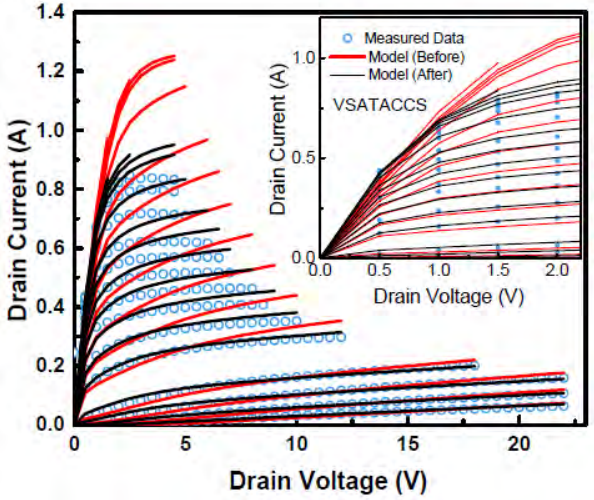
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



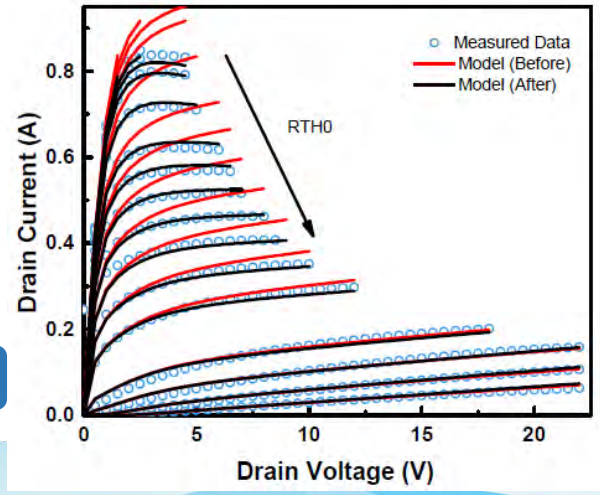
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



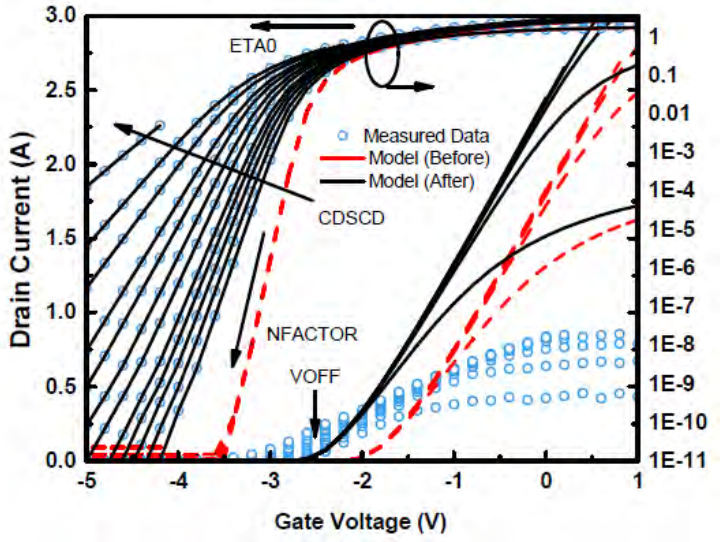
$I_d - V_d$ (Extract $V_{SATACCS}$)

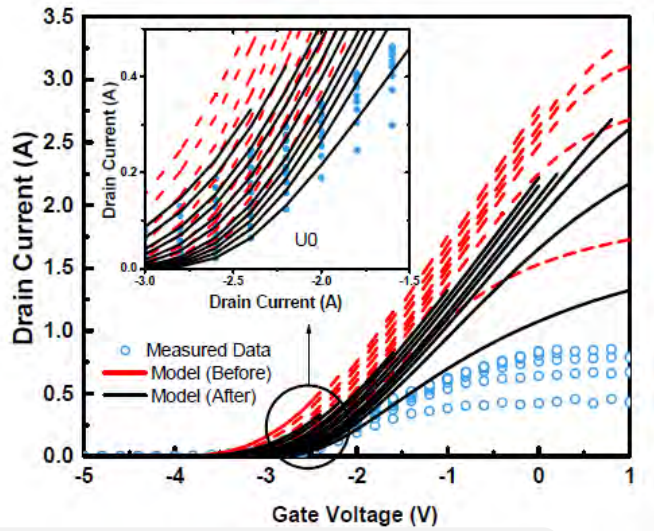


$I_d - V_d$ (Extract R_{TH0})

[1] S. A. Ahsan, *et al*, *MOS-AK Workshop*, Shanghai, [2016]

Extraction from Id - Vg curves





Start with $I_d - V_g$ characteristics in the log scale

ETA0 – DIBL Parameter

NFACTOR – Sub-threshold slope parameter

CDSCD – Captures the drain voltage dependence on the sub-threshold slope.

VOFF – Cut-Off Voltage

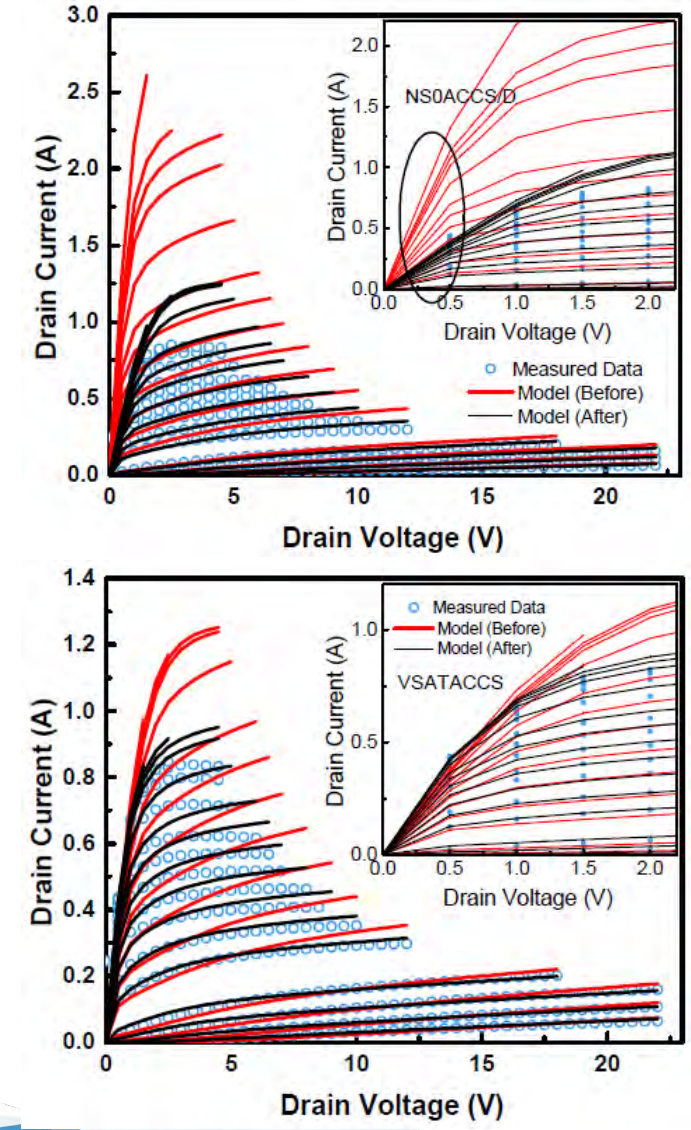
$I_d - V_g$ characteristics in the linear scale

U0 – Low field mobility

UA, UB – Mobility degradation parameters

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Extraction from Id - Vd curves



$I_d - V_d$ characteristics

$\boldsymbol{VSAT}$ – Velocity saturation parameter

$\boldsymbol{UA},\ \boldsymbol{UB}$ – Mobility degradation parameters

Access Region Parameters extracted from $I_d - V_d$ characteristics:

$\boldsymbol{NS0ACCS(D)}$ – 2DEG density in the access region.

$\boldsymbol{VSATACCS}$ – Saturation velocity in the access region.

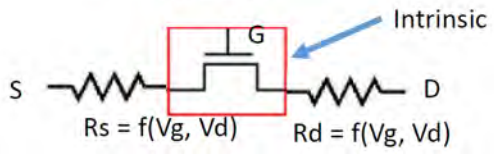
$\boldsymbol{U0ACCS(D)}$ – Low field mobility in the access region.

$\boldsymbol{U0ACCS(D)}$ independently tunes the access region resistance around Vds = 0 and helps extract g_{ds} at that point.

[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Bias-dependent access region resistance model: Overview

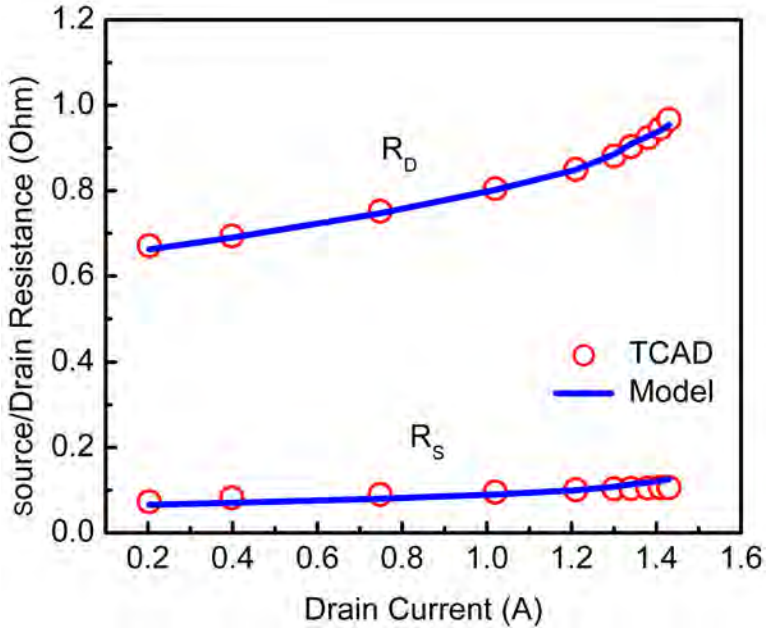
$$R_J = \frac{L_J}{q\mu_n n_{s0}} \qquad J = S, D$$



$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R/V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$\mathrm{I_{ds,acc}} = \frac{\mathrm{R_c}}{\mathrm{W \cdot N_f}} + \frac{\mathrm{L_{acc}}}{\mathrm{W \cdot N_f \cdot q \cdot N_{S0ACCS} \cdot U_{0ACCS}}} \times \left(1 - \left(\frac{\mathrm{I_{ds}}}{\mathrm{W \cdot N_f \cdot N_{S0ACCS} \cdot V_{SATACCS}}}\right)^2\right)^{-1/2}$$

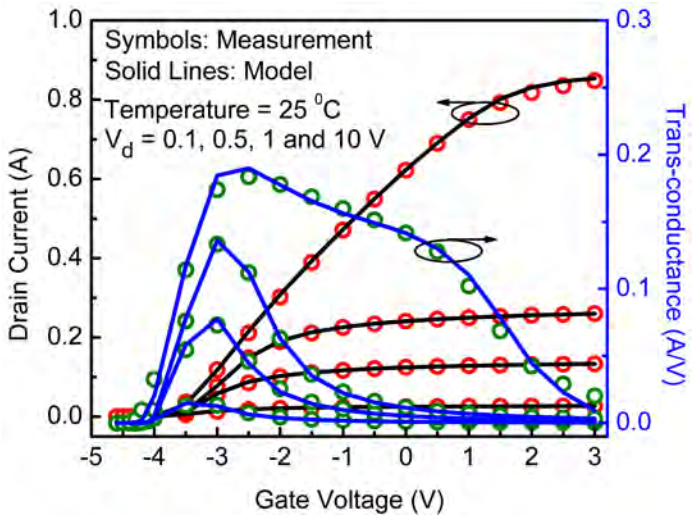


Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

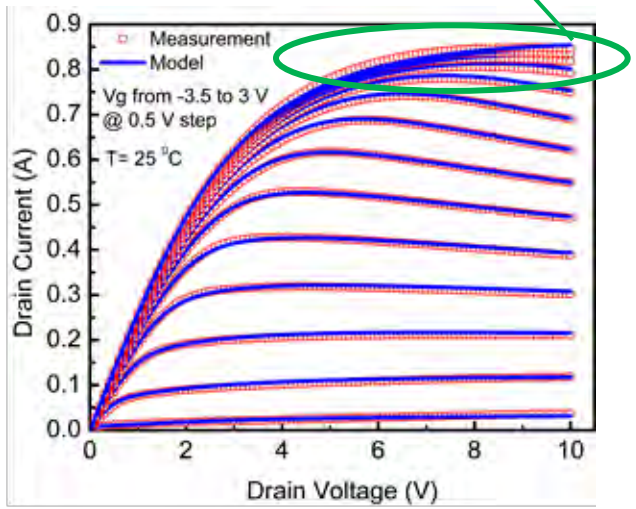
[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

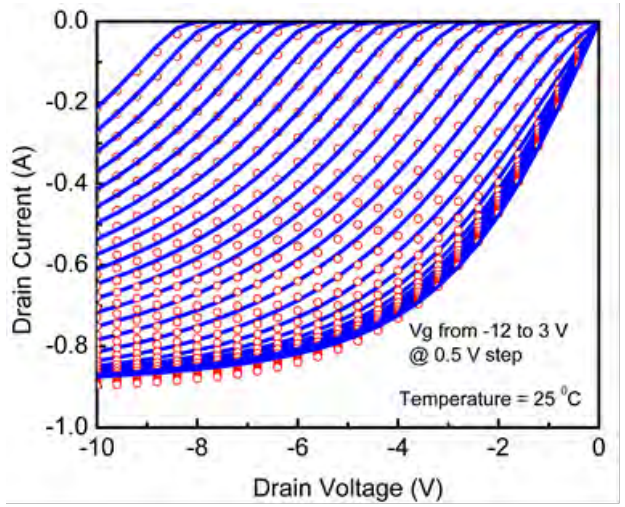
Bias-dependent access region resistance model: Results

Effect of high access region resistance at high V_g



Id - Vg and trans-conductance for the Toshiba power HEMT. Different slopes above Voff in gm-Vg: self-heating governs the first slope while velocity saturation in access region affects second slope.





Ids-Vds and reverse Ids-Vds fitting with experimental data. The non-linear Rs/d model shows correct behavior for the higher Vg curves in the Id-Vd plot; the S-P based model can accurately capture the reverse output characteristics.

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

Bias-dependent access region resistance model: Temperature scaling

The temperature dependence of $R_{d/s}$ model is extremely important as it increases significantly with increasing temperature

Temperature dependence of 2 -DEG charge density in the drain or source side access region:

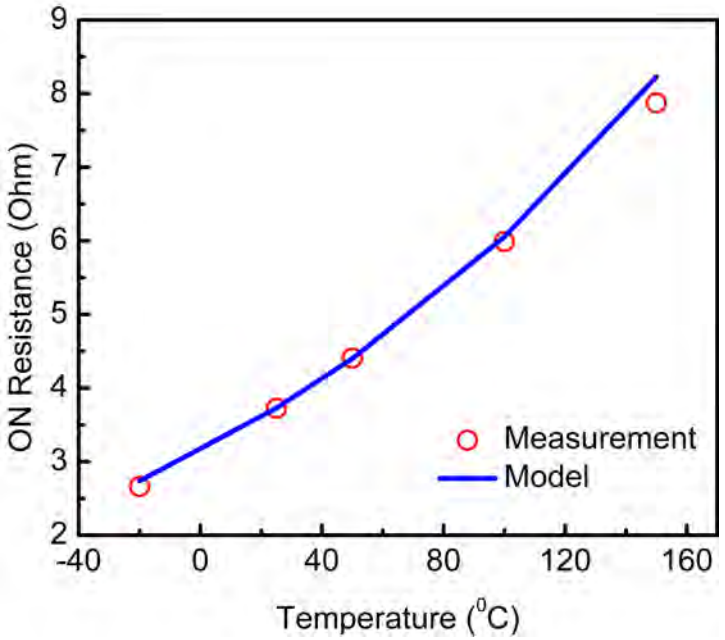
$$n_{s0}(T) = NS0ACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

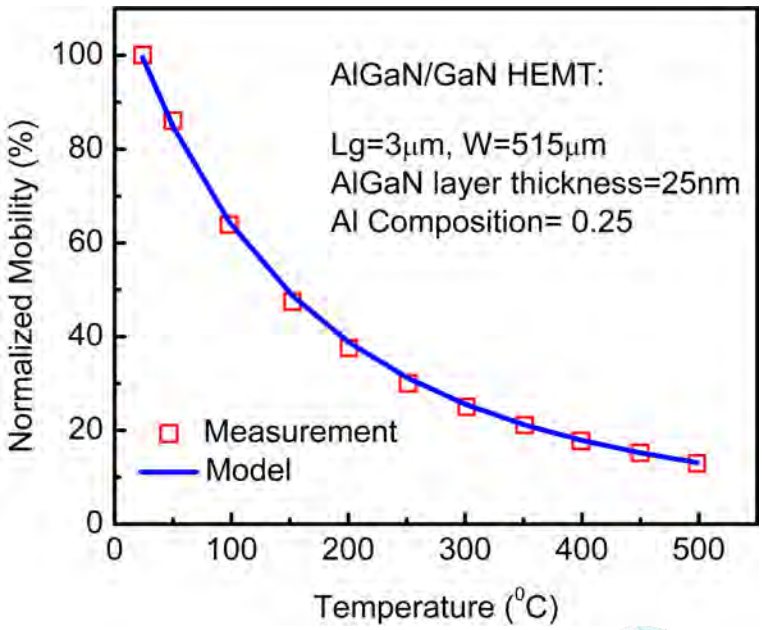
Temperature dependence of Saturation Velocity:

$$V_{sat}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

Temperature dependence of electron Mobility:

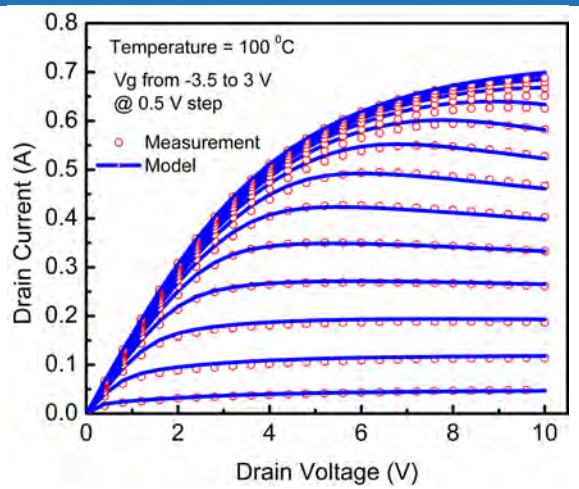
$$\mu_{acc}(T) = U0ACC \cdot \left(\frac{T}{TNOM}\right)^{UTEACC}$$



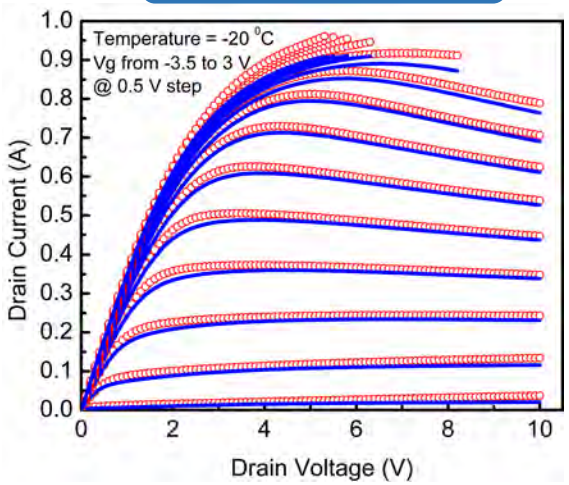


[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

ASM-HEMT: Temperature scaling results



Id - Vd at 100℃



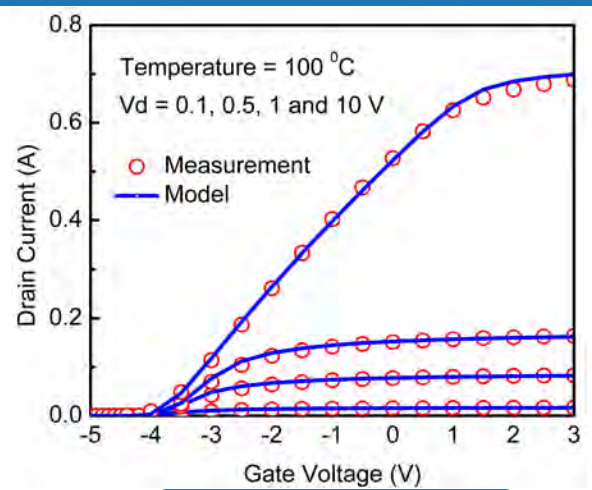
Id - Vd at -20℃

ASM-HEMT features a robust temperature scaling model which has been validated across a broad range of device temperatures.

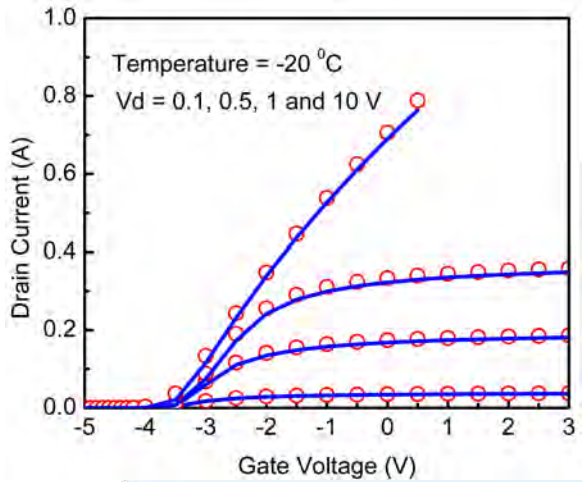
$$V_{off,DIBL}(T) = V_{off,DIBL} - \left(\frac{T_{dev}}{T_{NOM}} - 1\right) \cdot \boldsymbol{KT1} + TRAPVOFF \cdot vcap + voff_{trap}$$

$$U0(T) = U0 \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{UTE}}$$

$$VSAT(T) = VSAT \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{AT}}$$



Id - Vg at 100℃



Id - Vg at -20℃

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

Geometric Scaling I

Charge Scaling

$$Q_g = \frac{C_g LW}{V_{g0} - \psi_m + V_{tv}}[V_{g0}^2 + \frac{1}{3}(\psi_d^2 + \psi_s^2 + \psi_d\psi_s) - V_{g0}(\psi_d + \psi_s - V_{tv}) - V_{tv}\psi_m]$$

$$Q_d = -\frac{C_g LW}{120(V_{g0} - \psi_m + V_{tv})^2}[12\psi_d^3 + 8\psi_s^3 + \psi_s^2(16\psi_d - 5(V_{tv} + 8V_{g0}))$$
$$+2\psi_s(12\psi_d^2 - 5\psi_d(5V_{tv} + 8V_{g0}) + 10(V_{tv} + V_{g0})(V_{tv} + 4V_{g0}))$$
$$+15\psi_d^2(3V_{tv} + 4V_{g0}) - 60V_{g0}(V_{tv} + V_{g0})^2$$
$$+20\psi_d(V_{tv} + V_{g0})(2V_{tv} + 5V_{g0})]$$

Current Scaling

$$I_d = \frac{W}{L}\mu C_g(V_g0 - \psi_m + V_{th})\psi_{ds}$$

Where $\psi_m = (\psi_d + \psi_s)/2$, $\psi_ds = (\psi_d - \psi_s)$

Access Region Resistance Scaling

$$R_{source} = \frac{RSC(T)}{W \cdot NF} + TRAPRS \cdot vcap + \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS(T) \cdot U0ACCS(T)} \cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCS}\right)^{\frac{-1}{MEXPACCS}}$$

where

$$I_{sat,source} = W \cdot NF \cdot NS0ACCS(T) \cdot VSATACCS(T)$$

$$R_{drain} = \frac{RDC(T)}{W \cdot NF} + TRAPRD \cdot vcap + R_{trap}(T) + ron_{trap} + \frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD(T) \cdot U0ACCD(T)} \cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCD}\right)^{\frac{-1}{MEXPACCD}}$$

where $I_{sat,drain} = W \cdot NF \cdot NS0ACCD(T) \cdot VSATACCS(T)$

Geometric Scaling II

Thermal Noise and Flicker Noise Scaling

$$S_{if}(f) = \frac{k_B T}{W L^2 f^{EF}} \frac{I_{DS}^2 K_r}{C_g^2} \left[NOIA V_{th} C_g \left(\frac{1}{Q_{ch,d}} - \frac{1}{Q_{ch,s}} \right) + (NOIA + NOIB V_{th} C_g) ln \left(\frac{Q_{ch,d}}{Q_{ch,s}} \right) + (NOIB + NOIC V_{th} C_g)(-Q_{ch,d} + Q_{ch,s}) + \frac{NOIC}{2} (Q_{ch,d}^2 - Q_{ch,s}^2) \right]$$

$$S_{it} = \frac{4 k_B T_{dev}}{I_D L_{eff}^2} (\mu_{eff,sat} W q C_g)^2 \left(V_{go}^2 \psi_{ds} + \frac{\psi_d^3 - \psi_s^3}{3} - V_{go} (\psi_d^2 - \psi_s^2) \right)$$

Gate Current Scaling

$$I_{gs} = W \cdot L \cdot NF \cdot \left[IGSDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[exp\left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

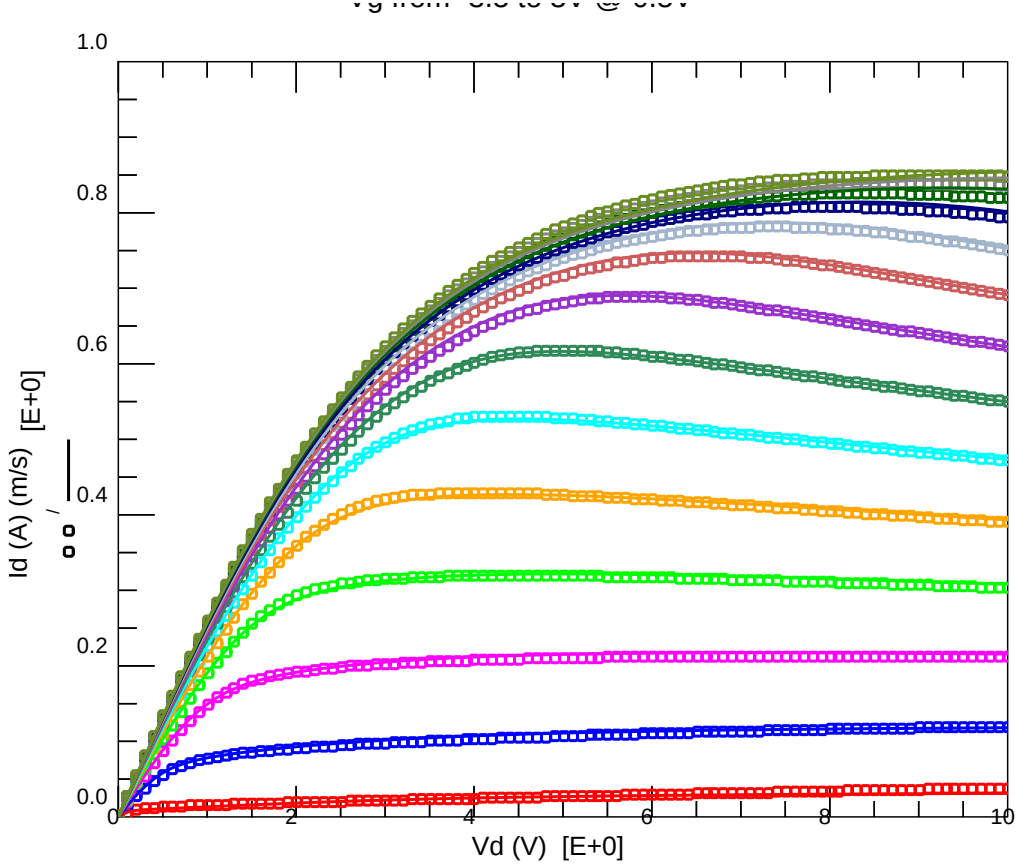
$$I_{gd} = W \cdot L \cdot NF \cdot \left[IGDDIO + \left(\frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGD \right] \left[exp\left\{ \frac{V_{gd}}{NJGD \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

Contents

Modeling Power Devices using ASM - HEMT

- *Modeling DC*
- *Modeling field plates*
- *Model comparison with a mixed mode device*

Modeling DC: Room Temperature Output Characteristics

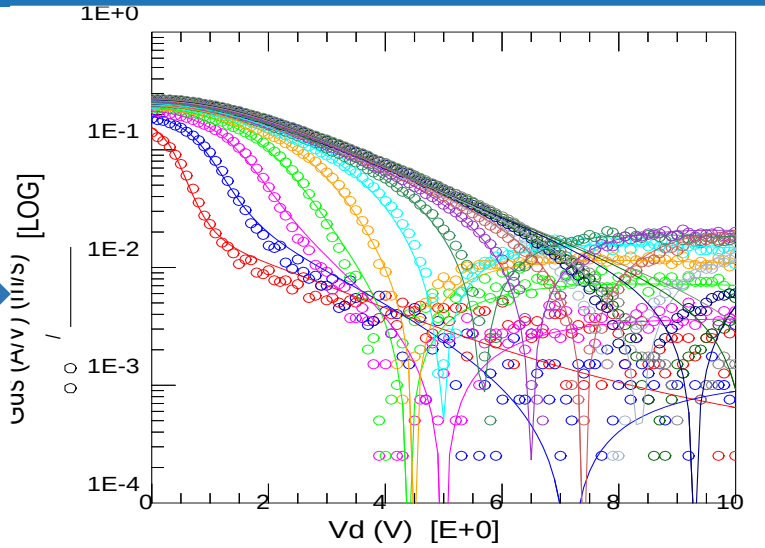


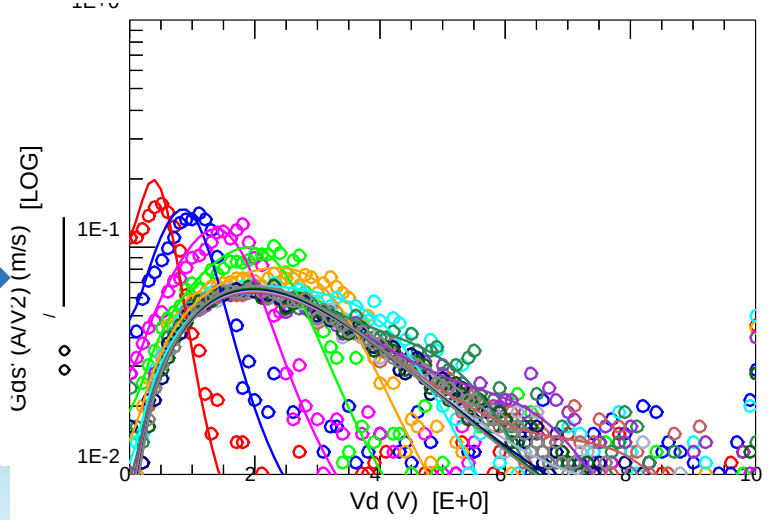
Output Characteristics at T=25 ℃

Output conductance versus Vd

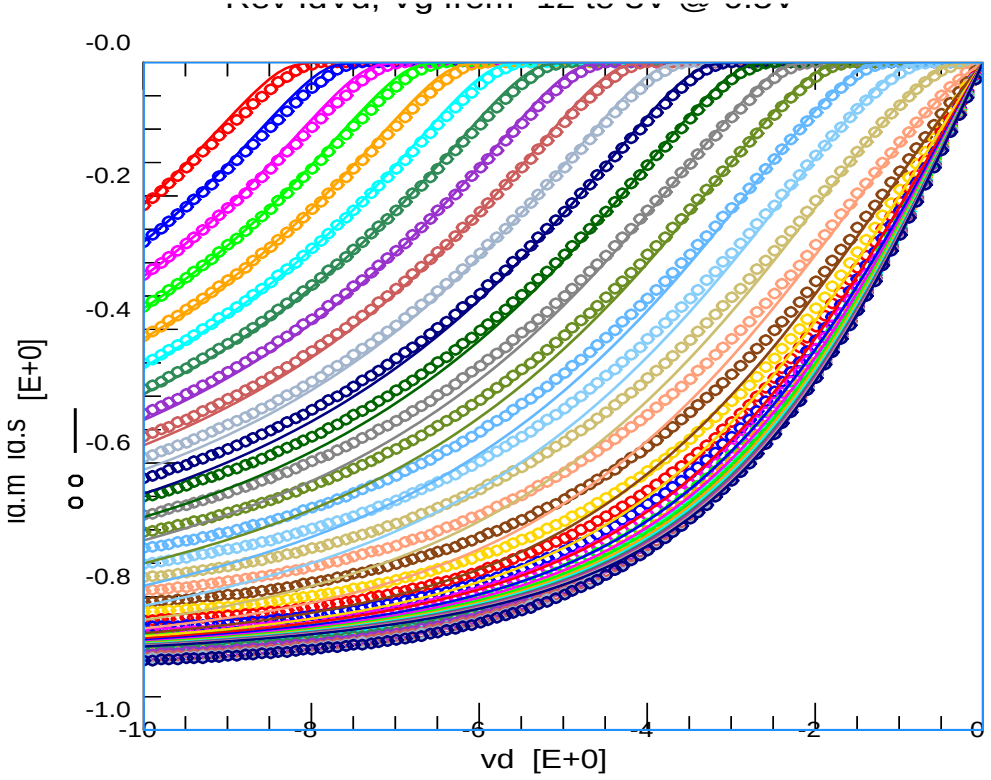
ASM-HEMT accurately captures the IV characteristics of a power GaN HEMT device.

Derivative of output conductance versus Vd



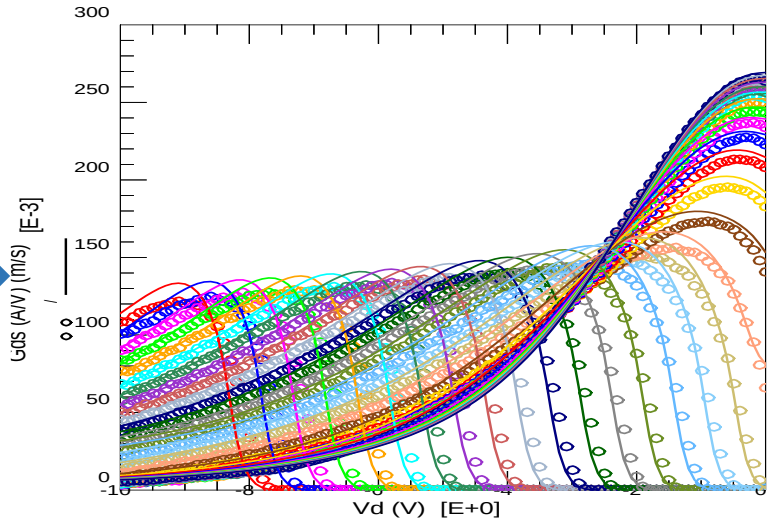


Modeling DC: Room Temperature Reverse Output Characteristics

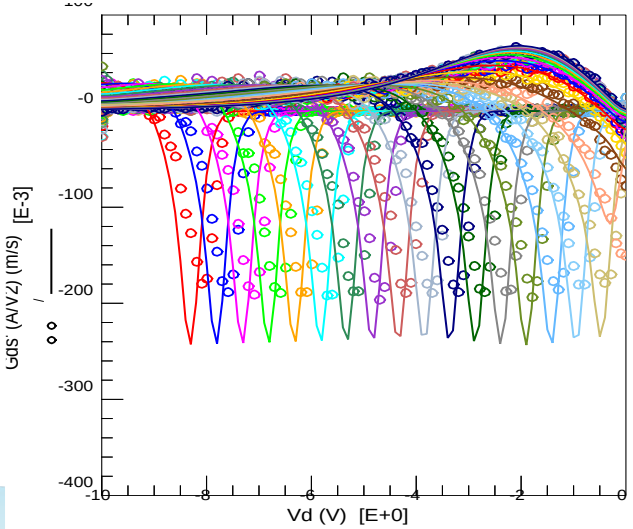


Reverse Output Characteristics at T=25℃

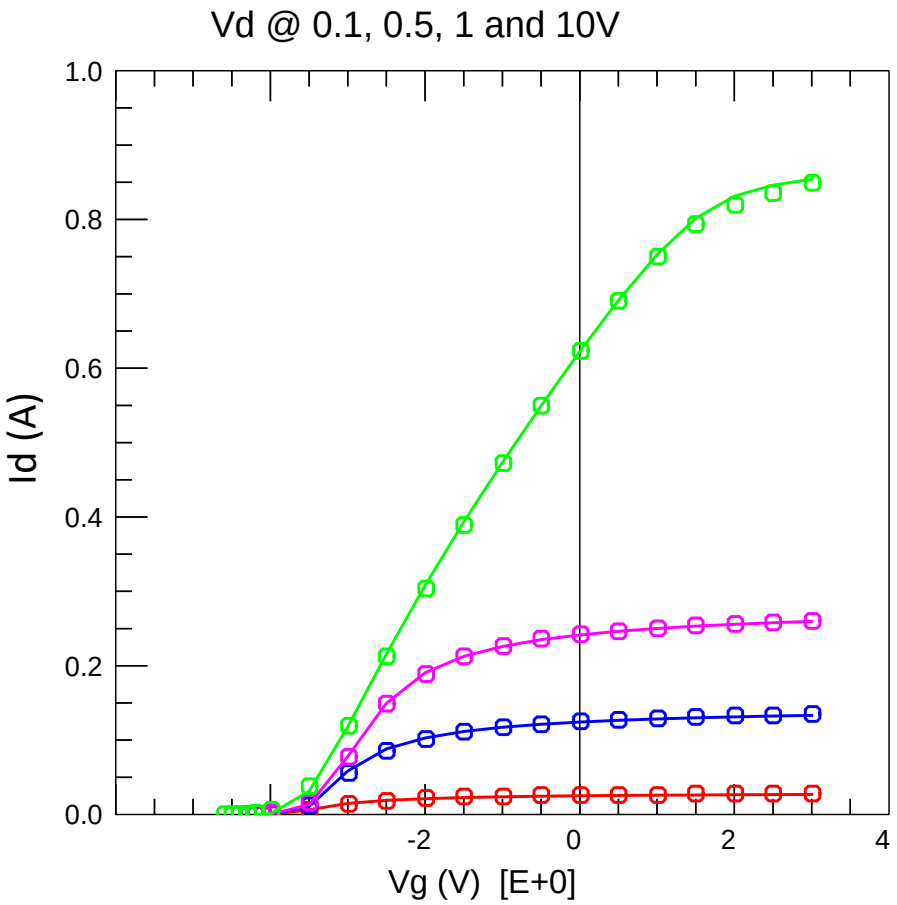
Reverse Output conductance versus Vd



Derivative of reverse output conductance versus Vd

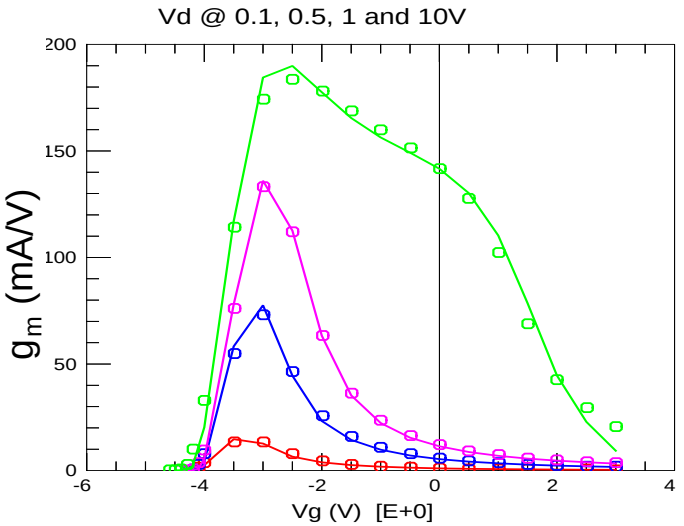


Modeling DC: Room Temperature Transfer Characteristics

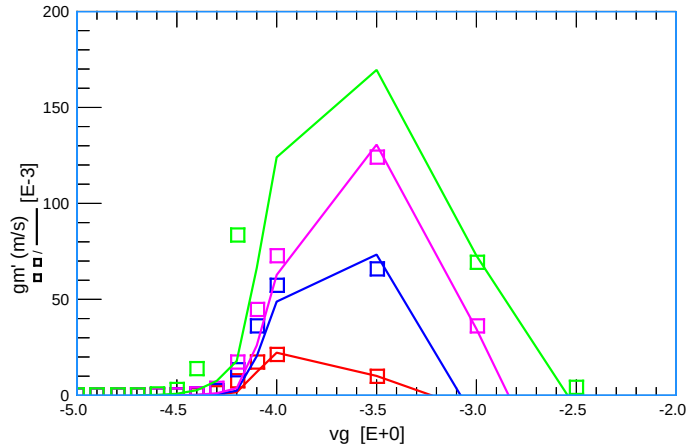


Transfer Characteristics at T=25℃

Transconductance versus Vg

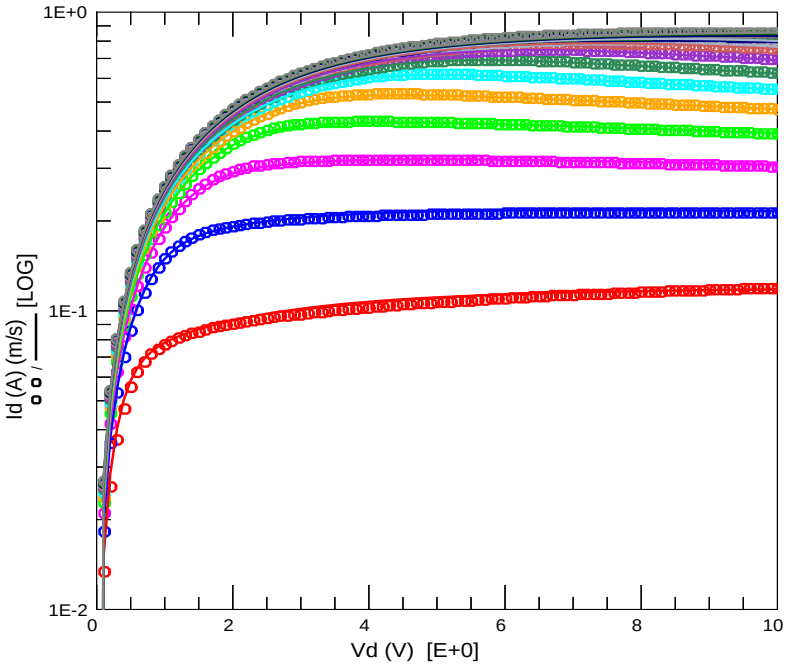


Derivative of transconductance versus Vg

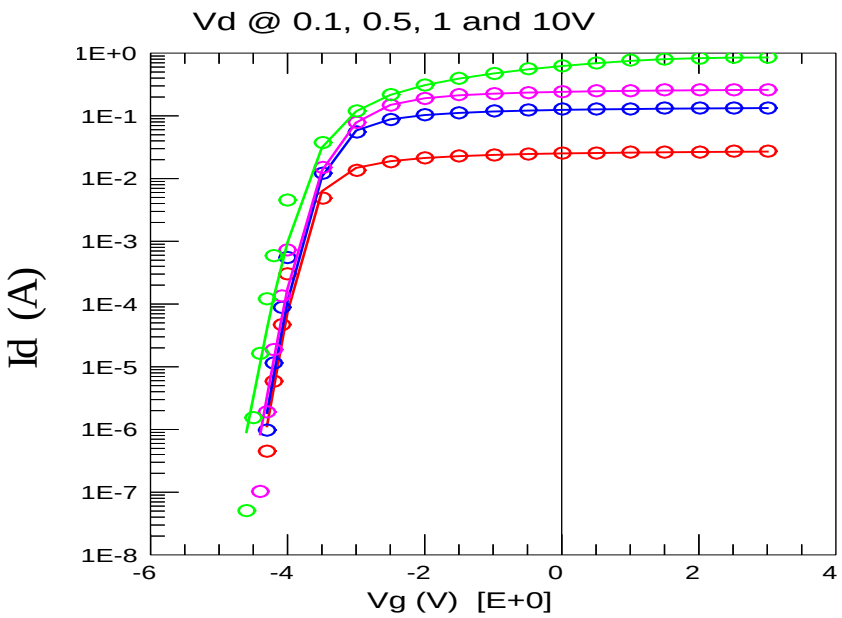


Modeling DC: Room Temperature IV – Log Scale

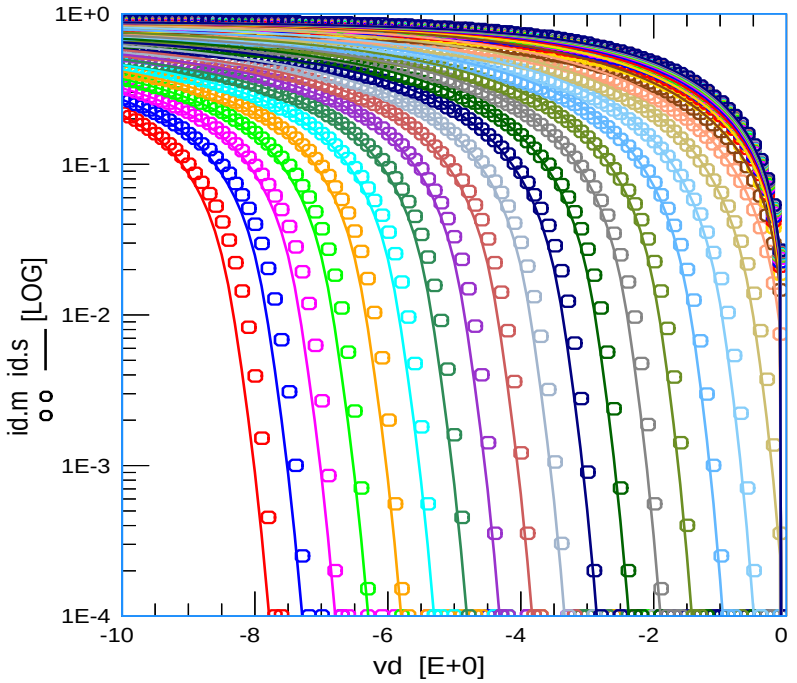
Log (Id) - Vds (Vd>0) T=25℃



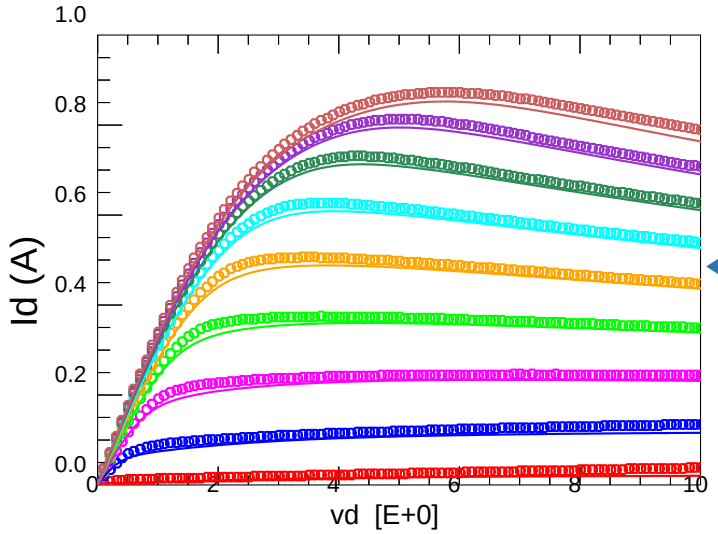
Log (Id) - Vgs T=25℃



Log (Id) - Vds (Vd<0) T=25℃

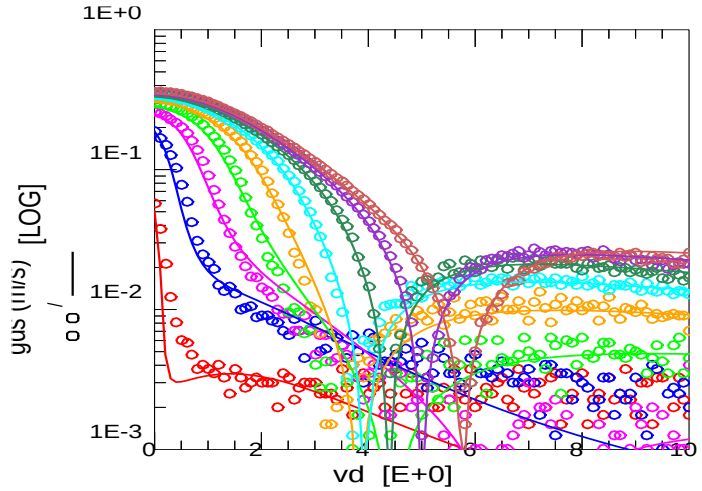


Modeling DC: Output Characteristics @ T=-20℃

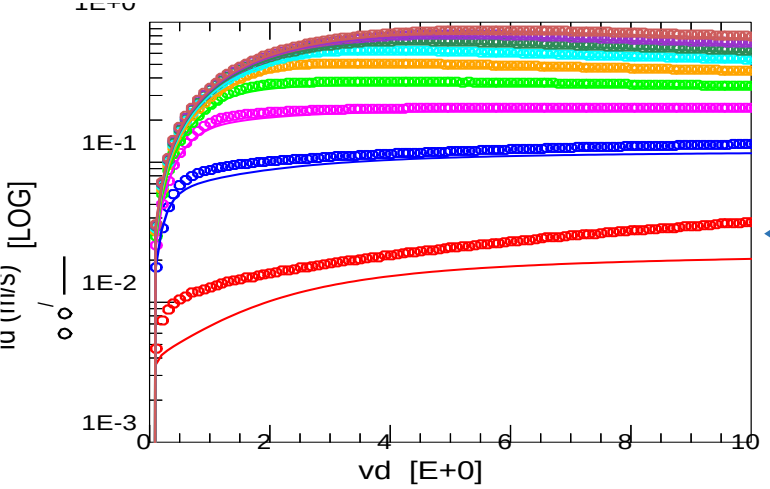


Output Characteristics @-20℃

Output conductance versus Vd @-20℃

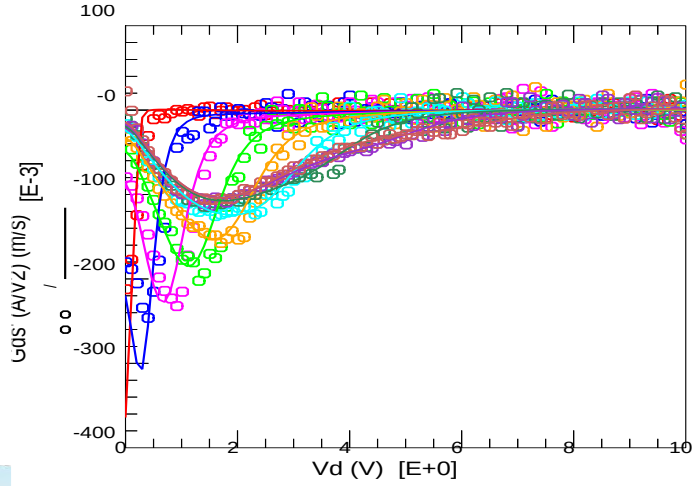


The model scales accurately to sub-zero temperatures.

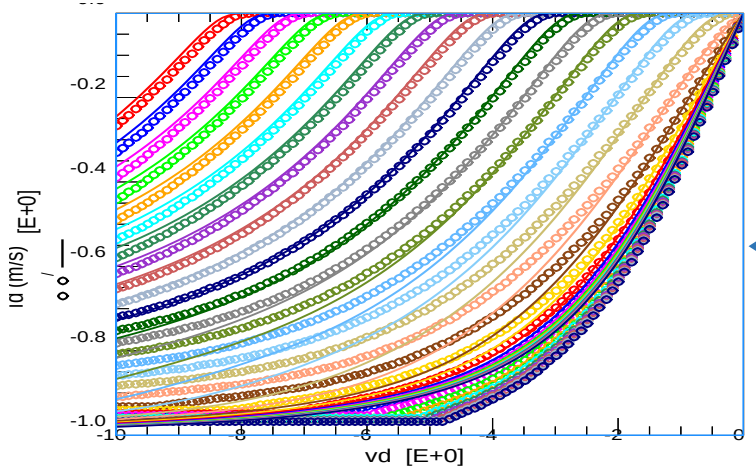


Log Output Characteristics @-20℃

Derivative of output conductance versus Vd @-20℃



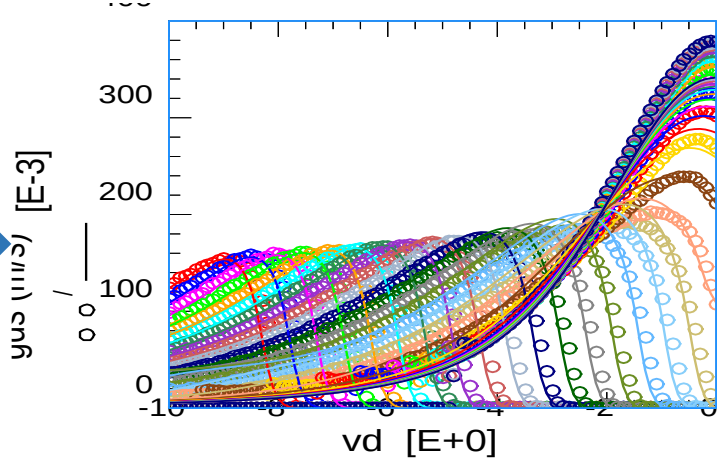
Modeling DC: Reverse Output Characteristics @ T=-20℃



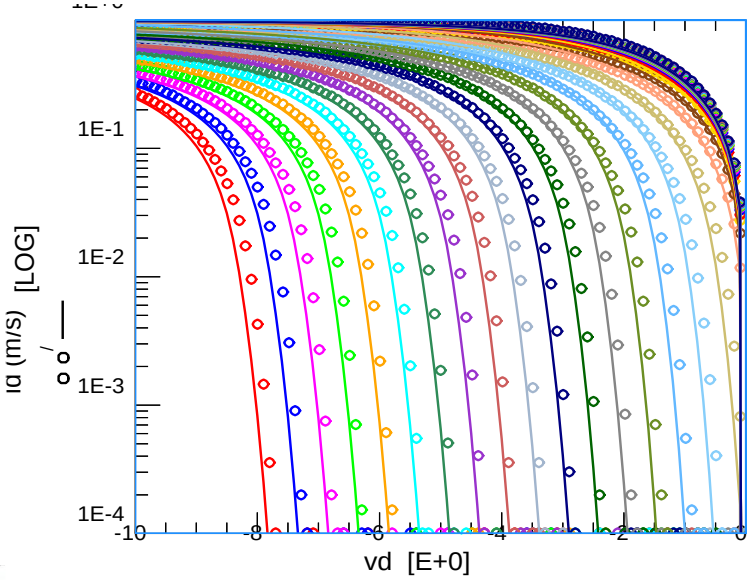
Vg from -12 to 3 V @ 0.5V step

Reverse Output Characteristics @-20℃

Reverse Output conductance versus Vd @-20℃

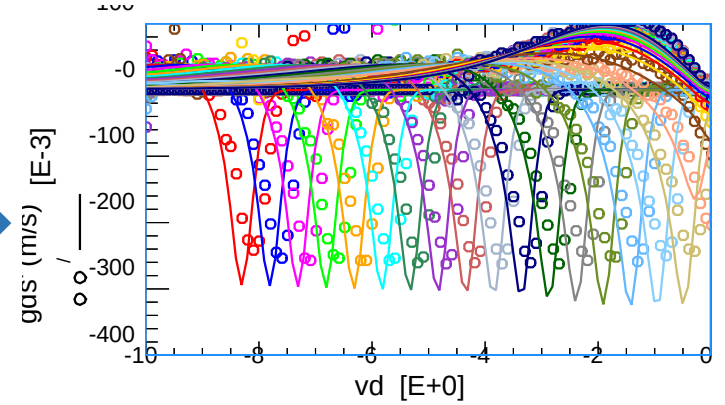


The model scales accurately to sub-zero temperatures.



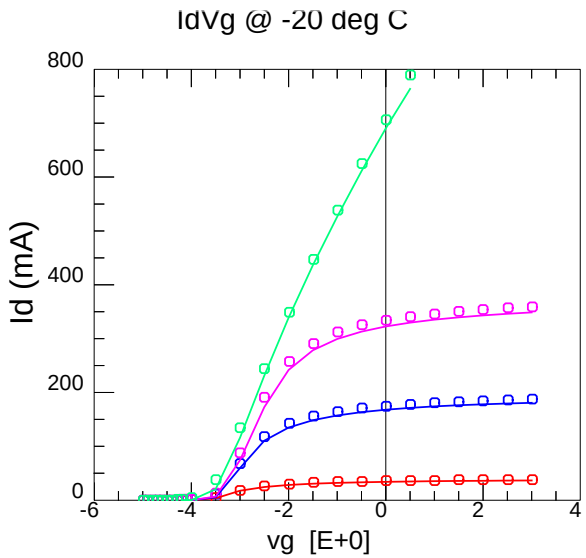
Log Output Characteristics @-20℃

Derivative of reverse output conductance versus Vd @-20℃

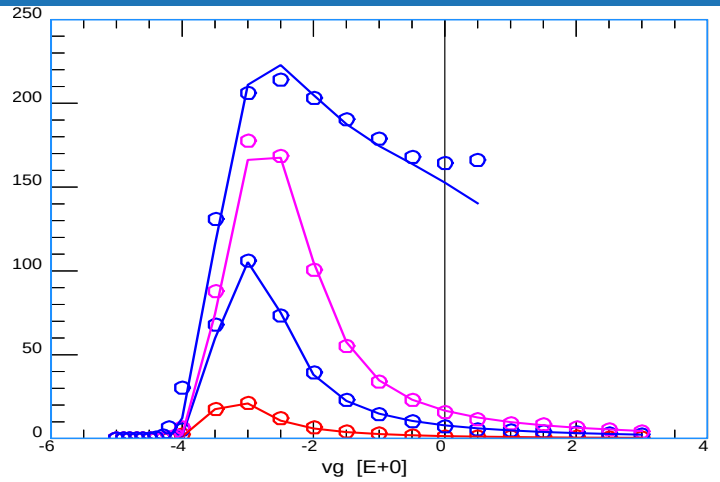


Modeling DC: Transfer Characteristics @ T=-20℃

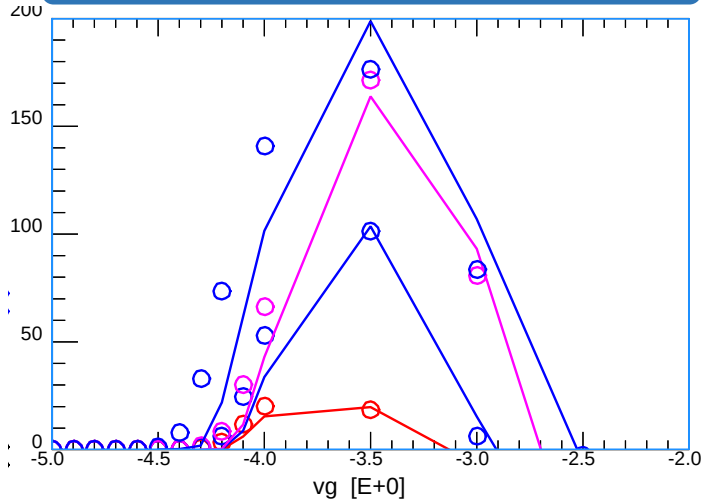
The model scales accurately to sub-zero temperatures.



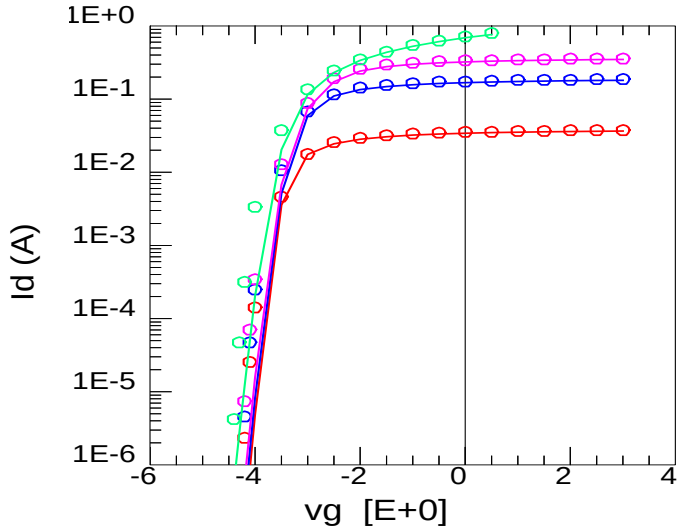
Transfer Characteristics @ T=-20℃



Transconductance @ T=-20℃

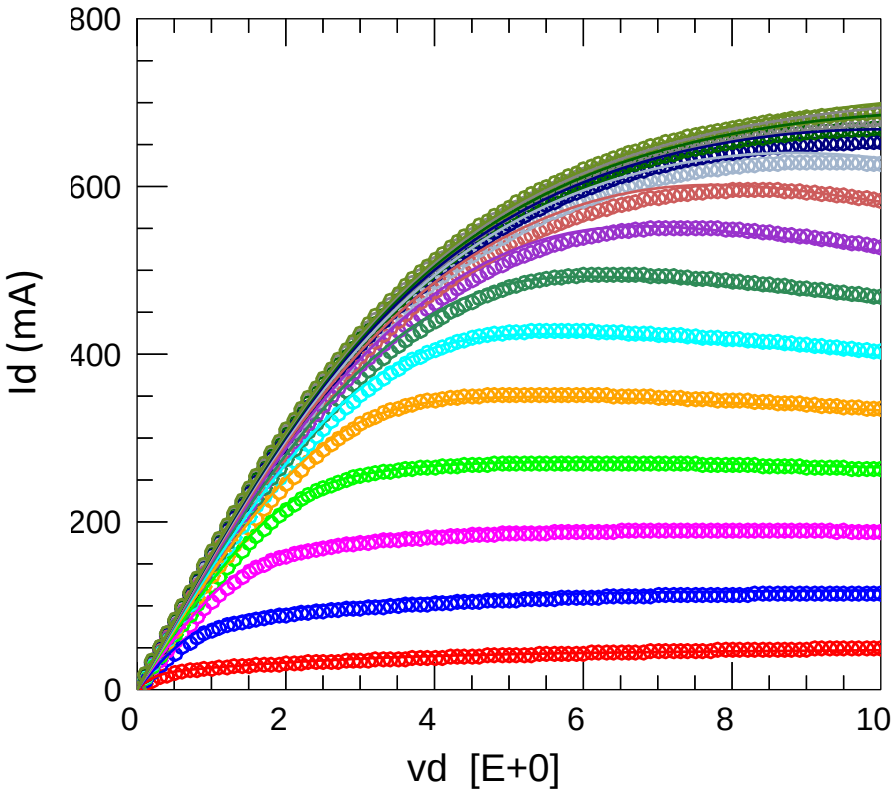


Derivative of Transconductance @ T= -20℃



Transfer Characteristics (Log) @ T=-20℃

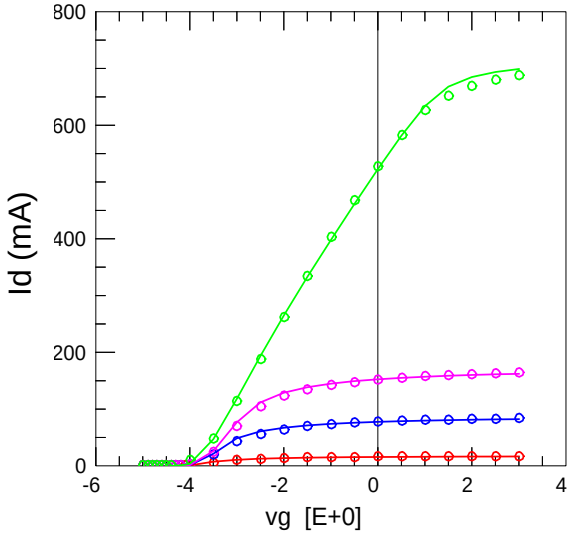
Modeling DC: IV Characteristics @ T=100℃



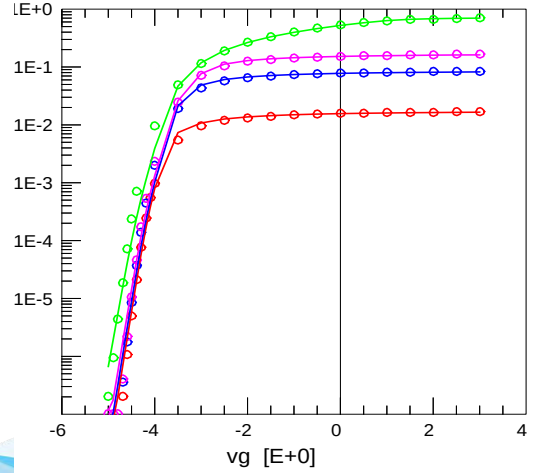
Output Characteristics @ T=100℃

The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.

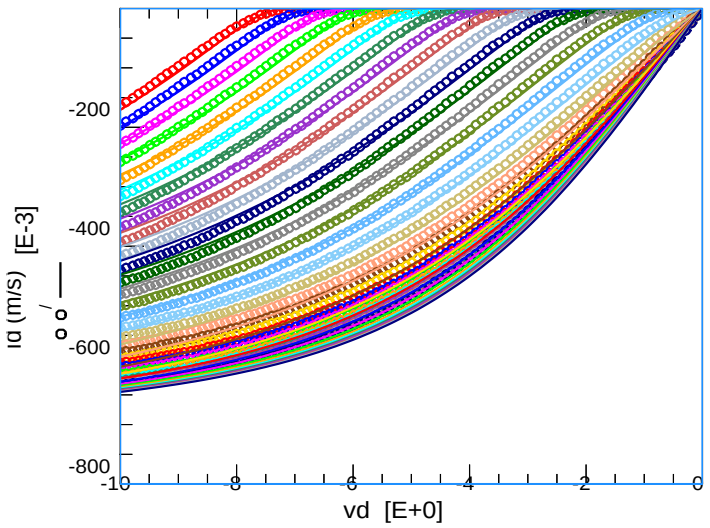
Transfer Characteristics @ T=100℃



Transfer Characteristics (Log) @ T=100℃



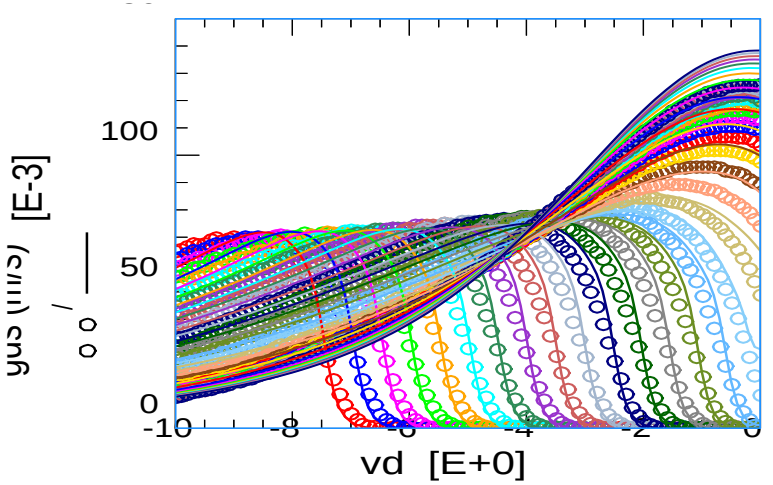
Modeling DC: Reverse Output Characteristics @ T=150℃



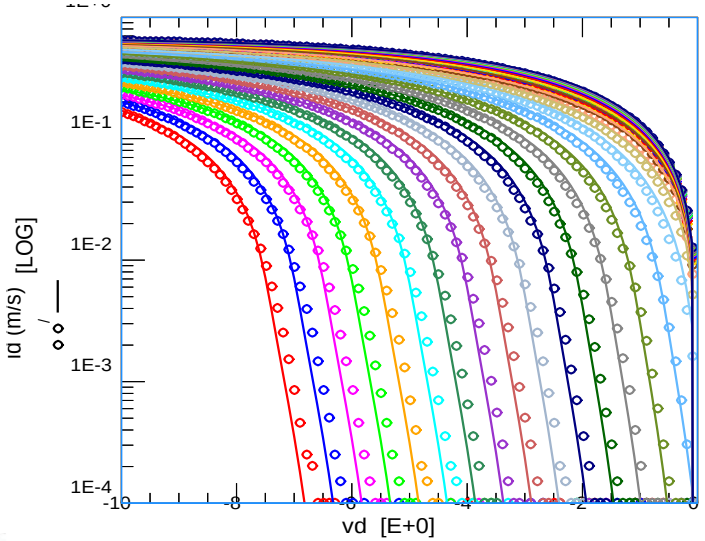
Vg from -12 to 3 V @ 0.5V step

Reverse Output Characteristics @ 150℃

Reverse Output conductance versus Vd @ 150℃

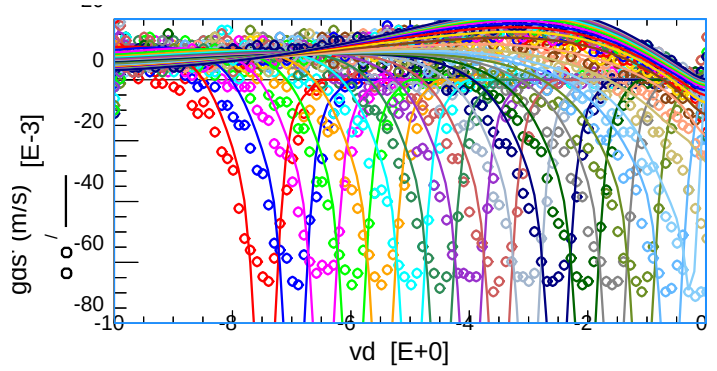


The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.

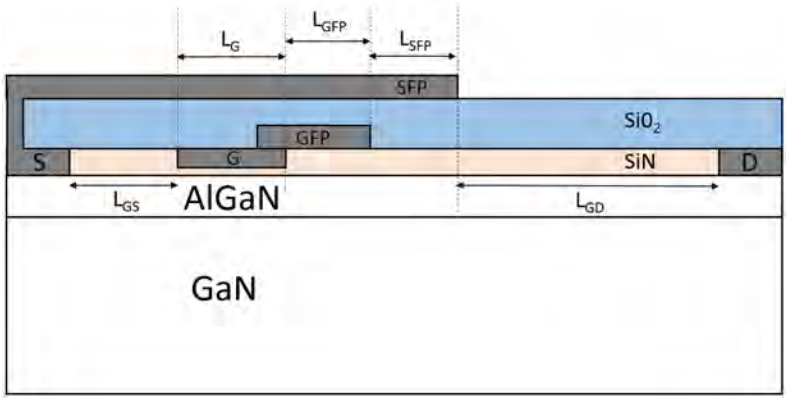


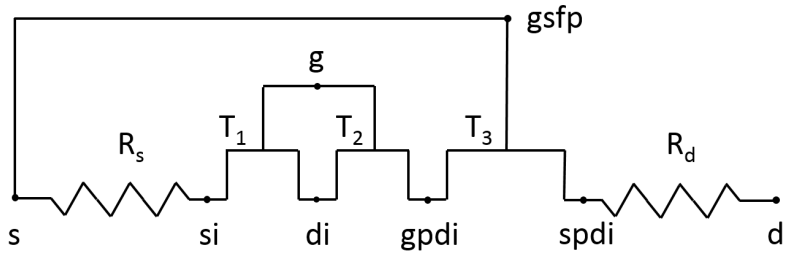
Log Output Characteristics @ 150℃

Derivative of reverse output conductance versus Vd @ 150℃



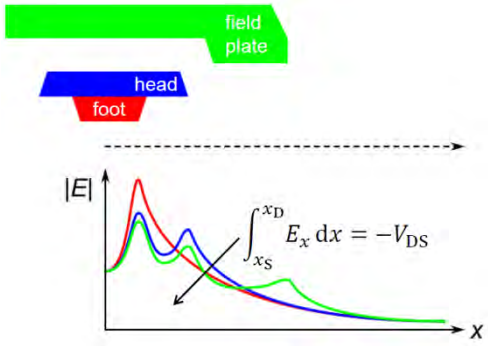
Modeling field plates: Structure

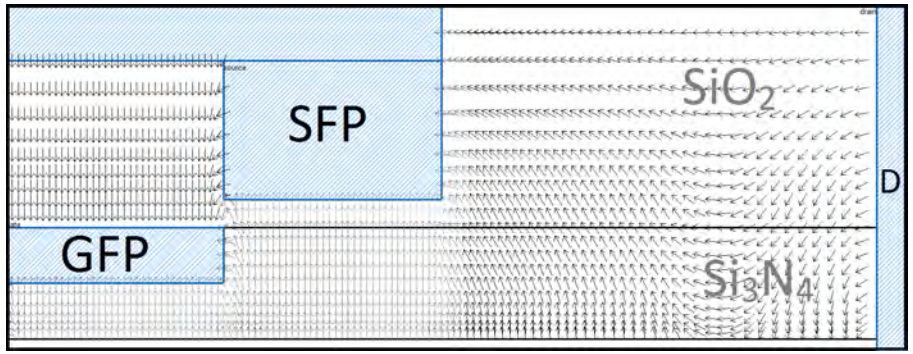




A Gate Field Plate (GFP) and a Source Field Plate (SFP) structure modeled as transistors in series.

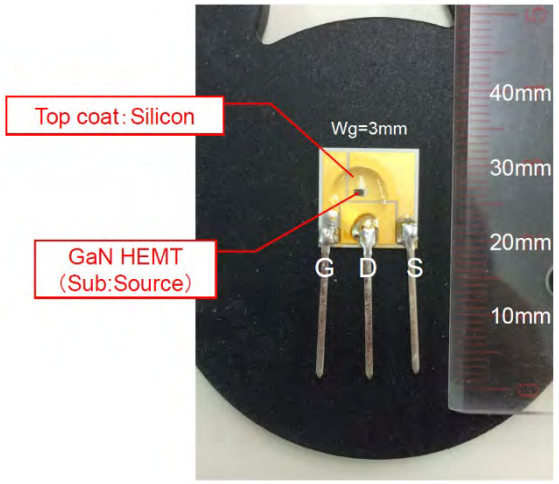
Field plates flatten out the peak in the electric field caused by the sudden drop in potential at the gate edge. TCAD showing field fluctuations leading to a distributed field inside the device.



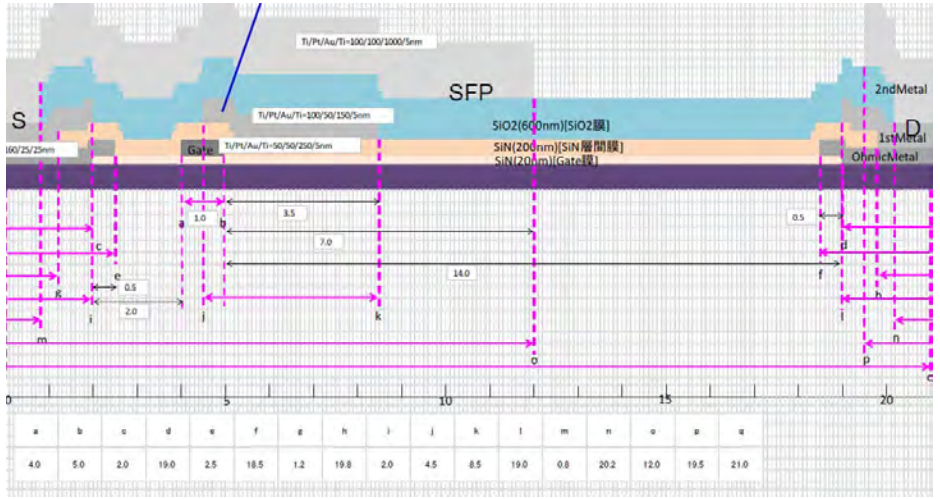


[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

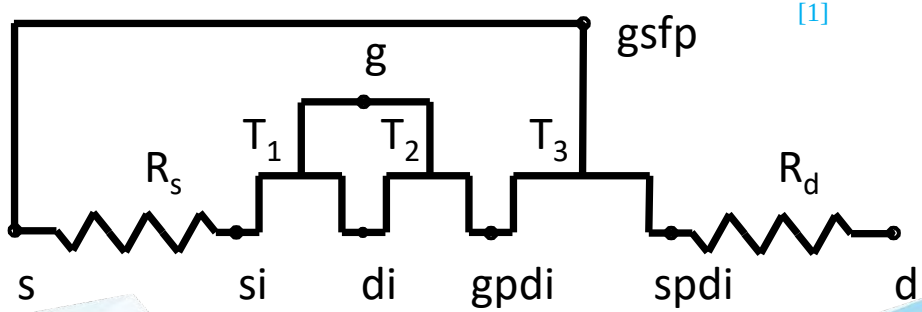
Dual FP GaN HEMT DUT



Picture of the GaN device under test

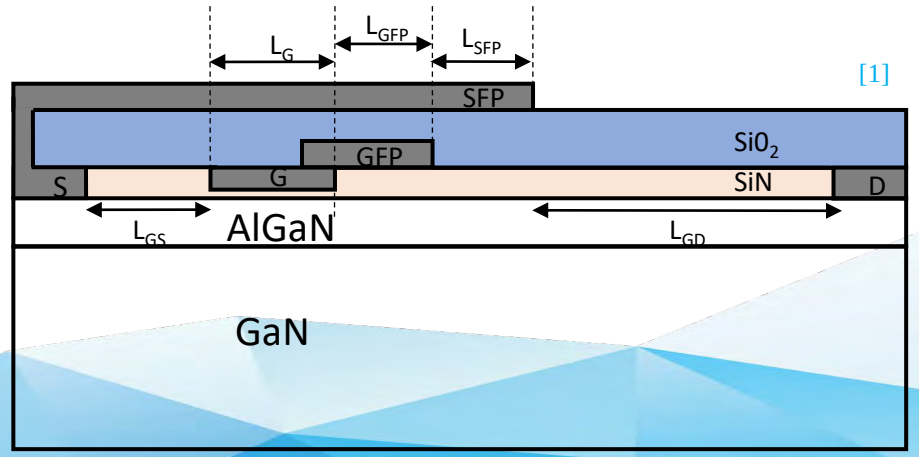


Field-plate configuration as provided by Toshiba



[1]

Model representation of the device

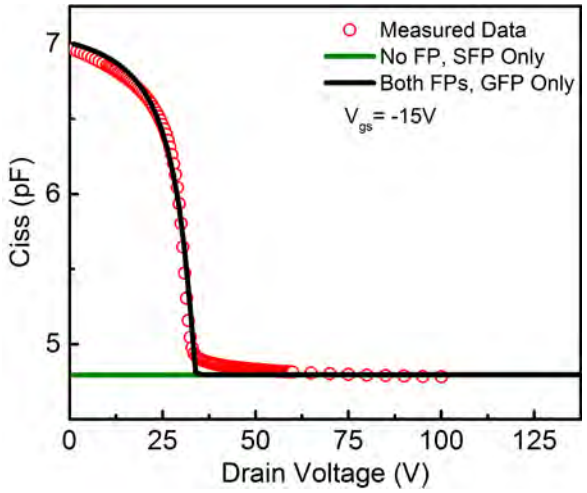


[1]

Schematic of the dual FP GaN device

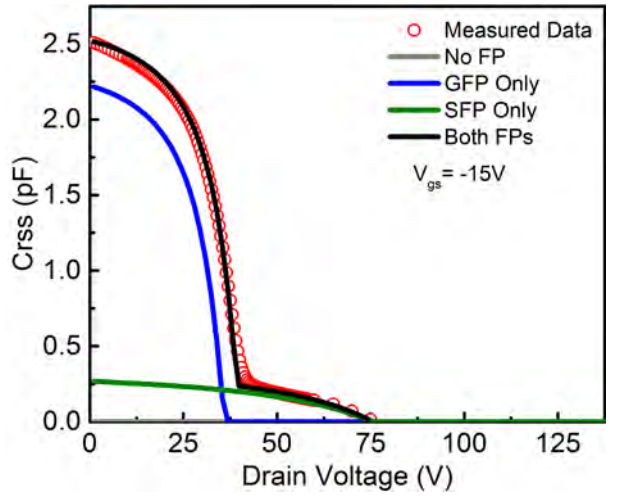
[1] S. A. Ahsan *et al.*, *IEEE Trans. Electron Devices*, **63 (2)**, [2016]

Modeling field plates: Trends w.r.t Drain Voltage

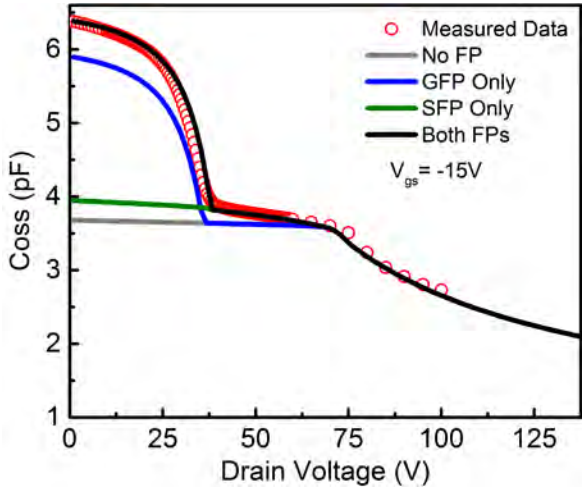


Terminal Capacitance: Input side (Ciss)

Terminal Capacitance: Reverse (Crss)

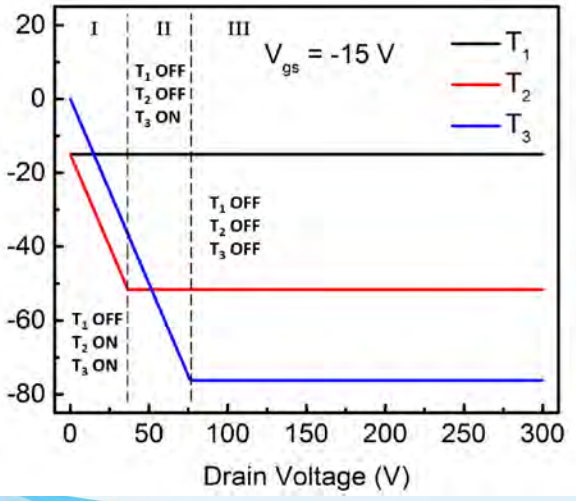


*The plateaus in each capacitance curve denote the **switching -off** of one of the transistors in series as depicted in the previous slide.*



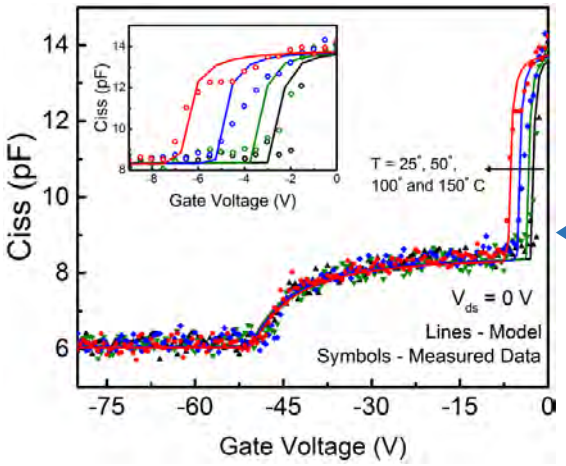
Terminal Capacitance: Output side (Coss)

Activation of different series transistors with increasing drain voltage at a fixed gate bias



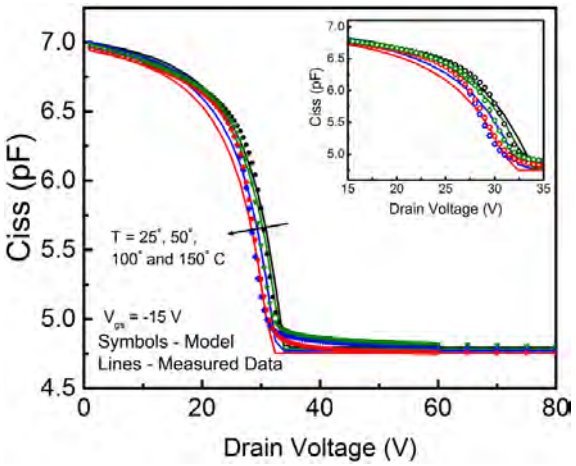
[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Field Plate Models: Trends w.r.t temperature

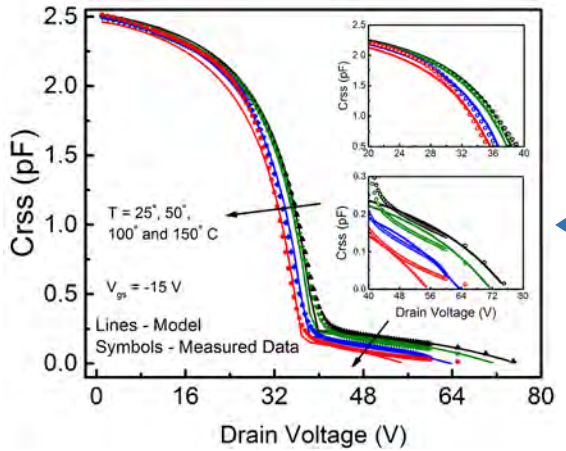


Terminal Capacitance: Input side (Ciss) with gate voltage

Terminal Capacitance: Input side (Ciss) with drain voltage

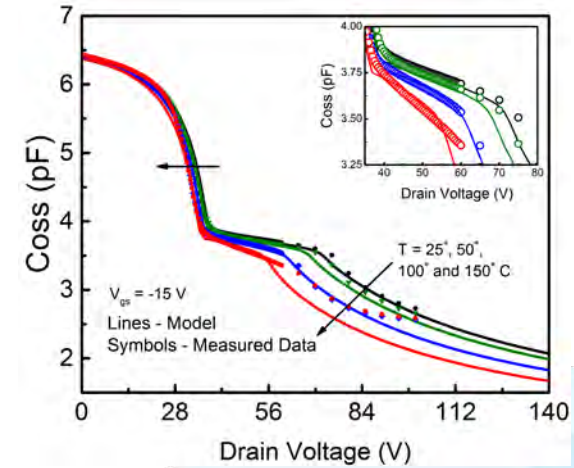


Increasing temperature shifts the threshold voltage in the negative direction – leading to a corresponding shift in the capacitance curves.



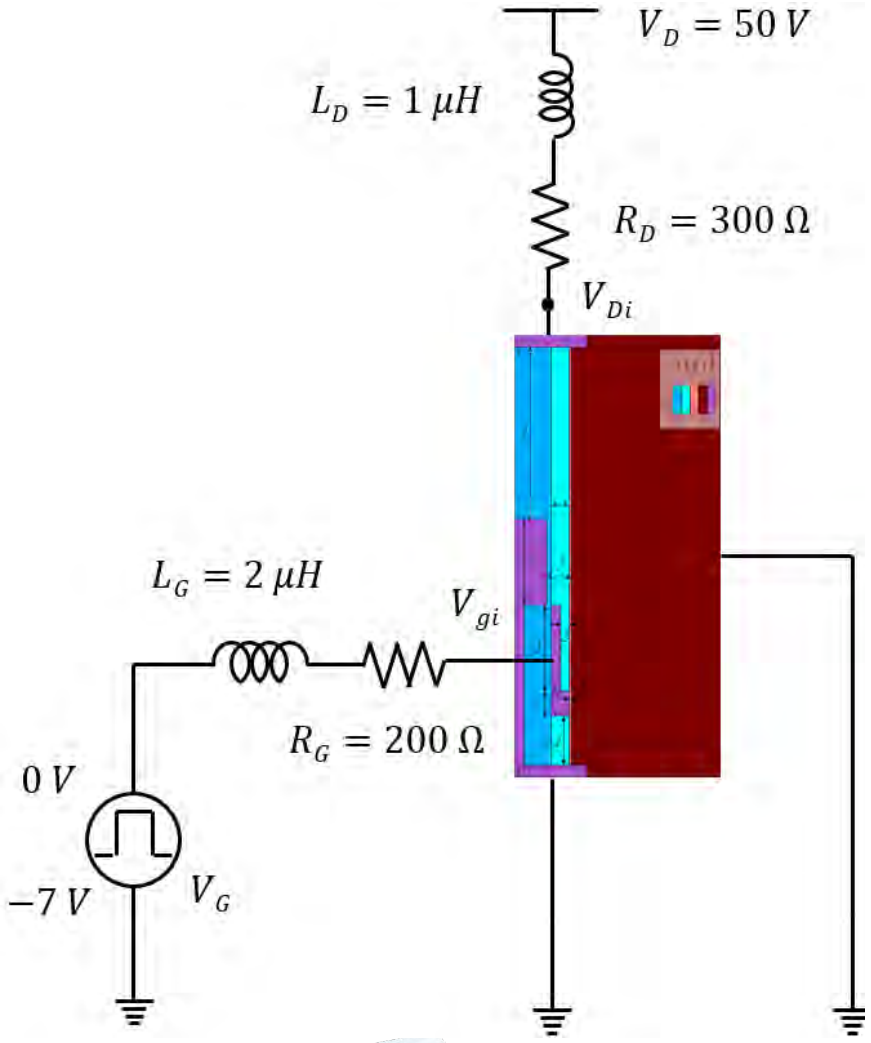
Terminal Capacitance: Reverse (Crss)

Terminal Capacitance: Output side (Coss)



[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

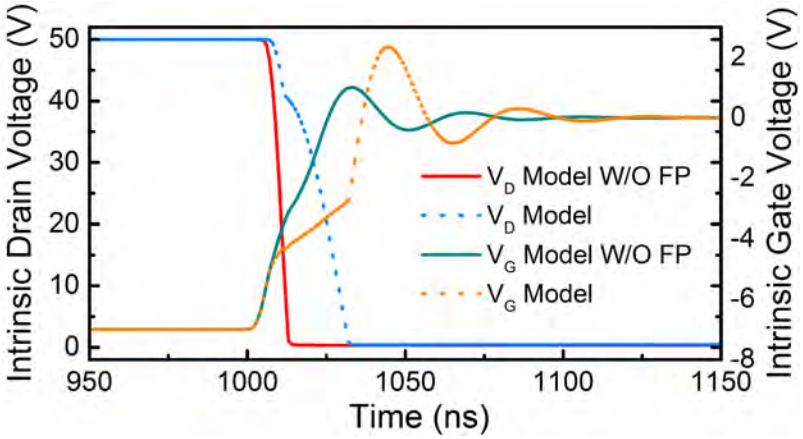
Mixed mode TCAD circuit using ATLAS



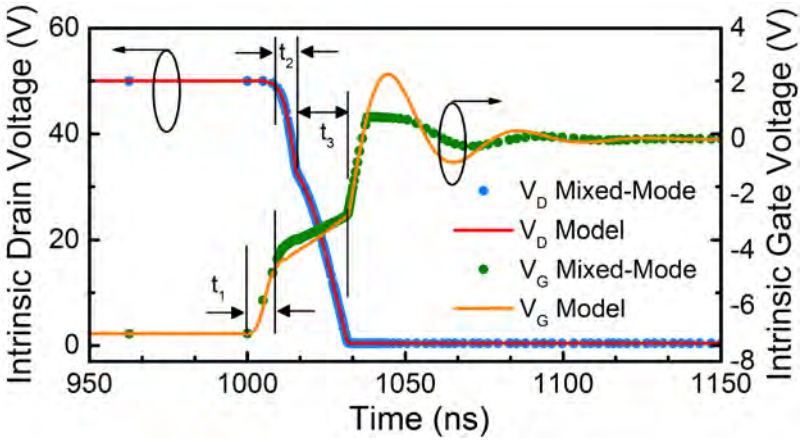
- *Schematic for Mixed-mode simulation using the numerical GaN FP device generated in Atlas.*
- *The FP-HEMT is put as the DUT with7 V and 0 V pulses of 1 MHz at gate.*
- *The pulse has a pulse-width of 480 ns 20 ns rise and fall times.*
- *Supply voltage of 50 V is chosen to capture the maximum effect of cross coupling capacitances on switching transients while an inductive load is put at the drain.*

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Voltage waveforms

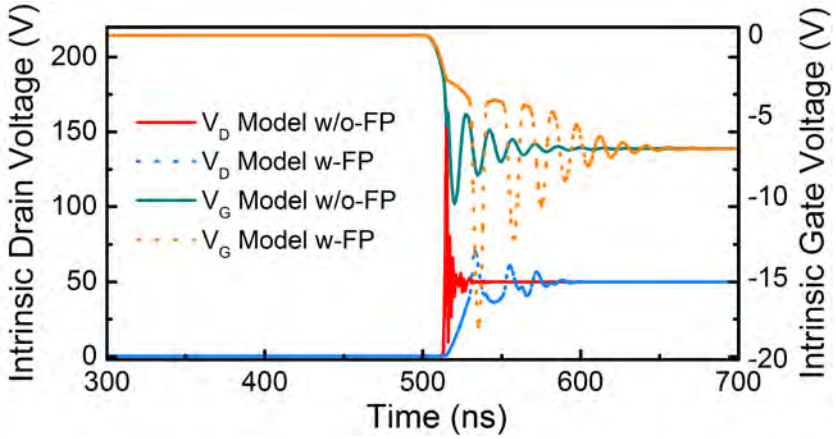


Turn-on by switching applied gate signal from 7 V to 0 V (FP vs no FP)

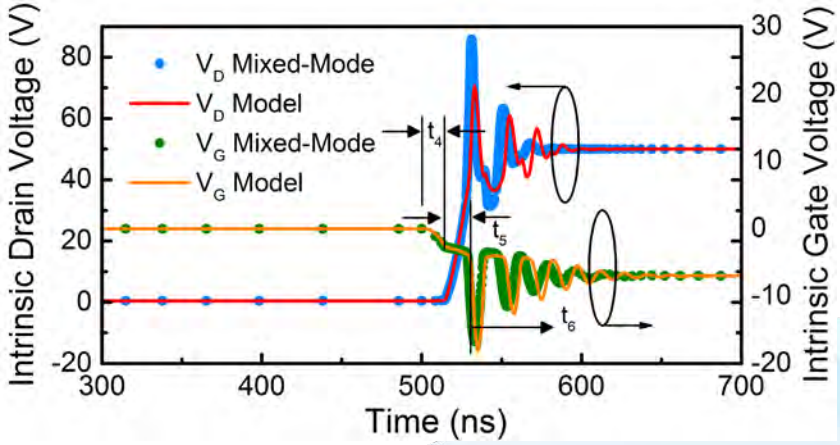


Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)

The model accurately predicts drain overshoots due to LC ringing, Miller plateaus due to accurate prediction in sharing of the gate drive current to charge Cgs and Cgd and the associated gate -drain charge, and the damping of the oscillations.



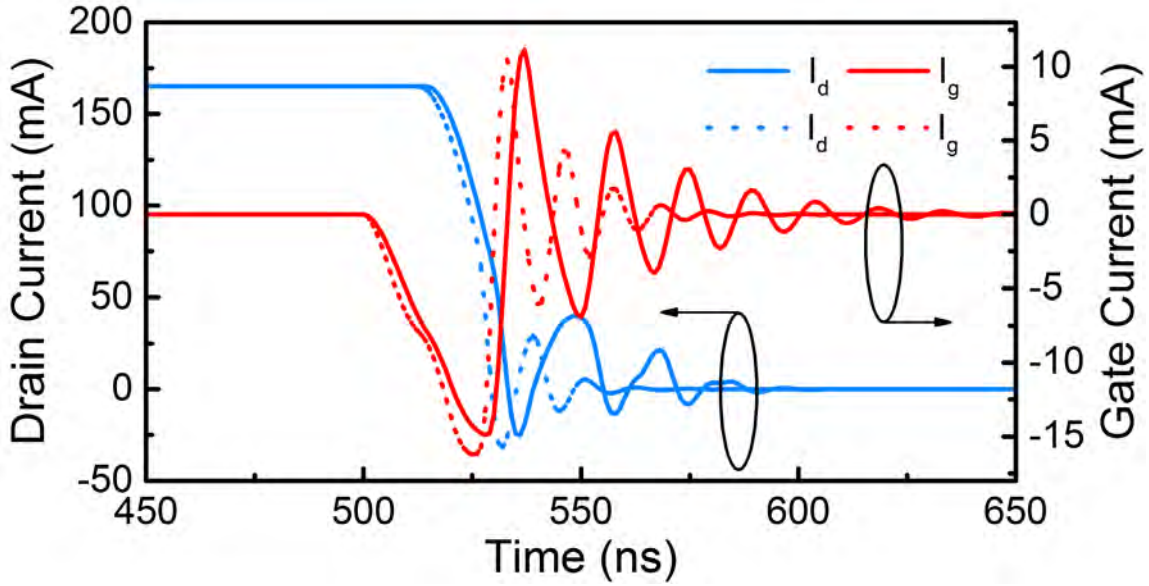
Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (FP vs No FP)



Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed -mode vs Model)

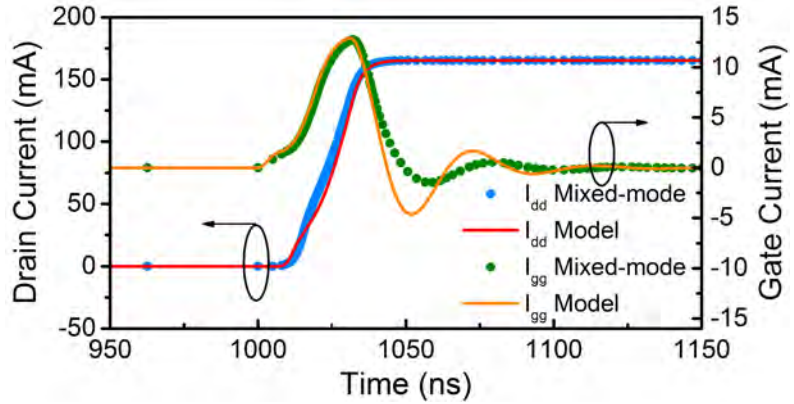
[1]S. A.Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Current Waveforms

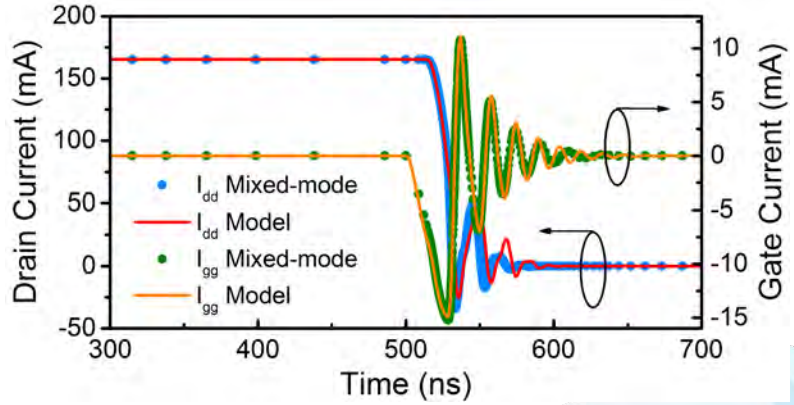


Comparison of modeled time -domain waveforms during turn -off with and without cross -coupling and substrate capacitances.

Solid lines = Cross-Coupling(CC) and substrate model included
Dotted lines = CC and substrate model excluded.



Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)



Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed-mode vs Model)

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

Contents

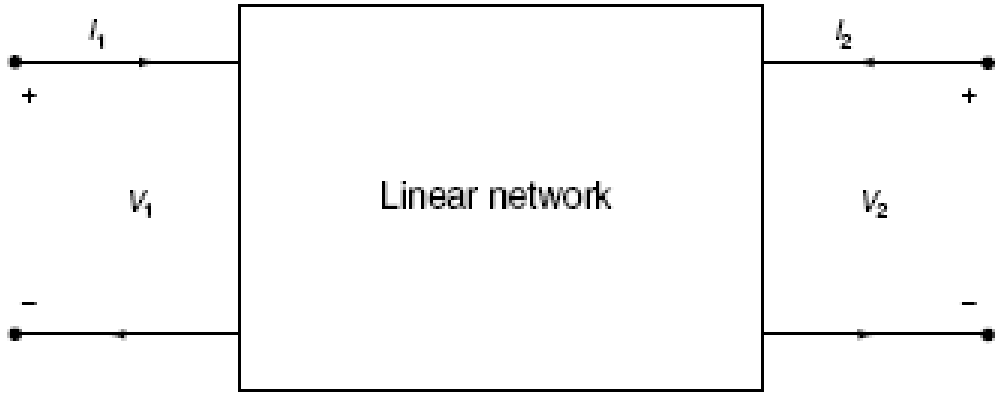
High-Frequency Characterization

- We seek to model the linear (small-signal) behavior of a device subject to a high-frequency test signal

- Such behavior is typically summarized by the N-port network parameters of the device
  - Impedance parameters (Z-Parameters)
  - Admittance parameters (Y-Parameters)
  - Hybrid parameters (H-Parameters)
  - Scattering parameters (S-Parameters)

- Focus on 2-port networks, which we can measure with our lab equipment

Network Analysis basics



Z-Parameters

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

$$Z_{ij} = \left.\frac{V_i}{I_j}\right|_{I_k=0 \text{ for } k\neq j}$$

Z_{ij} found by driving port j with current I_j, open-circuiting all other ports, & measuring open-circuit voltage at port i

Y-Parameters

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

$$Y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k=0 \text{ for } k\neq j}$$

Y_{ij} found by driving port j with voltage V_j, short-circuiting all other ports, & measuring short-circuit current at port i

H-Parameters

$$V_1 = h_{11}I_1 + h_{12}V_2$$
$$I_2 = h_{21}I_1 + h_{22}V_2$$

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

Short-circuit current gain

Network Analysis basics contd.

- Z-, Y-, and H-Parameters are an abstraction at high frequencies since voltages, currents, and impedances can not be measured in a direct manner
  - Desired quantities are non-unique for non-TEM modes of propagation
  - Require perfect open and short circuits which are difficult to achieve

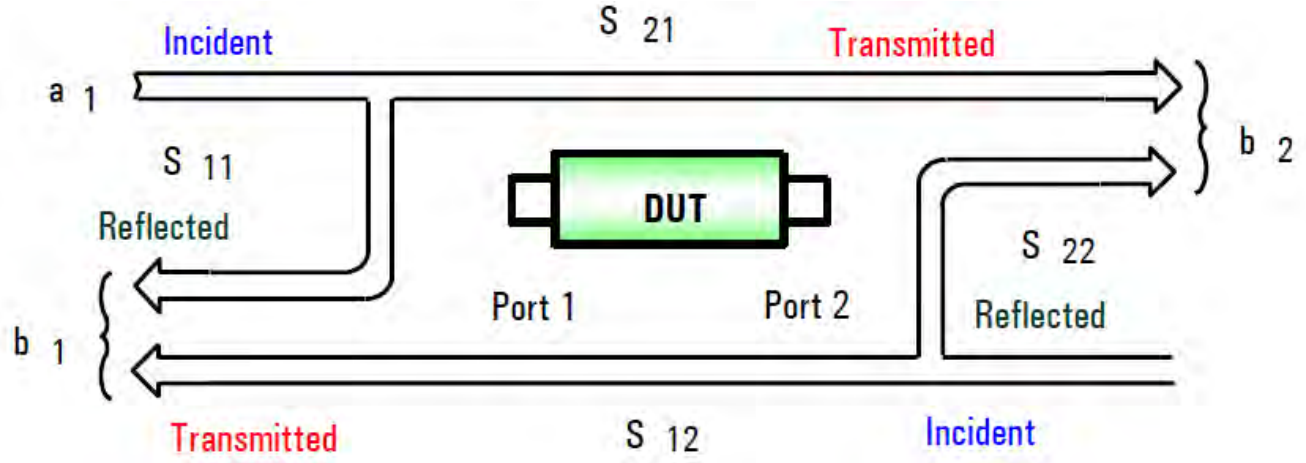
- S-Parameters are preferred because they are based on the concept of incident, reflected, and transmitted waves which are more easily measured at high frequencies in terms of amplitude and phase angle of the various waves

- Typically deal with 2-port network parameters for transistor compact modeling work

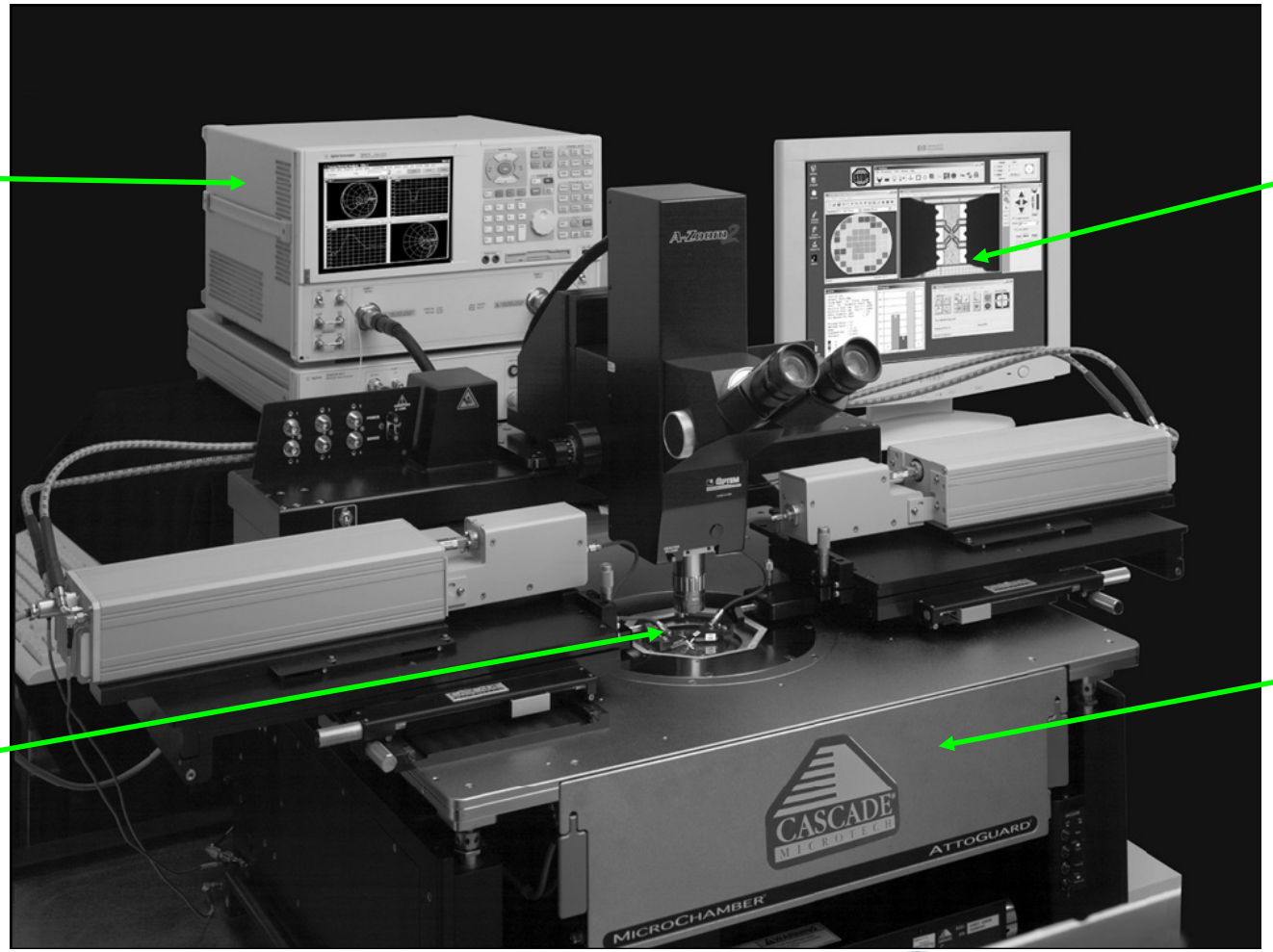
RF Measurements

S-Parameters

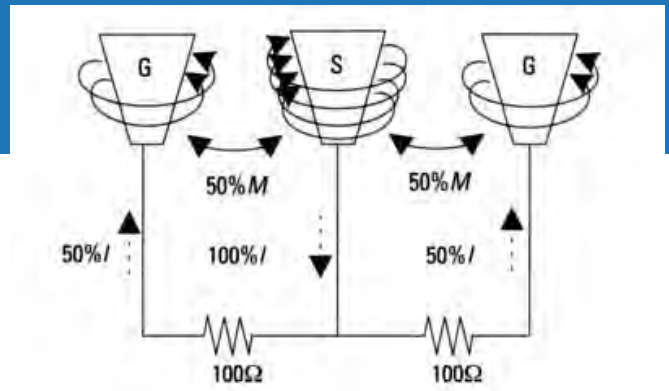
- Easy for high frequencies (hard to do open/short for Z/Y)
- Calculate other quantities
- Cascadable
- Transformation
- Compatibility with simulation tools

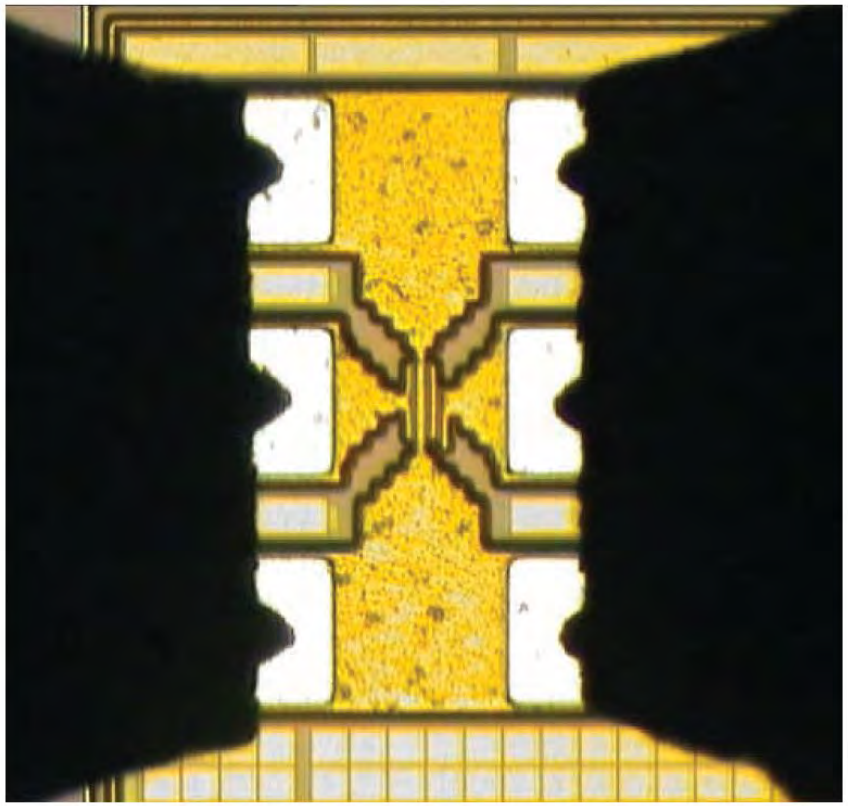


110GHz SParameter Measurement System

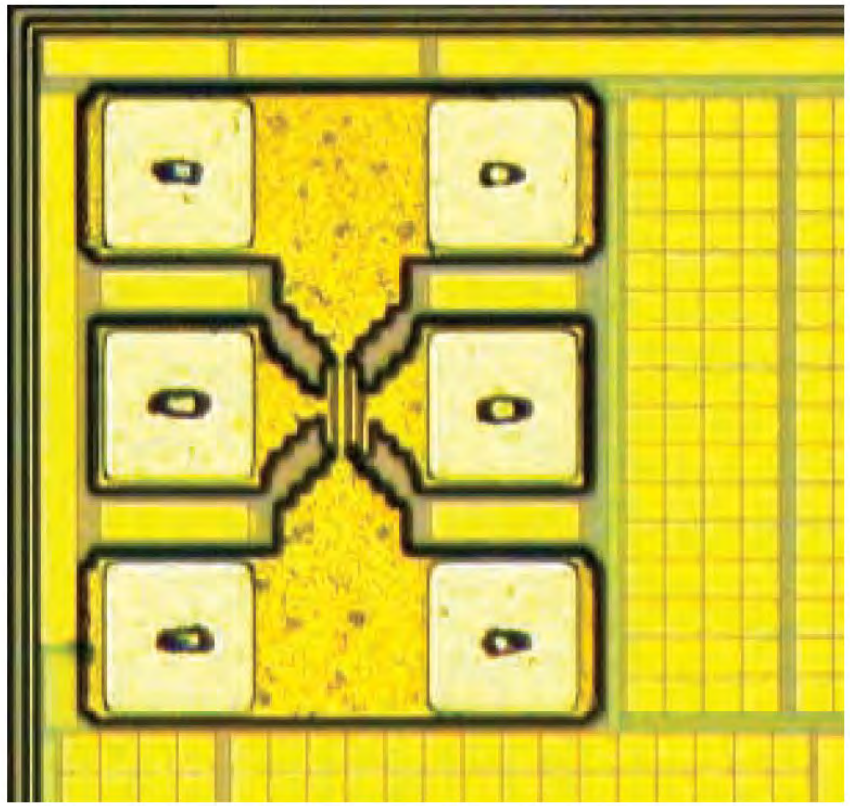


RF GSG probes



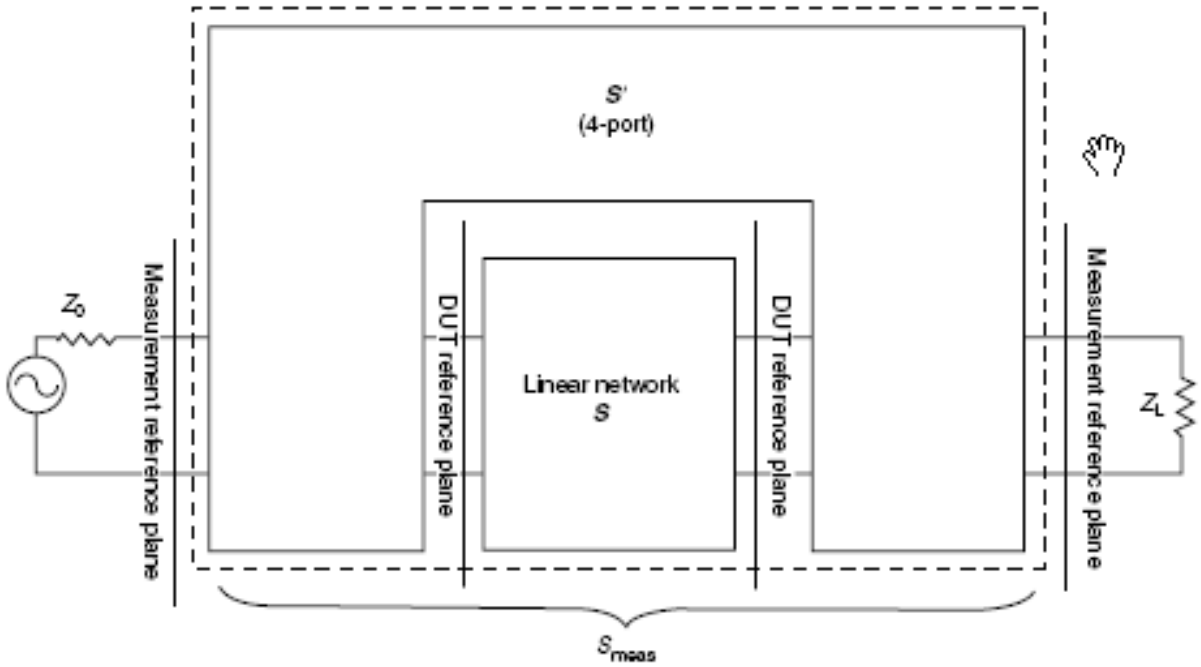


Excellent tip visibility Infinity Probe contacting Silicon RF device



Small contact marks enable contact to small pads

Calibration



- Calibration of measurement setup required to account for parasitics associated with connection of VNA to a DUT
  - Connection results in additional losses, reflective discontinuities, & phase shifts
- 4-port S' matrix implies 16 error terms
  - Passive nature of error network implies that it is reciprocal such that transmission terms are equal and a 12-term error model suffices to describe the S' matrix

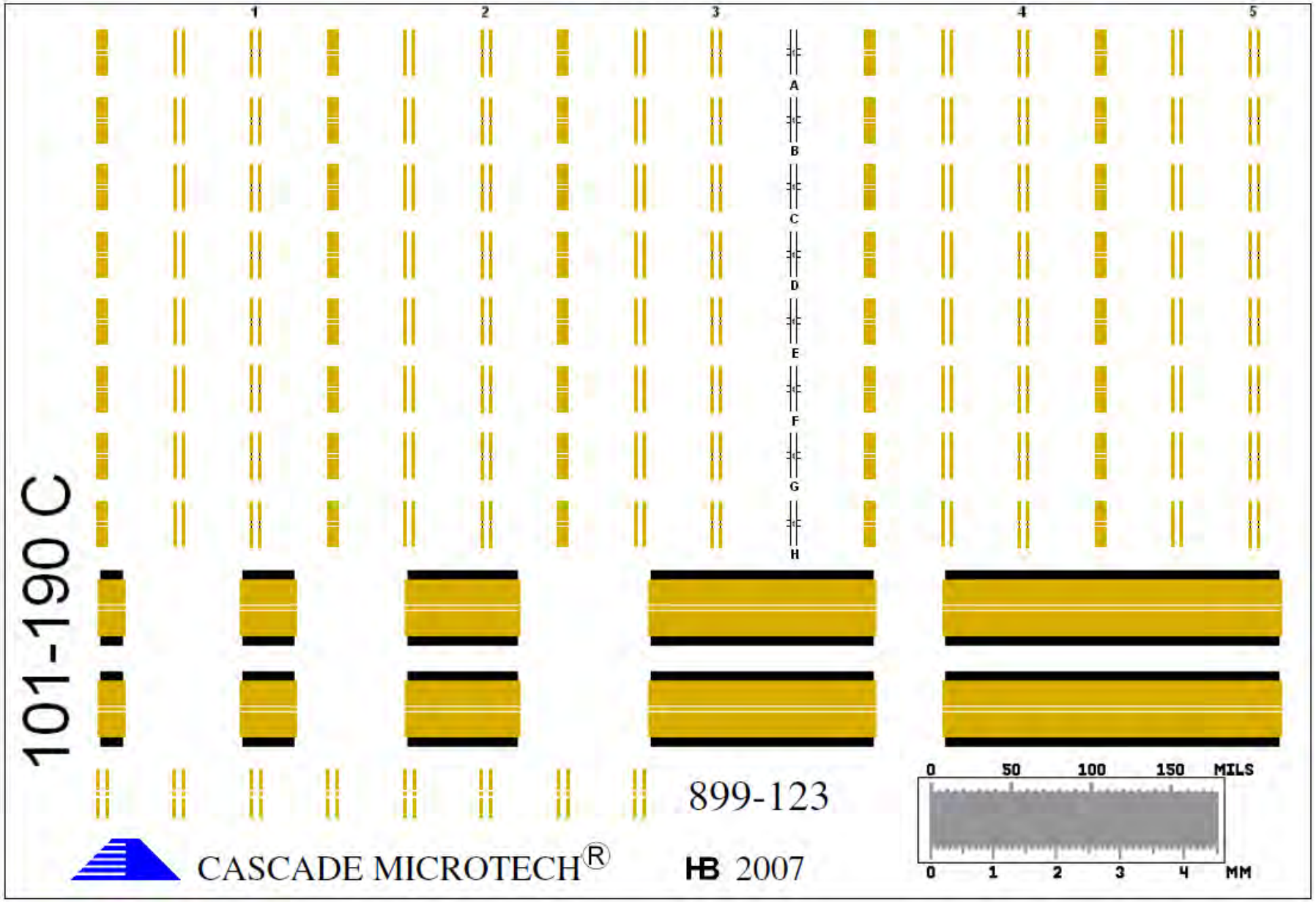
Calibration contd.

- Calibration achieved by measuring known standards located at DUT reference planes (probe tips for on-wafer measurements, and applying algorithms to determine the 12 error terms)
- Several calibration techniques available
  - Open-Short
  - SOLT (Short-Open-Load-Thru)
  - SOLR (Short-Open-Load-Reciprocal)
  - TRL (Thru-Reflect-Line)
  - LRM/LRRM (Line-Reflect-Match/Line-Reflect-Reflect-Match)
- Different standards required for different techniques, but, in general, standards must be precise with very low, known parasitics
- A special Impedance Standard Substrate (ISS) with precisely defined standards is used
  - Typically use SOLT even for 110GHz measurements

Impedance Standard Substrate

(Pitch: 100 – 250 um, Configuration: Ground-Signal-Ground)

P/N: 101-190, S/N:



Impedance Standard Substrate contd.

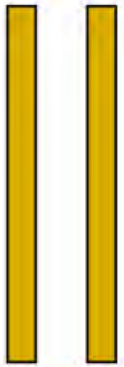
Thru

Thru delay: **1.0 ps**

Length: **220 um**

Impedance: **50 Ohm** (Nominal)

Note: Thru and Verification line lengths are signal conductor edge-to-edge dimension.

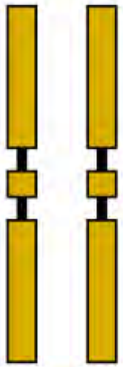


Short

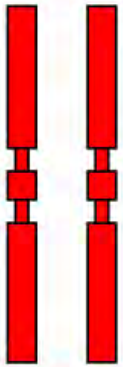
Recommended Overtravel:

ACP
75 - 125 um

Infinity
50 - 75 um



Load



Precision 50 Ohm Load

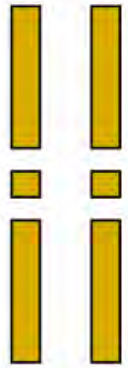
Note: Ensure the bias supply is turned **off** during calibration. Applying bias to the probe during calibration could cause the resistance of the load to change.

DC accuracy:
+/- 0.3 %

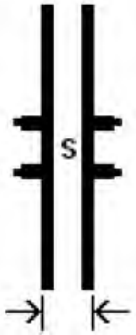
Note: For optimum calibration accuracy **only** the **Red** - marked load standards should be used.

Verification Lines

ps	um
3	450
7	900
14	1800
27	3500
40	5250



Open
(On Substrate)



130 um
Alignment Marks

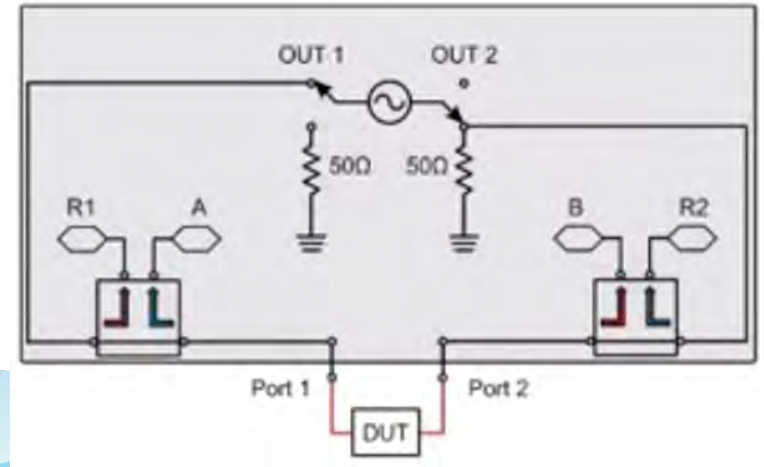
Note: By default, an **Open** is synthesized by raising the probes in air a minimum distance of 250 mm above the chuck surface. A Substrate Open structure is also provided as an alternative.

S-parameter measurement

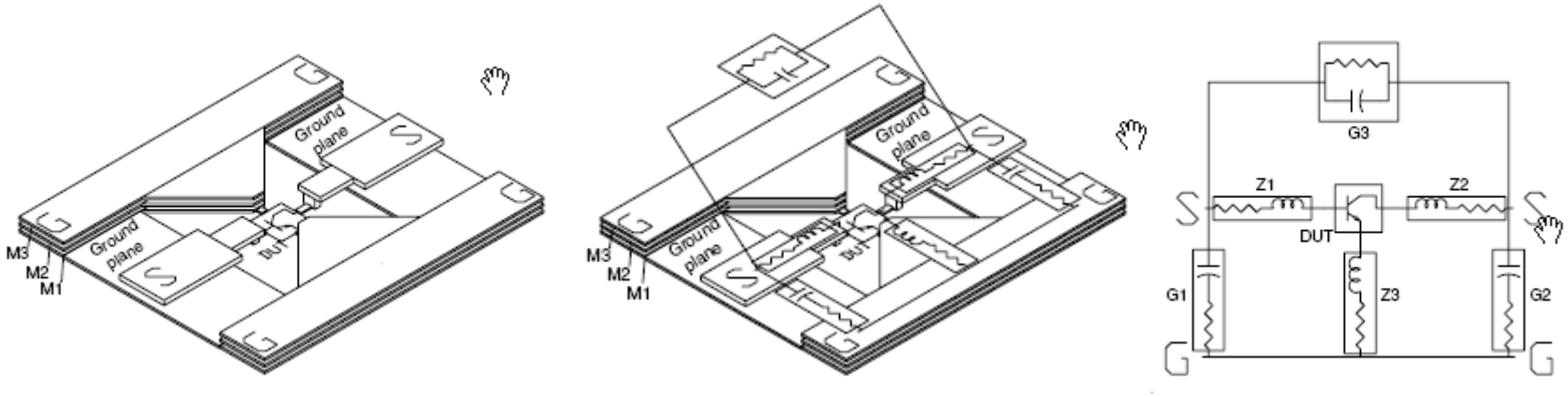
- S-parameters measured using vector network analyzer (VNA) (e.g. Agilent E5071C ENA with frequency range of 100 kHz–8.5 GHz)

- De-embedding
  - Use de-embedding to remove parasitics
  - Probe/wire parasitics are de-embedded using calibration substrate
  - Pads to device parasitics are de-embedded using OPEN-SHORT de-embedding

VNA Architecture



De-embedding



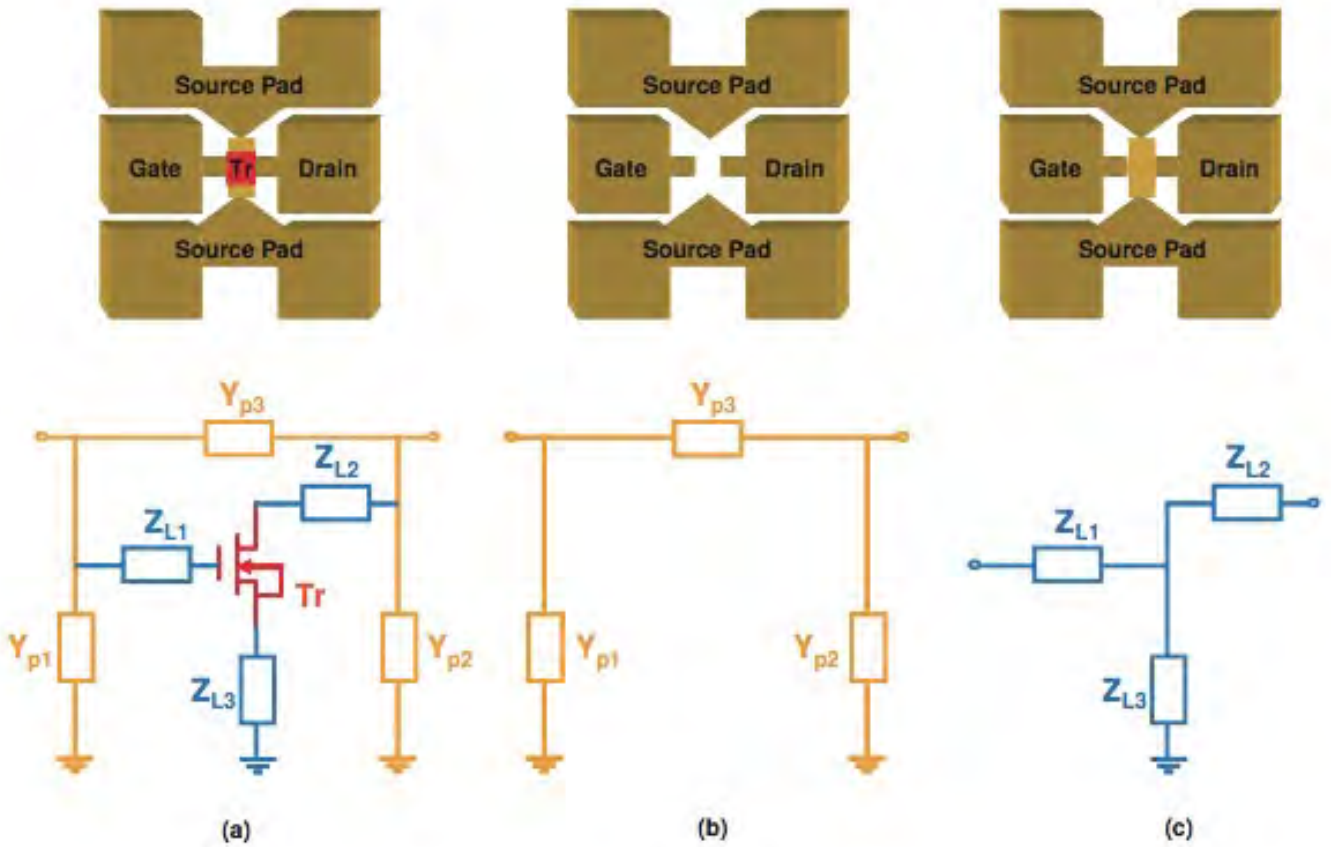
- Even with calibration, reference planes are still not at the boundaries of the intrinsic device due to on-wafer test structure interconnects (probe pads, transmission lines, ground planes, etc.)
  - Must measure additional on-wafer test structures to calibrate out (de-embed) the remaining parasitics

De-embedding contd.

- Most common on-wafer de-embedding technique is the OPEN-SHORT method where
  - OPEN test structure is designed to represent the parallel (G) parasitics
  - SHORT test structure is designed to represent the series (Z) parasitics

- De-embedding results are valid if OPEN, SHORT, and DUT are linear and time invariant (LTI) in nature
  - OPEN and SHORT are passive and, thus LTI
  - DUT is LTI if it behaves linearly with applied input power – care must be taken in choosing power level for S-Parameter measurements

Open-Short De-embedding



De-embed from Open:

$Y_{DUT/Open} = Y_{Total} - Y_{Open}$

$Y_{Short/Open} = Y_{Short} - Y_{Open}$

Convert to Z:

$Z_{DUT/Open} = Z(Y_{DUT/Open})$

$Z_{Short/Open} = Z(Y_{Short/Open})$

De-embed from Short:

$Z_{DUT} = Z_{DUT/Open} - Z_{Short/Open}$

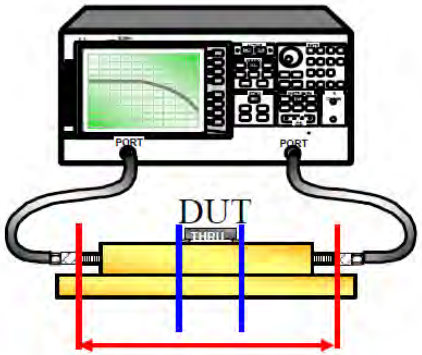
Convert to S:

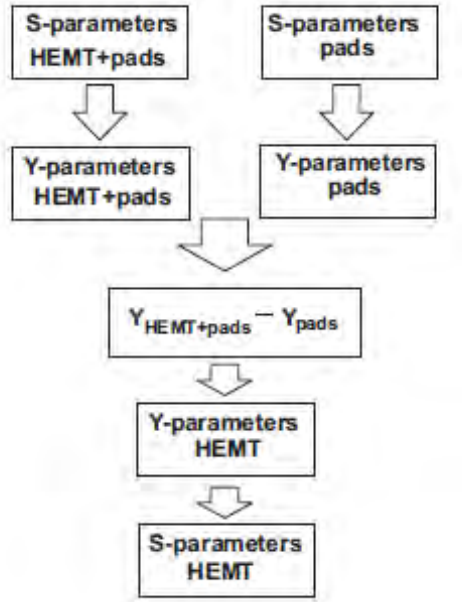
$S_{DUT} = S(Z_{DUT})$

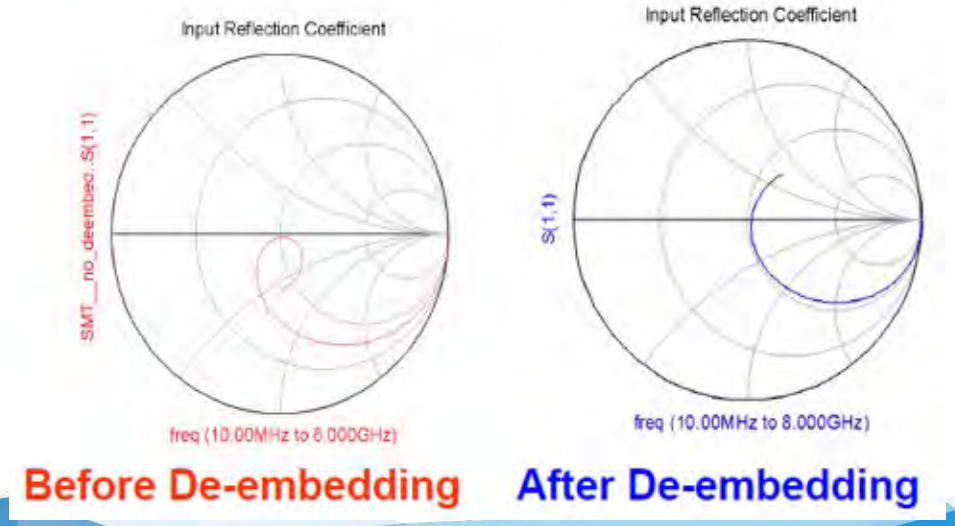
De-embedding: Negating effects of unwanted portion

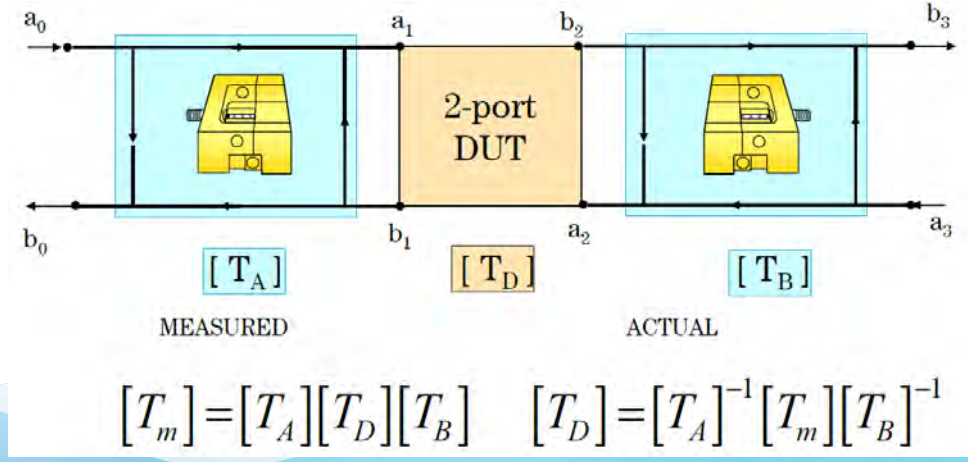
"Real" DUT SP= Measured SP–Fixture Characteristic

De-embedding is a mathematical process that removes the effects of unwanted embedded portions of the structure in the measured data by subtracting their contribution.







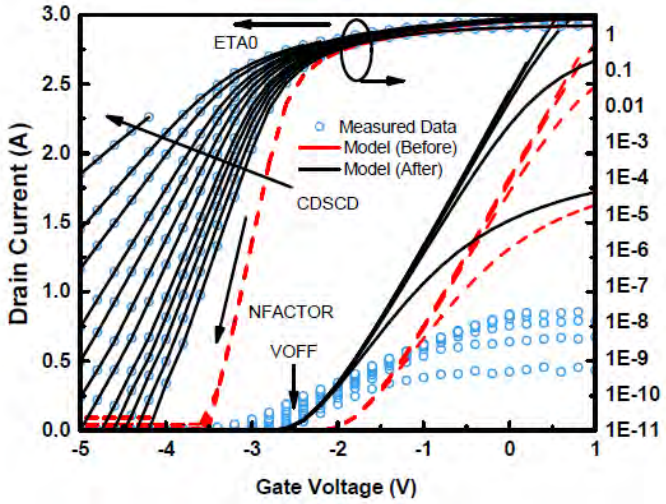


[De-embedding Techniques in Advanced Design System, Agilent Manual]

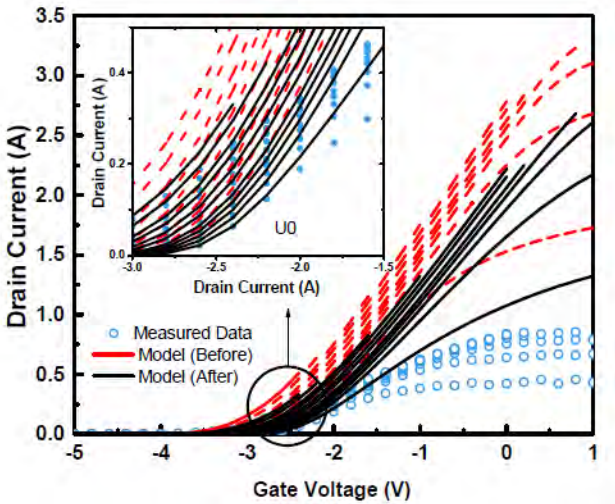
Modeling RF Devices using ASM -HEMT

- *Extracting DC Parameters*
- *RF Model Extraction*
- *Large signal simulations*
- *Load Pull Simulations*

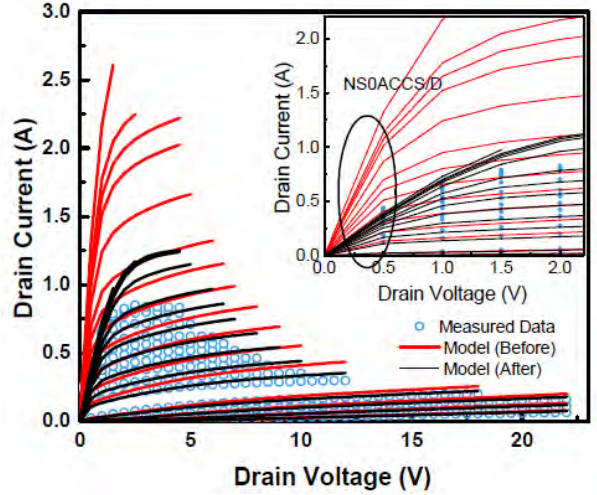
Extracting DC Parameters



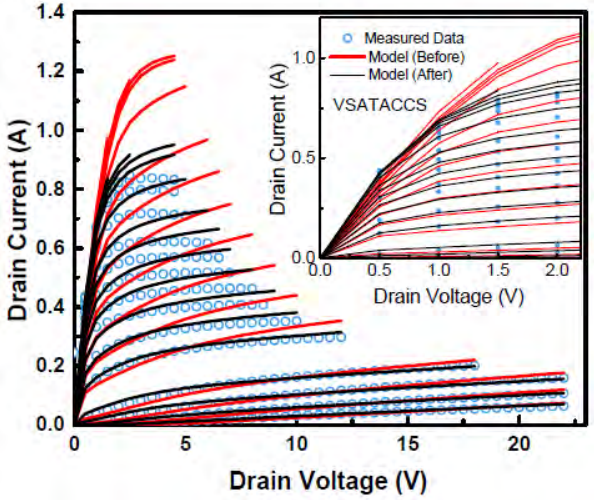
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



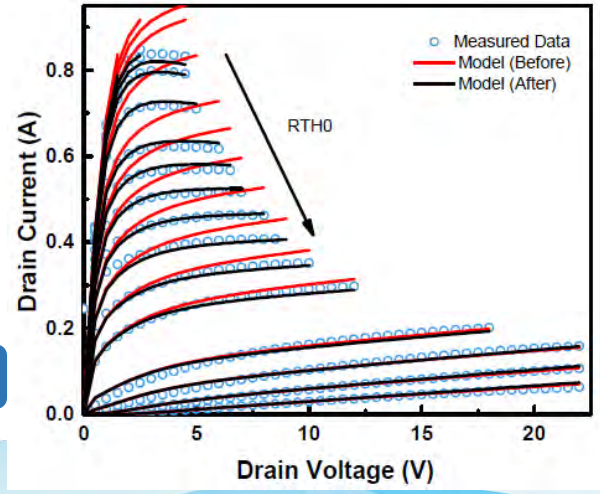
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



$I_d - V_d$ (Extract $V_{SATACCS}$)



$I_d - V_d$ (Extract R_{TH0})

[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

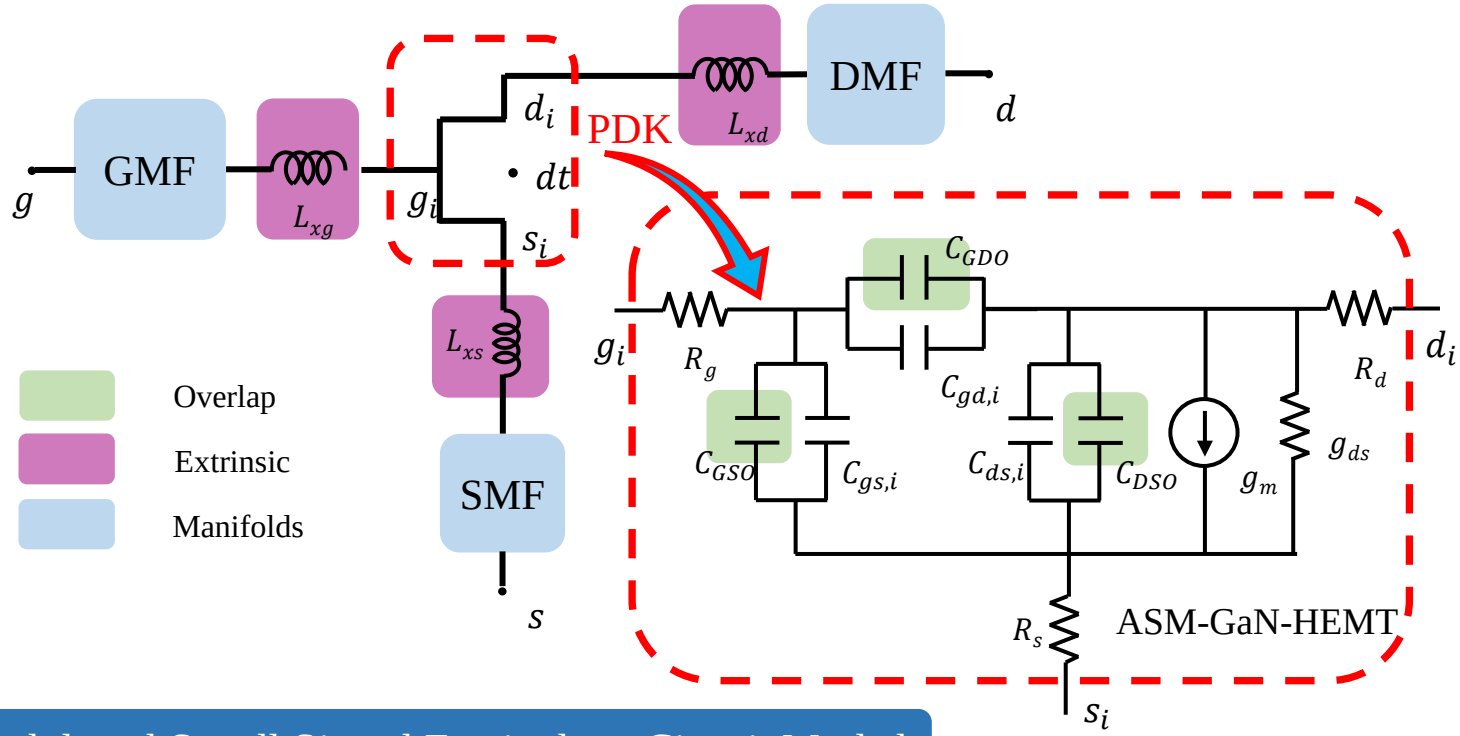
RF Model & Extraction I

Three step methodology

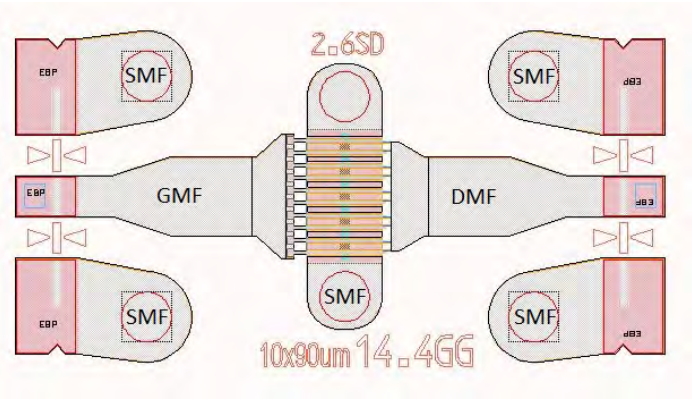
- De-embed manifolds
- Extract the intrinsic core model - Using low frequency Y-parameters
- Extract Inductances - Using high frequency Y-parameters

Model

- Core surface potential based PDK
- Access region resistances included in core
- Bus-inductances in extrinsics



Pad-level Small Signal Equivalent Circuit Model



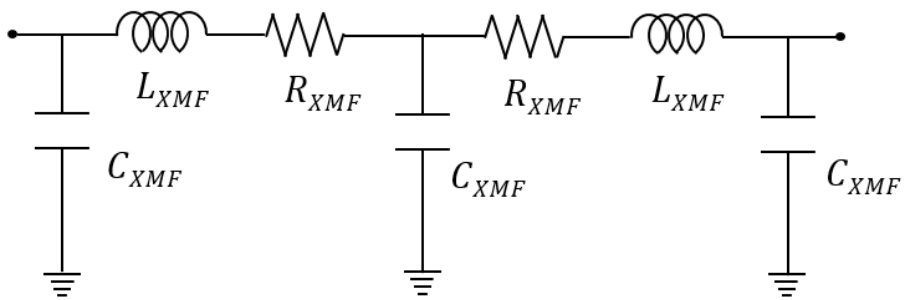
Device Layout

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

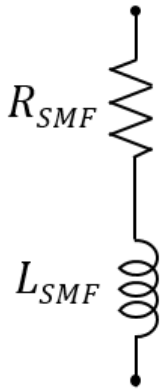
RF Model & Extraction II: Pad Parasitics

Manifolds/ Pads

- Used to probe the device
- Feed the signal to gate, drain & source bus-inductances
- Measurements obtained using TRL Calibration
- Transmission line type model
- Reciprocal (may/ may not be symmetric)
- De-embedded using "deembed" s2p components in ADS

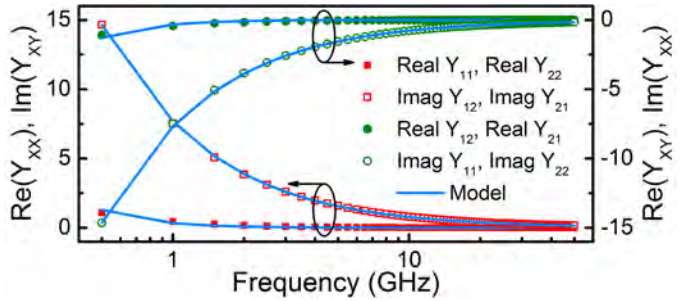


Symmetric network used for GMF/ DMF

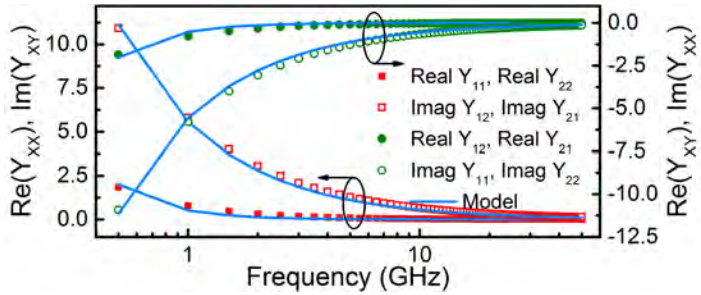


Single port SMF network

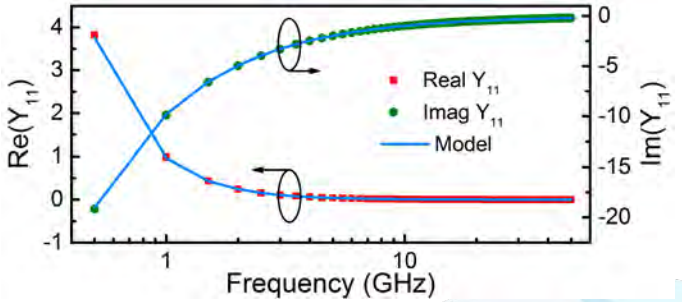
Y-parameters for DMF



Y-parameters for GMF



Y-parameters for SMF



[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

RF Model & Extraction III: Bus Inductances

[1]

$$Y_{11} = \frac{\omega^2 C_{gg}{}^2 R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} + \frac{j\omega C_{gg}}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{12} = -\frac{\omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} - \frac{j\omega C_{gd}}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{21} = \frac{g_m - \omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 C_{gg}{}^2 R_g^2} - \frac{j\omega(C_{gd} + g_m C_{gg} R_g)}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

$$Y_{22} = g_{ds} + \frac{\omega^2(C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg}(1+g_m R_g))}{1+\omega^2 C_{gg}{}^2 R_g^2} + j\omega C_{ds} + \frac{j\omega C_{gd}(1+g_m R_g) + j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2}{1+\omega^2 C_{gg}{}^2 R_g^2}$$

Key Pointers

- The effect of bus-inductances is ignored at low frequencies (assumption)
- Drain & Source access region resistances ignored from hand analysis (not an assumption, it is an advantage) [1]
- Ignore some terms at low frequency (~ 10 GHz) (assumption)
- Very simple – only need to adjust overlap capacitances & gate finger resistances (advantage)

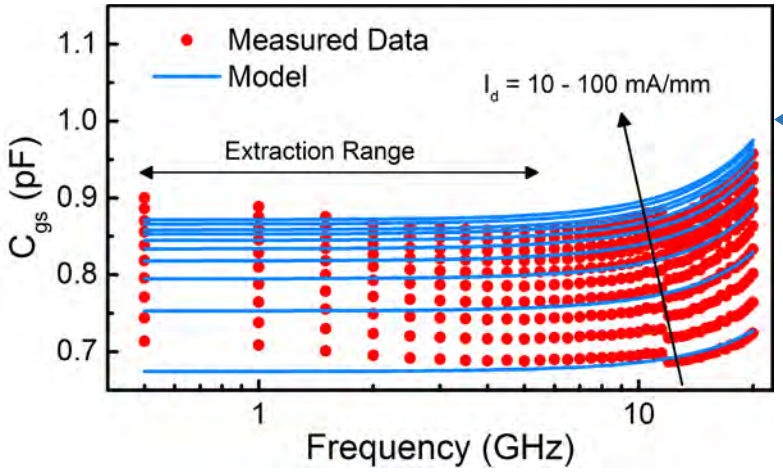
$$[\mathbf{Y}] \approx \begin{bmatrix} \omega^2 C_{gg}{}^2 R_g + j\omega C_{gg} & -\omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd} \\ g_m - j\omega\,(C_{gd} + g_m C_{gg} R_g) & g_{ds} + j\omega\,(C_{ds} + C_{gd}(1+g_m R_g)) \end{bmatrix}$$

$$\begin{bmatrix} C_{gs} & C_{gd} & C_{ds} \\ g_m & g_{ds} & R_g \end{bmatrix}$$

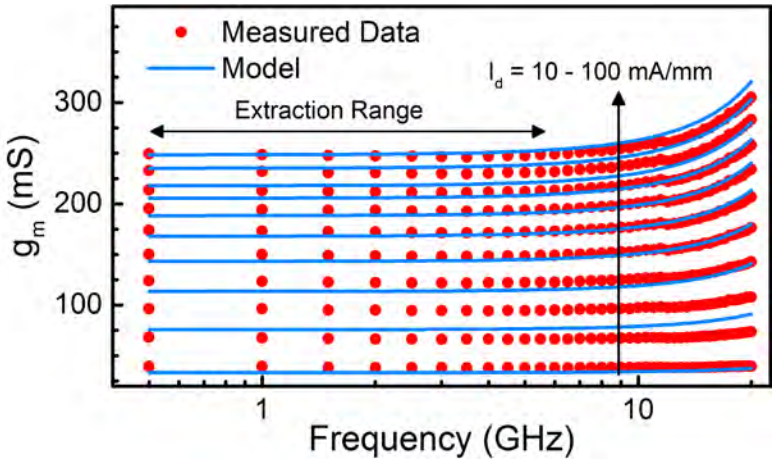
$$\begin{bmatrix} (\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}])/\omega & -\mathrm{Im}[Y_{12}]/\omega & \mathrm{Im}[Y_{22}]/\omega - C_{gd}(1+g_m R_g) \\ \mathrm{Re}[Y_{21}] & \mathrm{Re}[Y_{22}] & \mathrm{Re}[Y_{11}]/(\omega^2 C_{gg}^2) \end{bmatrix}$$

[1] I. Kwon et al., IEEE Trans. Microw. Theory Techn., 50 (6), [2002]

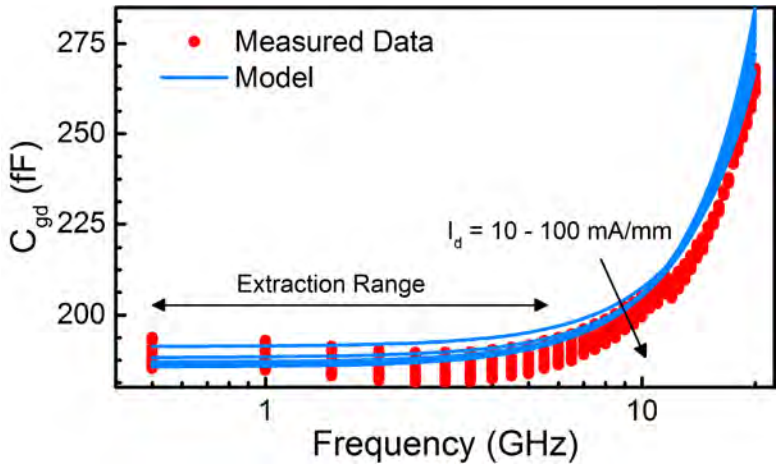
Fitting core model parameters using ADS



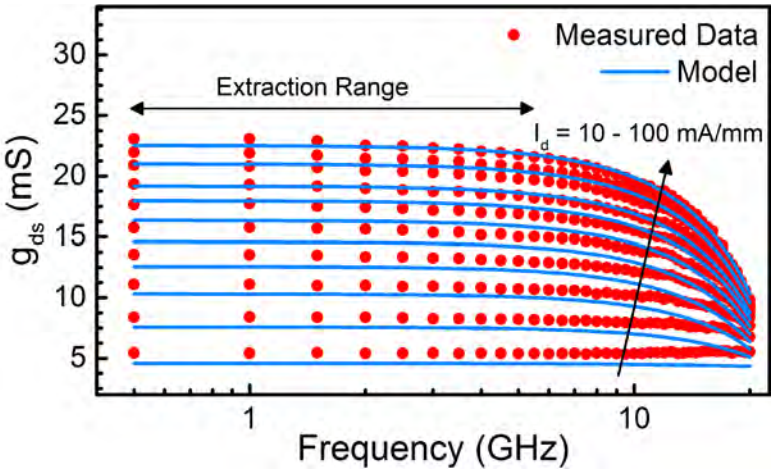
Extract C_{GSO}



g_m dispersion handled by trap model



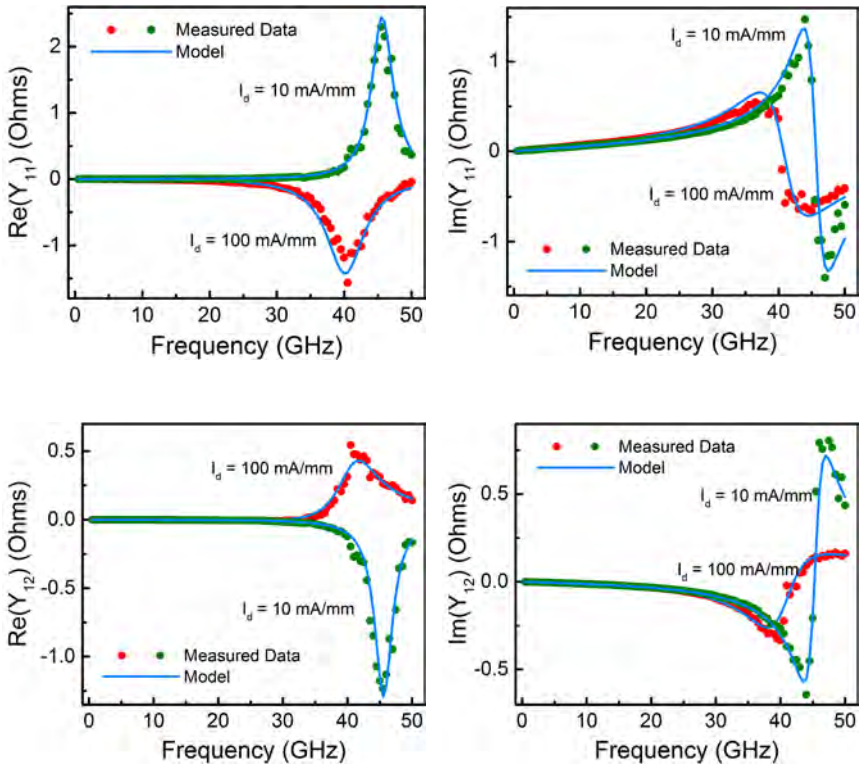
Extract C_{GDO}



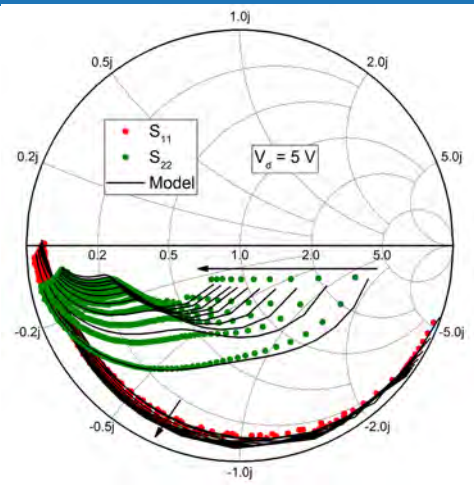
g_{ds} dispersion handled by trap model

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

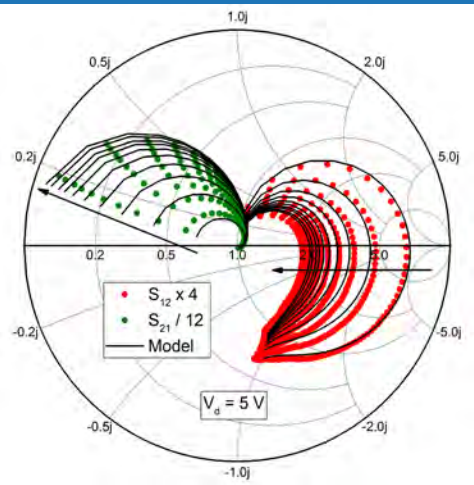
Bus Inductance fitting



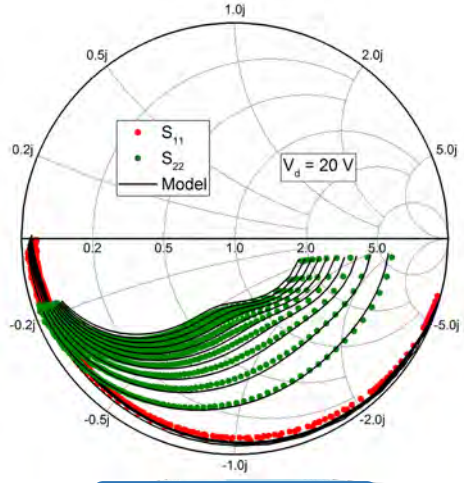
Resonant peaks due to interaction of inductances with intrinsic capacitances



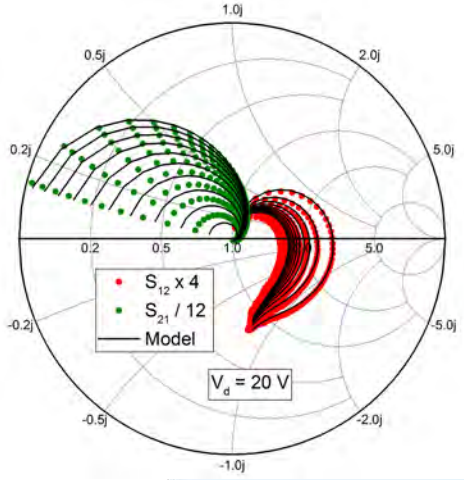
S_{11} & S_{22} (5V)



S_{12} & S_{21} (5V)



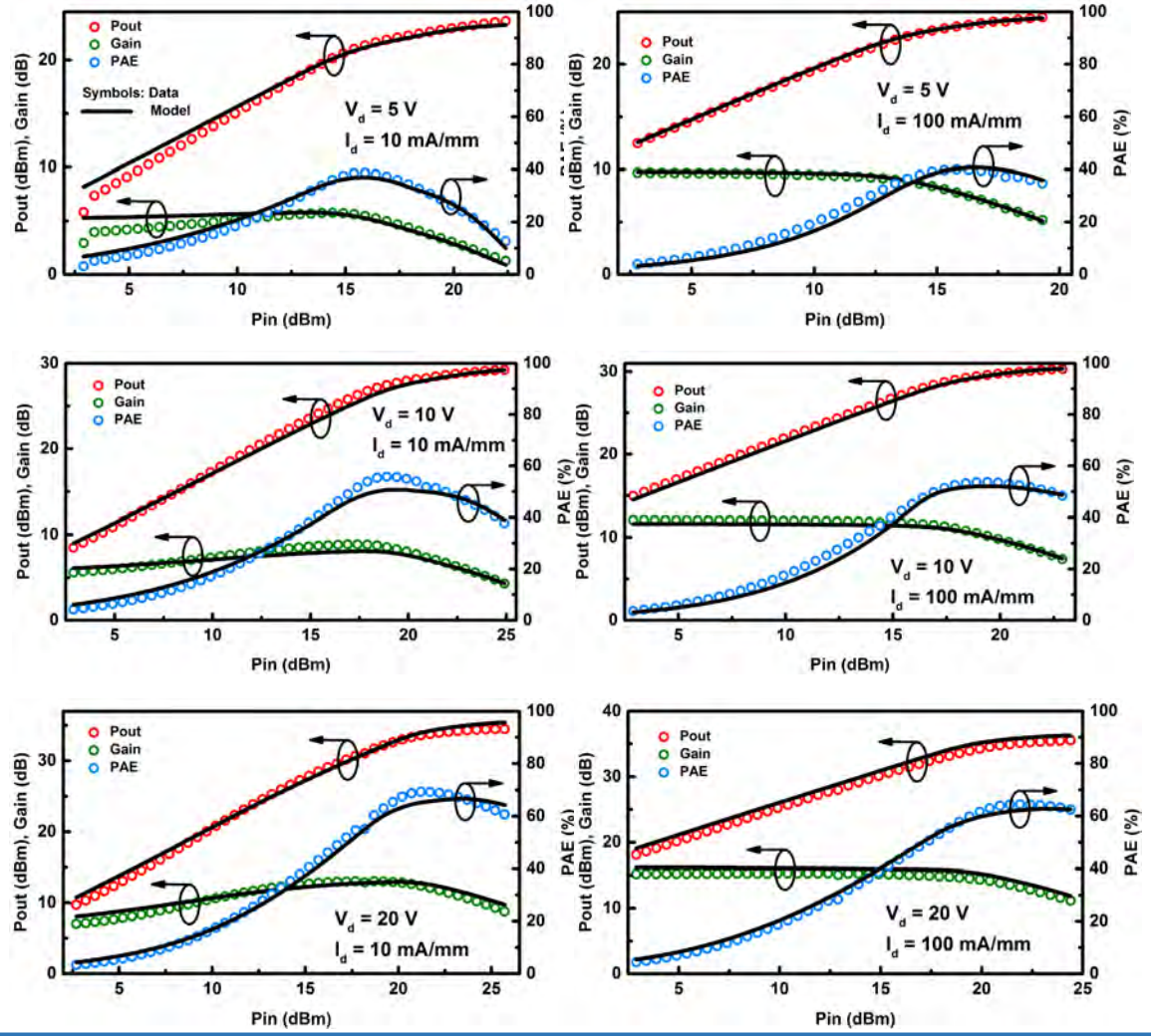
S_{11} & S_{22} (20V)



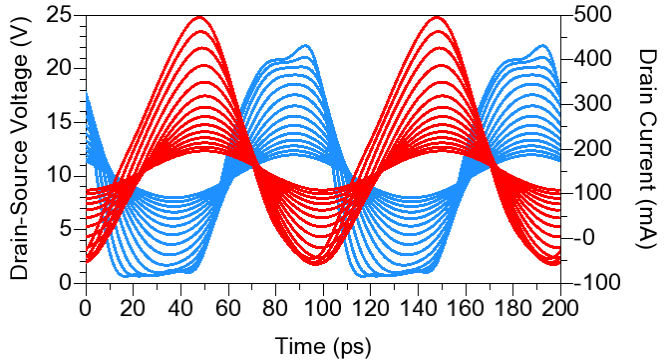
S_{12} & S_{21} (20V)

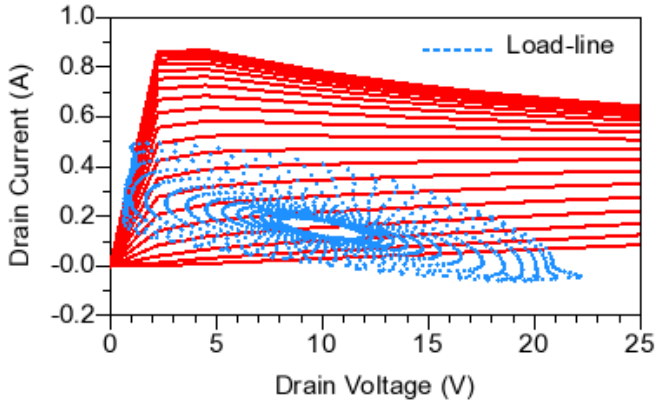
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Large Signal HB Simulations



Harmonic balance drive -up characteristics showing Pout, PAE & Gain



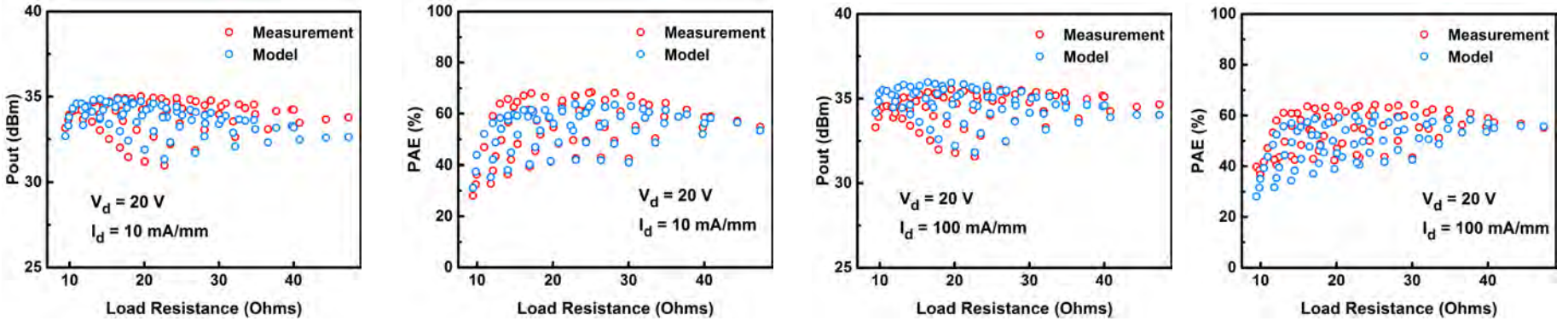


Time domain waveforms of drain voltage & current. Load line contours spanning the IV plane

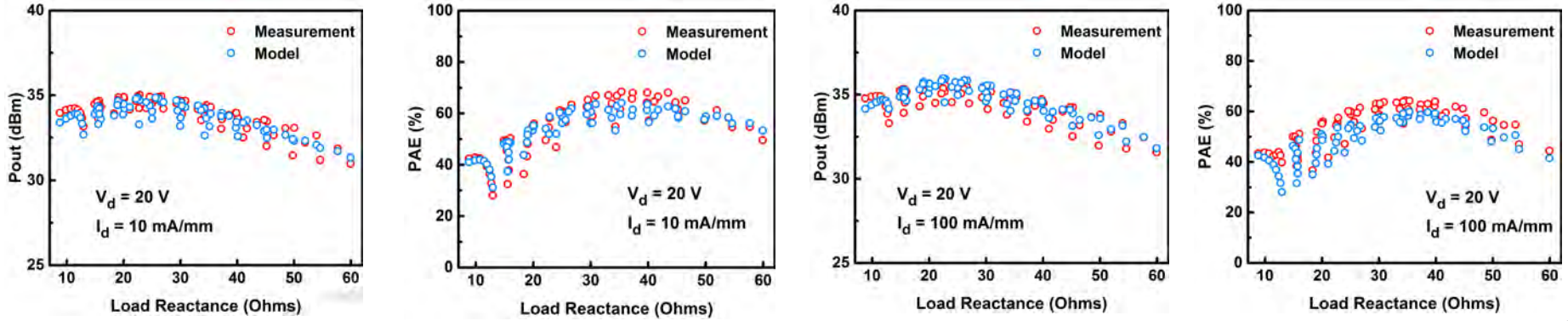
[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Validation – Real and Imaginary Loads

Fairly accurate in predicting the maxima for Pout & PAE



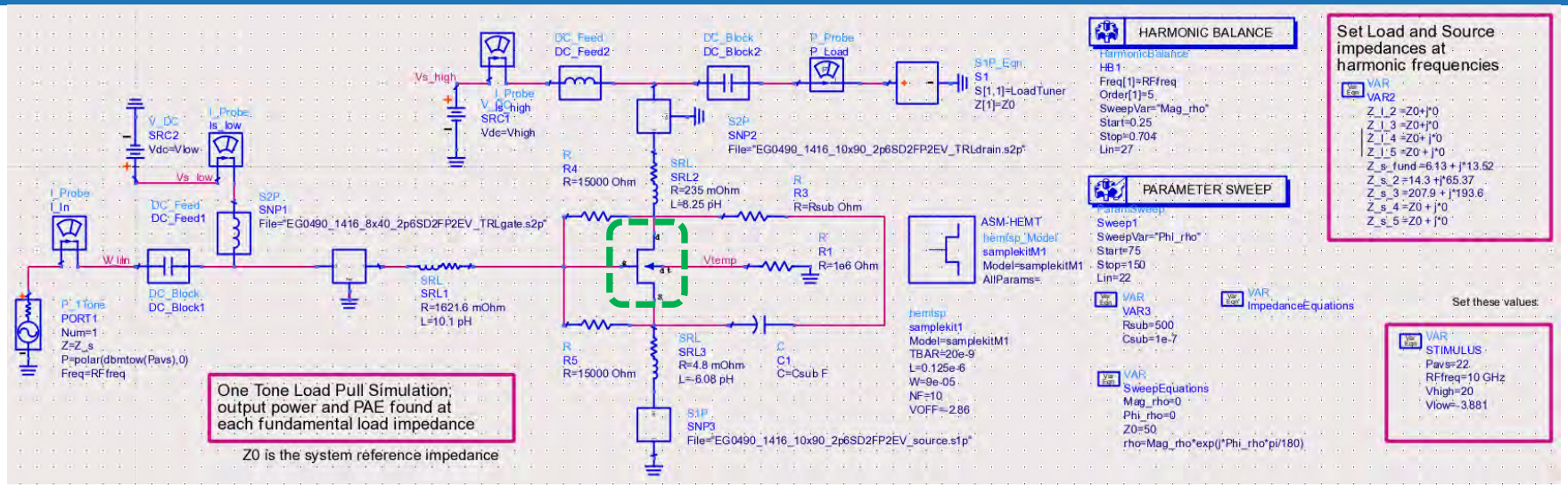
Pout & PAE against load resistance (real load)



Pout & PAE against load reactance (imaginary load)

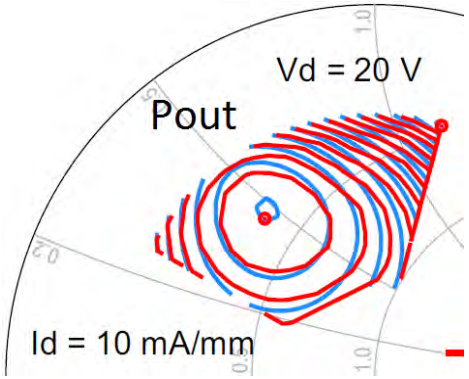
[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

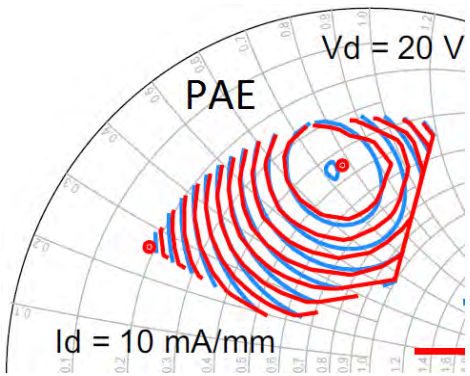
Load Pull simulations using ASM -HEMT

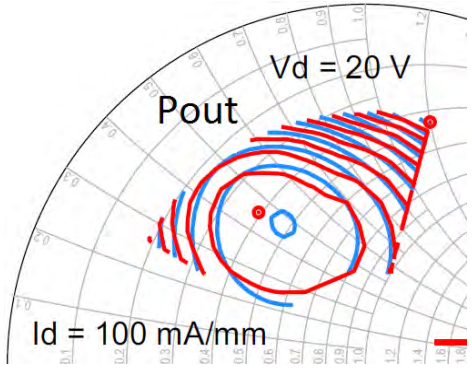


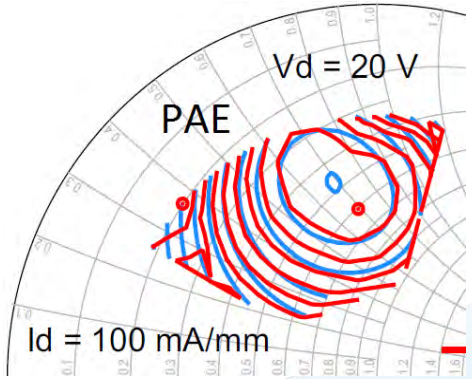
ADS Schematic for simulation of load -pull contours

22 dBm signal @ 10 GHz









Pout & PAE load pull contours for 10 mA/mm

Pout & PAE load pull contours for 100 mA/mm

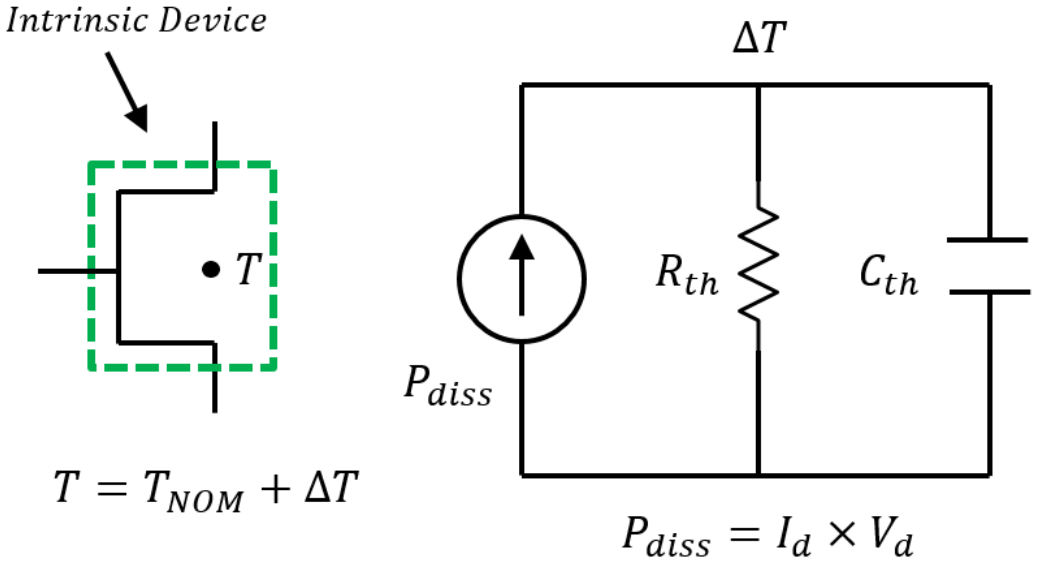
[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

Contents

Characterizing Self Heating and its Modeling

- *Self heating Model*
- *Characterization*

Self- Heating Model



Self-Heating Effect

- The self-heating circuit is defined in a thermal discipline.
- For the thermal discipline, power is the equivalent of "current" and temperature is the equivalent of "voltage"

Under these conditions, applying KCL on the thermal subcircuit, we have:

$$P(R_{th}) = \frac{Temp(R_{th})}{RTH0}$$

$$P(R_{th}) = \frac{d}{dt}(Temp(R_{th}) \cdot CTH0)$$

Characterization

$$T_{J1} = T_{NOM,1} + R_{th} \times P_{diss1}$$

$$T_{J2} = T_{NOM,2} + R_{th} \times P_{diss2}$$

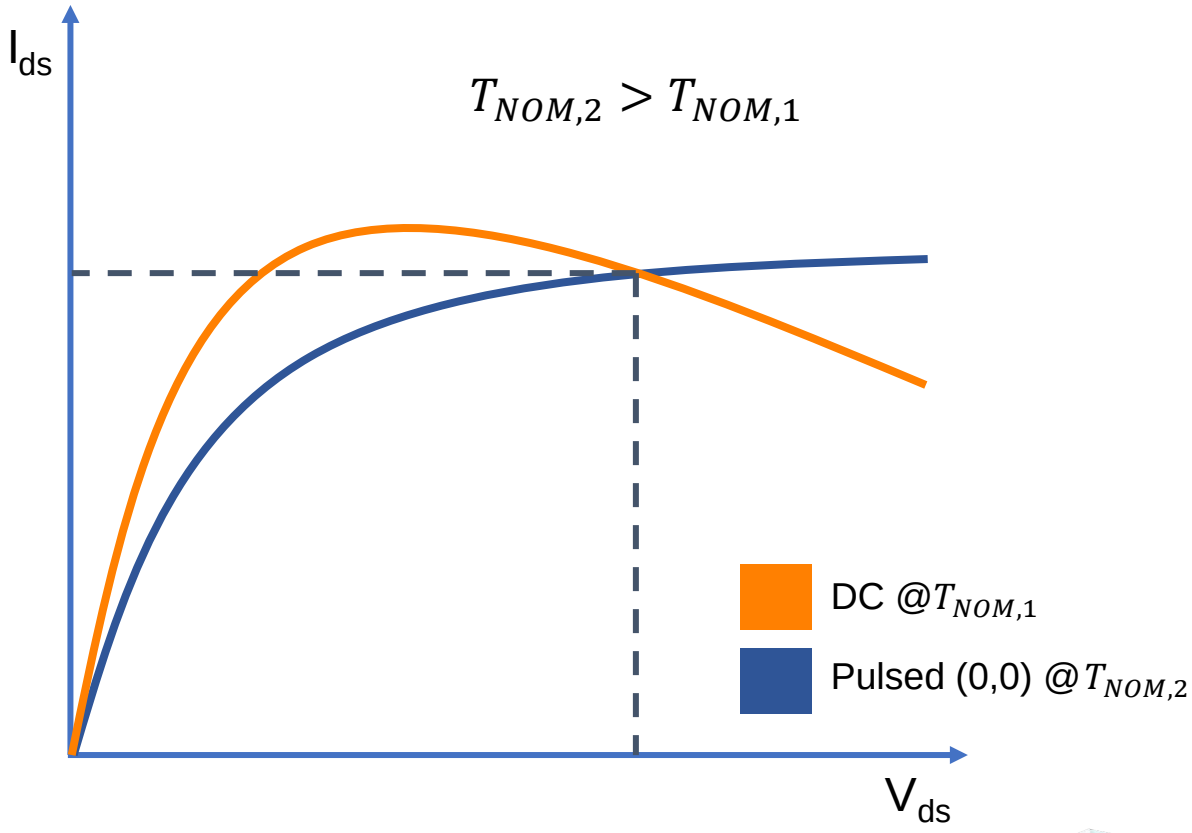
At the intersection point:

$$T_{J1} = T_{J2}$$

And $P_{diss2} = 0$ (Pulsed at (0,0))

$$\Rightarrow R_{th} = \Delta T_{NOM} / \Delta P_{diss}$$

With the ASM-HEMT model, the parameter **RTH0** is tuned till the simulated intersection point overlaps with the measured intersection point after thermal parameters like **UTE**, **AT** and **KT1** have been extracted.



Extracting R_{th} – Both curves are measured at the same Vgs. The intersection point denotes a common junction temperature.

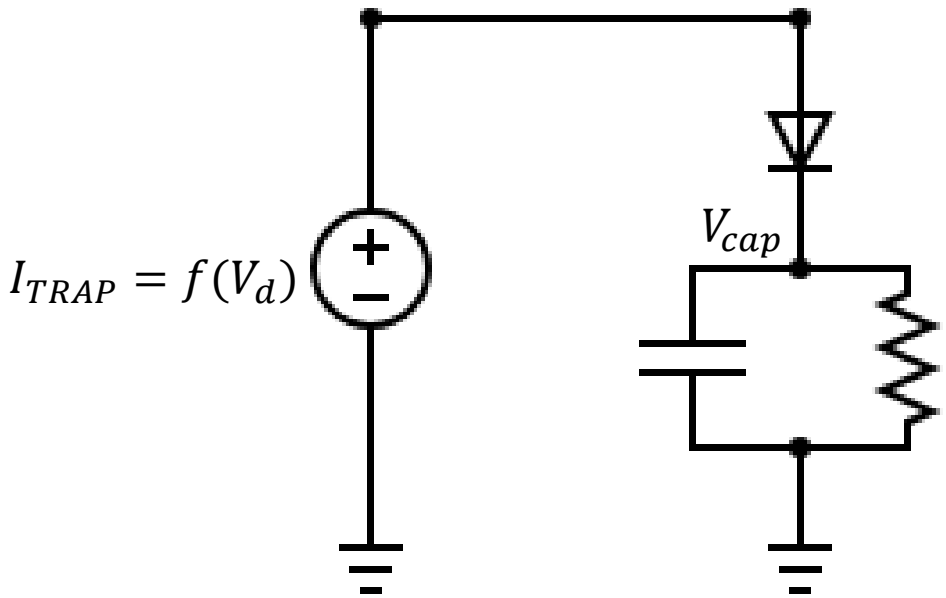
[1] T. Peyretaillade et al., 1997 IEEE MTT-S International Microwave Symposium Digest, Denver, CO, USA, 1997. doi: 10.1109/MWSYM.1997.596619.

Contents

Trapping models in ASM -HEMT

- *Trapping Models in ASM-HEMT*
- *Extraction using pulsed measurements*

Trapping Models in ASM -HEMT: TRAPMOD I



Key highlights

- Dependent on drain voltage only
- Bias-dependent and bias-independent options
- Scales with signal power levels
- Suitable for RF
- Affects threshold voltage, DIBL, AR Resistance.

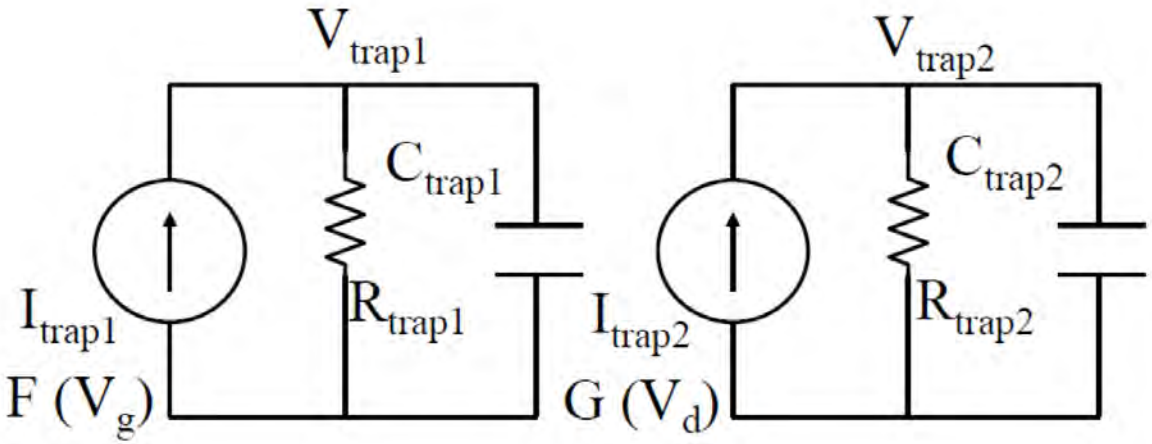
$$V_{OFF}(Trap) = V_{OFF} + (ATRAPVOFF + BTRAPVOFF \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_S(Trap) = R_S + (ATRAPRS + BTRAPRS \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_D(Trap) = R_D + (ATRAPRD + BTRAPRD \cdot e^{-\frac{1}{V_{cap}}})$$

$$\eta_0(Trap) = \eta_0 + (ATRAPETA0 + BTRAPETA0 \cdot e^{-\frac{1}{V_{cap}}})$$

Trapping Models in ASM -HEMT: TRAPMOD II



Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance
- Suitable for PIV simulation
- Affects threshold voltage, DIBL, Subthreshold Slope, AR Resistance.

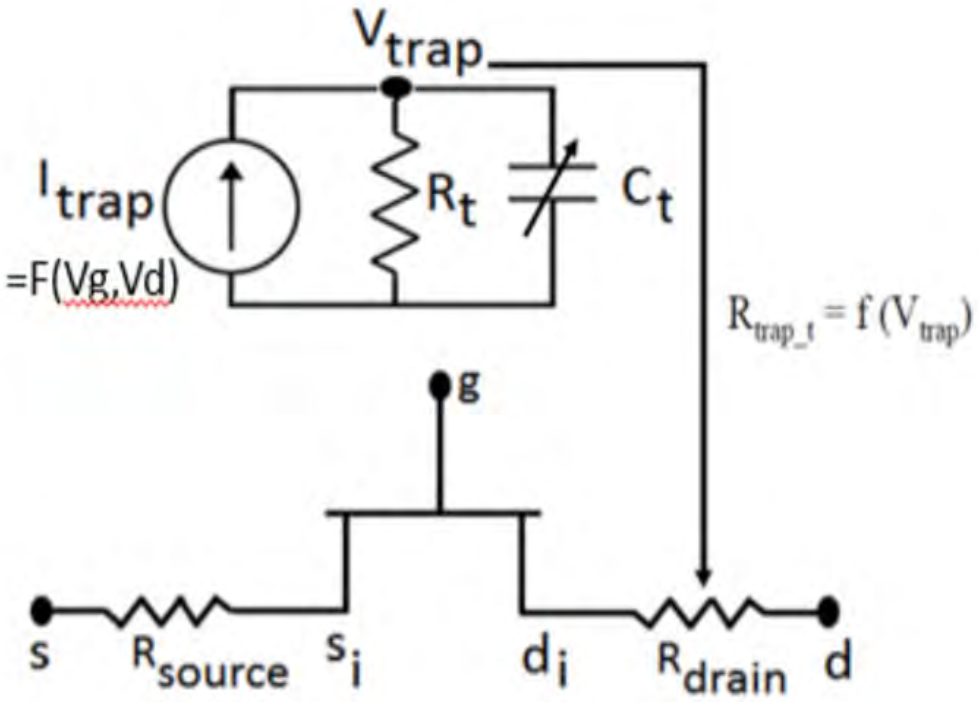
$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$

$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$

$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$

$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$

Trapping Models in ASM -HEMT: TRAPMOD Ⅲ

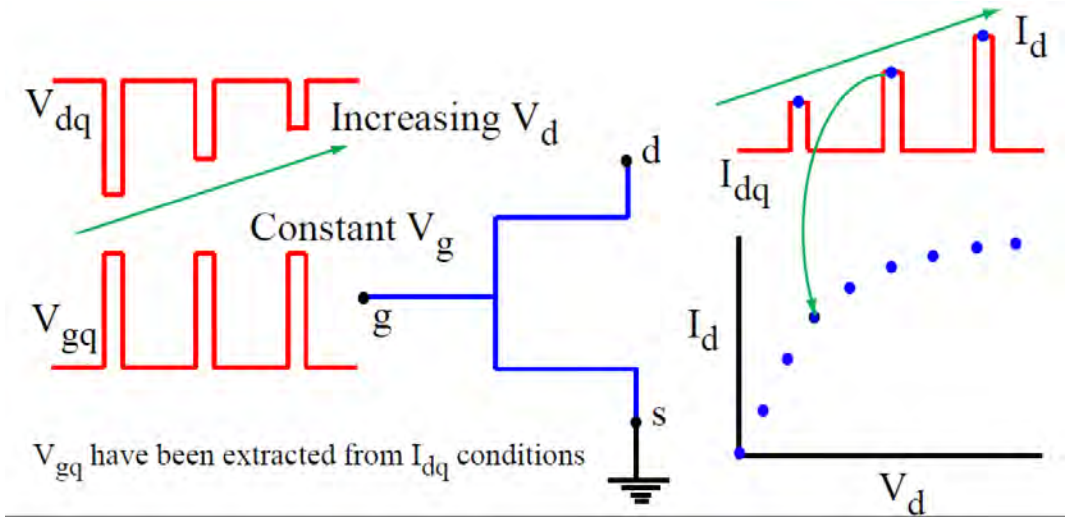


Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance for dynamic Ron
- Suitable for simulating Power Devices
- Incorporates temperature dependence.

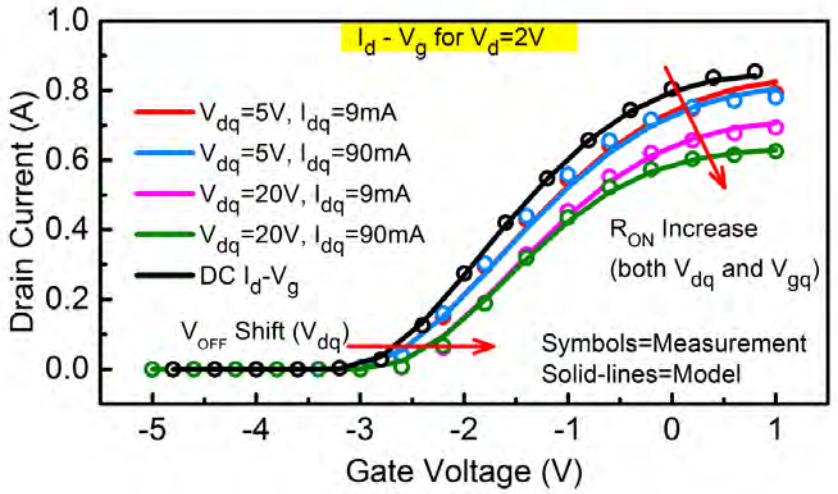
$$R_D(Trap) = R_D + \frac{V(trap1)}{VATRAP} \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{TALPHA}$$

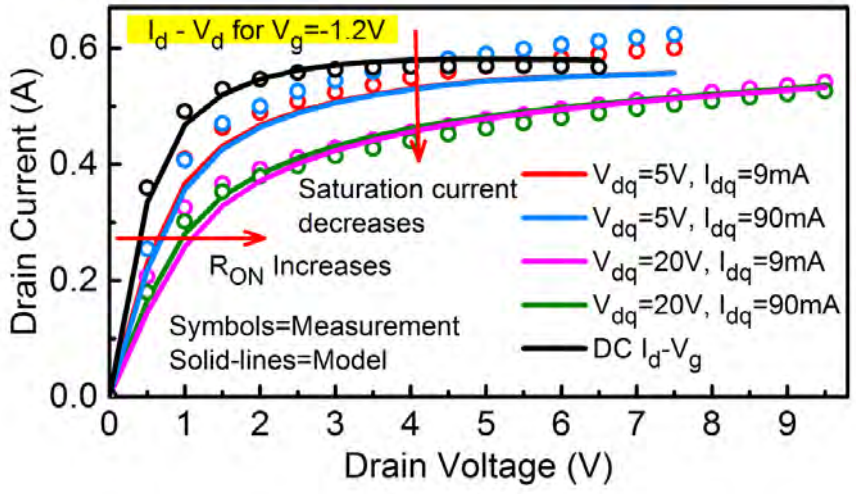
Extraction using pulsed measurements



Pulsed-IV Scheme used to simulate the P-IV Characteristics

- Pulsed IV characterization in dual-pulse mode at a pulse frequency of 1000 Hz with a duty-cycle of 0.02 %is performed under multiple quiescent drain and gate bias conditions such that both the gate and the drain voltages are pulsed simultaneously from the quiescent bias point.
- The pulse width of 200 ns and the measurement window of 40 ns within these 200 ns is short enough to ensure iso-thermal and iso-dynamic measurement of the pulsed-IV characteristics.





Pulsed – IV chacteristics for multiple quiescent conditions – using TRAPMOD II

Related Publications

Publications

1	S. Khandelwal, Y. S. Chauhan, T. A. Fjeldly, S. Ghosh, A. Pampori, D. Mahajan, R. Dangi, and S. A. Ahsan, "ASM GaN: Industry Standard Model for GaN RF and Power Devices - Part-I: DC, CV, and RF Model", IEEE Transactions on Electron Devices, 2019.
2	S. A. Albahrani, D. Mahajan, J. Hodges, Y. S. Chauhan, and S. Khandelwal, "ASM GaN: Industry Model for GaN RF and Power Devices - Part-II: Modeling of Charge Trapping", IEEE Transactions on Electron Devices, 2019.
3	A. Pampori, S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Compact Modeling of MSM-2DEG GaN-based Varactors for THz Applications", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Kobe, Japan, Mar. 2018.
4	S. A. Ahsan, A. Pampori, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "A New Small-signal Parameter Extraction Technique for large gate-periphery GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 10, Oct. 2017.
5	S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Multi-bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow", IEEE Journal of the Electron Devices Society, Vol. 5, Issue 5, Sept. 2017.
6	S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Pole-Zero Approach to Analyze and Model the Kink in Gain-Frequency Plot of GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 3, Mar. 2017.
7	S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Cross-Coupling and Substrate Capacitance in GaN HEMTs for Power-Electronic Applications", IEEE Transactions on Electron Devices (Special Issue), Vol. 64, Issue 3, Mar. 2017.
8	S. Ghosh, S. A. Ahsan, S. Khandelwal, A. Pampori, R. Dangi, and Y. S. Chauhan, "Physics Based Analysis and Modeling of Capacitances in a Dual Field Plated Power GaN HEMT", International Workshop on Physics of Semiconductor Devices (IWPSD), Delhi, India, Dec. 2017.
9	S. A. Ahsan, S. Ghosh, S. Khandelwal, A. Pampori, R. Dangi, and Y. S. Chauhan, "A Scalable Physics-based RF Large Signal Model for Multi-Finger GaN HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Delhi, India, Dec. 2017.
10	S. Khandelwal, S. Ghosh, S. A. Ahsan and Y. S. Chauhan, "Dependence of GaN HEMT AM/AM and AM/PM Non-Linearity on AlGaN Barrier Layer Thickness", IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpur, Malaysia, Nov. 2017.

Publications

11	S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Surface-potential-based Gate-periphery-scalable Small-signal Model for GaN HEMTs", IEEE Compound Semiconductor IC Symposium (CSICS), Miami, USA, Oct. 2017.
12	S. A. Ahsan, S. Ghosh, A. Dasgupta, K. Sharma, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling in Dual Field Plate Power GaN HEMT for Accurate Switching Behaviour", IEEE Transactions on Electron Devices, Vol. 63, Issue 2, Feb. 2016.
13	S. Ghosh, S. A. Ahsan, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "GaN HEMT Modeling for Power and RF Applications using ASM-HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
14	S. Ghosh, A. Dasgupta, A. K. Dutta, S. Khandelwal, and Y. S. Chauhan, "Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
15	S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Statistical Simulation for GaN HEMT Large Signal RF performance using a Physics-based Model", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
16	A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, N. Defrance, and Y. S. Chauhan, "Modeling DC, RF and Noise behavior of GaN HEMTs using ASM-HEMT Compact Model", IEEE International Microwave and RF Conference (IMaRC), Delhi, India, Dec. 2016.
17	S. Ghosh, S. A. Ahsan, S. Khandelwal and Y. S. Chauhan, "Modeling of Source/Drain Access Resistances and their Temperature Dependence in GaN HEMTs", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
18	S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Modeling of Kink-Effect in RF Behaviour of GaN HEMTs using ASM-HEMT Model", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
19	R. Nune, A. Anurag, S. Anand and Y. S. Chauhan, "Comparative Analysis of Power Density in Si MOSFET and GaN HEMT based Flyback Converters", IEEE International Conference on Compatibility and Power Electronics, Bydgoszcz, Poland, June 2016.
20	S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan, "Surface-Potential-Based Compact Modeling of Gate Current in AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 62, Issue 2, Feb. 2015.

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21	S. Agnihotri, S. Ghosh, A. Dasgupta, A. Ahsan, S. Khandewal, and Y. S. Chauhan, "Modeling of Trapping Effects in GaN HEMTs", IEEE India Conference (INDICON), New Delhi, India, Dec. 2015.
22	S. Ghosh, S. Agnihotri, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Trapping Effects in RF GaN HEMTs under Pulsed Conditions", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
23	K. Sharma, S. Ghosh, A. Dasgupta, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Capacitance Analysis of Field Plated GaN HEMT", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
24	S. A. Ahsan, S. Ghosh, J. Bandarupalli, S. Khandelwal, and Y. S. Chauhan, "Physics based large signal modeling for RF performance of GaN HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
25	S. A. Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling of a GaN HEMT with Gate and Source Field Plates", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015..
26	A. Dasgupta, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "ASM-HEMT: Compact model for GaN HEMTs", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 2015.
27	K. Sharma, A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Effect of Access Region and Field Plate on Capacitance behavior of GaN HEMT", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, June 2015.
28	C. Yadav, P. Kushwaha, S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling of GaN based Normally-off FinFET", IEEE Electron Device Letters, Vol. 35, Issue 6, June 2014.
29	C. Yadav, P. Kushwaha, H. Agarwal, and Y. S. Chauhan, "Threshold Voltage Modeling of GaN Based Normally-Off Tri-gate Transistor", IEEE India Conference (INDICON), Pune, India, Dec. 2014.
30	S. Khandelwal, C. Yadav, S. Agnihotri, Y. S. Chauhan, A. Curutchet, T. Zimmer, J.-C. Dejaeger, N. Defrance and T. A. Fjeldly, "A Robust Surface-Potential-Based Compact Model for GaN HEMT IC Design", IEEE Transactions on Electron Devices, Vol. 60, Issue 10, Oct. 2013.

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31	S. Agnihotri, S. Ghosh, A. Dasgupta, S. Khandewal, and Y. S. Chauhan, "A Surface Potential based Model for GaN HEMTs", IEEE PrimeAsia, Visakhapatnam, Dec. 2013.
32	S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, "Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices", IEEE Transactions on Electron Devices, Vol 59, Issue 8, Oct. 2012.

Thank You!

Questions