Modeling and Simulation of Negative Capacitance Transistors

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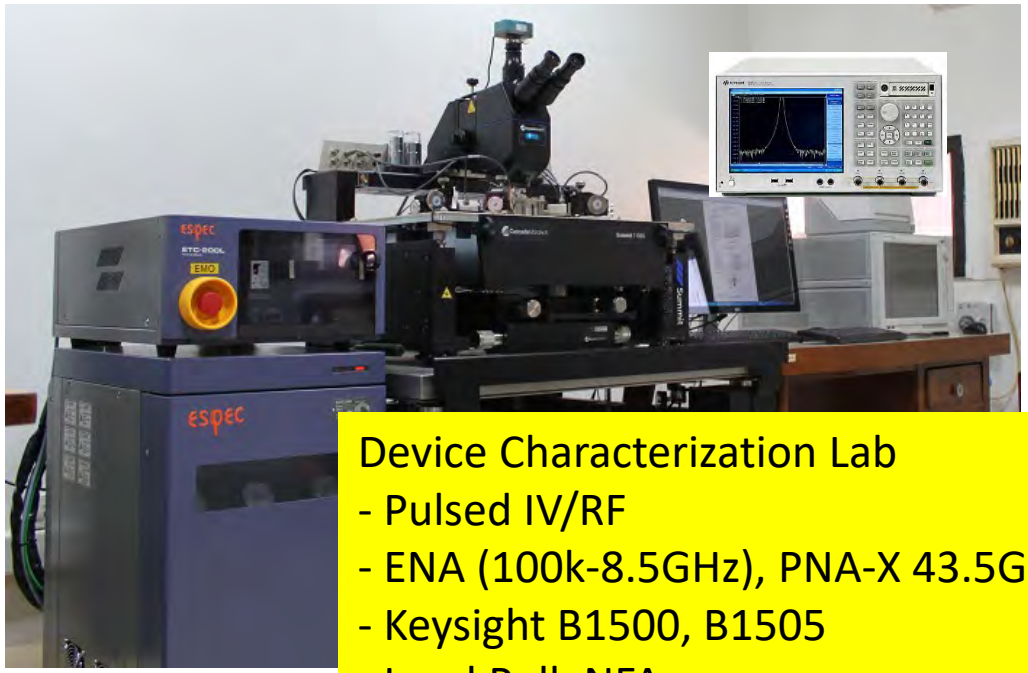
My Group and Nanolab

Current members – 38

- Postdoc – 3
- Ph.D. – 27
- 12 PhD graduated

	2021	2020	2019	2018	2017
Books			1		
Journal	17	16	14	20	19
Conference	5	11	15	19	11

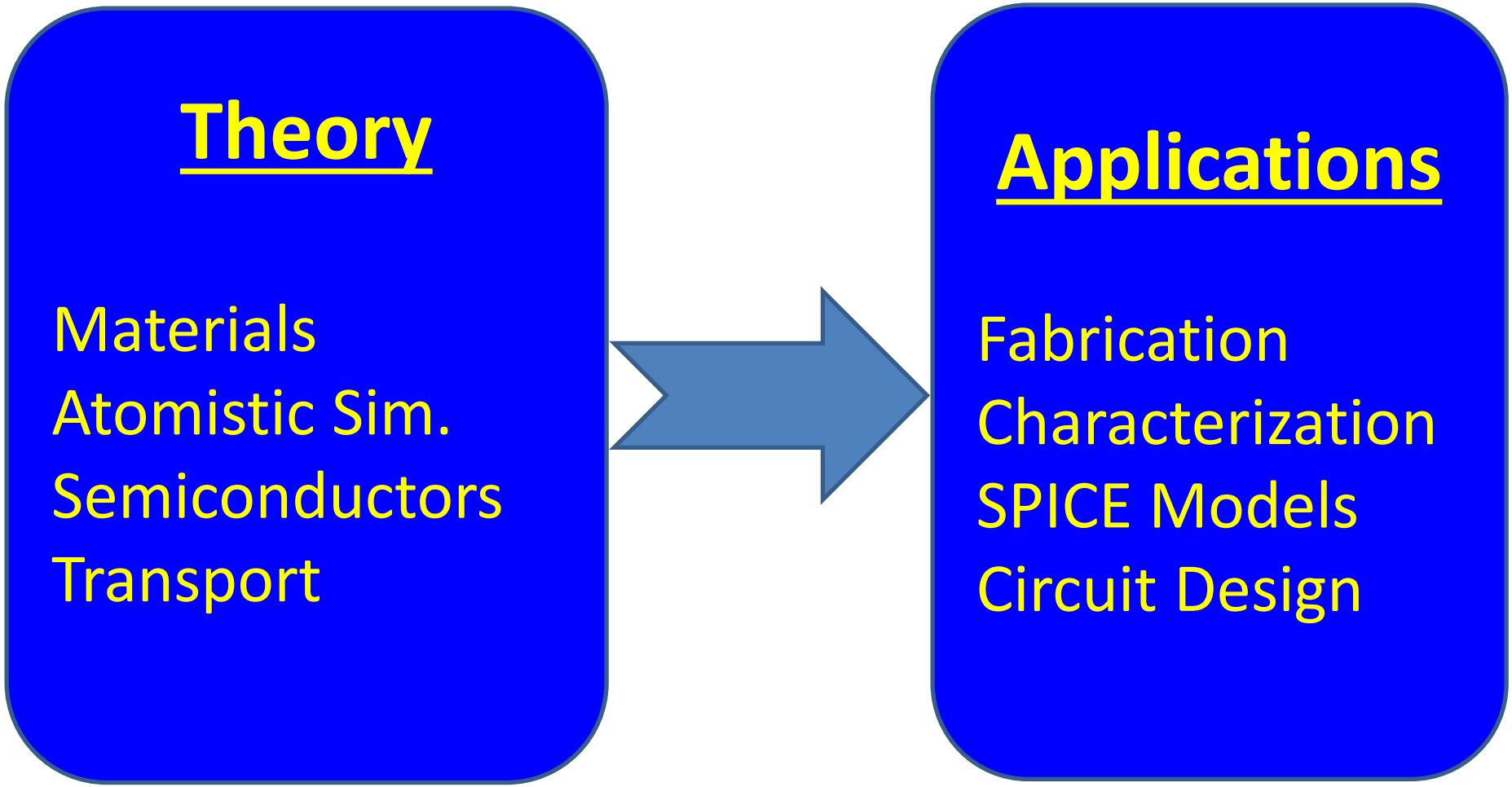


Device Characterization Lab
- Pulsed IV/RF
- ENA (100k-8.5GHz), PNA-X 43.5GHz
- Keysight B1500, B1505
- Load Pull, NFA

Alumni (PhD) of Nanolab

S. No.	Year	Name	Current Status
12.	2021*	Dinesh R.	Postdoc at UC Berkeley
11	2021*	Chetan Dabhi	Postdoc at UC Berkeley
10.	2020	Girish Pahwa	Postdoc at UC Berkeley
9.	2020	Shantanu Agnihotri	Asst. Prof. at Bennett University
8.	2020	Chetan Gupta	Micron Hyderabad
7.	2018	Priyank Rastogi	Intel Bangalore
6.	2018	Prateek Jain	Postdoc at IIT Bombay
5.	2018	Avirup Dasgupta	Asst. Prof. at IIT Roorkee
4.	2017	Sheikh Aamir Ahsan	Asst. Prof. at NIT Srinagar
3.	2017	Chandan Yadav	Asst. Prof. at NIT Calicut
2.	2017	Harshit Agarwal	Asst. Prof. at IIT Jodhpur
1.	2017	Pragya Kushwaha	SAC, ISRO

Nanolab@IITK:
From Theory to Applications

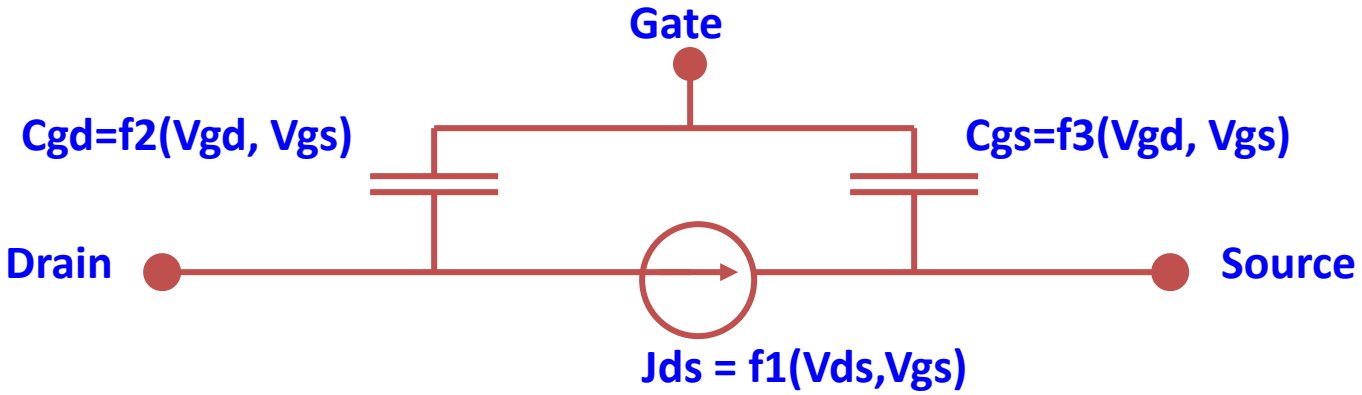


Joint Development & Collaboration

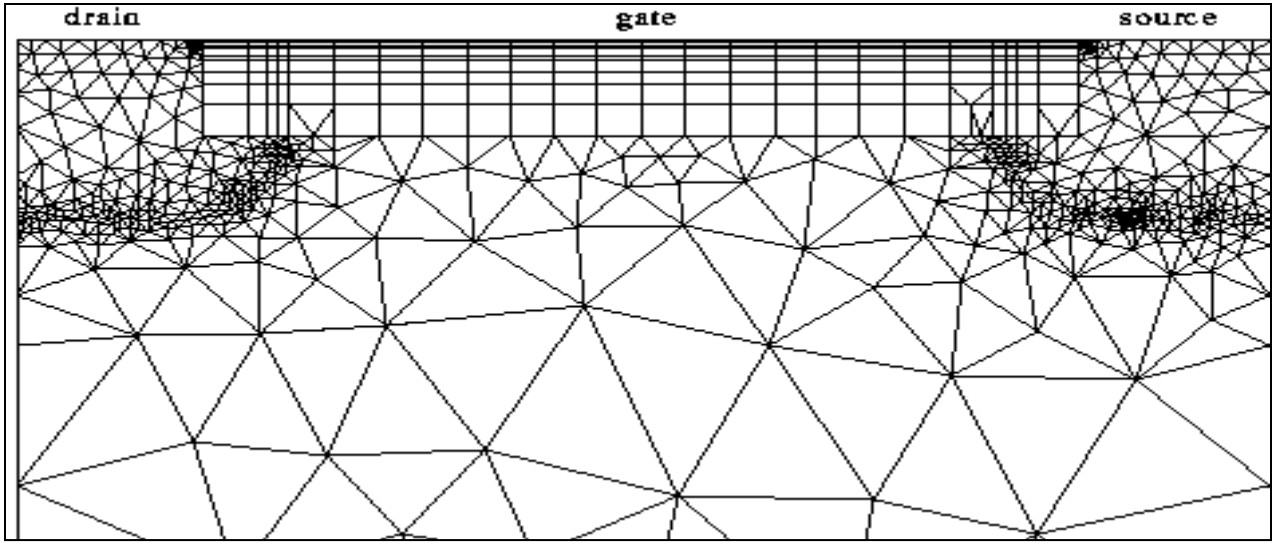
What is a Compact Model?

Compact MOSFET Model

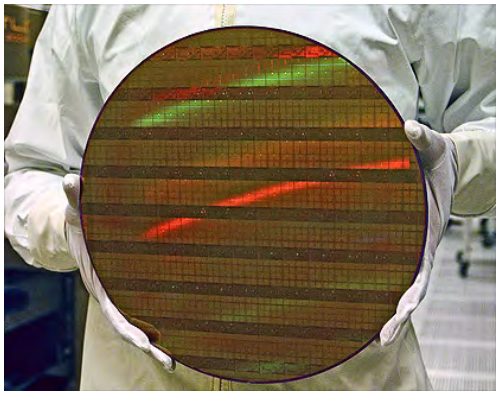
Compact Model



TCAD Model



Compact Modeling or SPICE Modeling



Medium of information exchange

- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~µs*ec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM-BULK, BSIM-CMG, BSIM-IMG

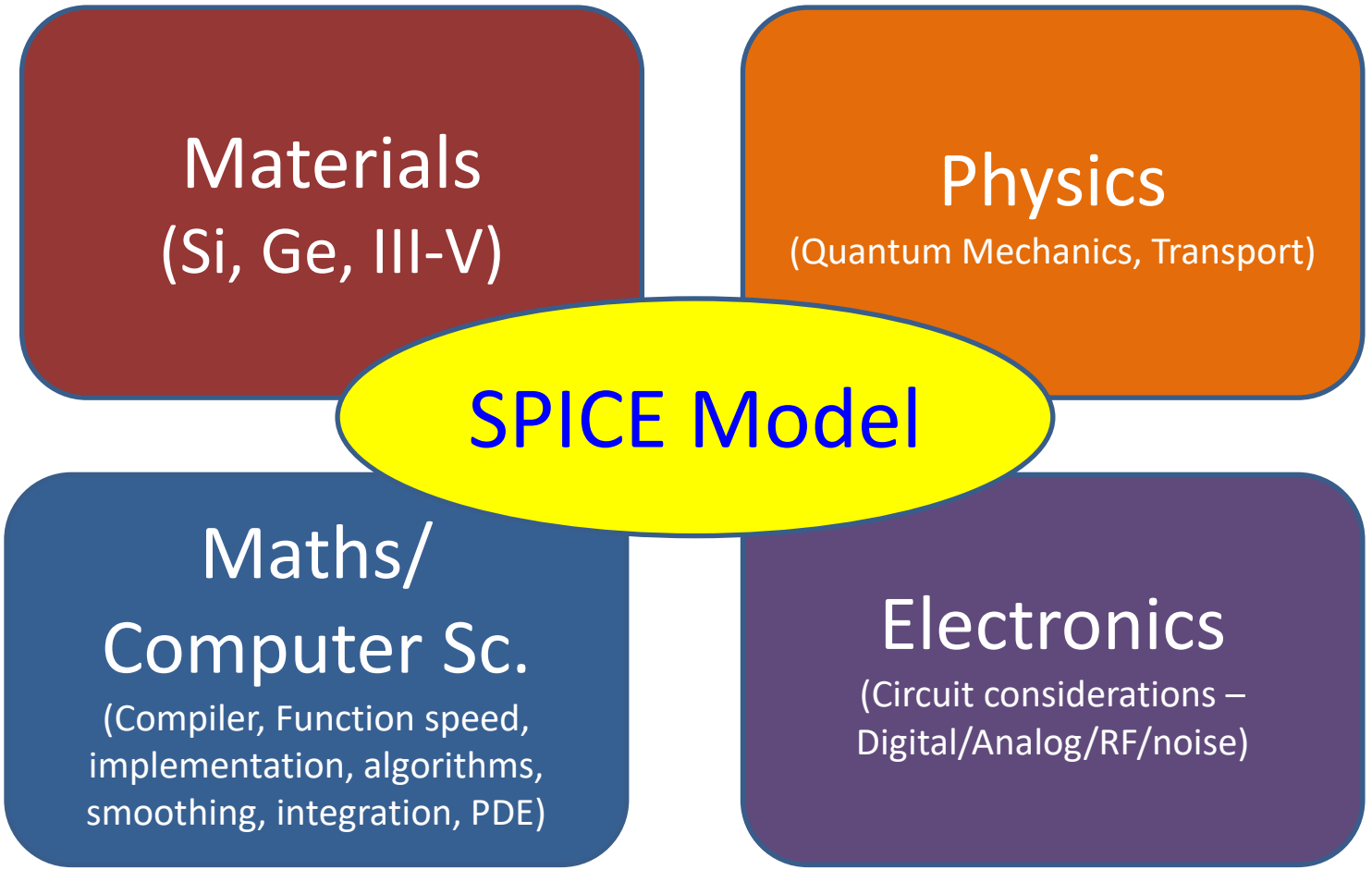
Industry Standard Compact Models

- Standardization Body – Compact Model Coalition

- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

http://www.si2.org/cmc/

Challenges in Compact Modeling

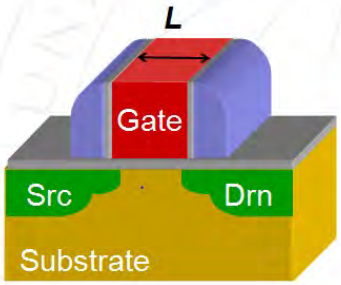


Some Snapshots from recent work

BSIM Family of Compact Device Models

1990 1995 2000 2005 2010

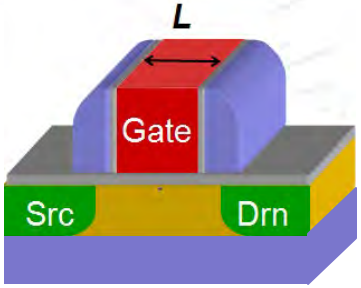
BSIM1,2 BSIM3



BSIM4

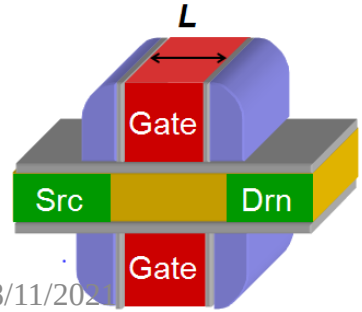
Conventional MOSFET

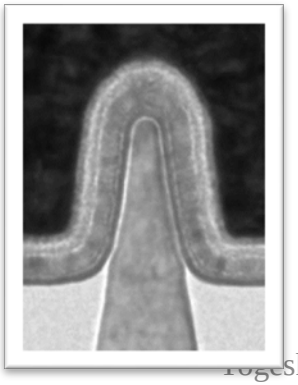
BSIM5 BSIM-BULK



Silicon on Insulator MOSFET

BSIMSOI





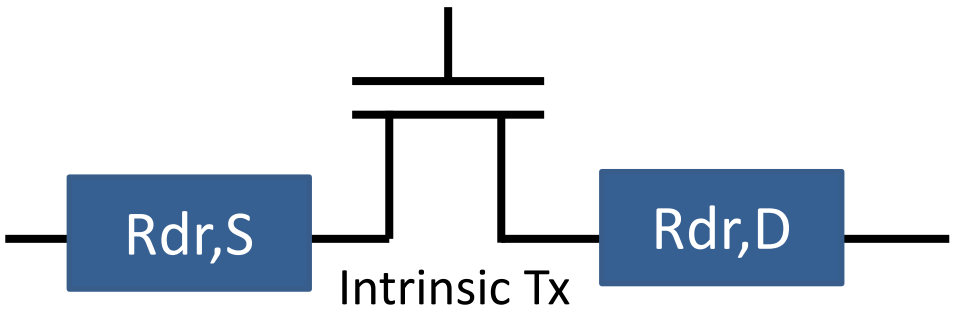
BSIM-CMG

BSIM-IMG

Multi-Gate MOSFETs

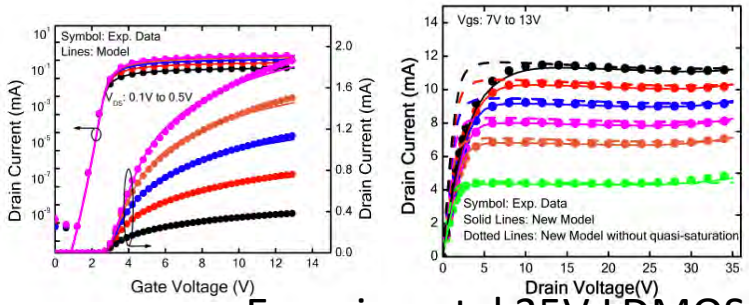
BSIM: Berkeley Short-channel IGFET Model

BSIM-HV: High Voltage MOSFET Model

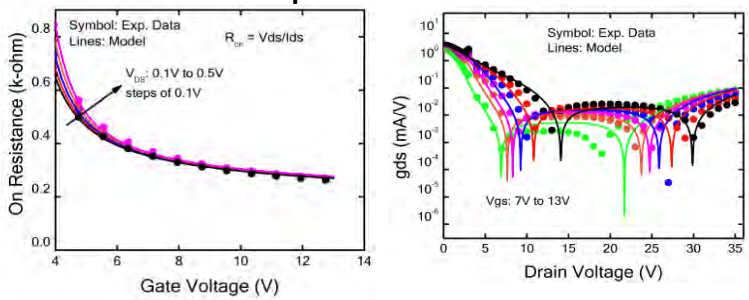


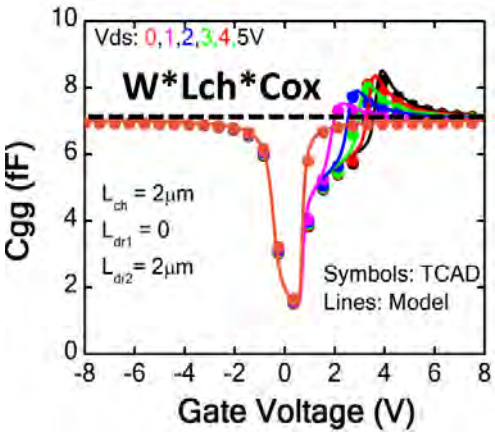
$$R_{dr,D} = \frac{RDLCW}{\left[1 - \delta_{HV}\left\{\frac{I_{ds}}{I_{dr,sat,D}}\right\}^{MDRIFT}\right]^{\frac{1}{MDRIFT}}}$$

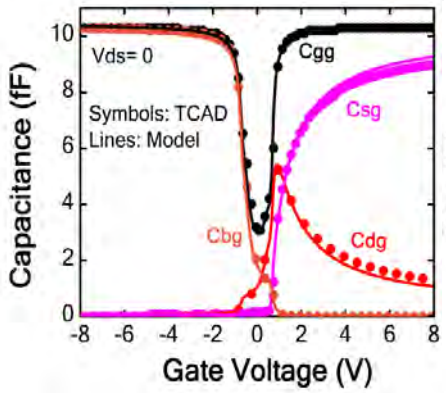
$$I_{dr,sat,D} = q * NDRIFTD * W_{eff} * VDRIFT$$

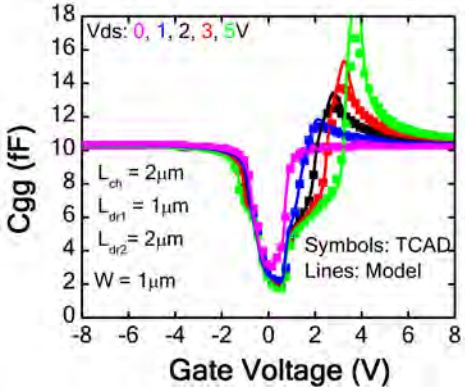


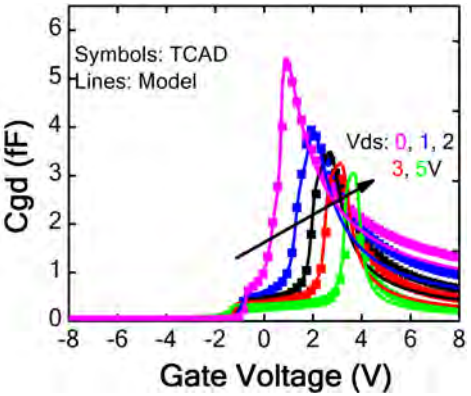
Experimental 35V LDMOS







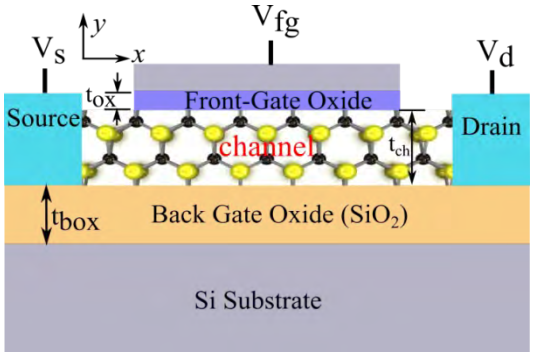


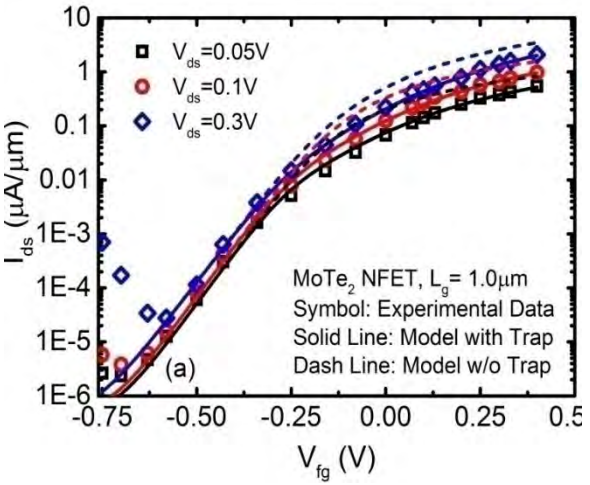


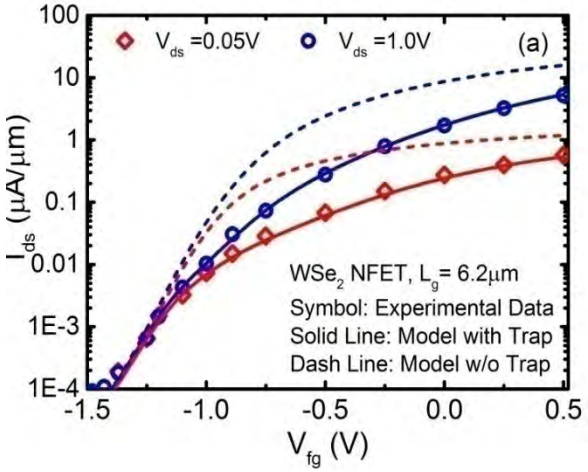
H. Agarwal, C. Gupta, R. Goel, P. Kushwaha, Y.-K. Lin, M.-Y. Kao, J.-P Duarte, H.-L. Chang, Y. S. Chauhan, S. Salahuddin, and C. Hu, "BSIM-HV: High Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect", IEEE Transactions on Electron Devices, Vol. 66, Issue 10, pp. 4258-4263, Oct. 2019.

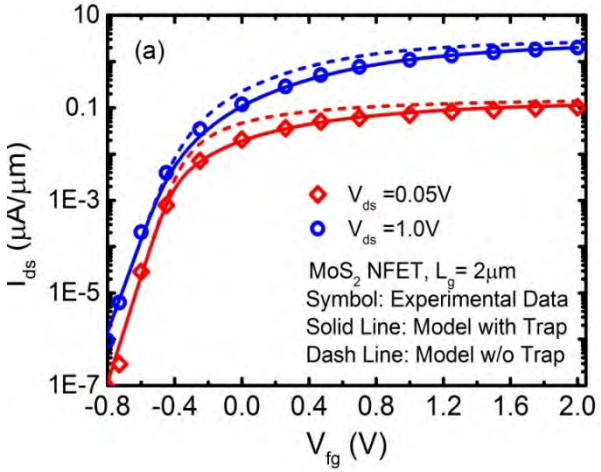
Modeling of TMD transistor

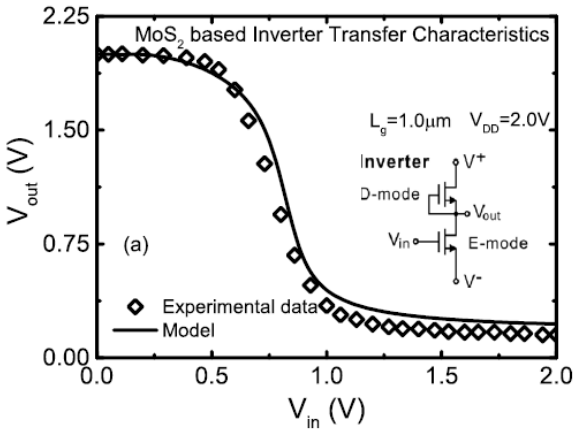
- 2D density of state
- Fermi–Dirac statistics
- Trapping effects











C. Yadav et. al. "*Compact Modeling of Transition Metal Dichalcogenide based Thin body Transistors and Circuit Validation*", IEEE TED, March 2017.

Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

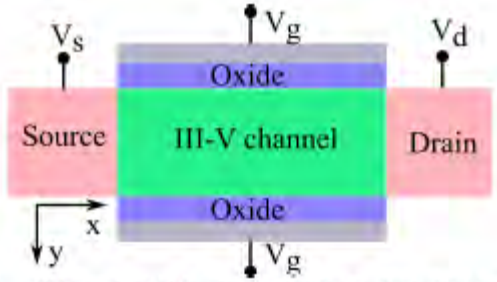
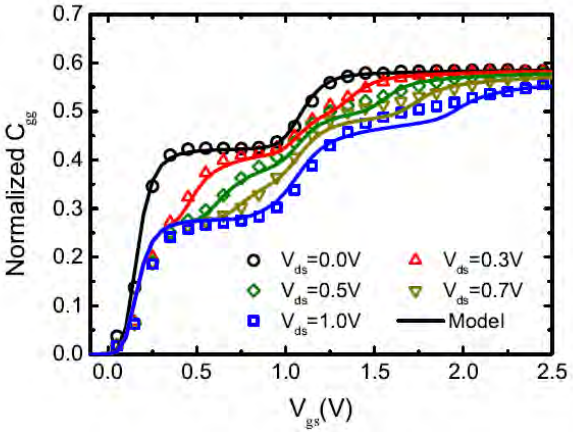
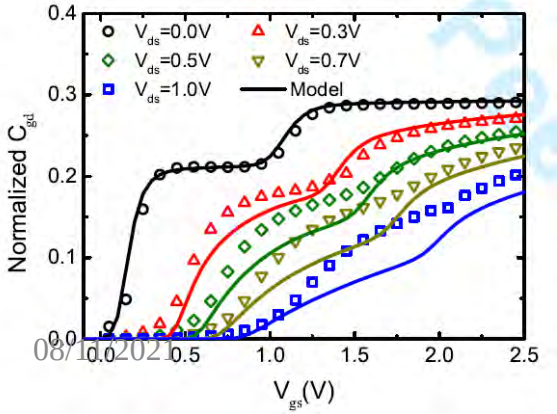
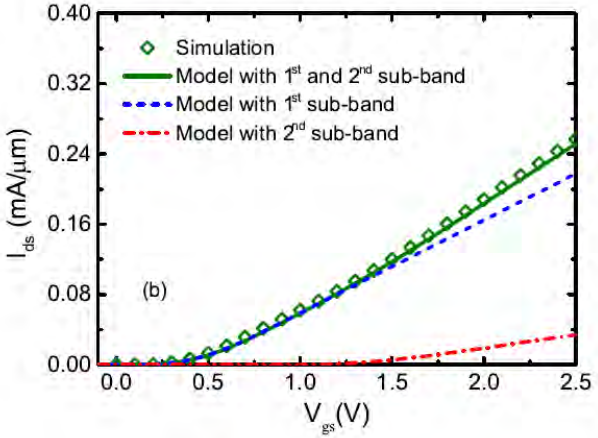
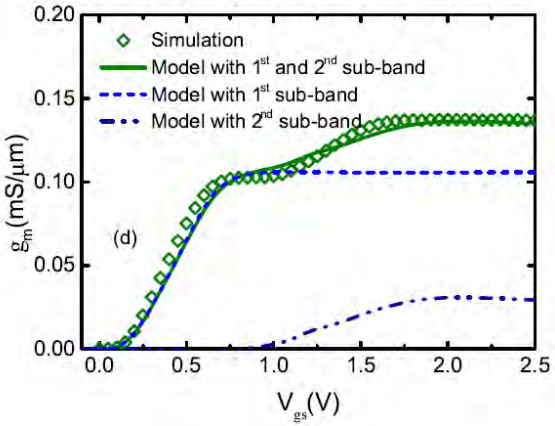


Fig. 1. Schematic of III-V channel double-gate field effect transistor (DGFET) used in the study where V_g, V_d and V_s denotes the applied voltage at gate, drain and source terminals, respectively.



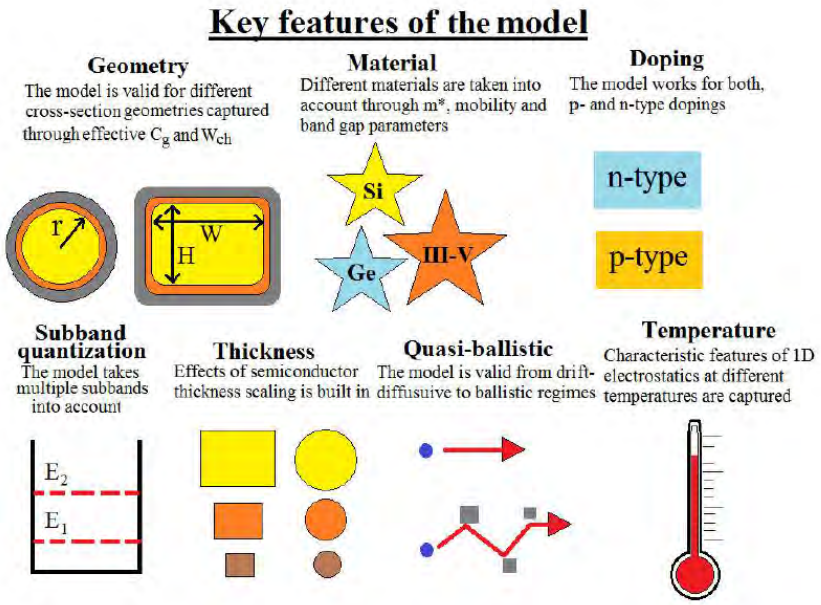


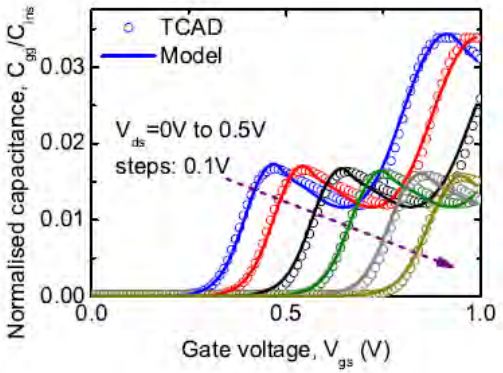


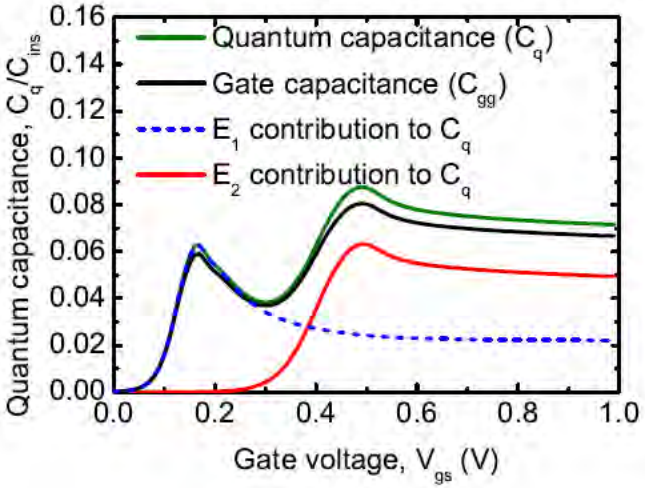


C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.

Modeling of Quasi-ballistic Nanowire FETs







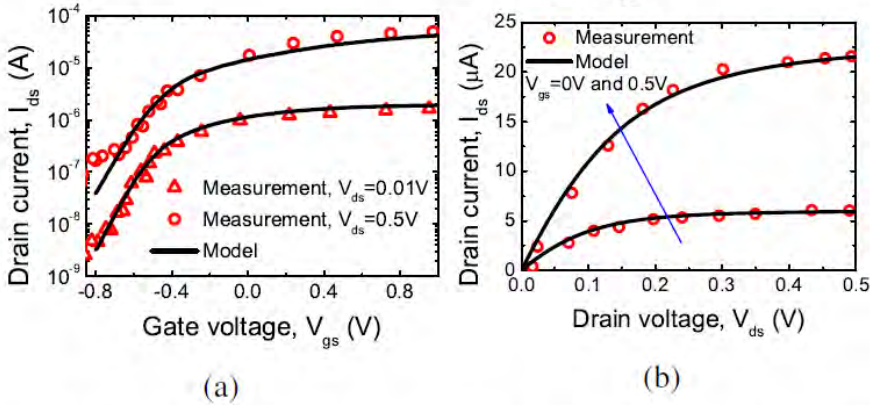


Fig. 12: **Circular quasi-ballistic InAs nanowire:** Drain current as a function of the gate and drain voltages for n-type $InAs$ nanowires, with a circular cross-section ($r = 7.5nm$), $L_g = 100nm$ and $EOT = 0.92nm$ (Device 5)[44], are shown in (a) and (b) respectively. Device works in the quasi-ballistic regime. Relevant parameter values are specified in Table II. Short channel effect related parameters have been used as in [19], [20].

A. Dasgupta et al., "An Improved Model for Quasi-Ballistic Transport in MOSFETs", IEEE TED, Jul. 2017.

A. Dasgupta et al., "Unified Compact Model for Nanowire Transistors including Quantum Effects and Quasi-ballistic Transport", IEEE TED, Apr. 2017.

IMT PhaseFET Including Hysteresis and Multidomain Switching

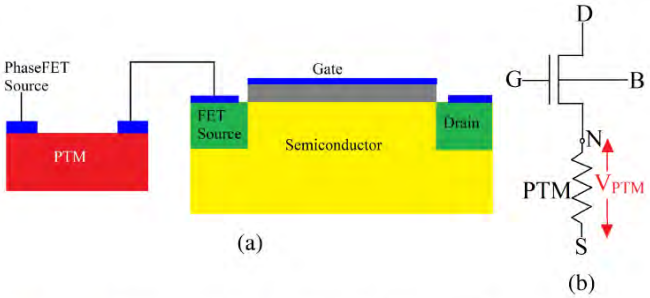


Fig. 1. (a) Graphical representation of a PhaseFET with an insulator–metal PTM at the source. (b) Schematic of a PhaseFET used for the simulations in this paper [4], [8], [9].

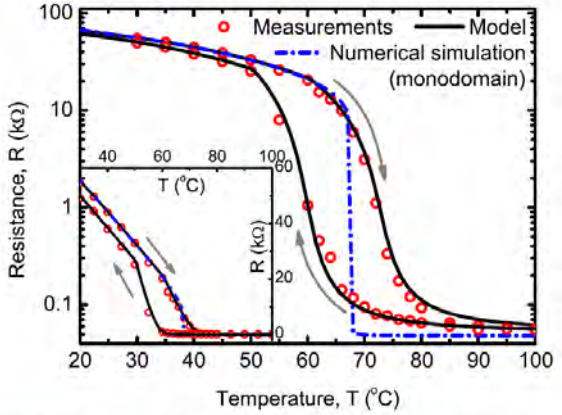


Fig. 2. Experimental data (symbols) and the model results (solid black) showing the variation of the resistance with temperature for a VO_2 resistor of 20-μm length and 100-μm width in log and linear (inset) scales [17]. The behavior smoothly changes from semiconductorlike to metallic with increasing temperature. Prediction from a single-domain-based numerical simulation (dotted blue), which shows sharp switching and no hysteresis, as suggested by the Landau theory [19], [20]. Our multidomain model is able to match the measurement, including the hysteresis, with a good accuracy.

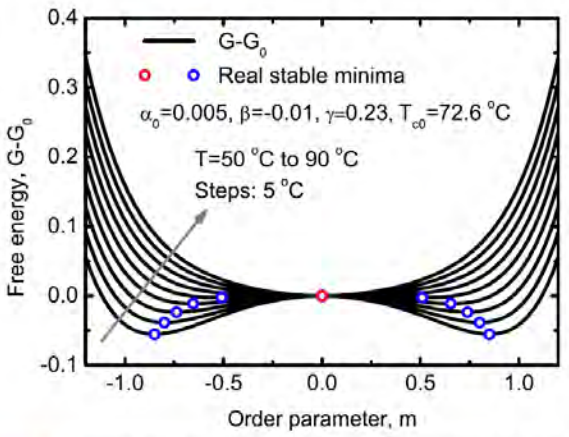
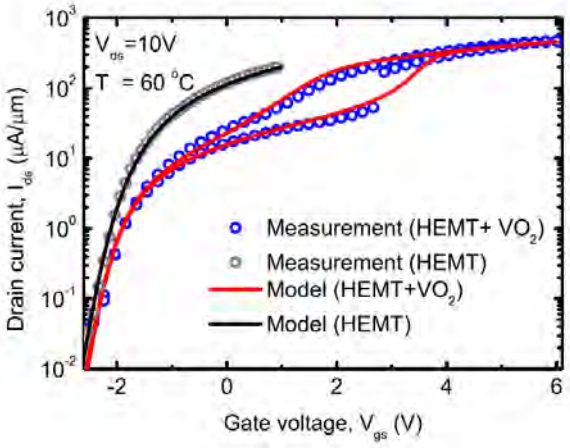
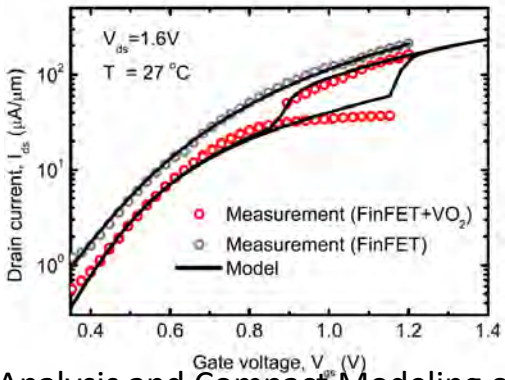


Fig. 3. Effective free energy illustrating the two real solutions to (1) in the form of the two stable minima (blue symbols) at low temperatures. With increasing temperature, the system exhibits only one stable minima (red symbol), giving rise to a switching behavior as shown in Fig. 2.





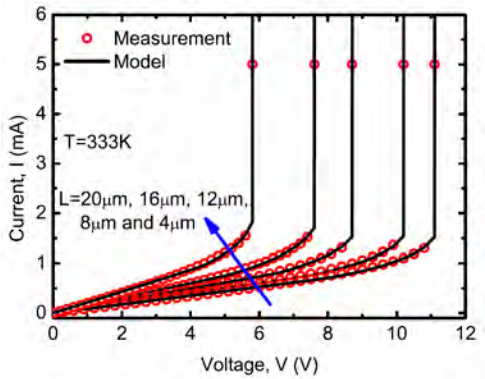
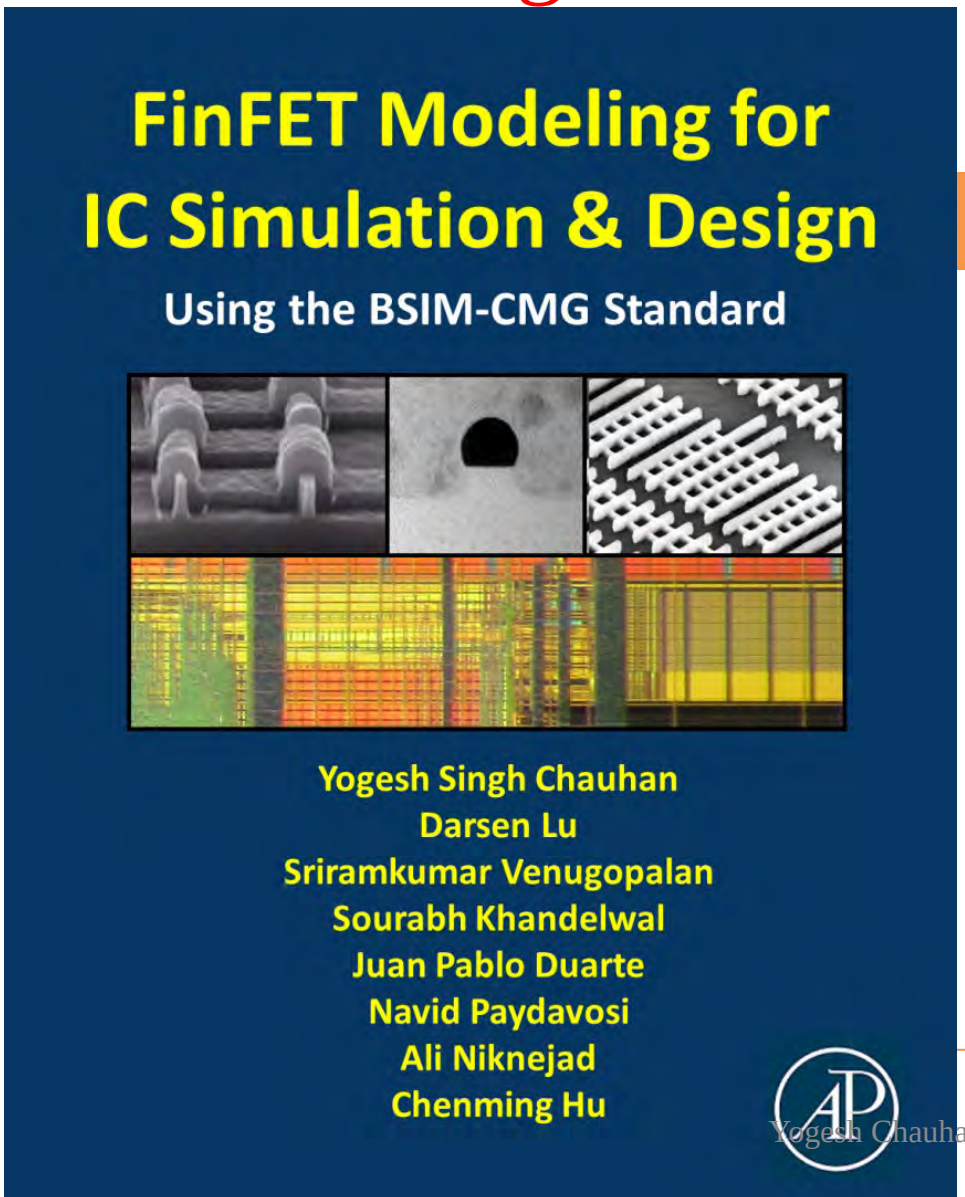


Fig. 6. Experimental data along with model prediction for *I–V* characteristics of 100-μm wide VO_2 resistors of different lengths, such as L = 20, 16, 12, 8, and 4 μm, at T = 60 °C [17]. The self-heating model captures the variation of device temperature with applied voltage and current flow, enabling accurate modeling of the device behavior. Parameter values are listed in Table I.

A. Dasgupta, A. Verma, and Y. S. Chauhan, "Analysis and Compact Modeling of Insulator-Metal-Transition Material based PhaseFET Including Hysteresis and Multi-domain Switching", IEEE TED, Jan. 2019.

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard



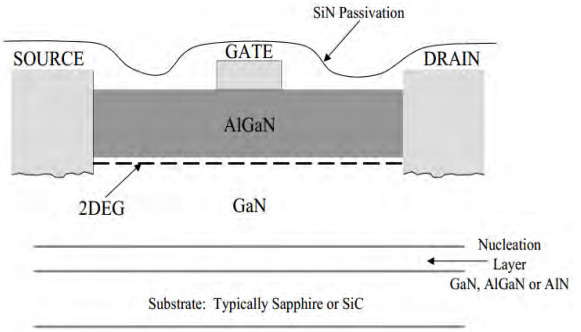
Chapters

Industry Standard FDSOI Compact Model BSIM-IMG for IC Design

Chapters

1. Fully Depleted Silicon on Oxide Transistor and Compact Model
2. Core Model for Independent Multigate MOSFETs
3. Channel Current Model With Real Device Effects in BSIM-IMG
4. Leakage Current and Thermal Effects
5. Model for Terminal Charges and Capacitances in BSIM-IMG
6. Parameter Extraction With BSIM-IMG Compact Model
7. Testing BSIM-IMG Model Quality
8. High-Frequency and Noise Models in BSIM-IMG

News (March 2018)



- Our ASM-GaN-HEMT Model is world's first industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

Si
Compact Models

Si2 Approves IC Design Simulation Standards for Gallium Nitride Devices

March 14, 2018 / 0 Comments / in Compact Model, Frontpage /

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

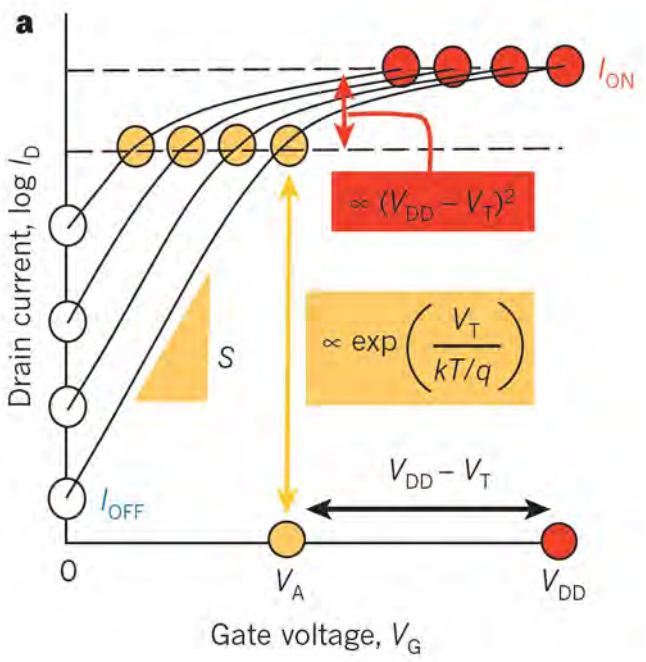
http://www.si2.org/cmc/

http://www.si2.org/2018/03/14/gallium-nitride-models/

Outline

- Motivation
- Understanding Negative Capacitance
- Experimental realization of Negative Capacitance
- NCFETs: Modeling and Analysis
- MFIS vs MFMIS configurations
  - Long Channel
  - Short Channel
- Performance of NCFET based Circuits
- Conclusion

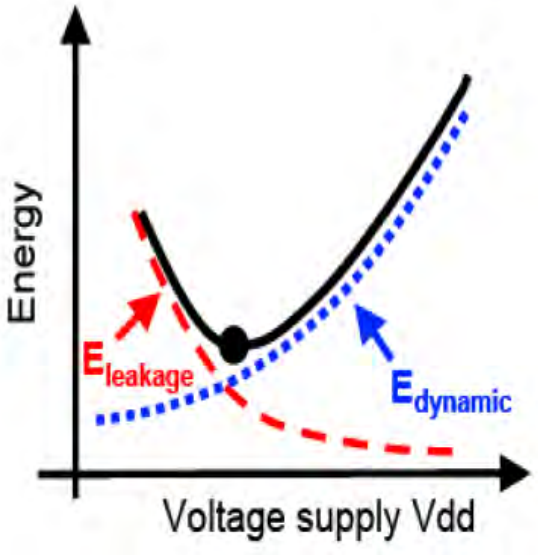
Power challenge



$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

$$I_{OFF} \propto 10^{\left(\frac{-V_{TH}}{SS}\right)}$$

$$P = C_L V_{DD}{}^2 \alpha f + I_{leakage} V_{DD} + P_{SC}$$



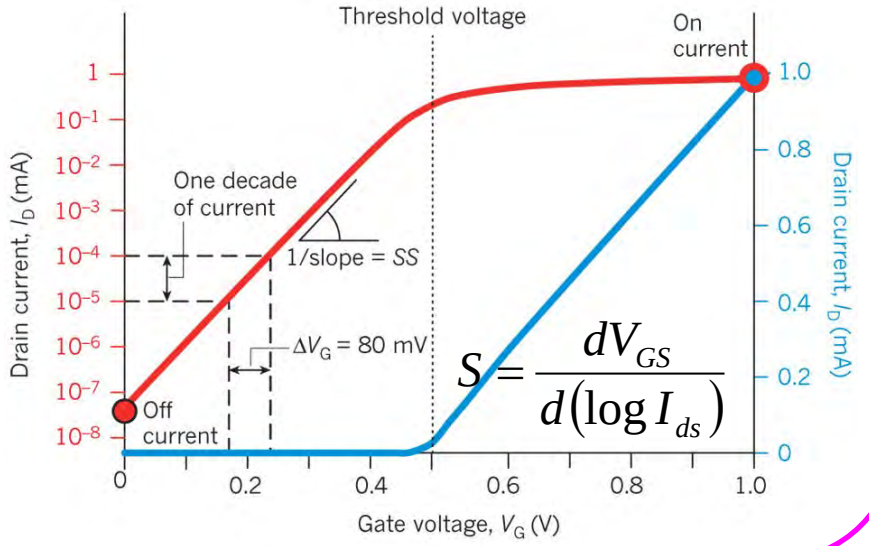
Scaling both the V_{DD} and V_T maintains same performance (I_{ON}) by keeping the overdrive (V_{DD} - V_T) constant.

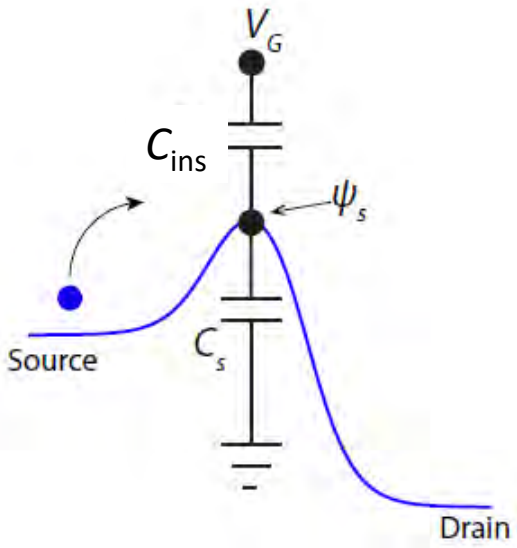
A.M. Ionescu, H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", *Nature* 479, 329 (2011)

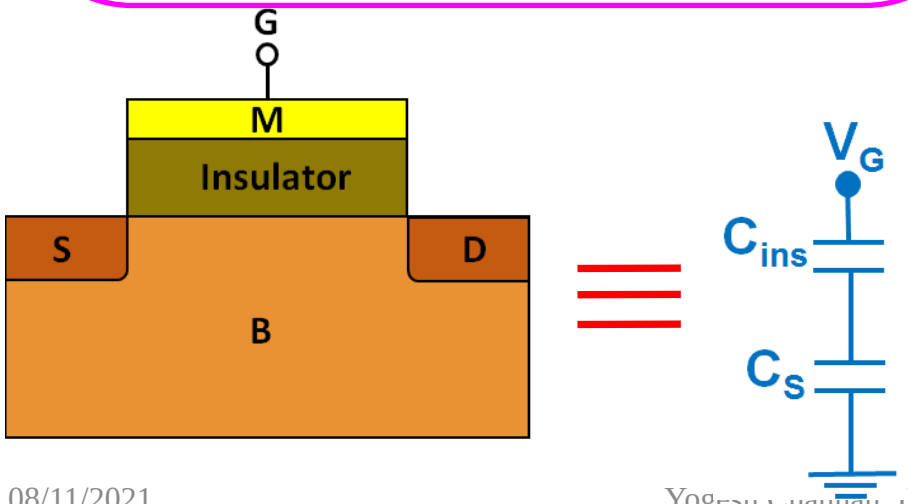
A. M. Ionescu, Kathy Boucart, "Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch", *IEDM 2009.*

Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.







$$S = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial \psi_S} \frac{\partial \psi_S}{\partial \log_{10} I_D}$$

$$= \left(1 + \frac{C_S}{C_{ins}}\right).60\text{mV/decade}$$

As $1 + \frac{C_S}{C_{ins}} \geq 1$, $S \geq 60mV/decade$

Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as
- 1: $C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1}$ = inverse curvature of free energy density
- 2: $C_{ins} = \frac{\partial P}{\partial E}$ = slope of the polarization vs electric field curve

P = Polarization in dielectric, G = Free energy density, E = Externally applied electric field

- Two types of non-linear dielectrics:
  - Paraelectric : No polarization when electric field is removed.
  - Ferroelectric : Two possible states of polarization when electric field is removed.

Capacitance Definition

Charge-Voltage Relation

$$C = \frac{dQ}{dV}$$

If $C < 0$ → As V↓, Q↑

More Definitions

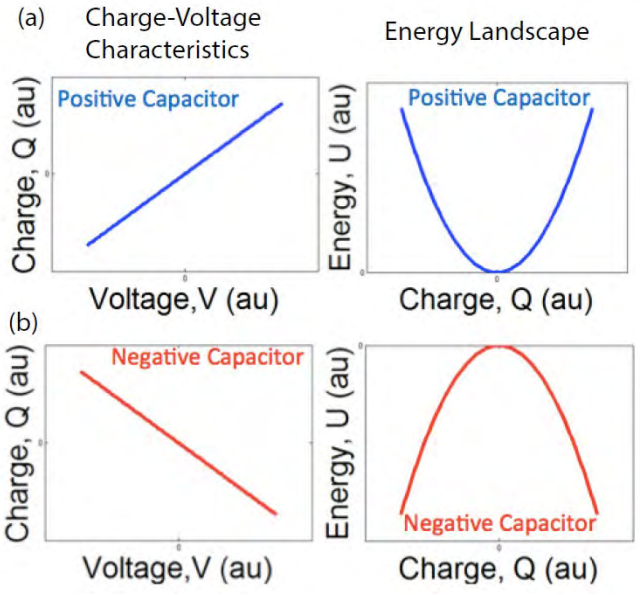
Capacitance of a general dielectric:

$$C = \left(\frac{\partial^2 G}{\partial Q^2}\right)^{-1}$$

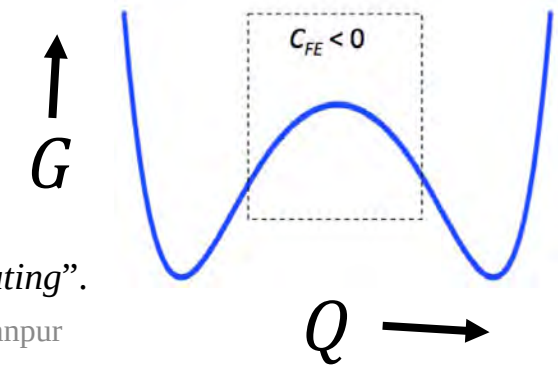
Inverse curvature of free energy density

G = Free energy density

Linear capacitor: Parabolic, $G = \frac{Q^2}{2C}$



Non-linear capacitor: e.g. Ferroelectric



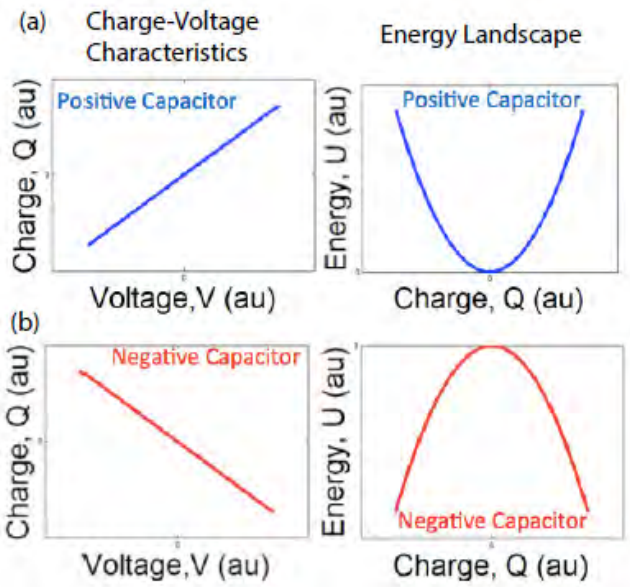
Ref. - A.I. Khan, "*Negative Capacitance for Ultra-low Power Computing*". PhD thesis, University of California at Berkeley, 2015.

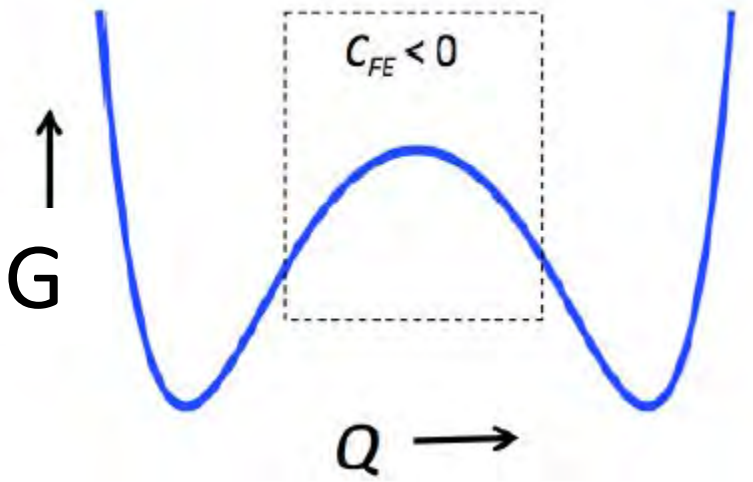
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!

  $C_{ins} < 0$ and $\frac{C_S}{C_{ins}} < 0$, then $\left(1 + \frac{C_S}{C_{ins}}\right) < 1 \rightarrow S < 60\text{mV/decade}$

- For a capacitor
  - Energy $G = \frac{Q^2}{2C} \rightarrow$ Capacitance $C = {}^{1}\!/_{\frac{d^2G}{dQ^2}} = 1/Curvature$





Energy landscape of ferroelectric materials.

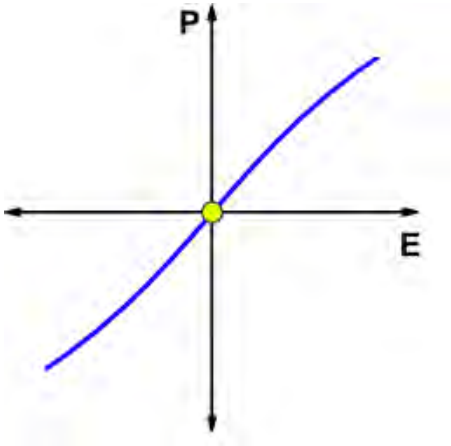
$Q = \epsilon E + P \cong P$

Ref. – S. Salahuddin et. al., *Nano Letters,* 2008.

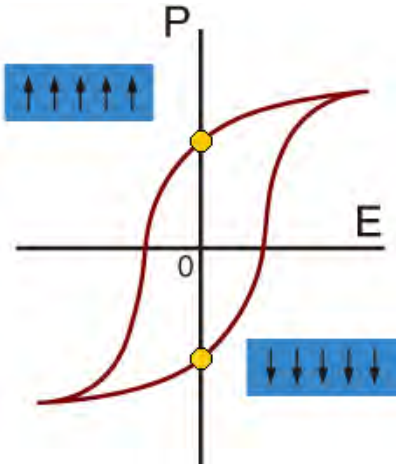
Para- and Ferro-electric Materials

- Paraelectric : No polarization when electric field is removed.

- Ferroelectric : Two possible states of polarization when electric field is removed –Spontaneous/Remnant Polarization.



Paraelectric



Ferroelectric

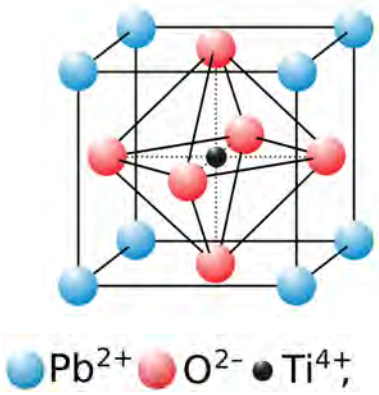
Ferroelectricity

Requirements:

- Spontaneous electric polarization: Non-Centrosymmetricity (for crystalline materials)
- Reversible polarization state by the application of electric field

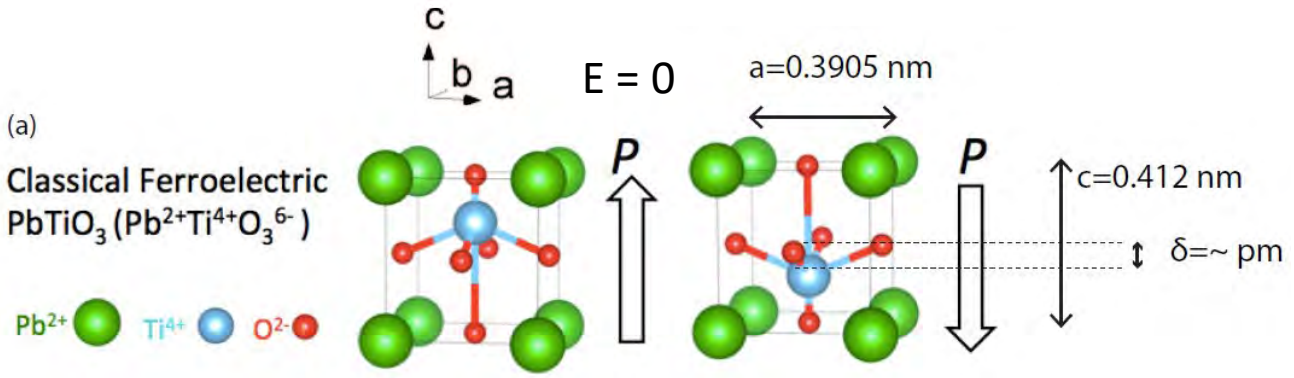
e.g. Lead titanate $PbTiO_3$, HZO

Centrosymmetric:- Paraelectric

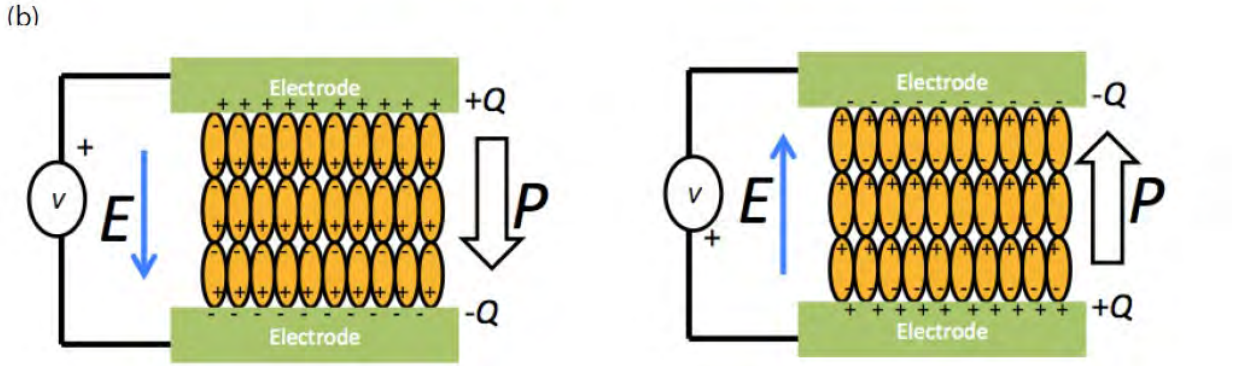


P=0 at E=0

Non-Centrosymmetric:- Ferroelectric



P≠0 at E=0



[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

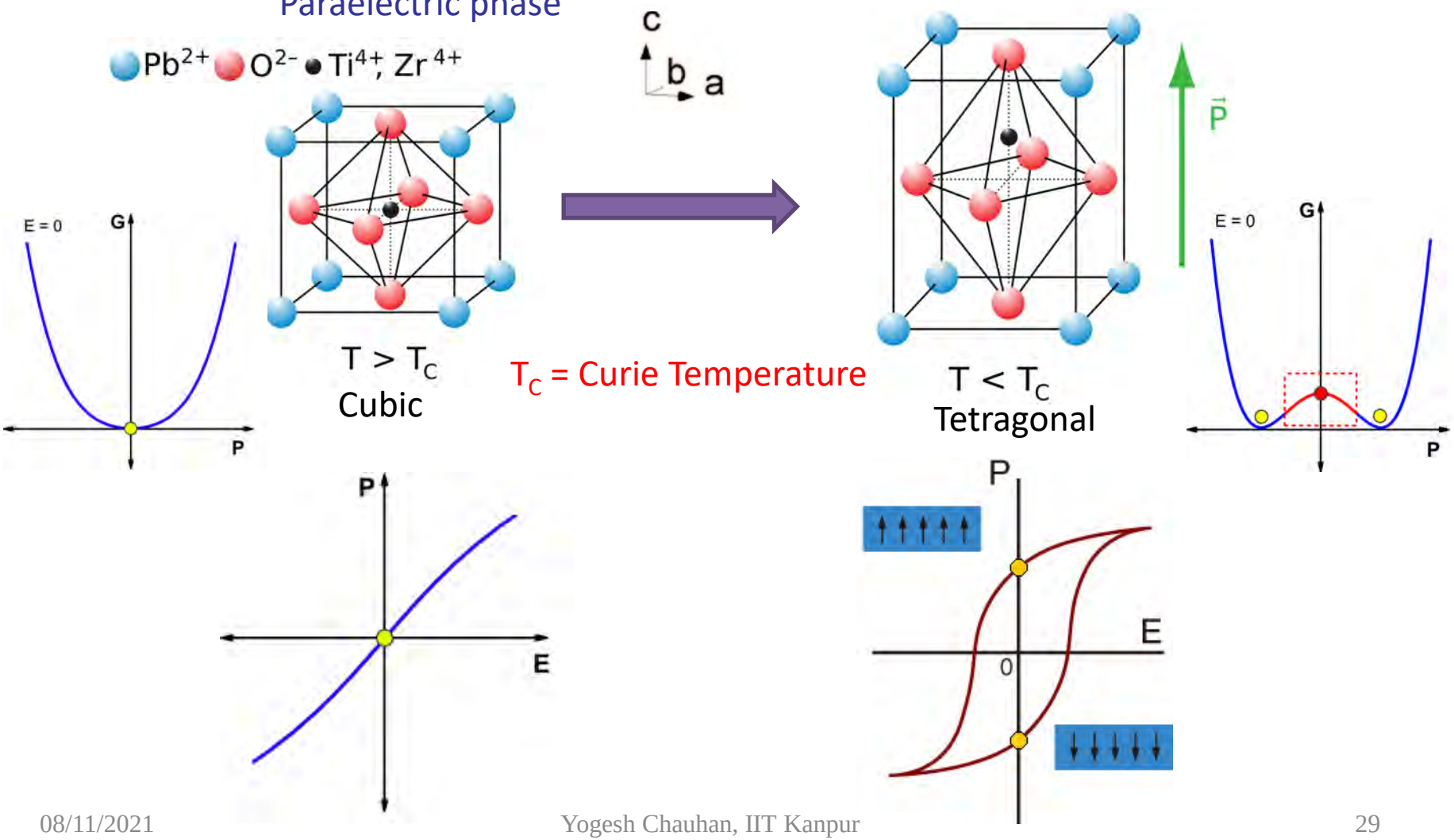
[2] A.I. Khan, *Negative Capacitance for Ultra-low Power Computing*. PhD thesis, University of California at Berkeley, 2015.

Paraelectric to Ferroelectric Phase Transition

e.g. $Pb[Zr_xTi_{1-x}]O_3$ Lead Zirconium Titanate (PZT)

Paraelectric phase

Ferroelectric phase



[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- In general, α and β can be +ve or –ve but γ is always +ve for stability reasons.
- Dynamics of G is given by $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$

δ = Polarization damping factor

- In the steady state, $\frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

For $\alpha > 0$ and at $E = 0$, there exit only one real root

$P = 0$

A Paraelectric Material

For $\alpha < 0$ and at $E = 0$, there exit three real roots

$P = 0, \pm P_r$ where $P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$

A Ferroelectric Material has a non-zero P at zero E.

Assumptions

Free energy of a non-linear dielectric

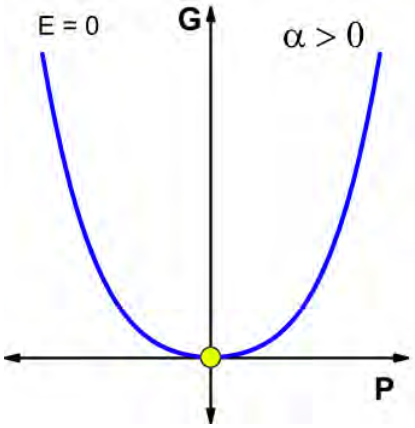
$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- Polarization and Electric field are uniaxial. (perpendicular to electrodes)
- Polarization and Electric field magnitudes are uniform throughout the ferroelectric.
- Piezo-electricity is ignored.

L-K explanation of Phase Transition

For E = 0, $G = \alpha P^2 + \beta P^4 + \gamma P^6$ and $\alpha = \alpha_0(T - T_0), \alpha_0 > 0$

Paraelectric Material

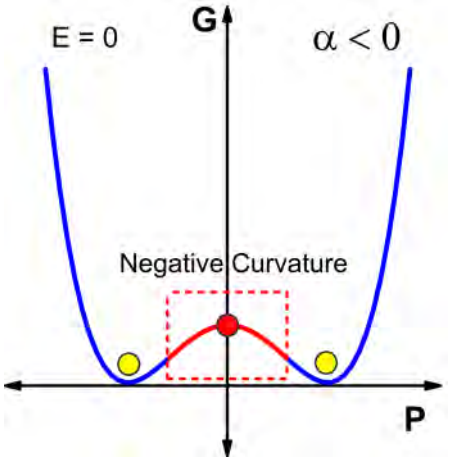


$$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

- $\alpha > 0$ i.e. for $T > T_0$; at $E = 0$, there exists only one real root, $P = 0$
- i.e. No polarization when electric field is removed

$$[P = 0 \text{ at } E = 0]$$

Ferroelectric Material



- Note, P = 0 has a maximum.
- Not possible in an isolated ferroelectric.

$$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

- $\alpha < 0$ i.e. for $T < T_0$; at $E = 0$, there exist three real roots

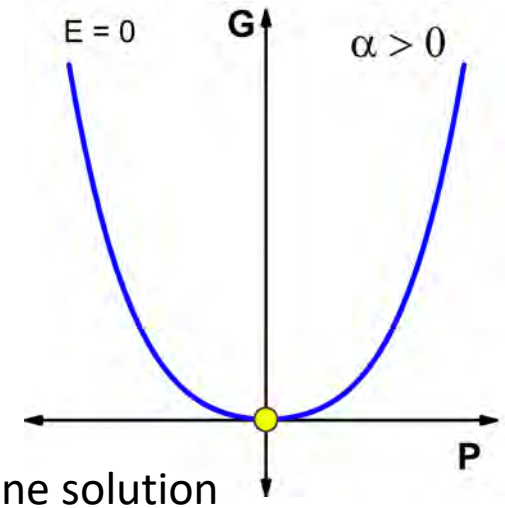
$$P = 0, \pm P_r \text{ where}$$

$$P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$$

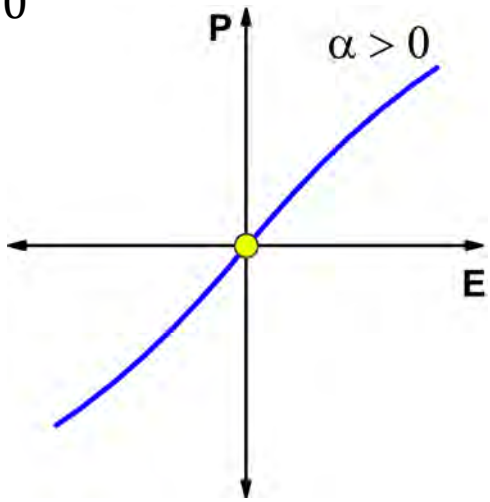
- Two possible states of polarization when electric field is removed.

[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

Positive and Negative Capacitances

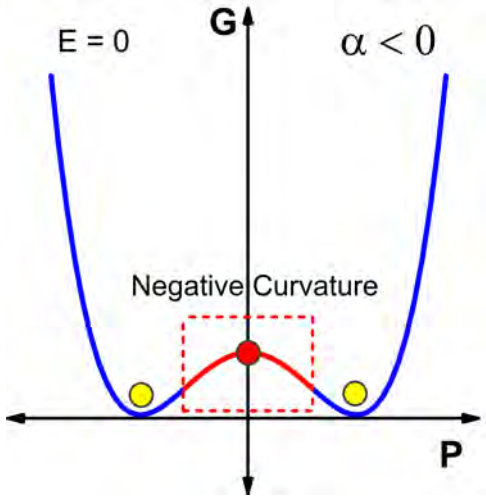


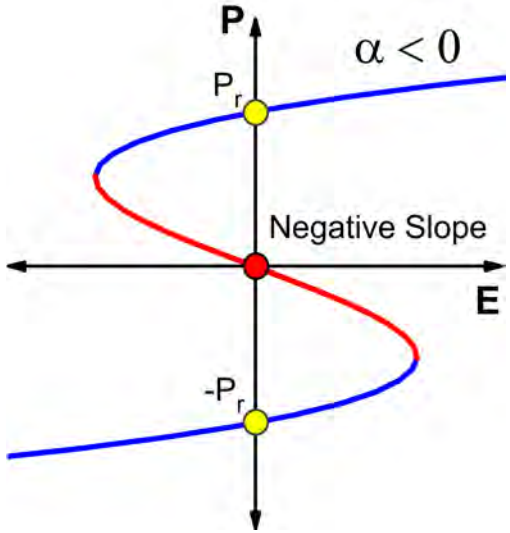
Only one solution at $E = 0$



Paraelectric

A Positive Capacitor





Ferroelectric

A Conditionally Negative Capacitor

Three possible solutions at $E = 0$

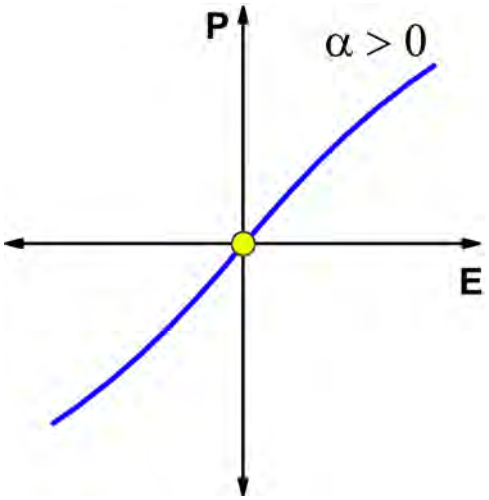
$P = 0$ is not possible in a isolated Ferroelectric due to maxima of energy or a negative capacitance

$$C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1} = \frac{\partial P}{\partial E} < 0$$

Application of Electric Field

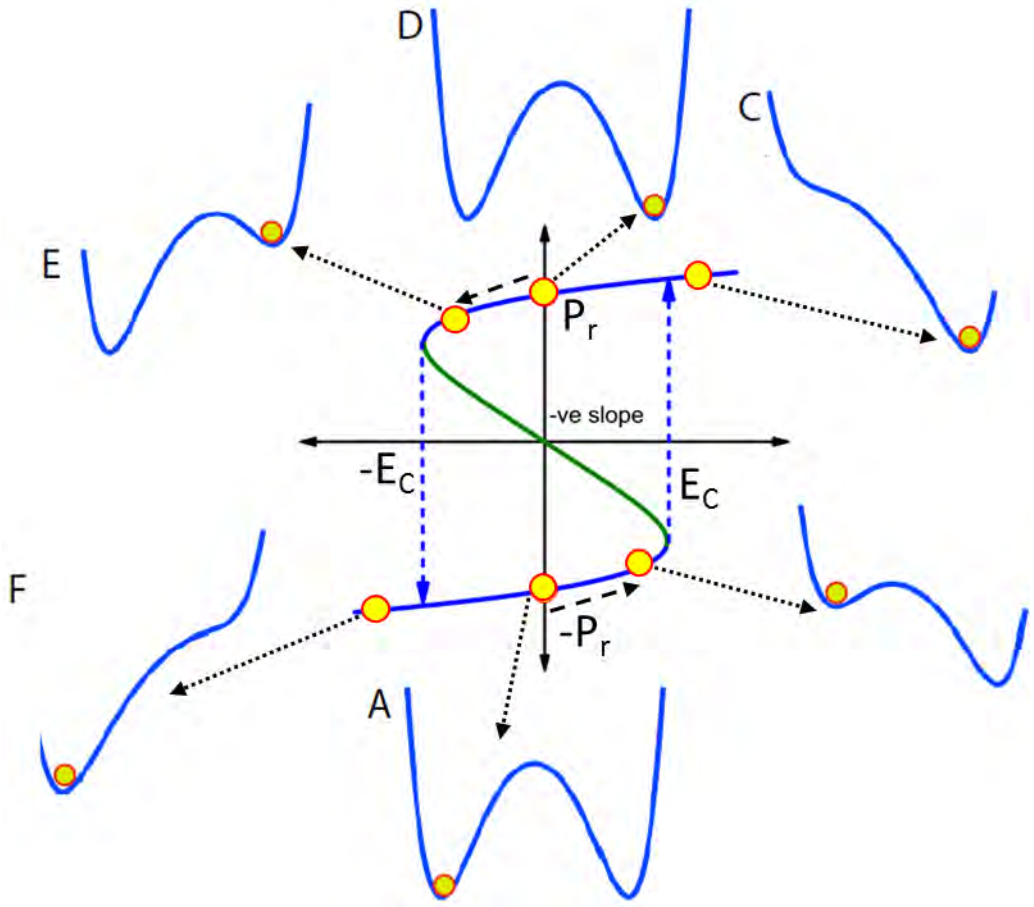
$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$



Paraelectric

[A Positive Capacitor]



Isolated Ferroelectric

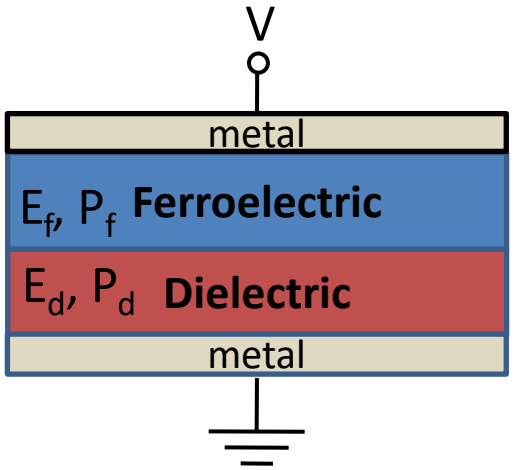
[A Conditionally Negative Capacitor]

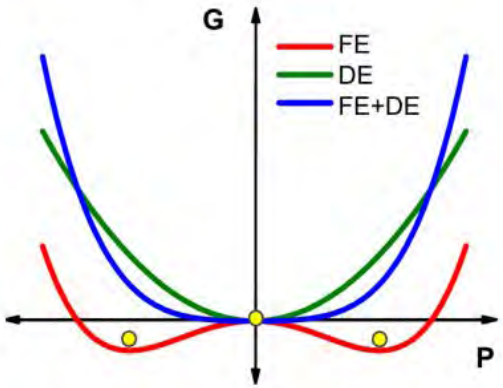
[1] K. M. Rabe, C. H. Ahn, and J.-M. Triscone, Eds., *Physics of Ferroelectrics: A Modern Perspective*, vol. 105. Berlin, Germany: Springer, 2007.

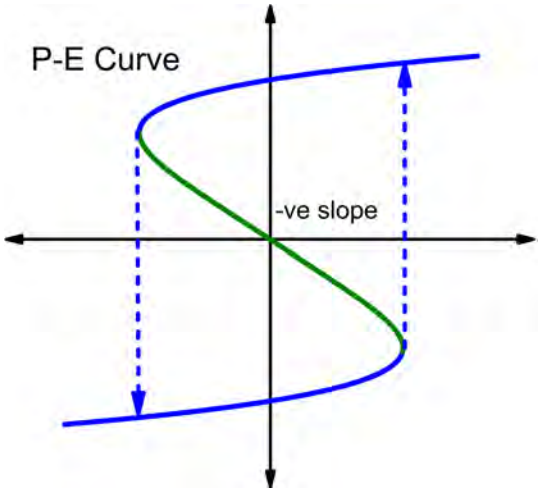
[2] A.I. Khan, *Negative Capacitance for Ultra-low Power Computing*. PhD thesis, University of California at Berkeley, 2015.

How to stabilize a Negative Capacitance?

Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.







Total energy of the FE + DE system

$$G = G_f + G_d$$

$$Q = \epsilon_0 E_f + P_f = \epsilon_0 E_d + P_d$$

Assuming V is small

$$Q \approx P_f \approx P_d$$

$$\Longrightarrow \frac{\partial^2 G}{\partial Q^2} = \frac{\partial^2 G_f}{\partial Q^2} + \frac{\partial^2 G_d}{\partial Q^2}$$

For a stable system $\frac{\partial^2 G}{\partial Q^2} > 0$ (minimum)

$$\Longrightarrow \frac{1}{C_{tot}} = \frac{1}{C_f} + \frac{1}{C_d} > 0$$

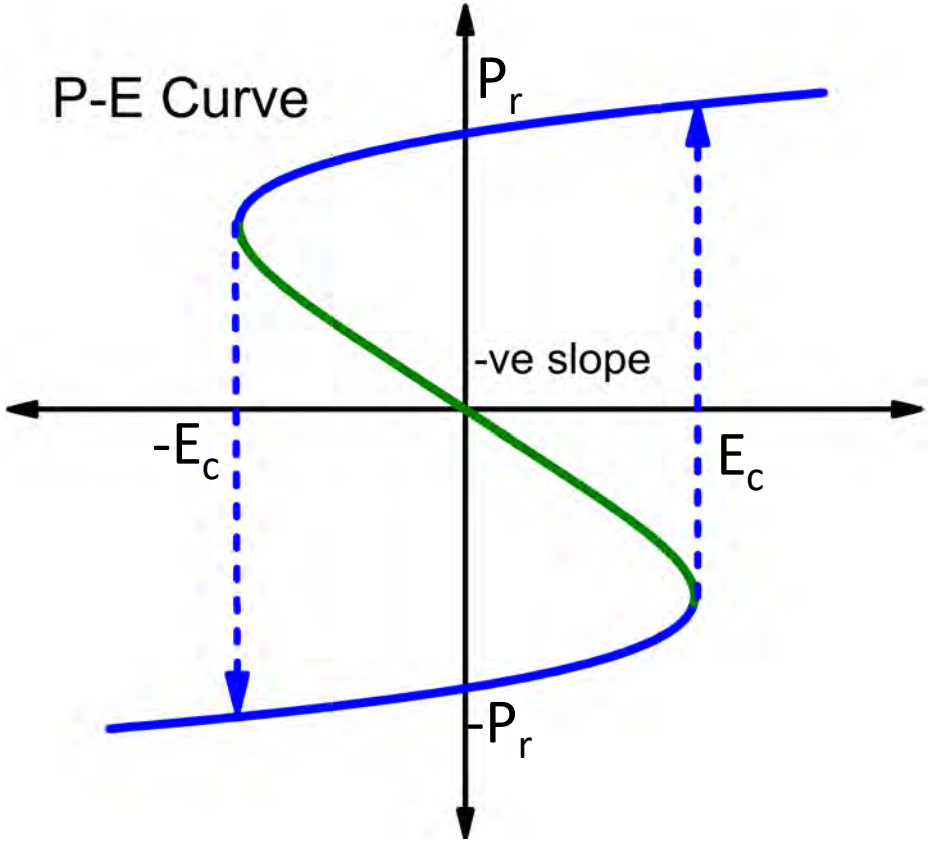
$$C_{tot} = \frac{C_d . |C_f|}{|C_f| - C_d} > 0$$

For a stable system

$$|C_f| > C_d$$

$$C_{tot} > C_d$$

Negative Capacitance in Ferroelectric



$$C_{ins} = C_{fe}$$

Negative slope region can be stabilized if

$$C_{total} = \left(\frac{1}{-|C_{fe}|} + \frac{1}{C_S}\right)^{-1} > 0$$

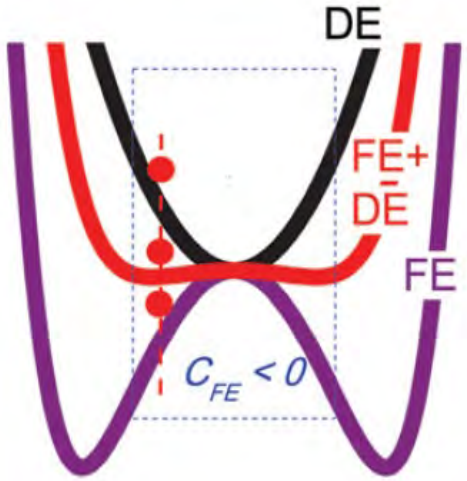
or,

$$|C_{fe}| > C_S$$

S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008.

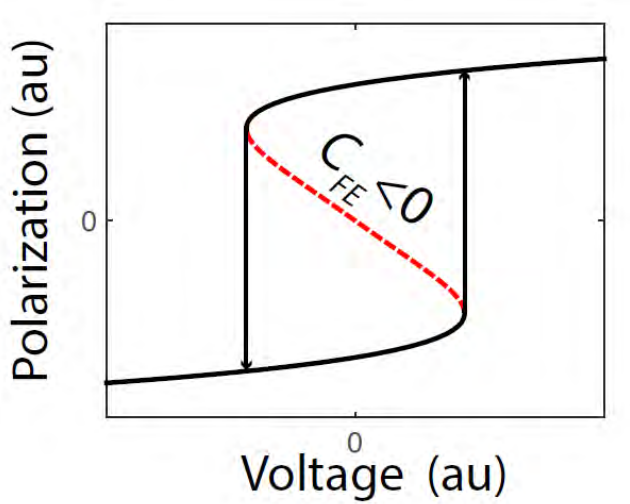
How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

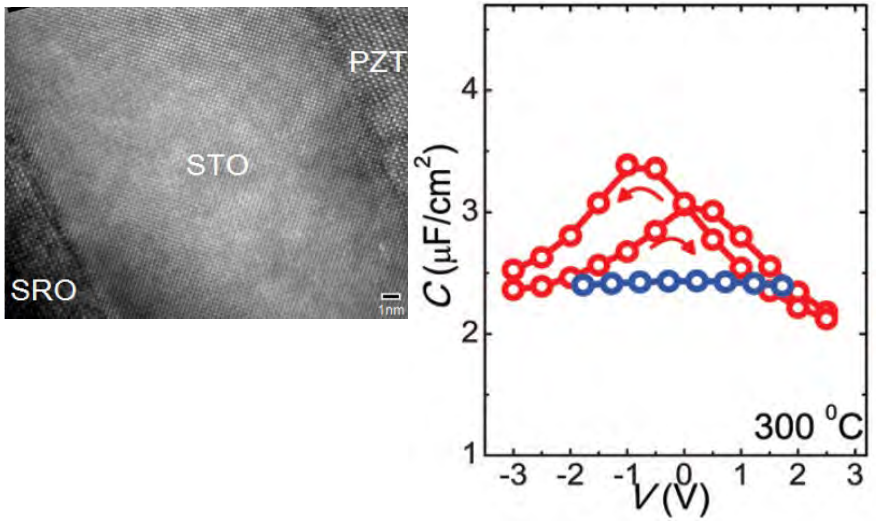


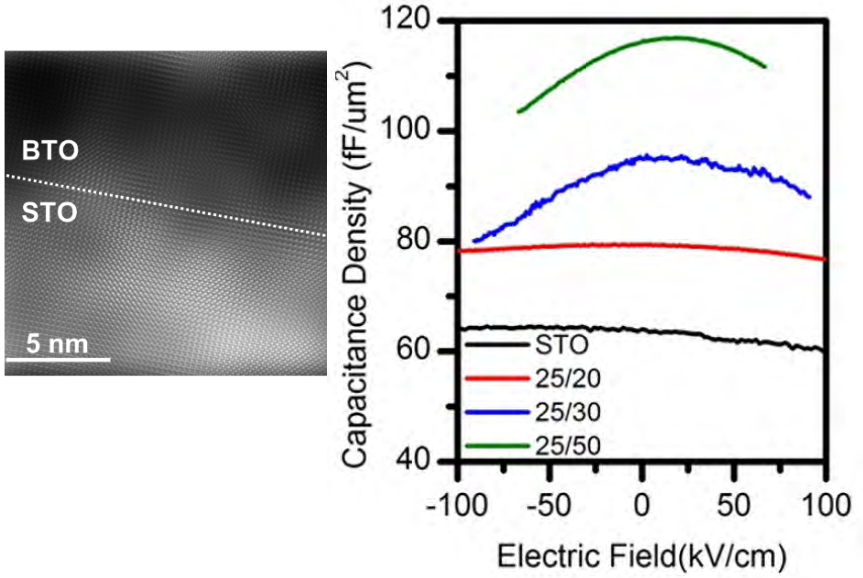
A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011

- $\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0$
- $C_{DE} < |C_{FE}|$ and $C_{FE} < 0$
- $C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$



Ferroelectric-Dielectric Systems





A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011.

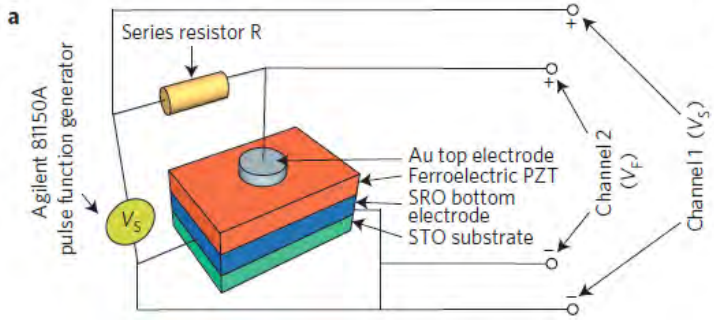
D. J. Appleby et al., Nano Letters, vol. 14, no.7, pp. 3864–3868, 2014.

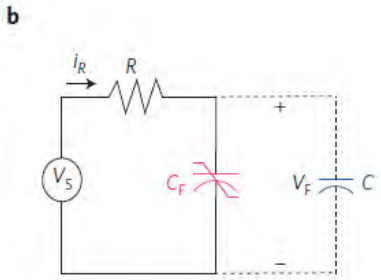
Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.

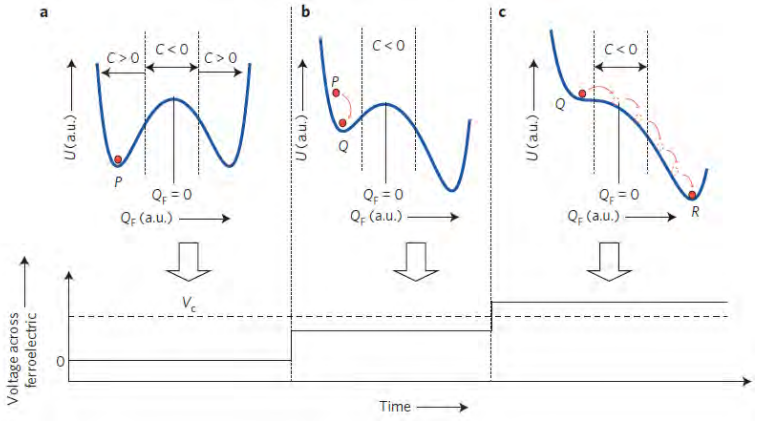
$$C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$$

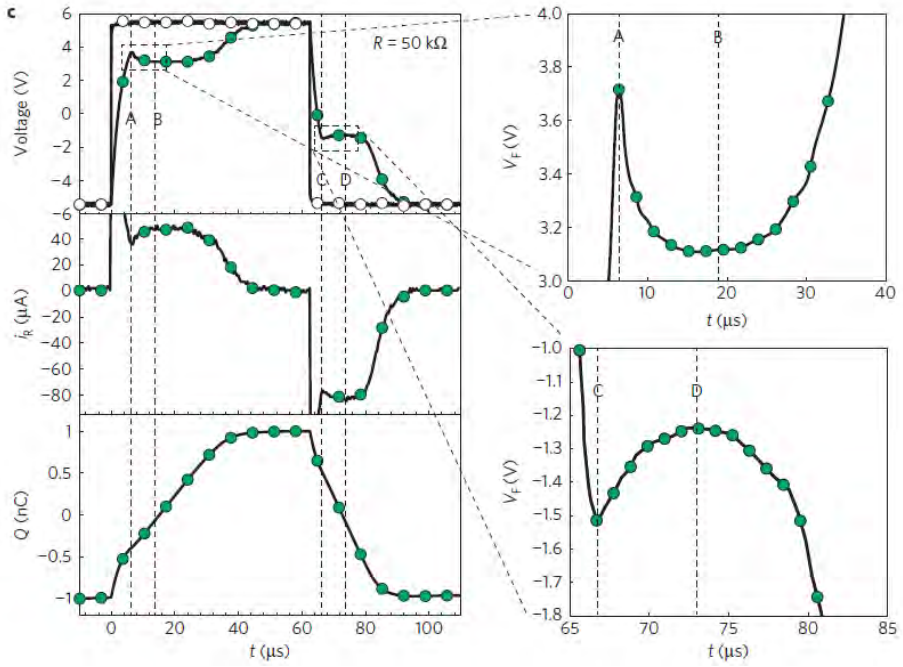
Ferroelectric-Resistor System

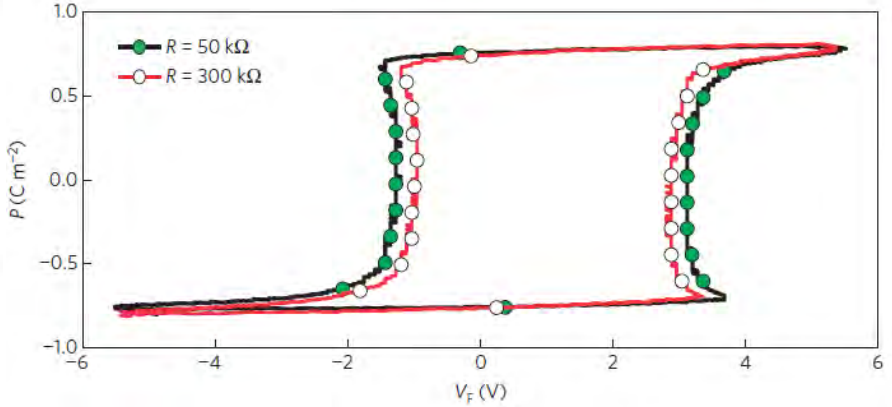
PZT ferroelectric ($PbZr_{0.2}Ti_{0.8}O_3$)







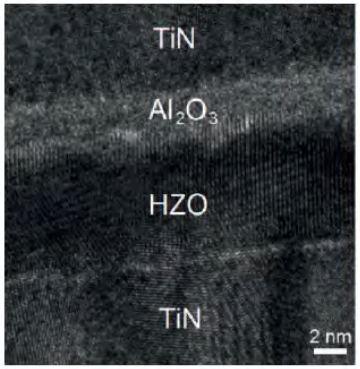




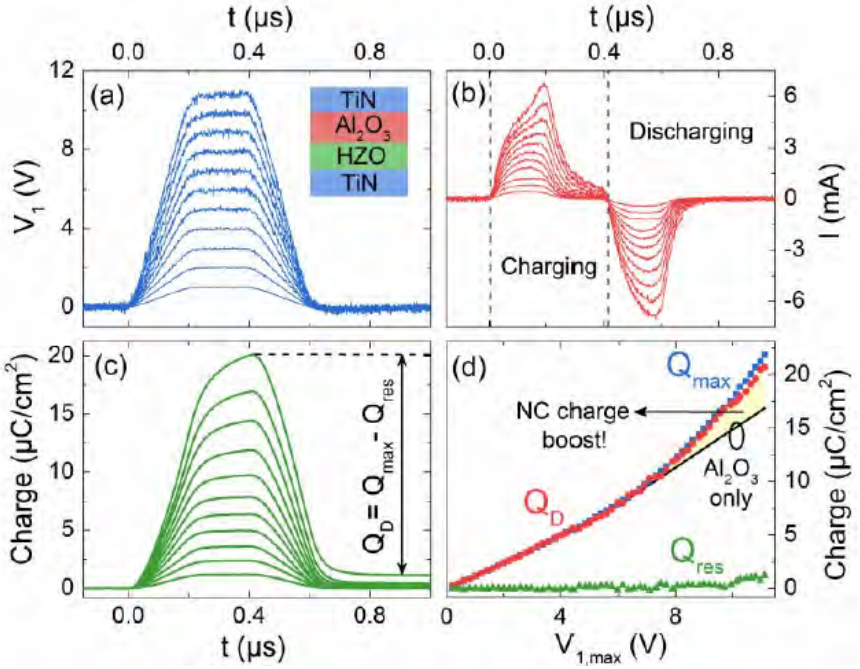
- NC is observed only for a small duration ($\sim \mu s$) during polarization switching.
- Difficult to stabilize.

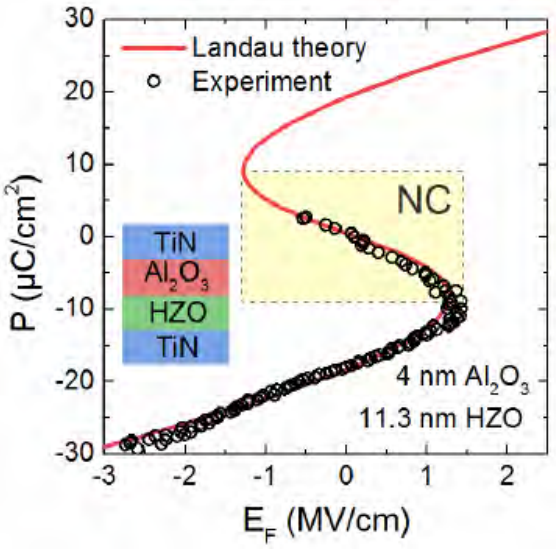
A. I. Khan *et al.*, "Negative capacitance in a ferroelectric capacitor," *Nature Mater.*, vol. 14, no. 2, pp. 182–186, 2015.

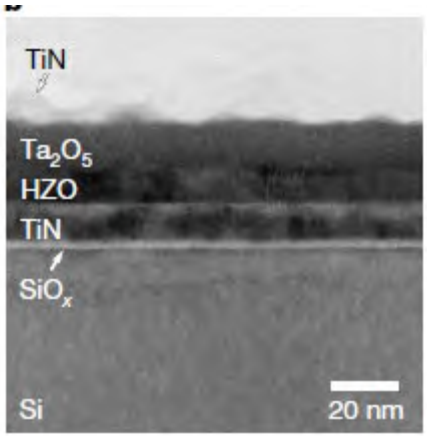
First ever demonstration of S-curve



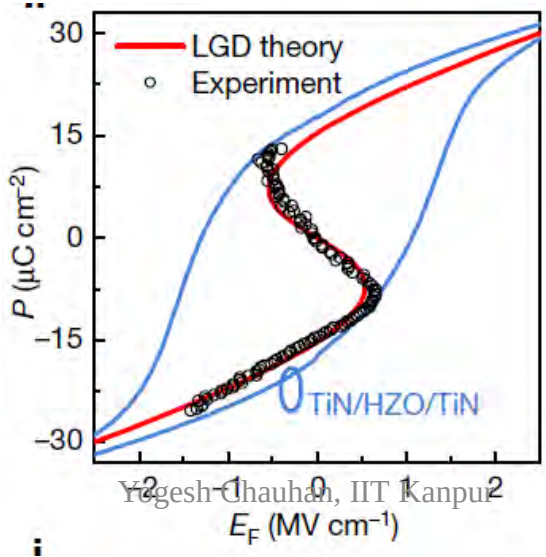
Hoffmann et al.
IEDM, Dec 2018

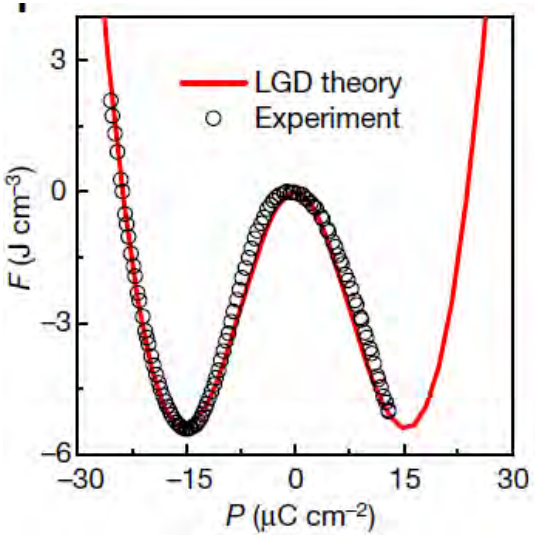




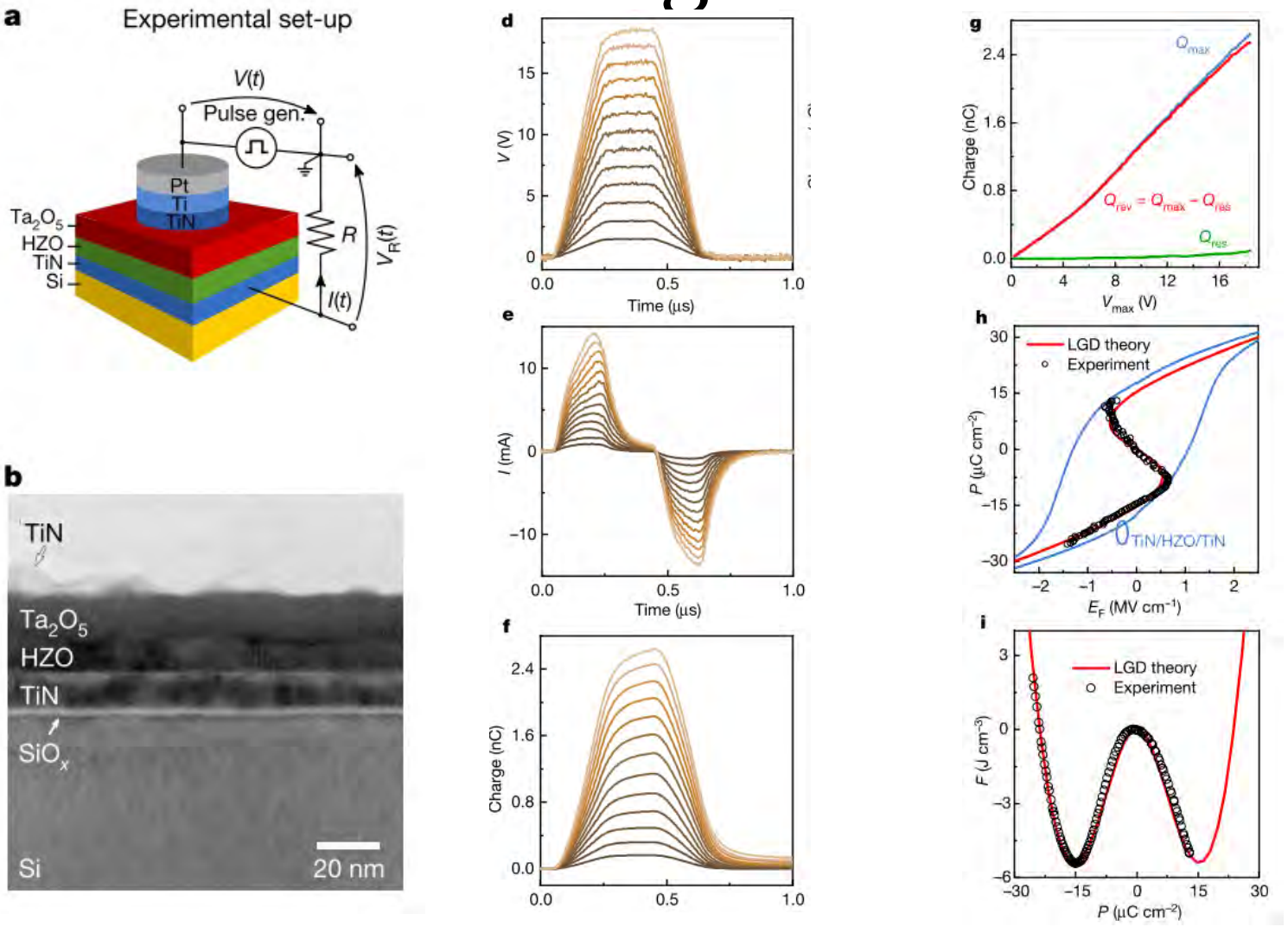


Hoffmann et al. *Nature Lett.*, Jan 2019





Measuring S-Curve



Ref. – Thomas Mikolajick et al., “Unveiling the double-well energy landscape in a ferroelectric layer”, Nature, Jan. 2019.

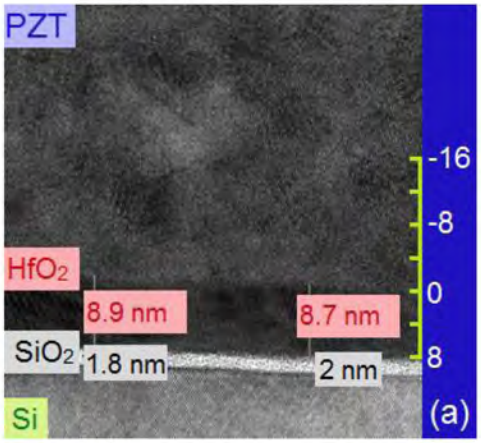
Negative Capacitance FETs

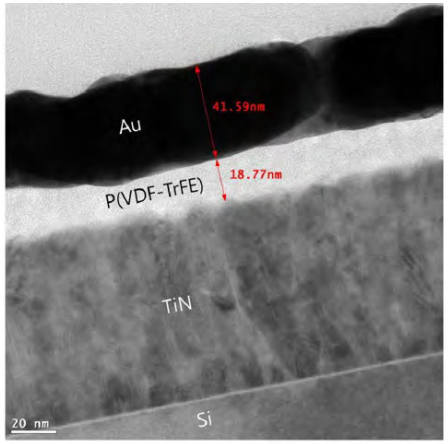
$PbZr_{0.52}Ti_{0.48}O3$ FE with HfO_2 buffer interlayer

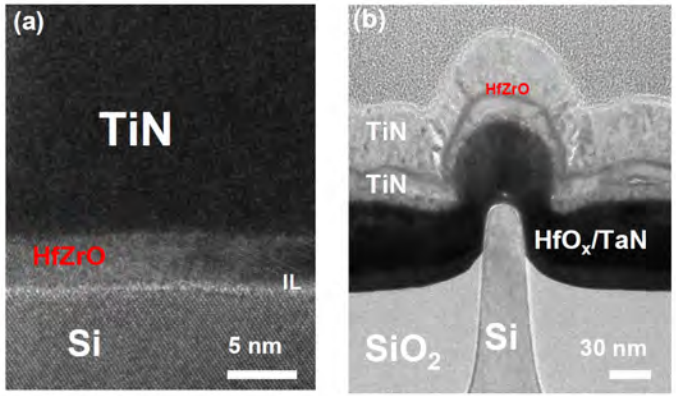
$P(VDF_{0.75}\text{-}TrFE_{0.25})$ Organic Polymer FE

HfZrO FE

CMOS compatible FE







S. Dasgupta et al., IEEE JESCDC, 2015.

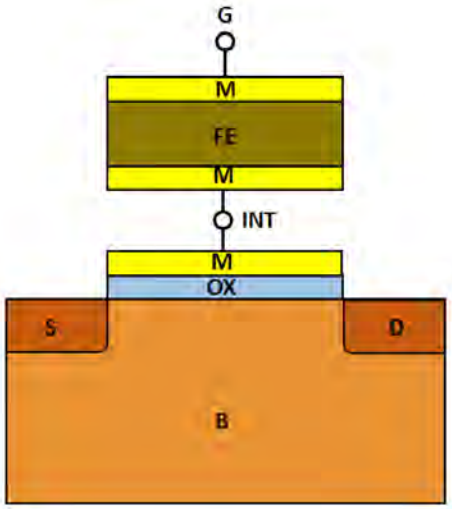
J. Jo et al., Nano Letters, 2015

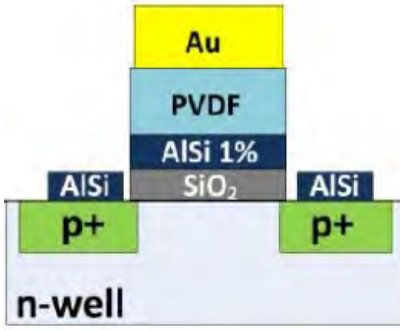
K.-S. Li et al., in IEEE IEDM, 2015.

NCFET Structures

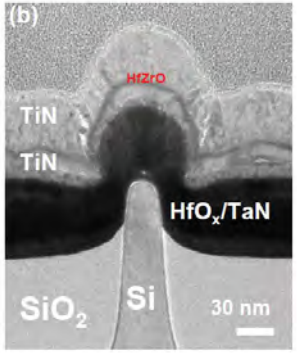
MFMIS Structure

Metal
Ferroelectric
Metal
Insulator
Semiconductor





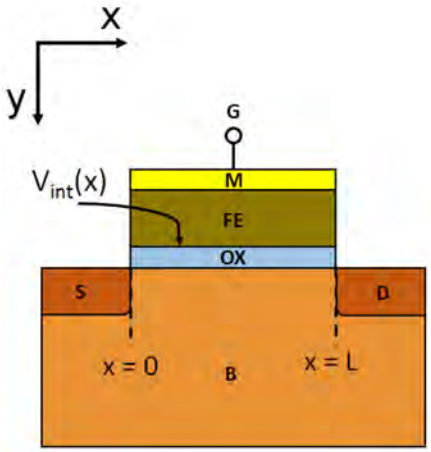
46 mV/decade
[Rusu et al. IEDM '10]

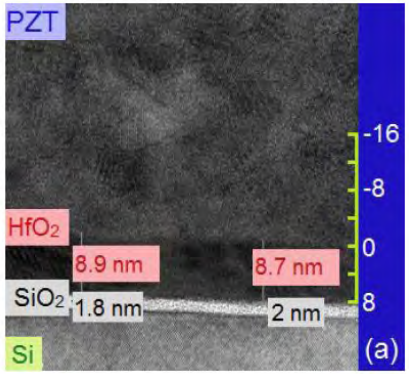


NC-FinFET
(FE: $Hf_{0.42}Zr_{0.58}O_2$)
Lg = 30 nm
[Li et al. IEDM '15]

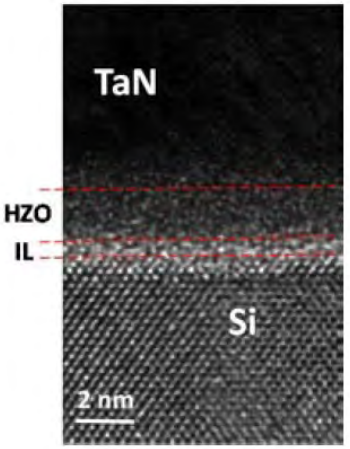
MFIS Structure

Metal
Ferroelectric
Insulator
Semiconductor





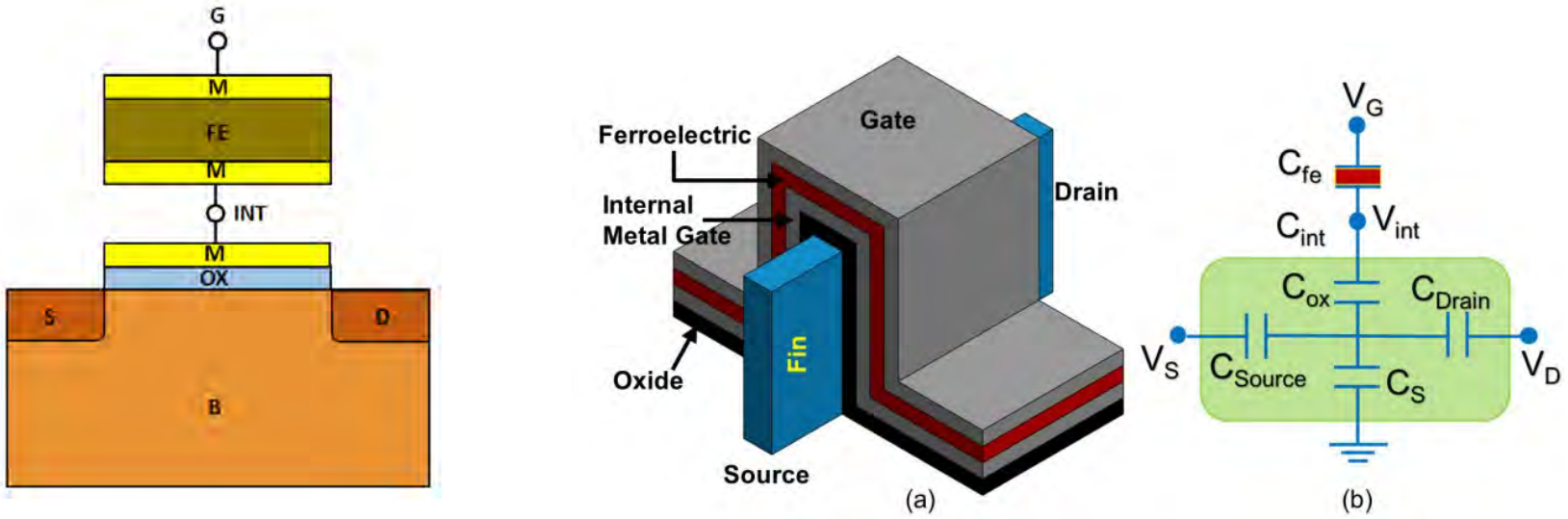
13 mV/decade
Lg = 10 µm
[Dasgupta et al., IEEE JESCDC, '15]



52 mV/decade
t_{fe} = 1.5 nm
[Lee et al., IEDM '16]

MFMIS NCFET Modeling

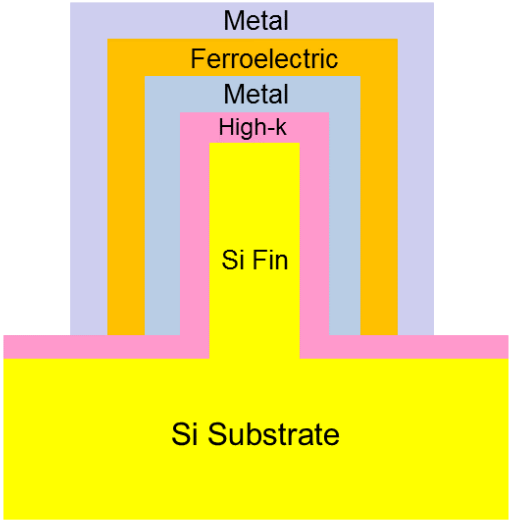
MFMIS Structures

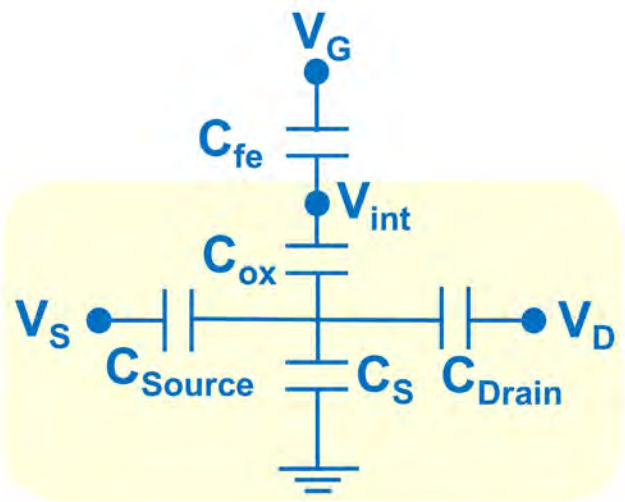


- Metal internal gate → equipotential surface with a spatially constant V_{int}.
- Ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire → Simplified modeling

Device Structure

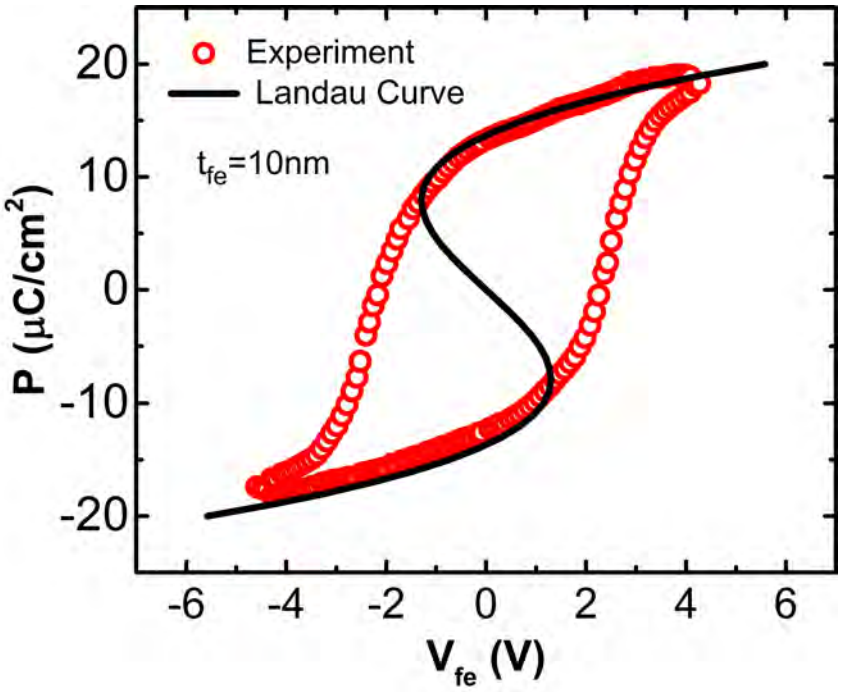
Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)





- Metal internal gate provides an equipotential surface with a spatially constant V_{int}.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.

Experimental Calibration of L-K Model



Calibration of L-K with P-V_{fe} curve for Y-HfO2 with 3.6 mol% content of $YO_{1.5}$[3]

$\alpha = -1.23 \times 10^9$ m/F

$\beta = 3.28 \times 10^{10}$ m/F

$\gamma = 0$ (2nd order phase transition)

Gibb's Energy,

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

Dynamics of G is given by

$$\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$$

In the steady state, $\frac{dP}{dt} = 0$

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$

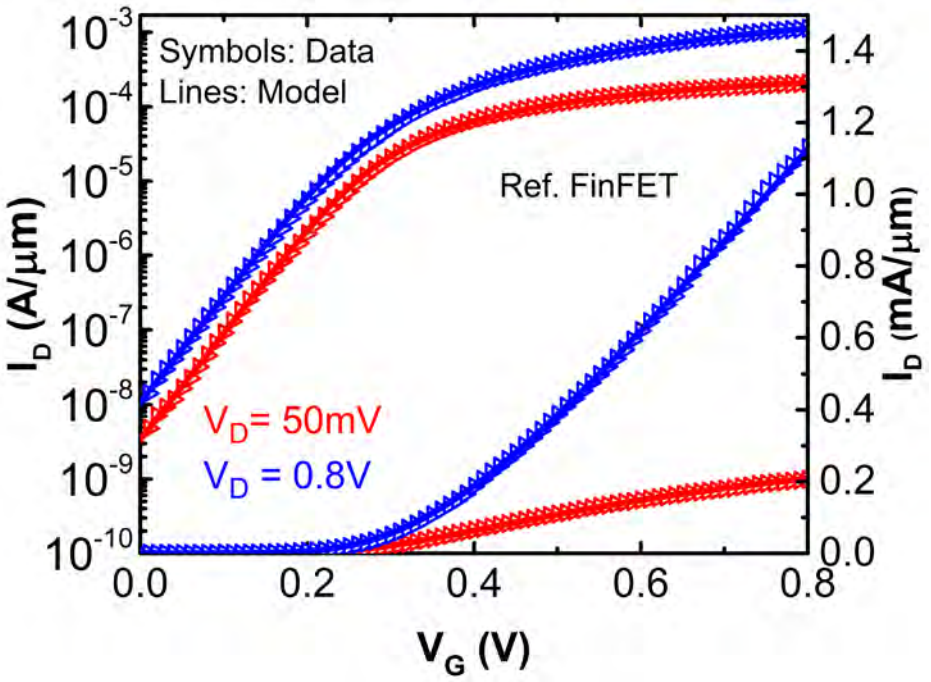
[1] Devonshire et al., The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 40, no. 309, pp. 1040–1063, 1949.

*[2] Landau, L. D. & Khalatnikov, I. M. On the anomalous absorption of sound near a second order phase transition point. Dokl. Akad. Nauk **96,** 469472 (1954).*

[3] J. M¨uller et al., JAP, vol. 110, no. 11, pp. 114113, 2011.

Calibration of Baseline FinFET

Calibration of baseline FinFET with
22 nm node FinFET.



BSIM-CMG model is used to model baseline FinFET.

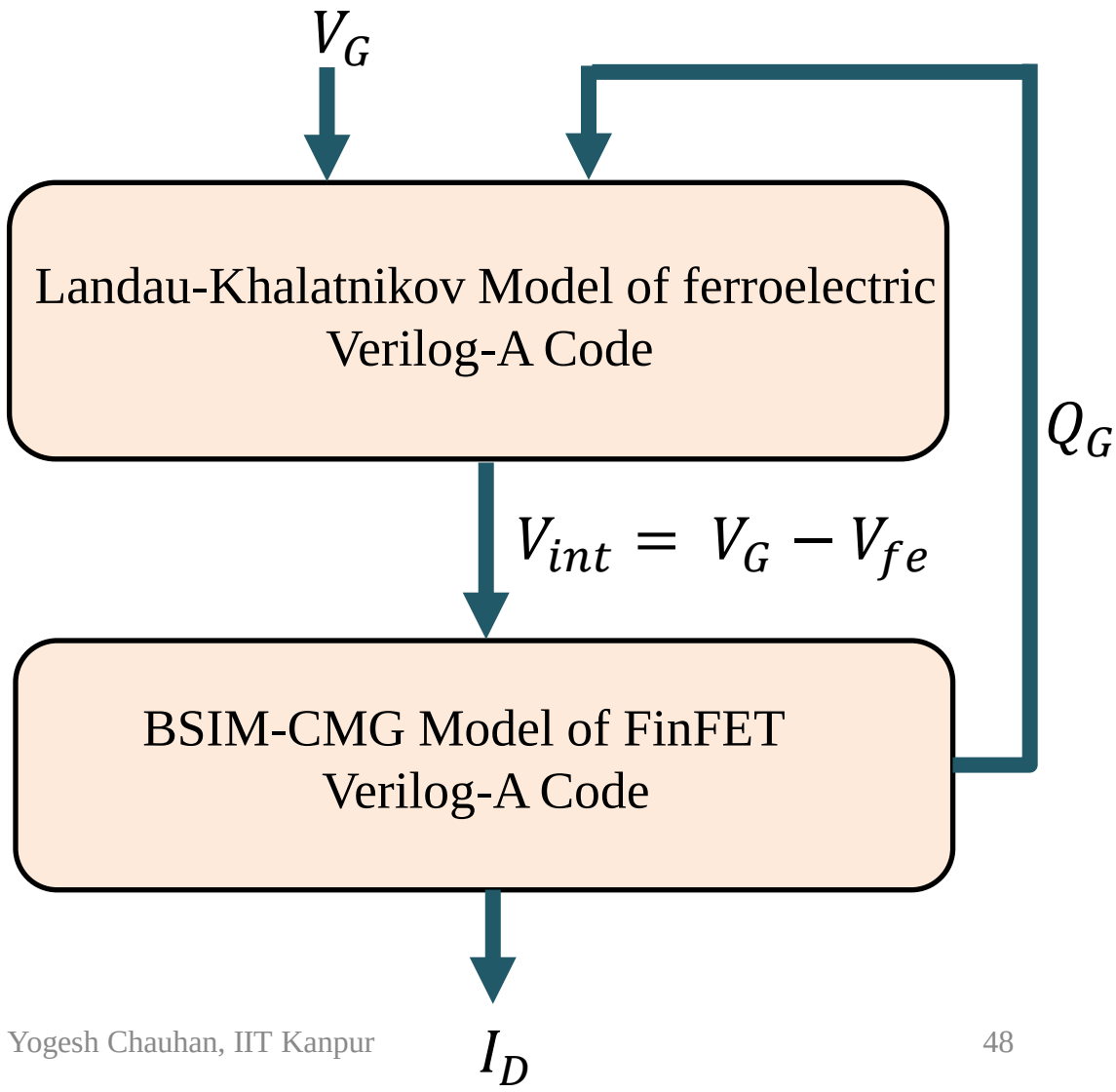
Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

C. Auth et al., in VLSIT, 2012, pp. 131–132.

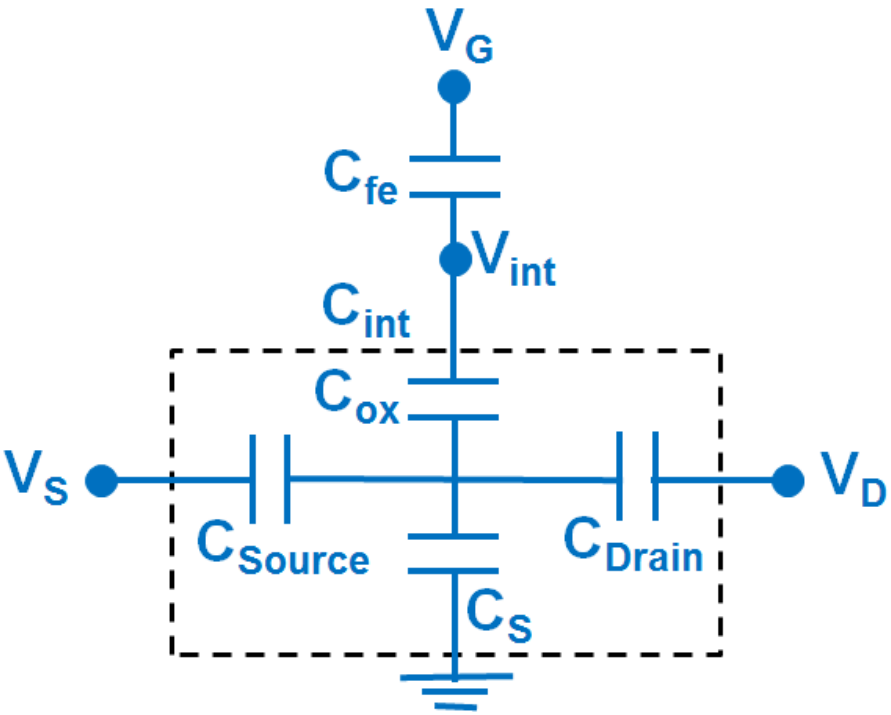
Complete Modeling Flowchart

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$



Capacitances and Voltage Amplification



$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

$$C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)}$$

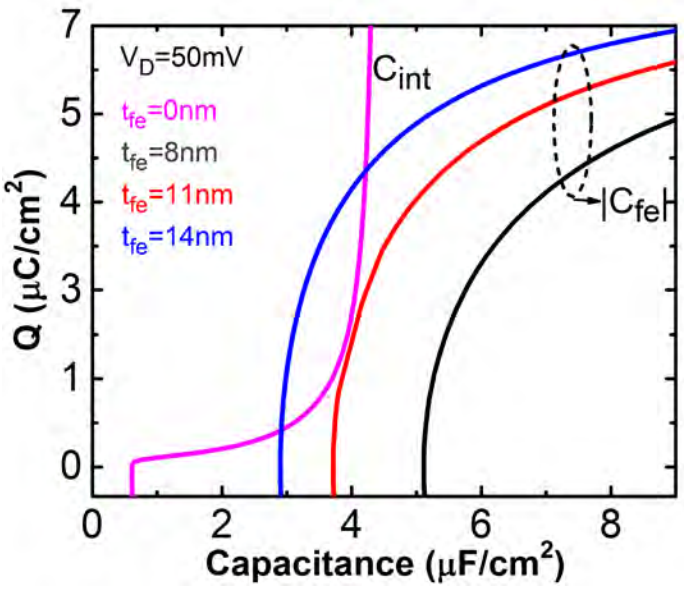
$$\frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}}$$

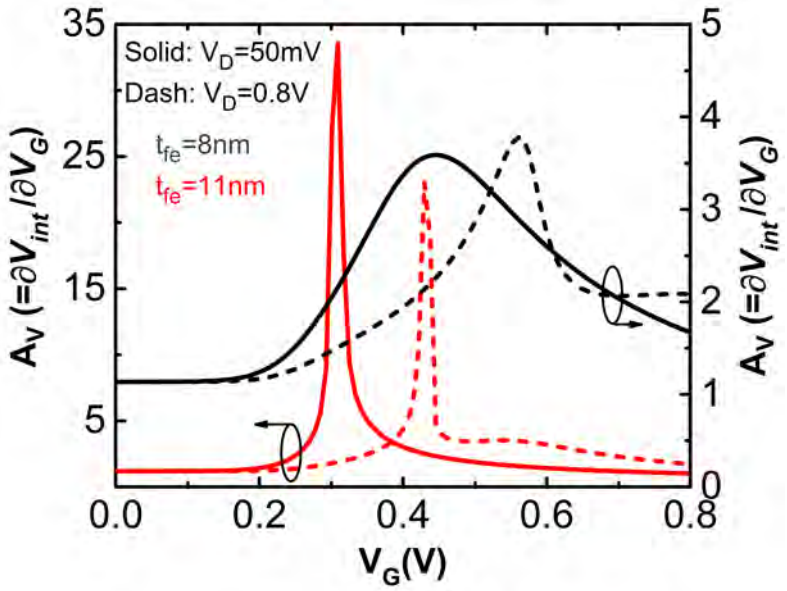
Capacitance matching between $|C_{fe}|$ and C_{int} increases the gain.

Internal Voltage Gain,

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

Capacitance Matching





- Capacitance matching increases with t_{fe} which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.

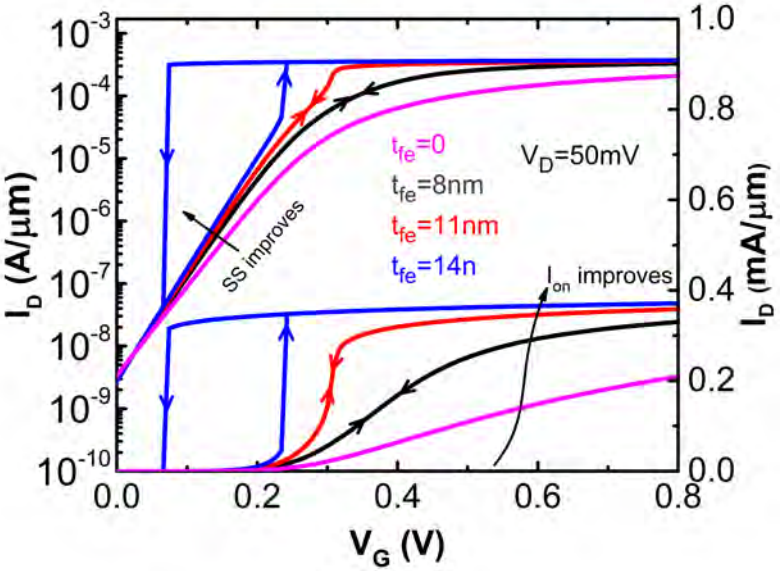
- Increase in V_D reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.

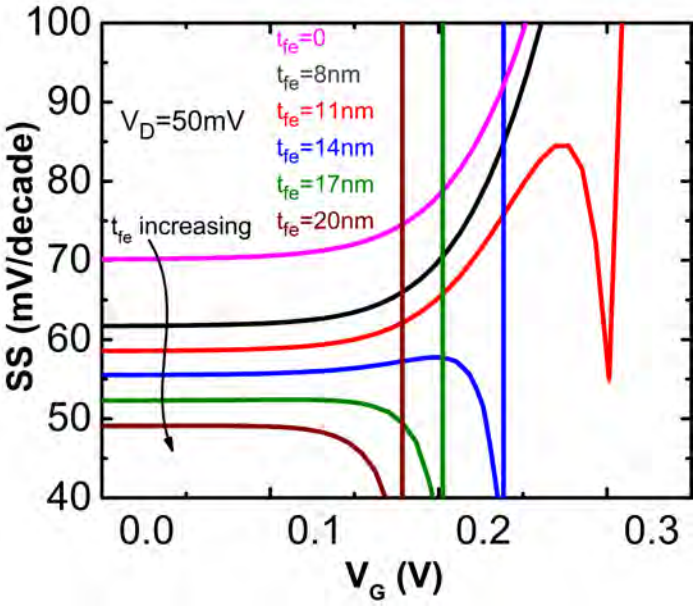
I_D-V_G Characteristics – SS region

- As t_{fe} increases
  - Capacitance matching is better
  - C_S and C_{ins} are better matched

$$S = \left(1 - \frac{C_S}{|C_{ins}|}\right).60\text{mV/dec}$$

- As $t_{fe}\uparrow \rightarrow SS\downarrow$



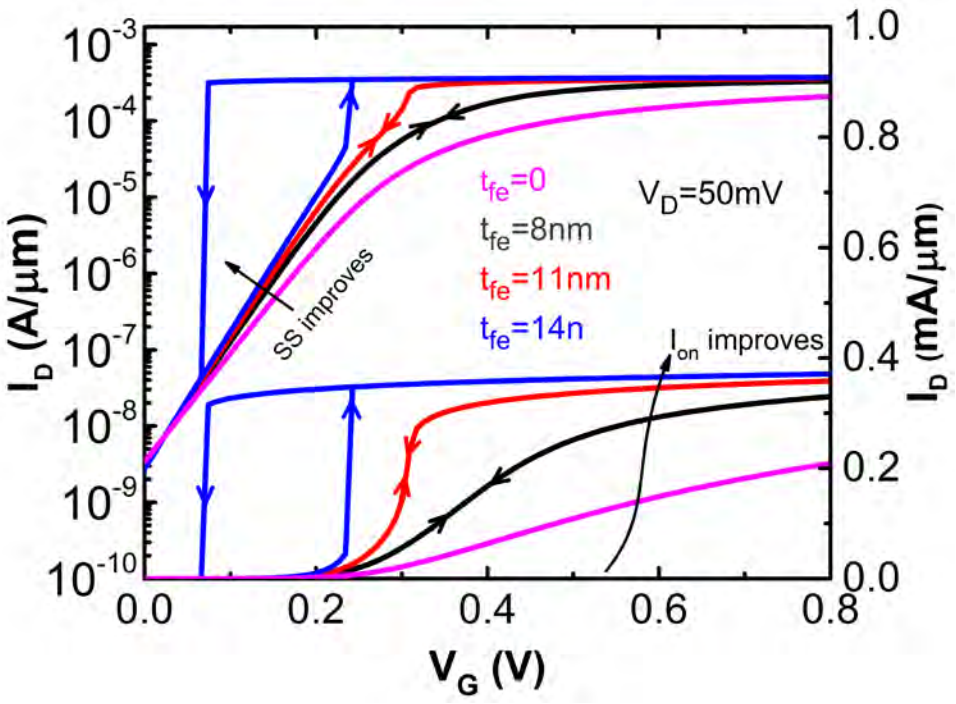


I_D-V_G Characteristics – ON region

- As t_{fe} increases
  - Capacitance matching is better

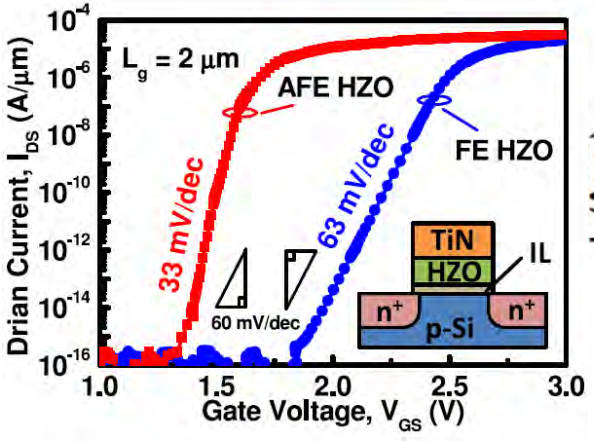
$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, I_{ON} increases.



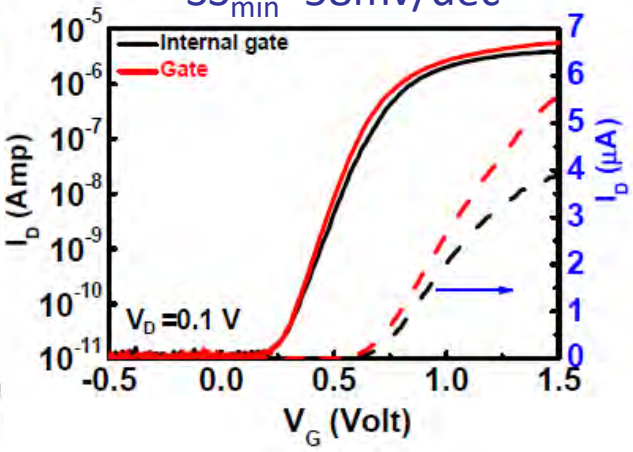
Note the significant improvement in I_{ON} compared to SS.

I_D-V_G Experimental Demonstration

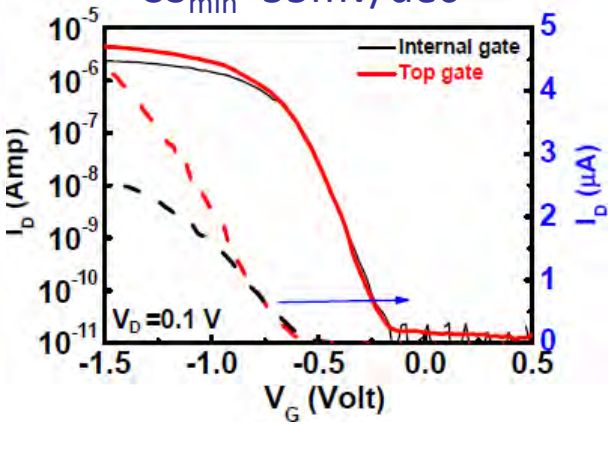


M. H. Lee *et al*., in *IEEE JEDS*, July 2015.

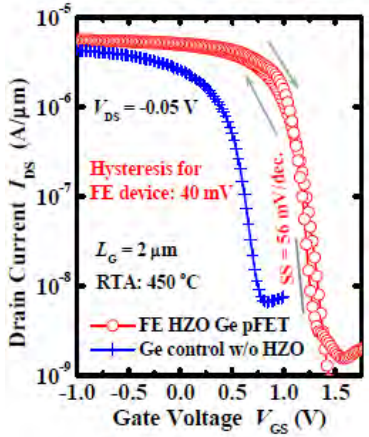
SS_{min}=58mv/dec

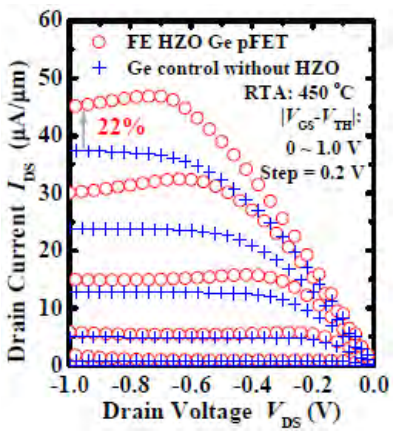


SS_{min}=55mv/dec

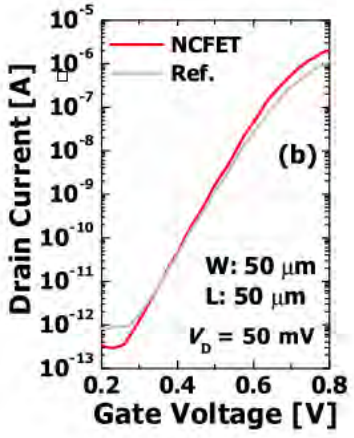


K. S. Li *et al*., in *IEEE IEDM* , 2015

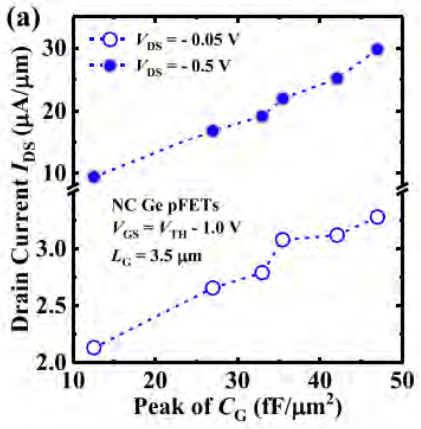




J. Zhou et al., in IEEE IEDM, 2016.



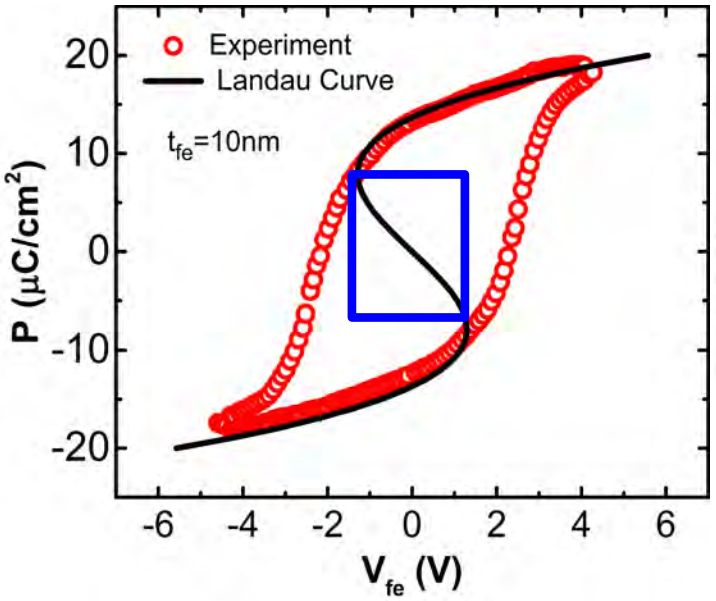
D. Kwon et al., in IEEE EDL, 2018

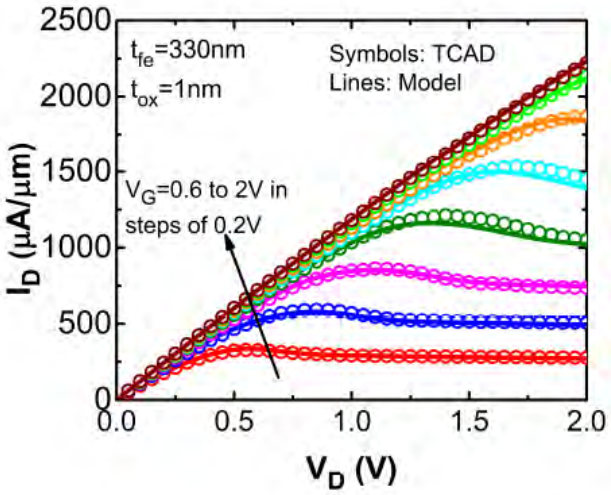


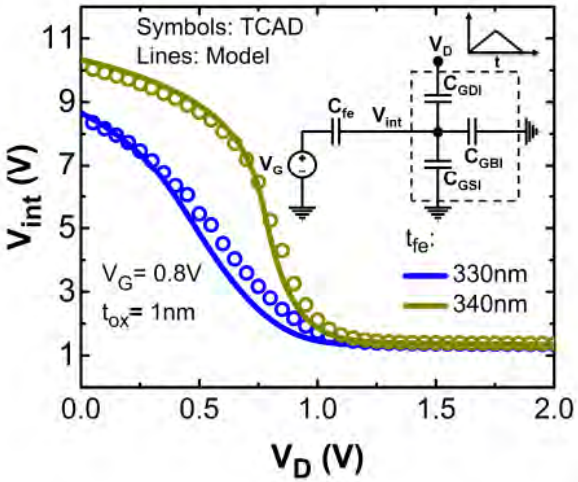
Jing Li et al., in IEEE EDL, 2018

I_D-V_D Characteristics

FE material is different.





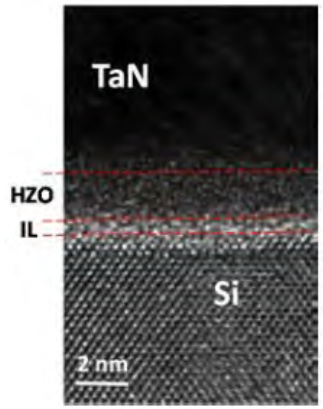


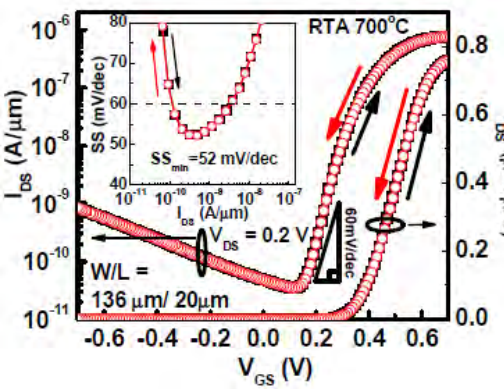
- NCFET is biased in negative capacitance region.
  - Q_G or P is positive → V_{fe} is negative.

- V_{DS}↑ → Q_G or P↓ → $|V_{fe}|$ ↓ → $V_{int}=V_G+|V_{fe}|$ ↓ → A_V ↓ → Current reduces

G. Pahwa, …, Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance", IEEE TED, Dec. 2016.

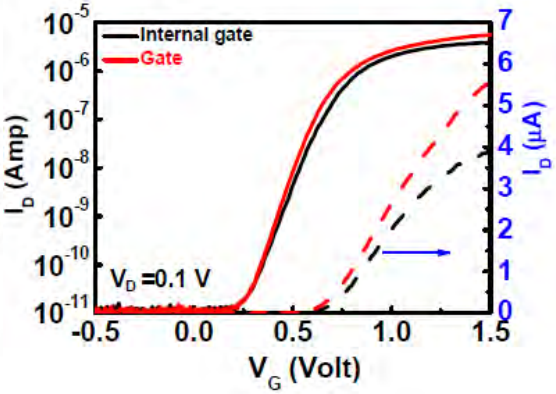
Experimental Demonstration





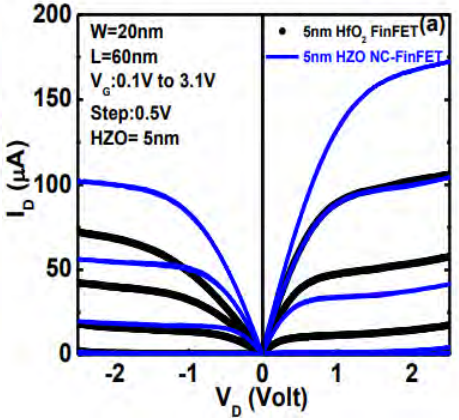
1.5 nm HZO
Compatible with sub-10nm technology node

M. H. Lee *et al*, *IEDM*, pp. 12.1.1–12.1.4., 2016

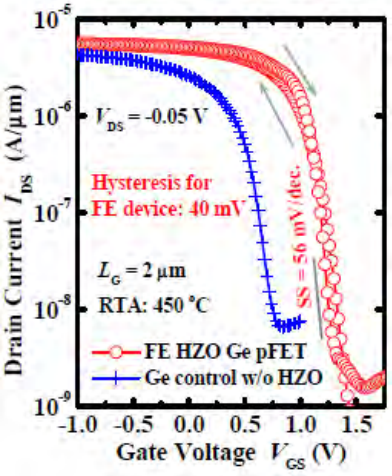


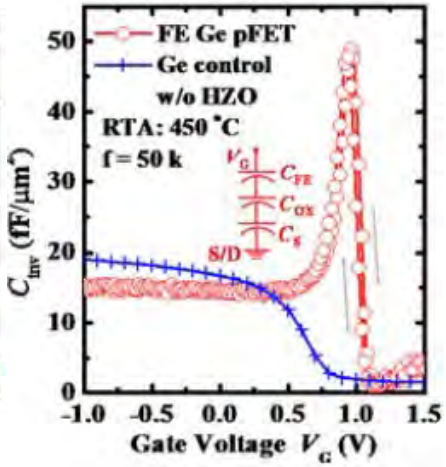
SS$_{min}$=58mv/dec

K. S. Li *et al.*, in *IEEE IEDM* , 2015

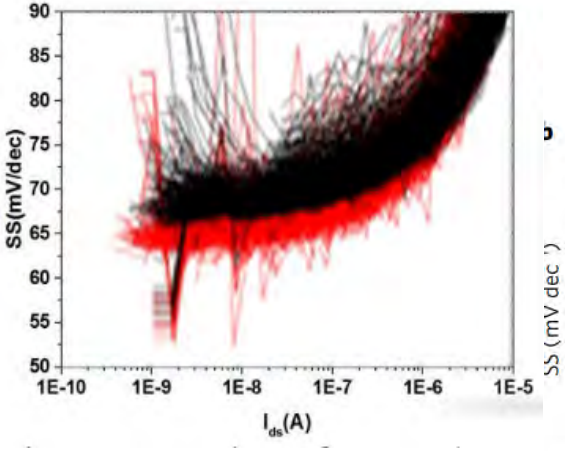


K. S. Li *et al.*, in *IEEE IEDM* , 2018



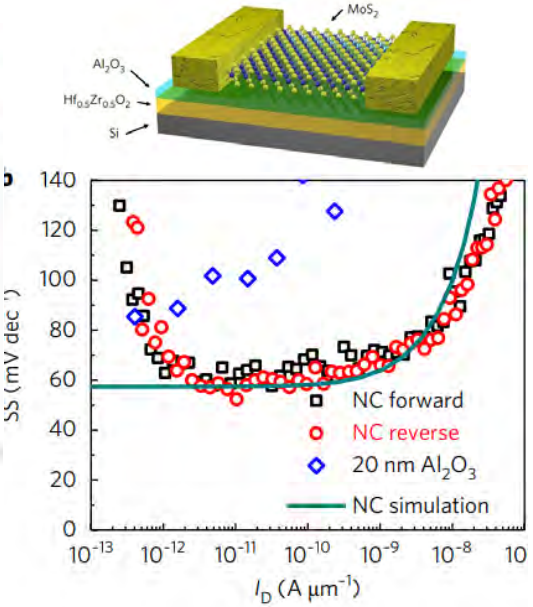


J. Zhou *et al.*, *IEDM*, 2016, pp. 12.2.1-12.2.4.



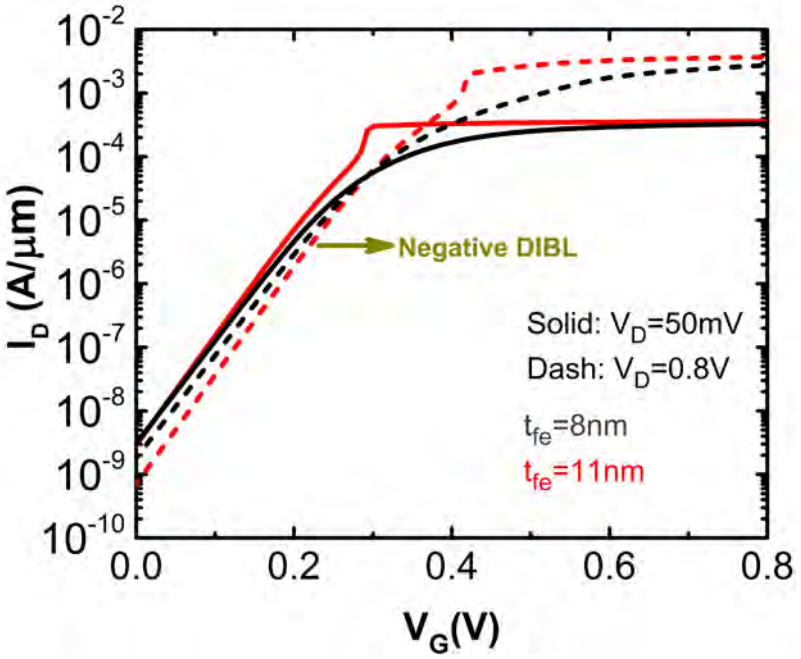
14nm node NCFinFET by Global Foundries

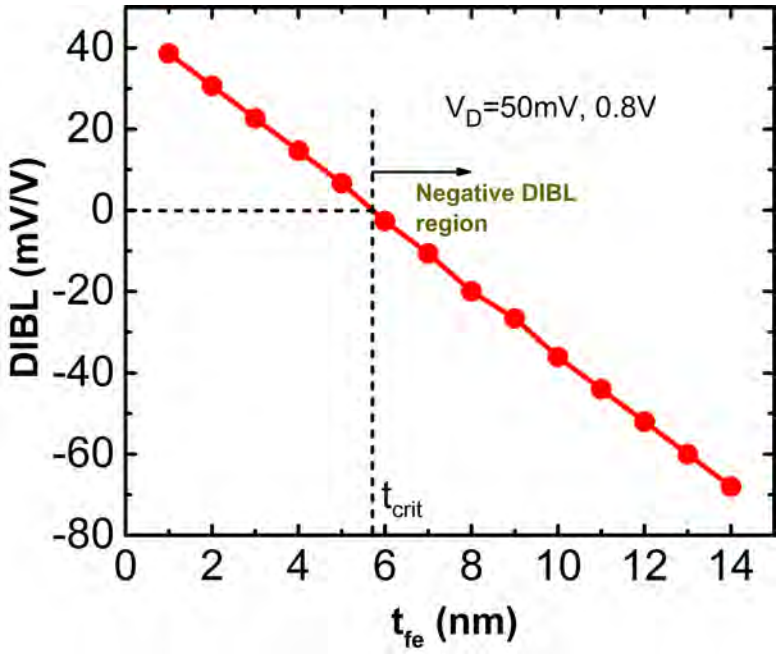
Krivokapic et al., *IEDM*, 2017, pp. 15.1.1–15.1.4.



M. Si et al., *Nature Nanotechnol.*, vol. 13 , pp. 24–28, 2018.

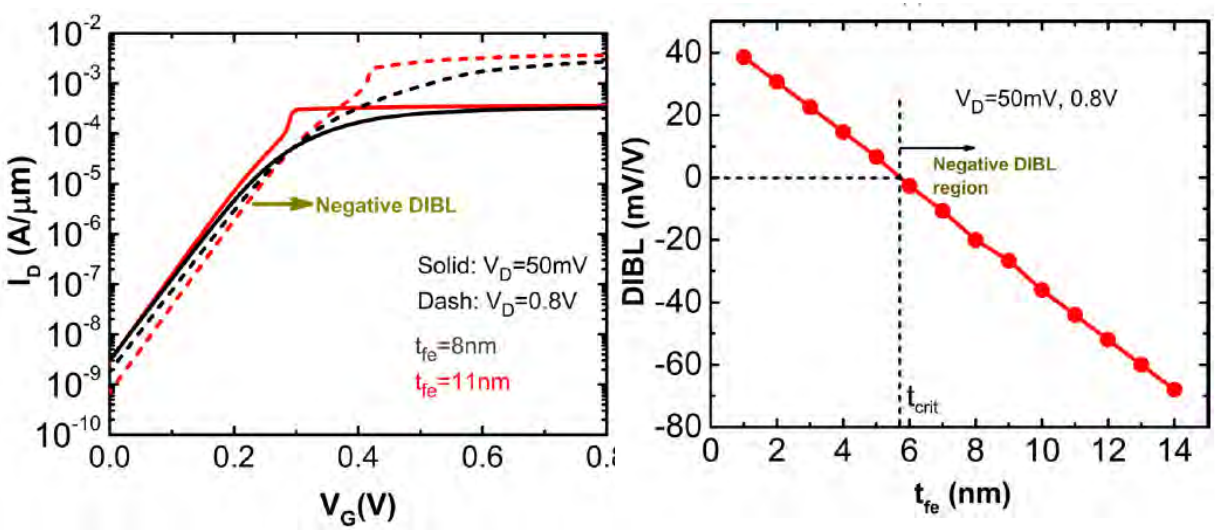
Negative DIBL



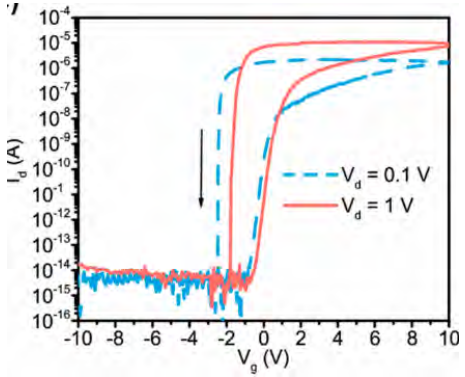


- V_D reduces Q_G which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with t_{fe} due to increased V_{fe} drop.
- V_{th} increases with V_D instead of decreasing.
  - Higher I_{ON} still lower I_{OFF}!

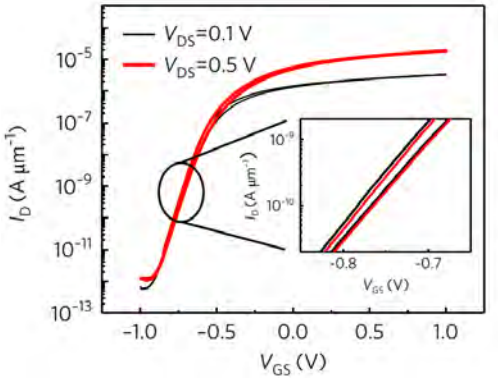
Negative DIBL/DIBR Effect



G. Pahwa et al., *IEEE Eur. Solid-State Device Res. Conf. (ESSDERC),* Sep. 2016, pp. 41–46.



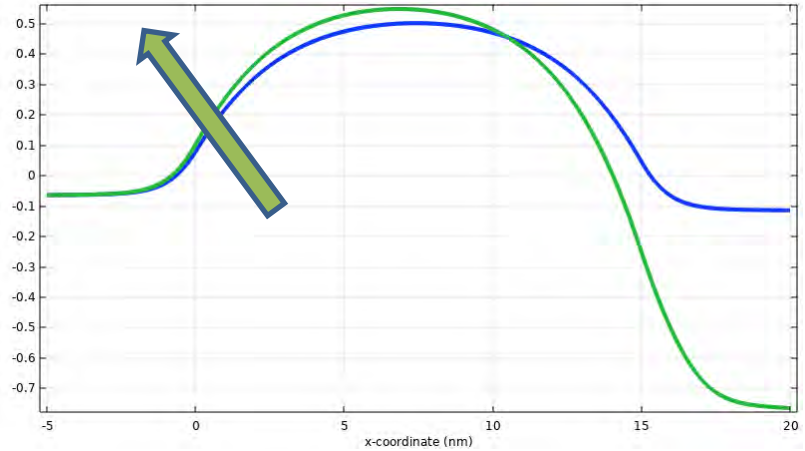
Xu et al., *ACS Nano*, 2018



M. Si et al., *Nature Nanotechnol.*, vol. 13 , pp. 24–28, 2018.

$$V_D \uparrow, Q_G \downarrow, V_{fe} \uparrow, V_{int} \downarrow, V_{th} \uparrow$$

V_D increases



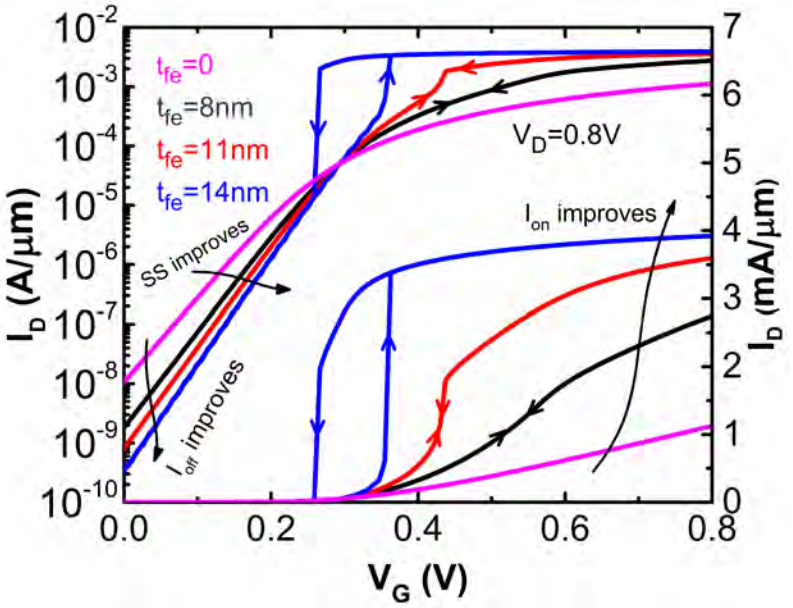
- V_{th} increases with V_D instead of decreasing. Higher I_{ON} still lower I_{OFF}!
- Negative DIBL increases with t_{fe} due to increased V_{fe} drop.

I_D-V_G Characteristics – High V_{DS}

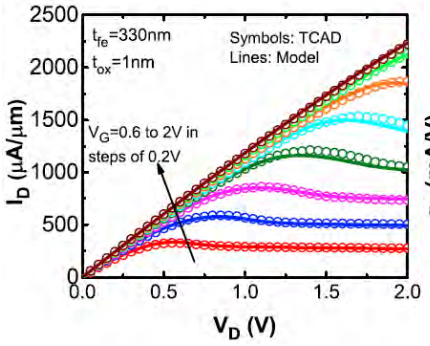
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is the region of instability.

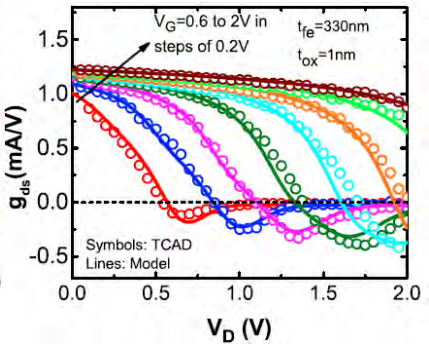
- As t_{fe} increases
  - SS reduces, I_{ON} increases.
  - I_{OFF} reduces for high V_D.

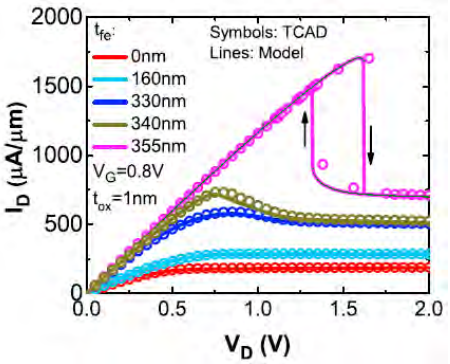
- Width of hysteresis at larger thicknesses can be controlled with V_D.



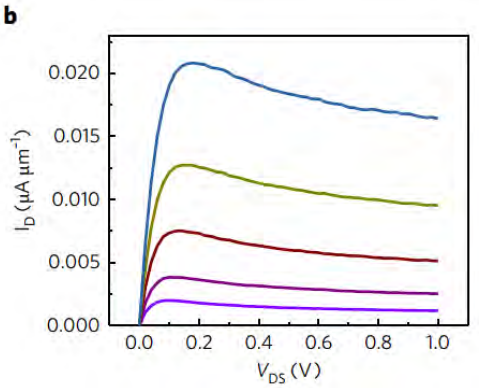
Negative Output Differential Resistance



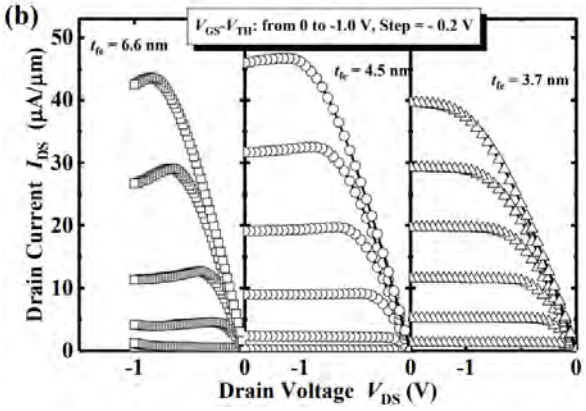


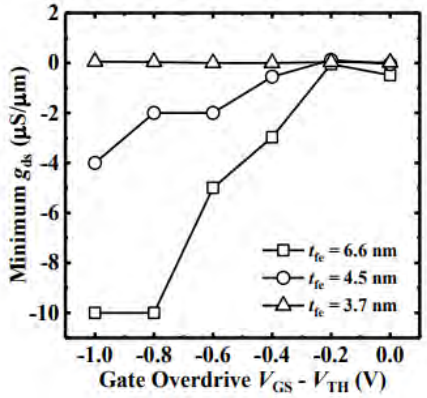


G. Pahwa *et al.*," *IEEE TED*, Dec. 2016

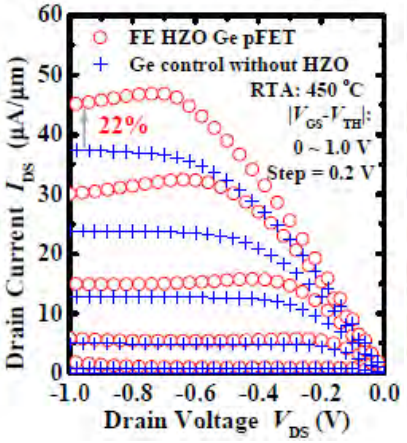


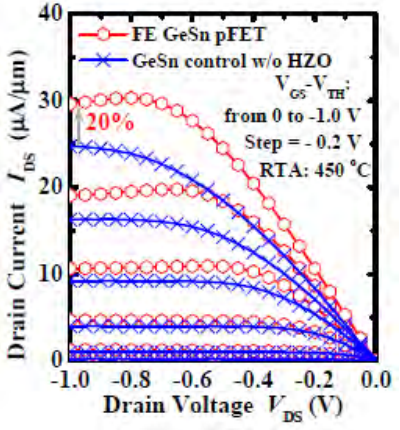
Mengwei Si *et al.*, *Nature Nanotechnology, 2018*





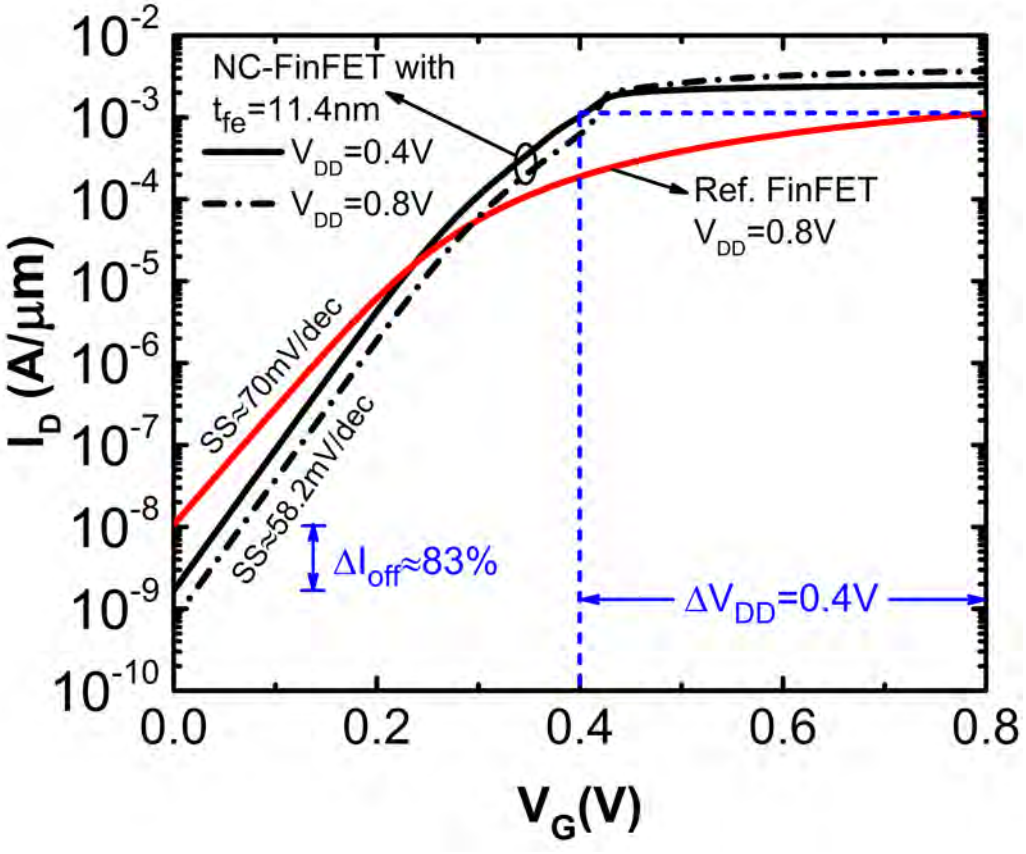
J. Zhou *et al.*, *IEEE, JEDS, 2018*





J. Zhou *et al.*, *IEDM 2016*

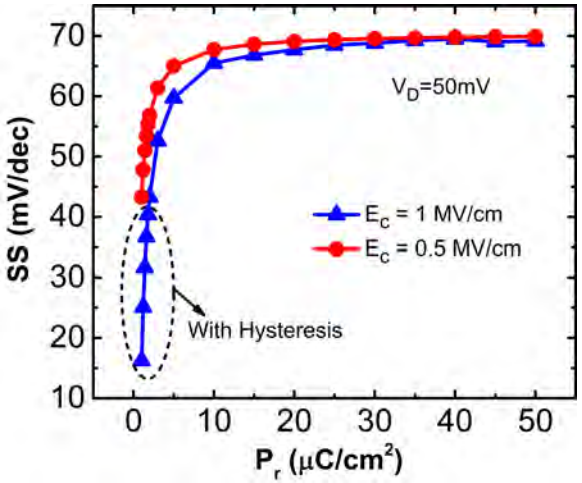
Optimum NC-FinFET

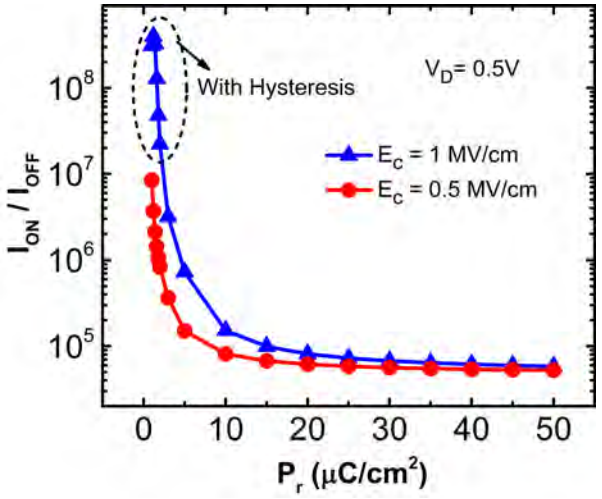


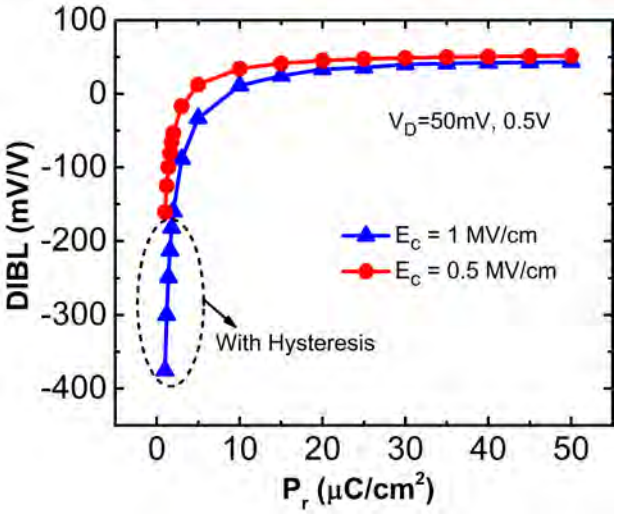
- Same I_{ON} as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- V_{DD} reduction by 0.4 V.
- I_{OFF} reduction by 83 %.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE European Solid-State Device Research Conference (ESSDERC), Lausanne, Switzerland, Sept. 2016. (Invited)

Ferroelectric Parameters Variation







If $\gamma = 0$,

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{{P_r}^3}$$

P_r = Remnant Polarization

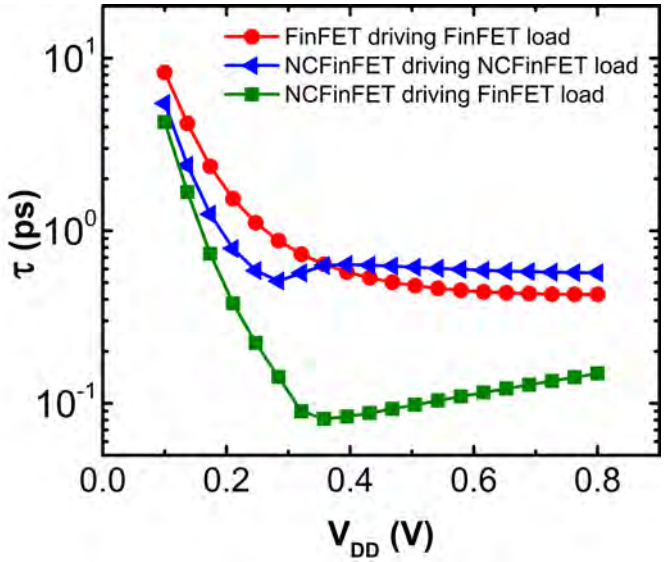
E_c = Coercive Field

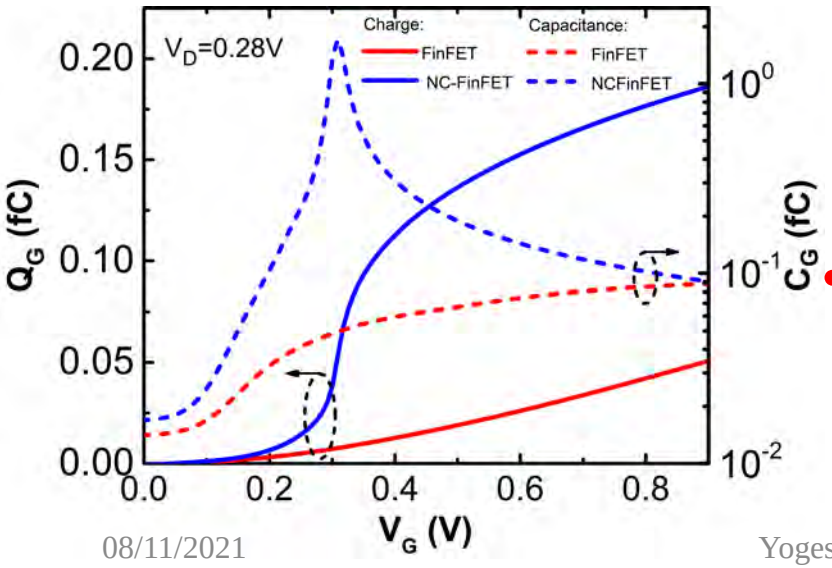
$$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$$

- Low P_r and high E_c
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I_{ON} but reduce I_{OFF} due to a more negative DIBL ⇒ high I_{ON}/I_{OFF}.

D. Ricinschi et al., JPCM, vol. 10, no. 2, p. 477, 1998.

Intrinsic Delay



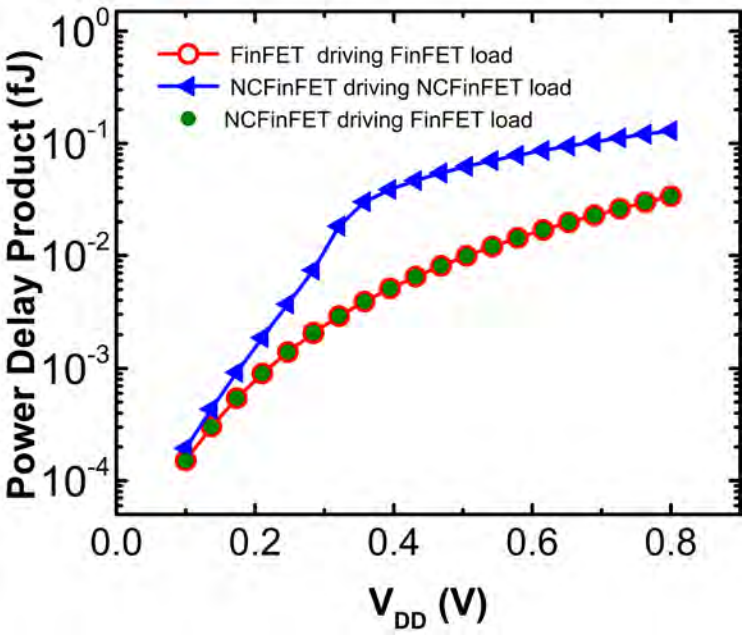


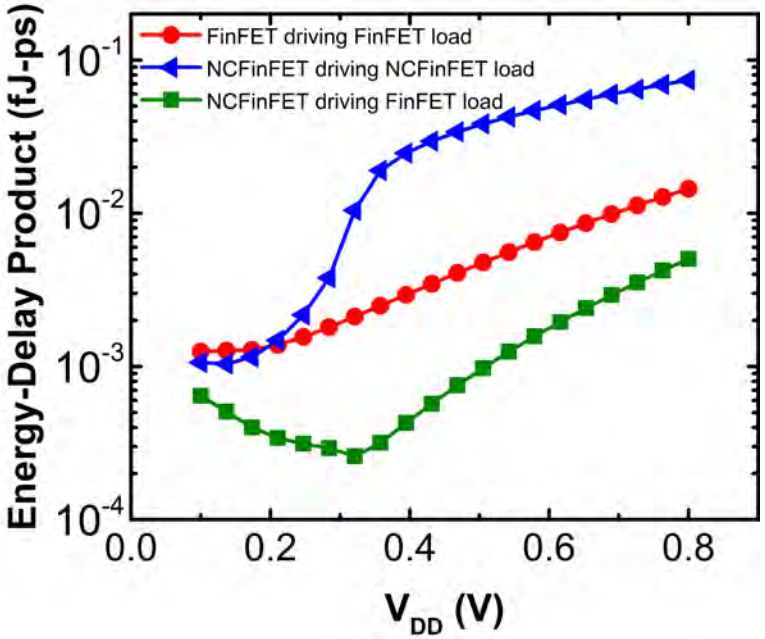
$$\text{Delay, } \tau = \frac{\Delta Q_G}{I_{ON}}$$

$$\Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD})$$

- NC-FinFET driving NC-FinFET
  - For high V_{DD}, high I_{ON} advantage is limited by large amount of ΔQ_G to be driven.
  - Outperforms FinFET at low V_{DD}.
  - Minimum at $V_{DD} \approx 0.28$ V corresponds to a sharp transition in Q_G.
- NC-FinFET driving FinFET load provides full advantage of NC-FinFET.

Power and Energy Delay Products



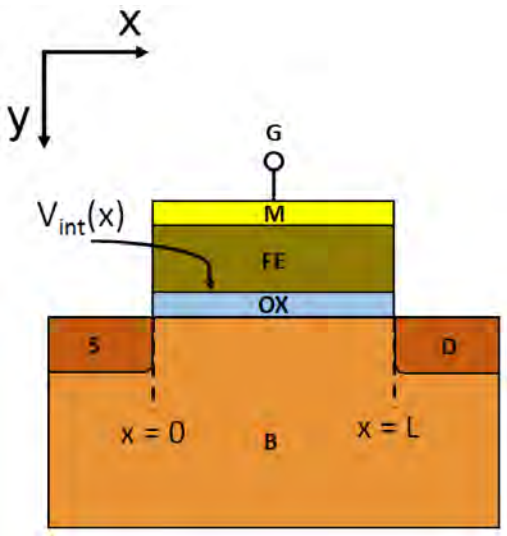


$$PDP = \Delta Q_G . V_{DD}$$

$$EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}}$$

- NC-FinFET driving NC-FinFET shows advantage only for low V_{DD}.
- NC-FinFET driving FinFET load is the optimum choice.

Modeling of MFIS NCFET



Contrast with MFIMS structure:

- P and V_{int} vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models[1,2]:

Implicit equations – tedious iterative numerical solutions

[1] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.

[2] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct. 2010.

Explicit Modeling of Charge

$$V_{fe} = Et_{fe} = aQ_G + bQ_G{}^3$$

Voltage Balance:

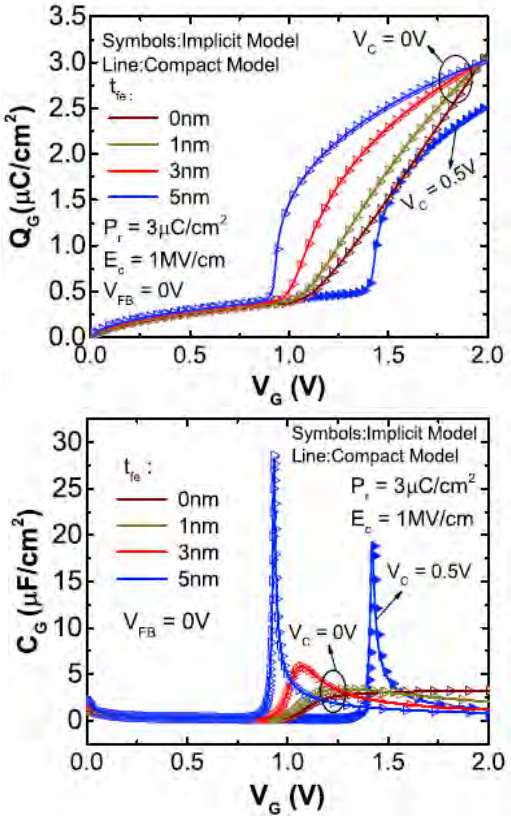
$$V_G - V_{FB} = V_{fe} + \frac{Q_G}{C_{ox}} + \psi_S = a_{eff} Q_G + bQ_G{}^3 + \psi_S$$

$Q_G - \psi_S$ relation[1]

$$Q_G = \text{sign}(\psi_S)\gamma C_{ox}\left[\psi_S + V_t(e^{-\psi_S/V_t} - 1) + e^{-(2\phi_F+V_C)/V_t}(V_t e^{\psi_S/V_t} - \psi_S - V_t)\right]^{1/2}$$

→ Implicit equation in Q_G

→ **Goal:** Explicit Model with good initial guesses for each region of NCFET operation

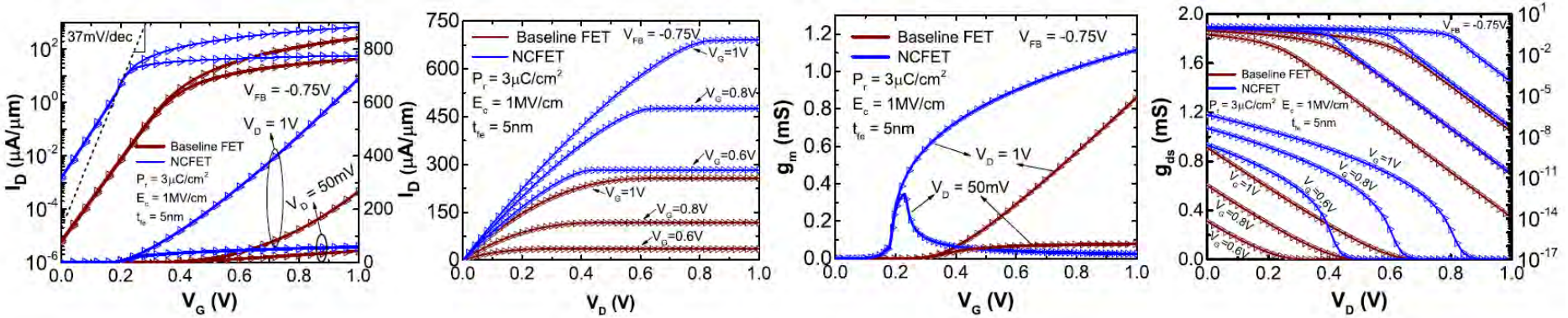


Both the Q_G and its derivatives match well with implicit model

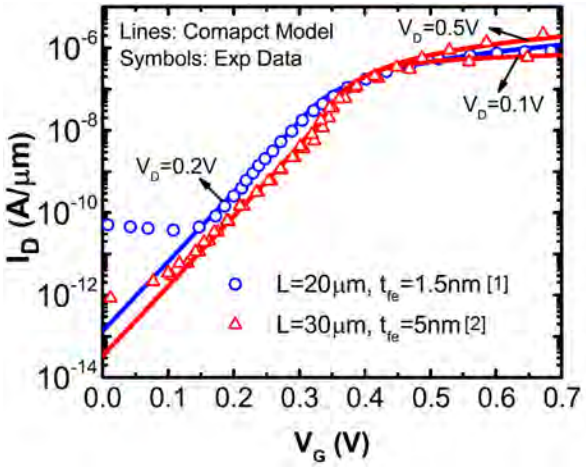
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," in *IEEE Transactions on Electron Devices*, March 2017.

Drain Current Model Validation

Against Full Implicit Calculations



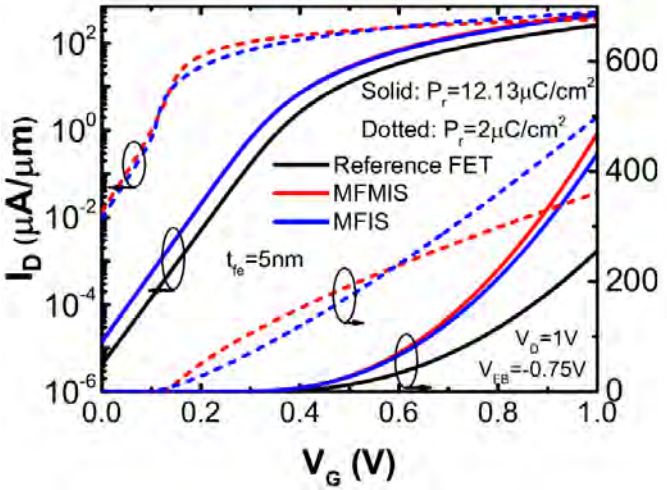
Against Experimental Data

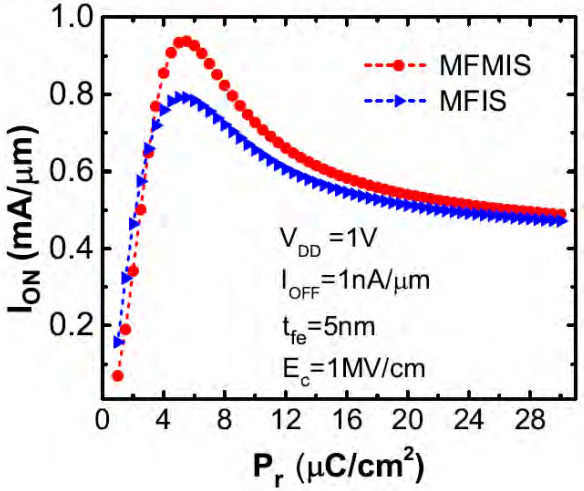


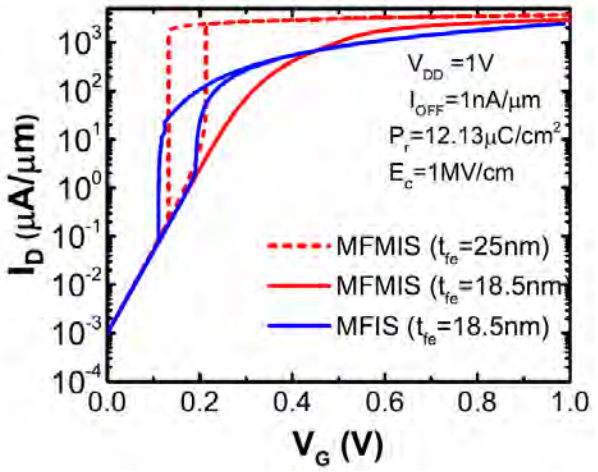
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," *IEEE Transactions on Electron Devices*, March 2017.

[1] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.1.1–12.1.4. [2] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.5.1–22.5.4.

MFIS Vs MFIS







- MFIS excels MFMIS for low P_r ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, pp. 867-873, March 2018.

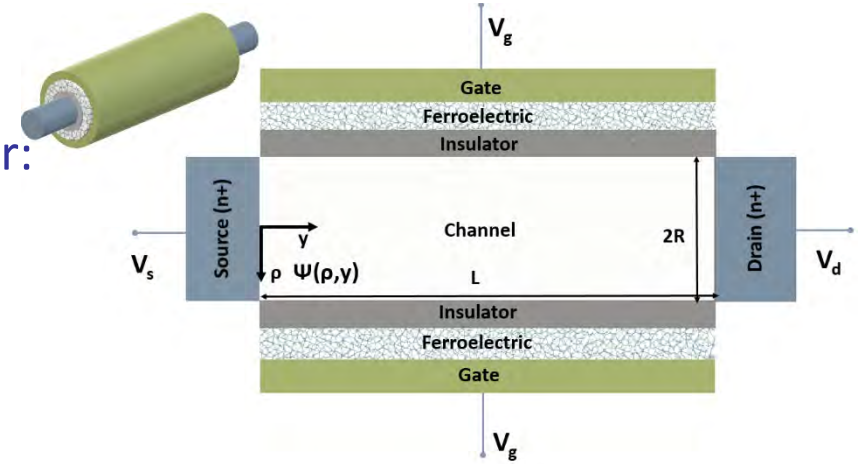
Compact Modeling of MFIS GAA-NCFET

$$V_{fe} = a_0 Q + b_0 Q^3$$

Radial Dependence in Ferroelectric Parameter:
(Ignored in others work)

$$a_0 = 2aR\ln[1 + t_{fe}/(R + t_{ins})]$$

$$b_0 = 2bR^3[1/(R + t_{ins})^2 - 1/(R + t_{ins} + t_{fe})^2]$$



Mobile Charge Density:

$$Q = \varepsilon_{si}\left(\frac{d\psi}{d\rho}\right)\Big|_{\rho=R} = \left(\frac{2\varepsilon_{si}}{R}\right)\left(\frac{2kT}{q}\right)\left(\frac{\beta^2}{1-\beta^2}\right)$$

Voltage Balance:

$$V_g - \Delta\phi - \psi_s = (a_0 + 1/C_{ins})Q + b_0 Q^3$$

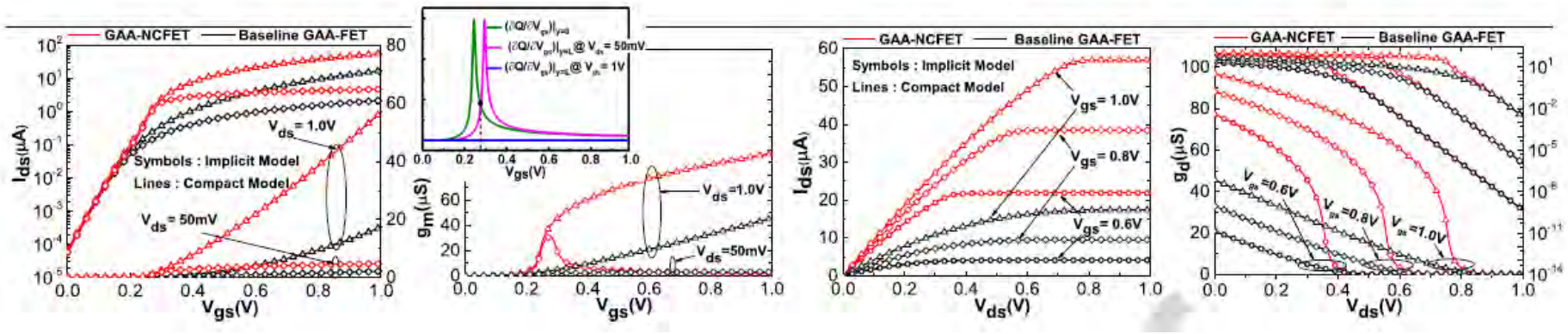
Implicit Equation in β:

$$\ln(\beta) - \ln(1-\beta^2) + m\left(\frac{\beta^2}{1-\beta^2}\right) + n\left(\frac{\beta^2}{1-\beta^2}\right)^3 - G = 0$$

→ **Goal:** Explicit Model for β with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.

Drain Current Model Validation

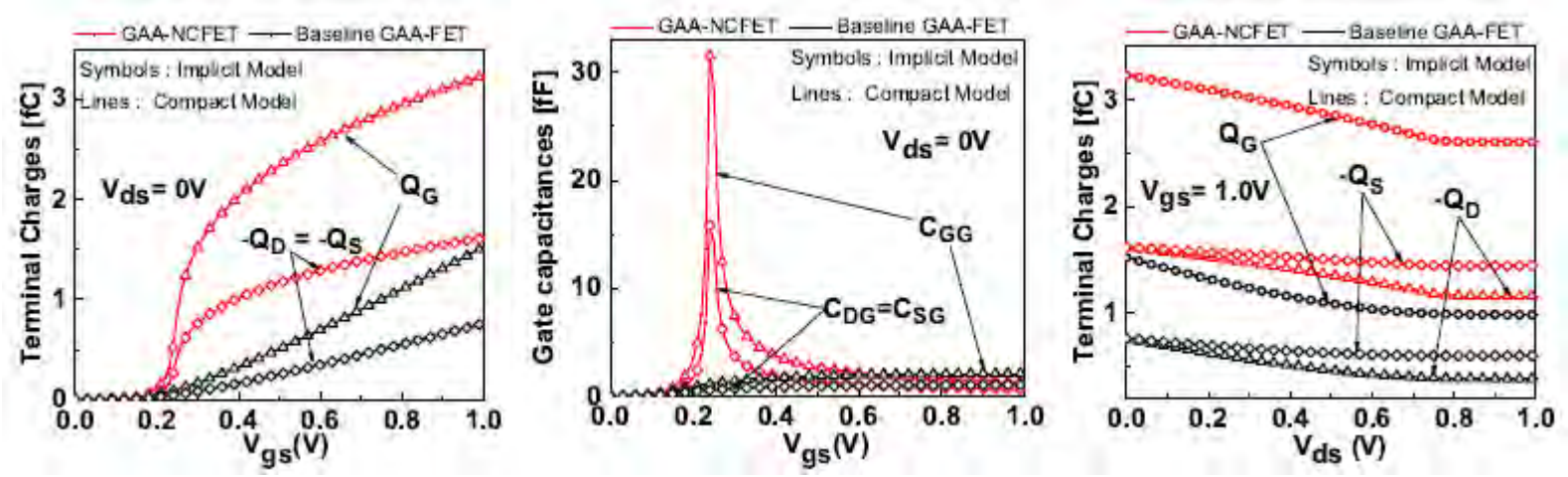
Against Full Implicit Calculations



- In contrast to bulk-NCFETs
  - Multi-gate NCFETs with an undoped body exhibit same I_{OFF} and V_{th} due to absence of bulk charges.
  - GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.

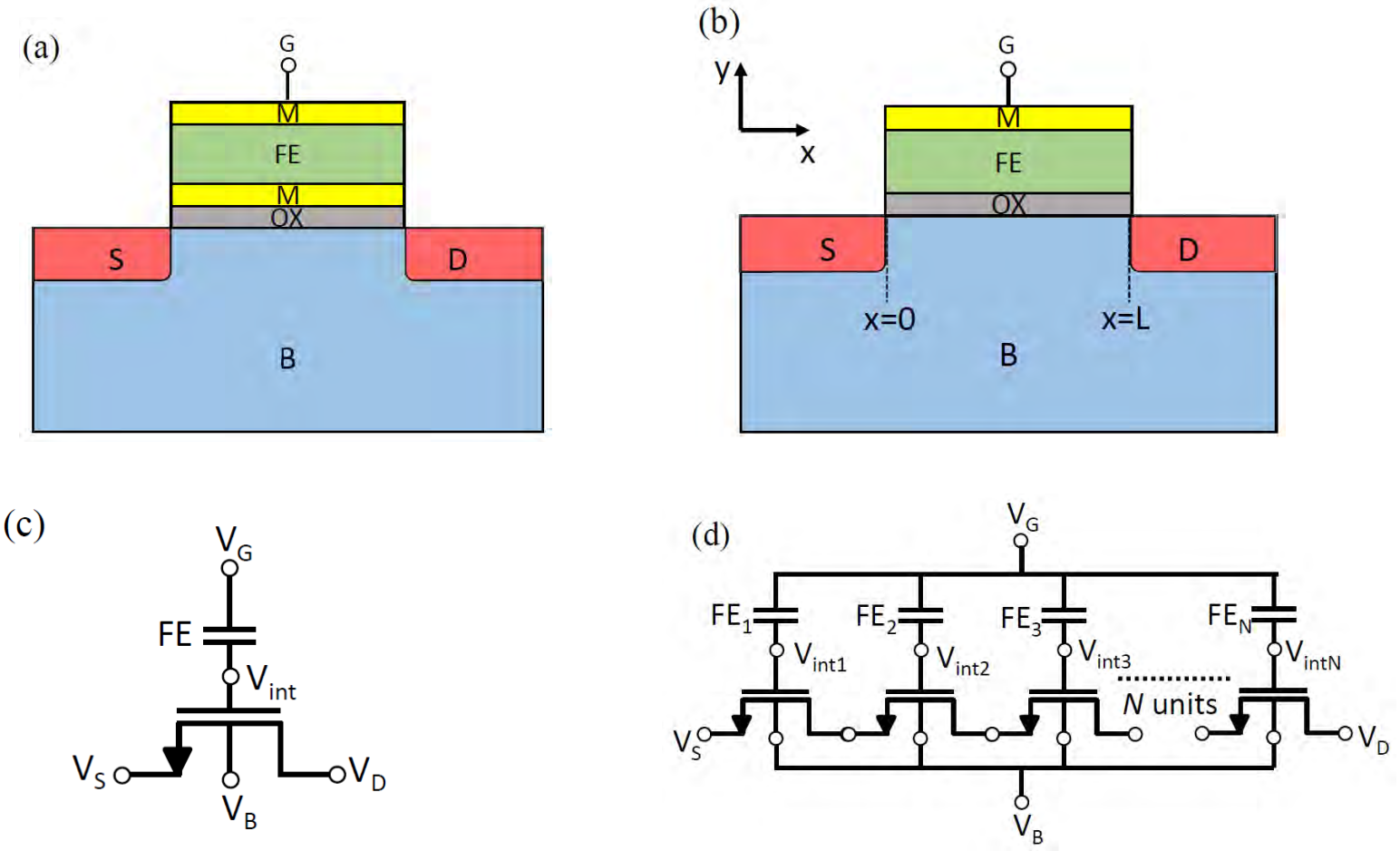
A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", IEEE Transactions on Electron Devices, Vol. 65, Issue 5, pp. 2024-2032, May 2018.

Terminal Charges in GAA-NCFET



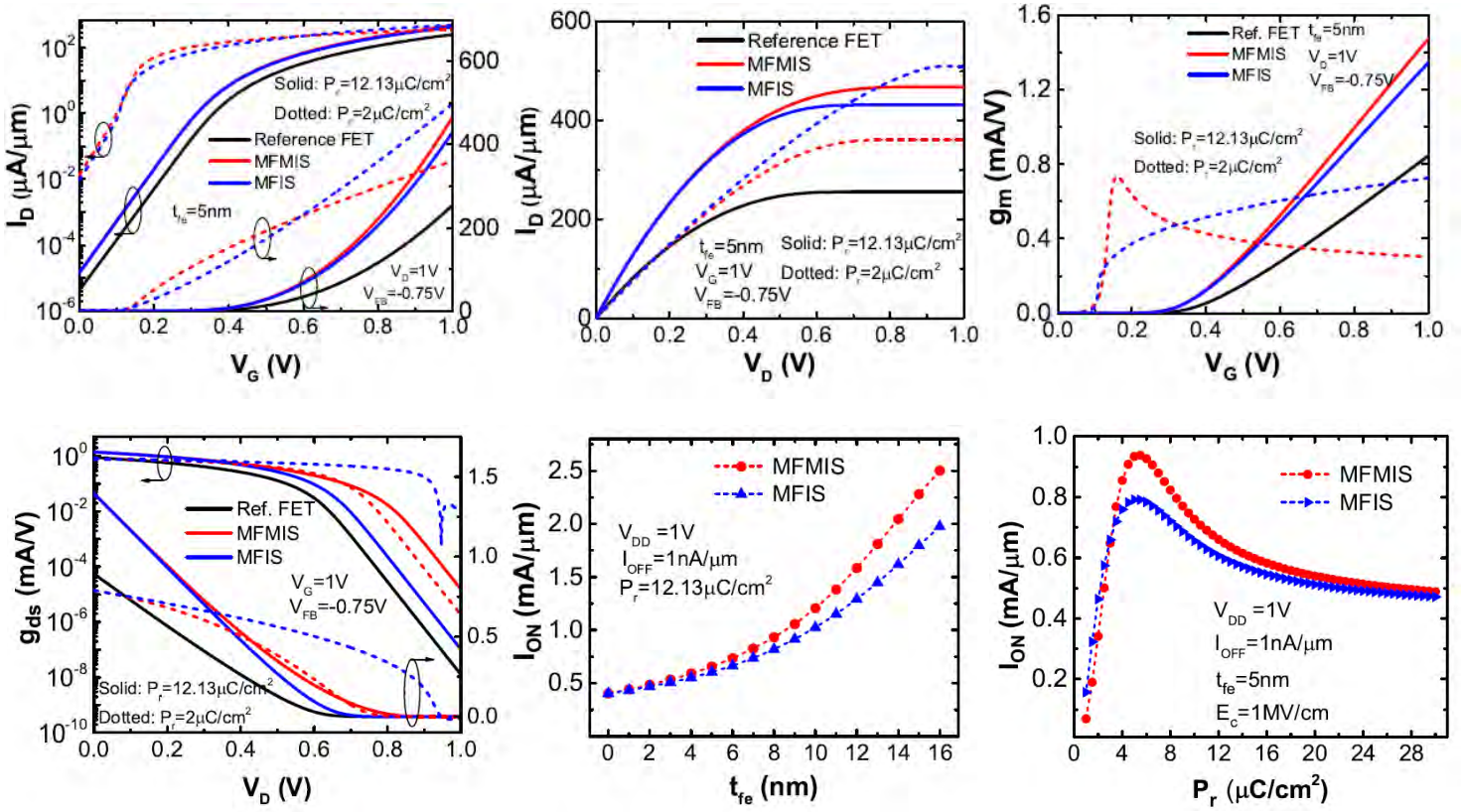
- Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
- For high V_{DS}, the Q_G for GAA-NCFET is saturates to $(4/5)^{th}$ of the maximum value (at Vds = 0) in contrast to conventional devices for which it saturates to $(2/3)^{rd}$ of the maximum value.

MFMIS Vs MFIS



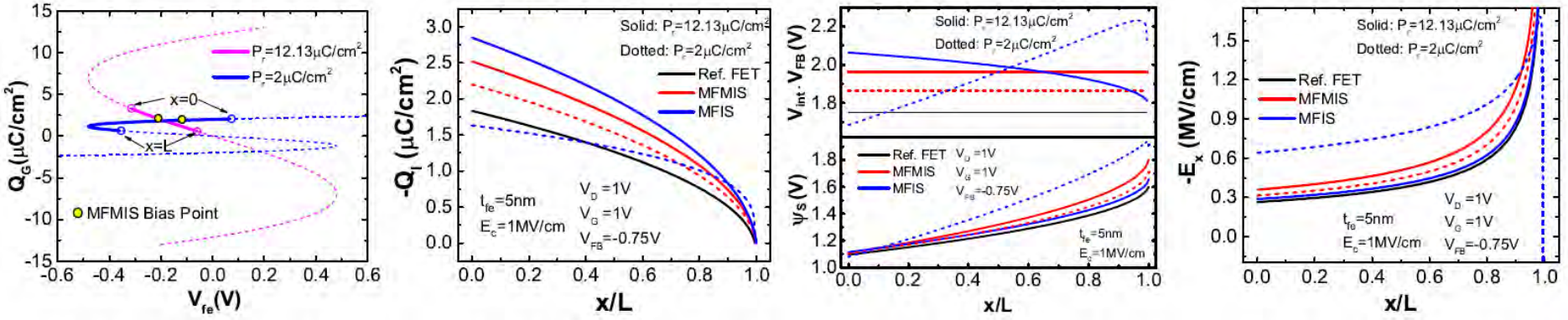
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

Comparing I_D-V_G and I_D-V_D Characteristics (long channel)



- MFIS excels MFMIS for low P_r ferroelectrics only, in long channel NCFETs.

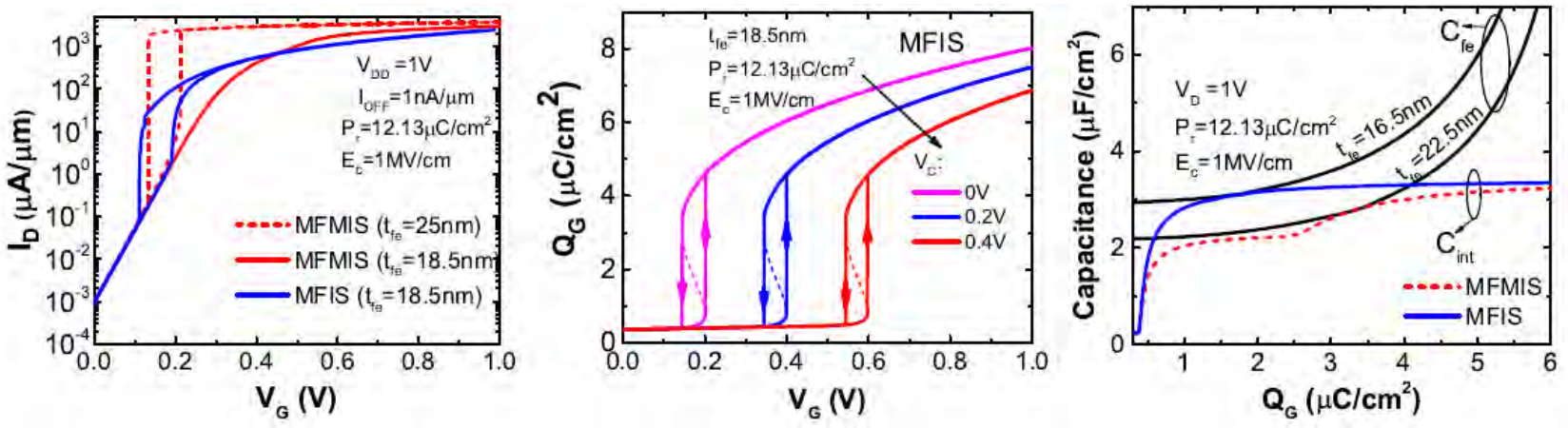
Understanding different trends with P_r



- Total current in ON regime ≈ drift current = inversion charge * horizontal electric field
- For high P_r, charge is higher for MFIS, but electric field in channel is low due to a decreasing V_{int} profile from source to drain, which results in lower current than MFMIS.
- For low P_r, charge is lower for MFIS, but electric field in channel is high due to a increasing V_{int} profile from source to drain, which results in higher current than MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

Hysteresis Behavior



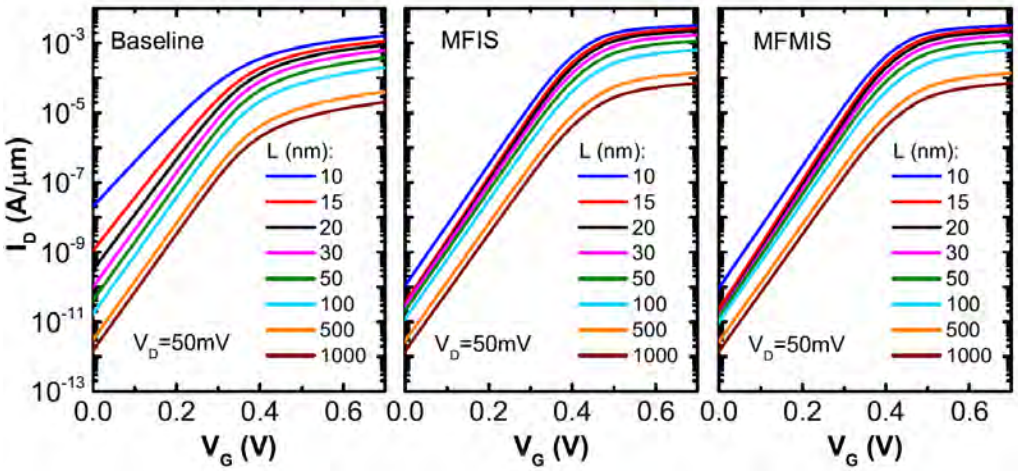
- Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
- Source end dipole switches, first, owing to its least hysteresis threshold.
- Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

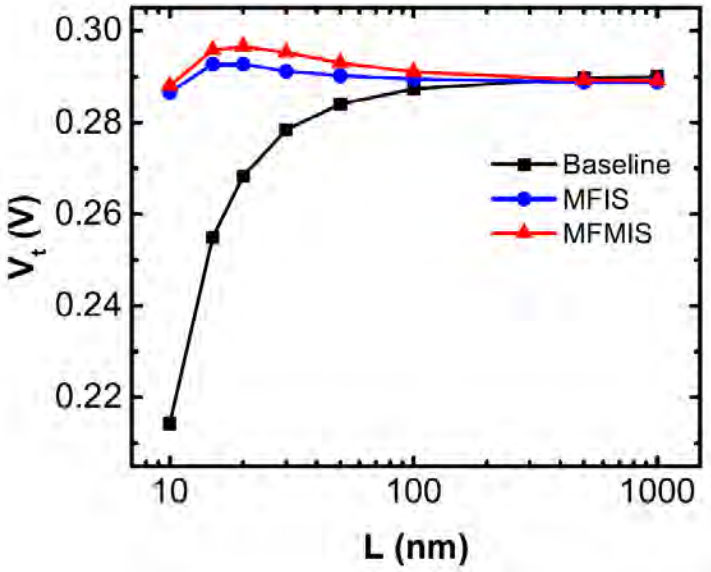
G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "*Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures*", IEEE Transactions on Electron Devices, Vol. 65, Issue 3, Mar. 2018.

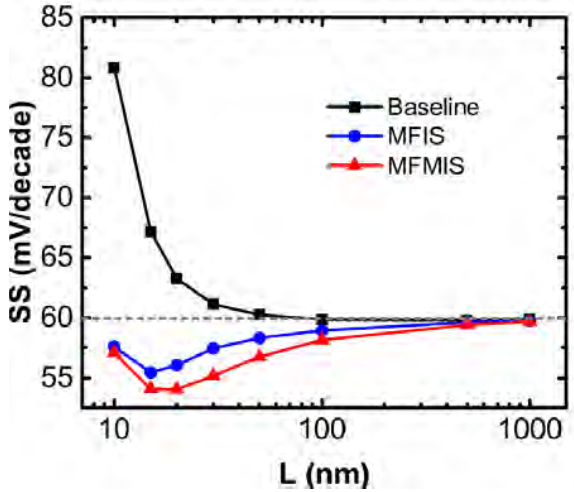
MFMIS vs MFIS: Short Channel Effects

OFF Regime (low V_D)

2D Numerical Simulation Results in COMSOL





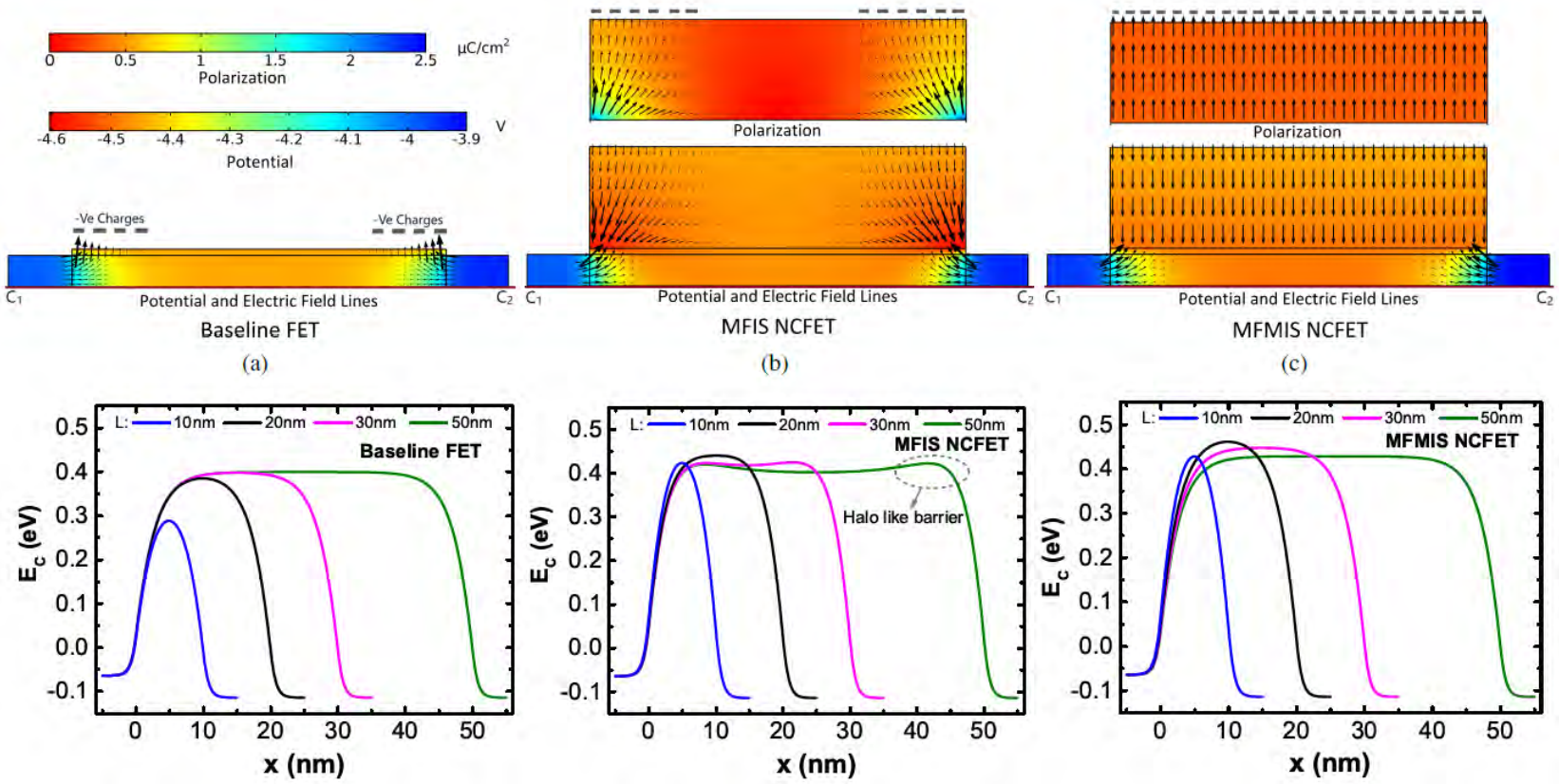


P_r=0.1213 μC/cm^2 E_C=1MV/cm t_{fe}=8nm

NCFETs exhibit reverse trends in V_t and SS with scaling except for very small lengths.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", IEEE Transactions on Electron Devices, Vol. 65, Issue 11, pp. 5130-5136, Nov. 2018.

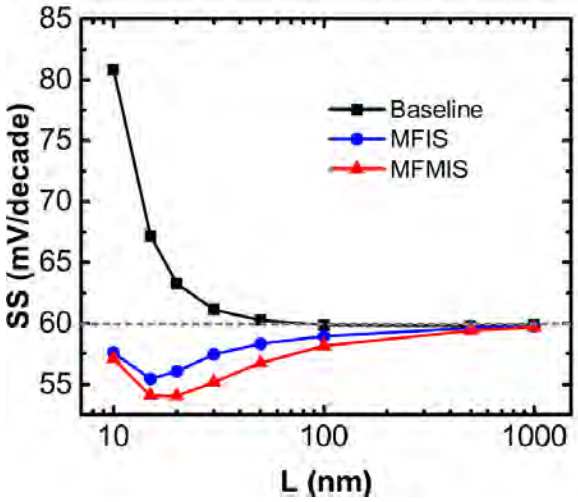
Reverse V_t Shift with Scaling

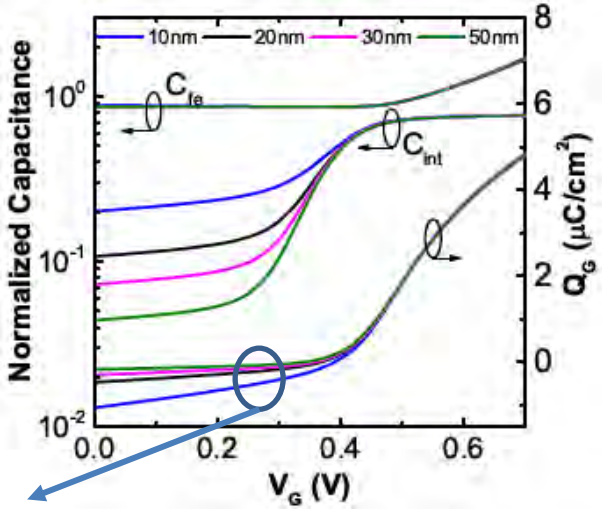


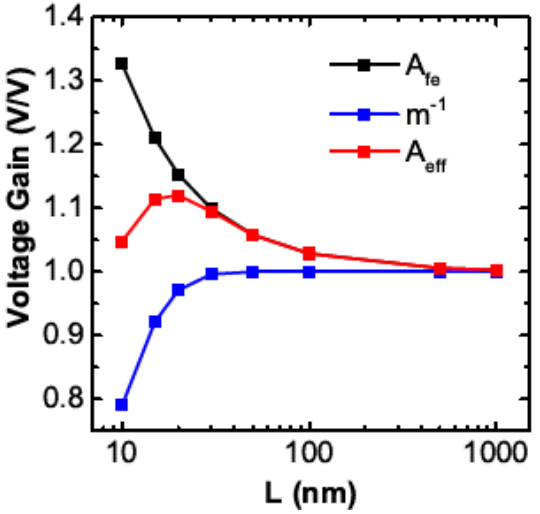
- Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.
- In MFIS, fringing effect remains localized to channel edges only → Halo Like barriers.
- In MFMIS, internal metal extends this effect to the entire channel → larger V_t than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", IEEE Transactions on Electron Devices, Vol. 65, Issue 11, pp. 5130-5136, Nov. 2018.

Reverse SS trends with Scaling







Negative Fringing Charge

$$\mathrm{SS} = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial \psi_c}{\partial \log_{10} I_D} \frac{m}{A_{\mathrm{fe}}}$$

$m = \partial V_{\mathrm{int}} / \partial \psi_c$ = Body Factor

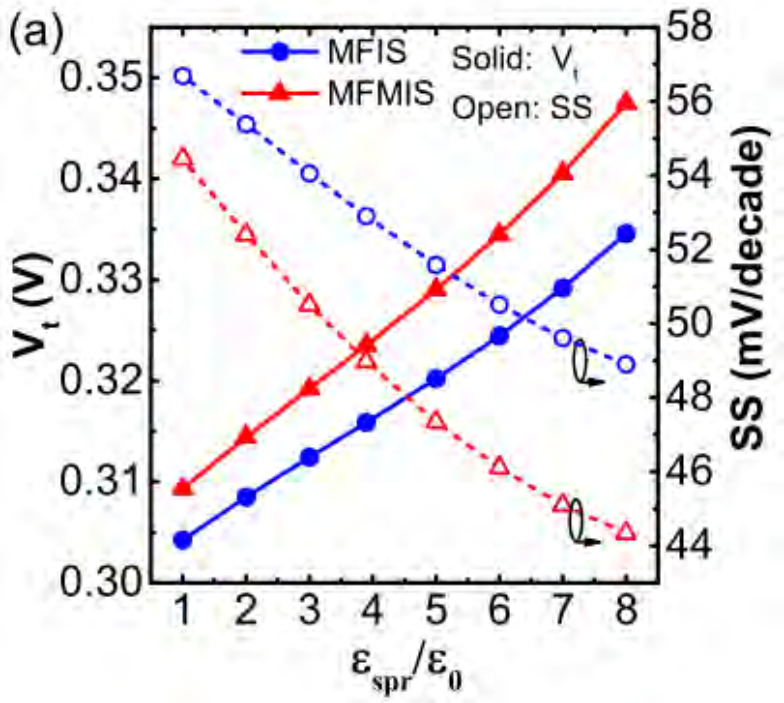
$A_{\mathrm{fe}} = \partial V_{\mathrm{int}} / \partial V_G$ = Ferroelectric gain

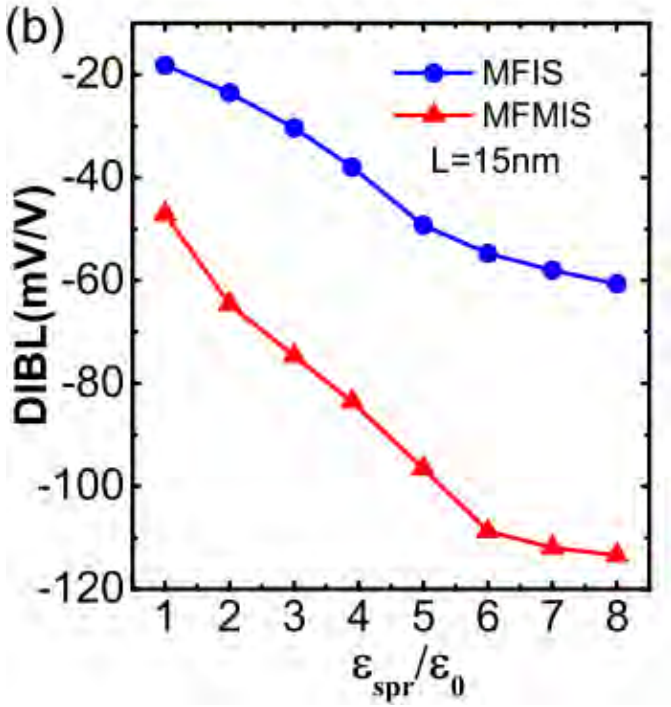
$$A_{\mathrm{eff}} = m^{-1} A_{\mathrm{fe}} = \frac{1}{1 - \frac{C_{\mathrm{int}}}{|C_{\mathrm{fe}}|}}$$

$L \downarrow, \frac{C_{int}}{|C_{fe}|} \uparrow, A_{fe} \uparrow, m \downarrow, A_{eff} \uparrow, SS \downarrow$ (except for very small lengths where m dominates).

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", IEEE TED, Nov. 2018.

Impact of Spacer Permittivity

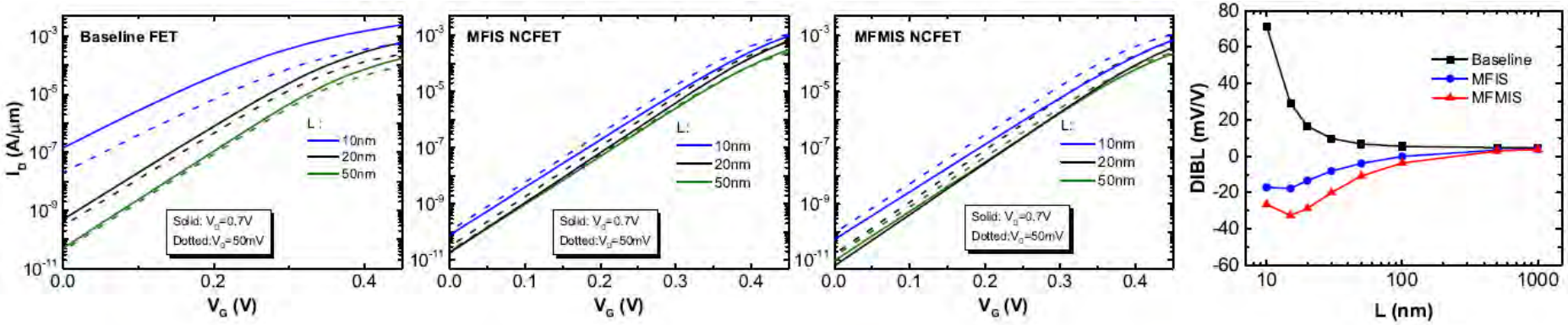


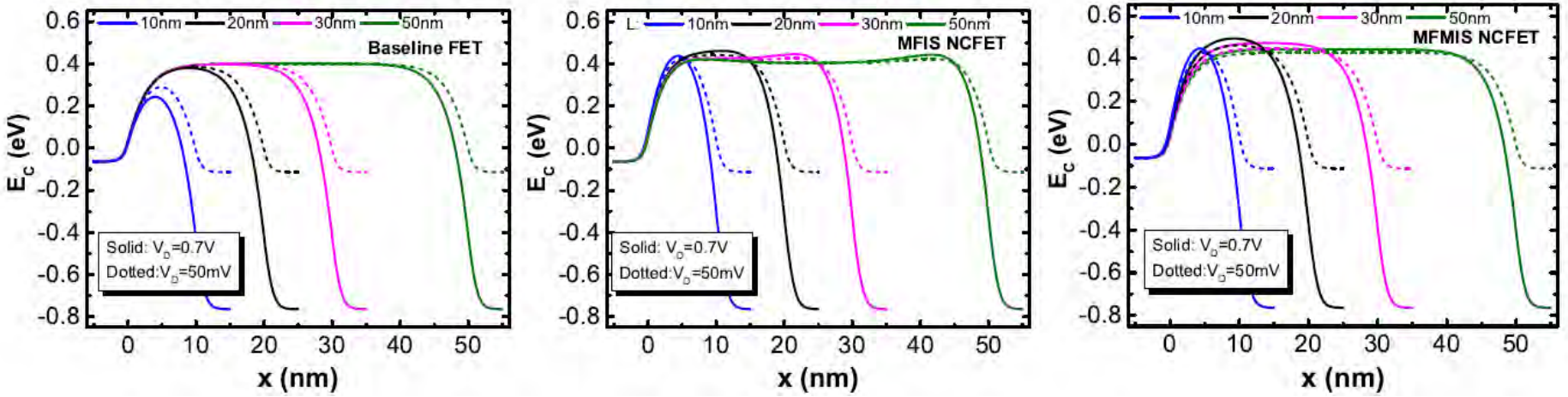


Increasing the spacer permittivity enhances the outer fringing electric field, which leads to a rise in Vt and reduction in SS and DIBL.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior*", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130–5136, Nov. 2018.

OFF Regime (high V_{DS}): Negative DIBL

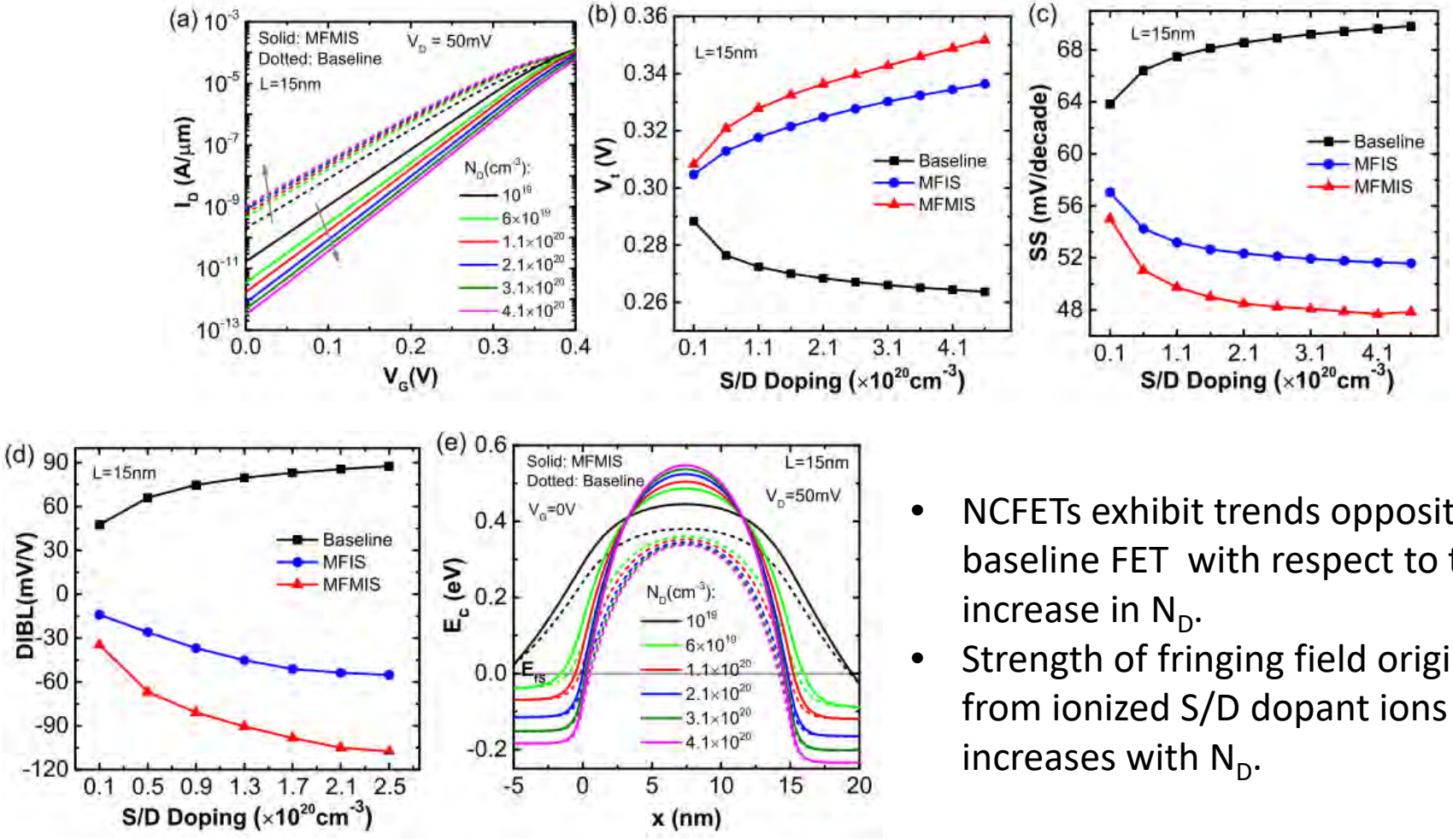




- Negative DIBL effect increases with Scaling.
- More pronounced in MFMIS than MFIS.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior", IEEE Transactions on Electron Devices, Vol. 65, Issue 11, pp. 5130-5136, Nov. 2018.

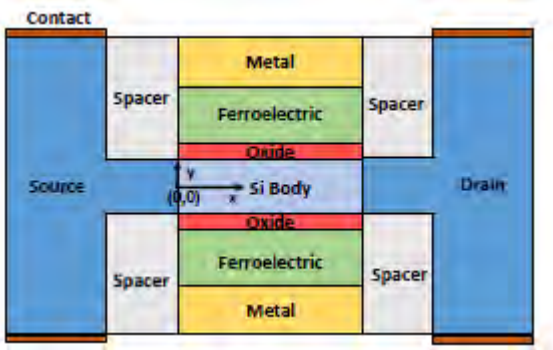
Impact of S/D doping

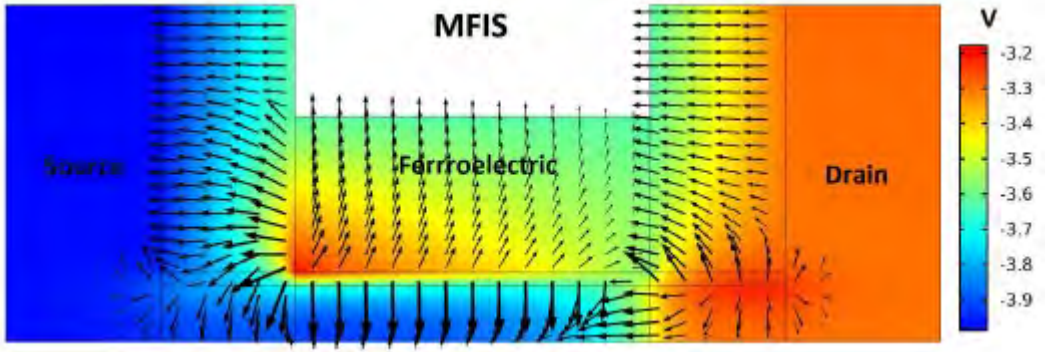


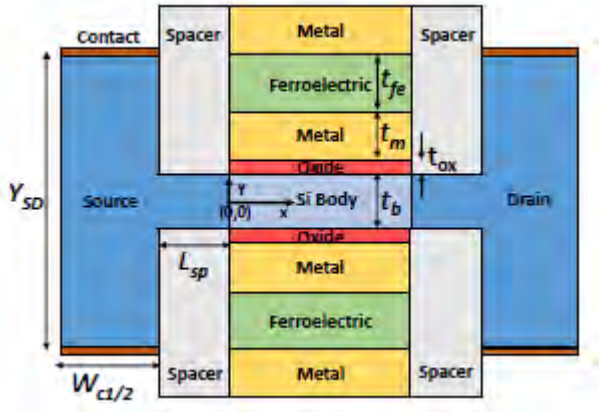
- NCFETs exhibit trends opposite to baseline FET with respect to the increase in N_D.
- Strength of fringing field originated from ionized S/D dopant ions increases with N_D.

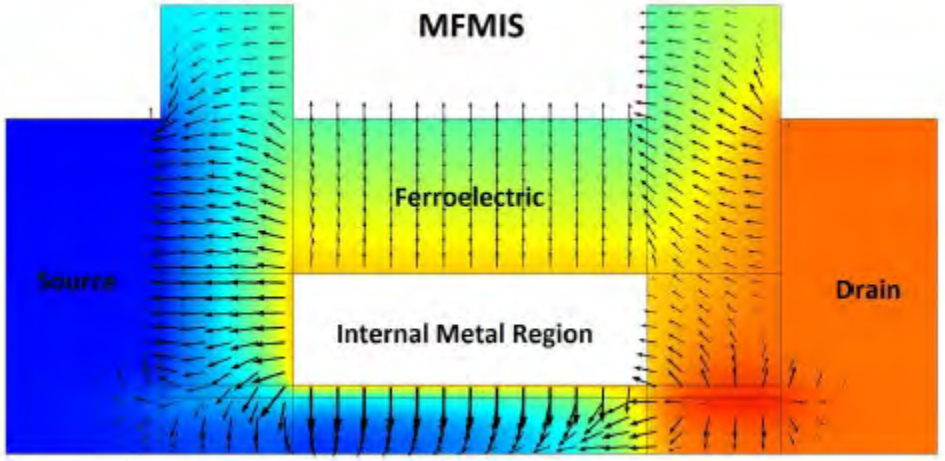
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "*Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior*", in IEEE Transactions on Electron Devices, vol. 65, no. 11, pp. 5130–5136, Nov. 2018.

ON Regime: Potential and field distribution







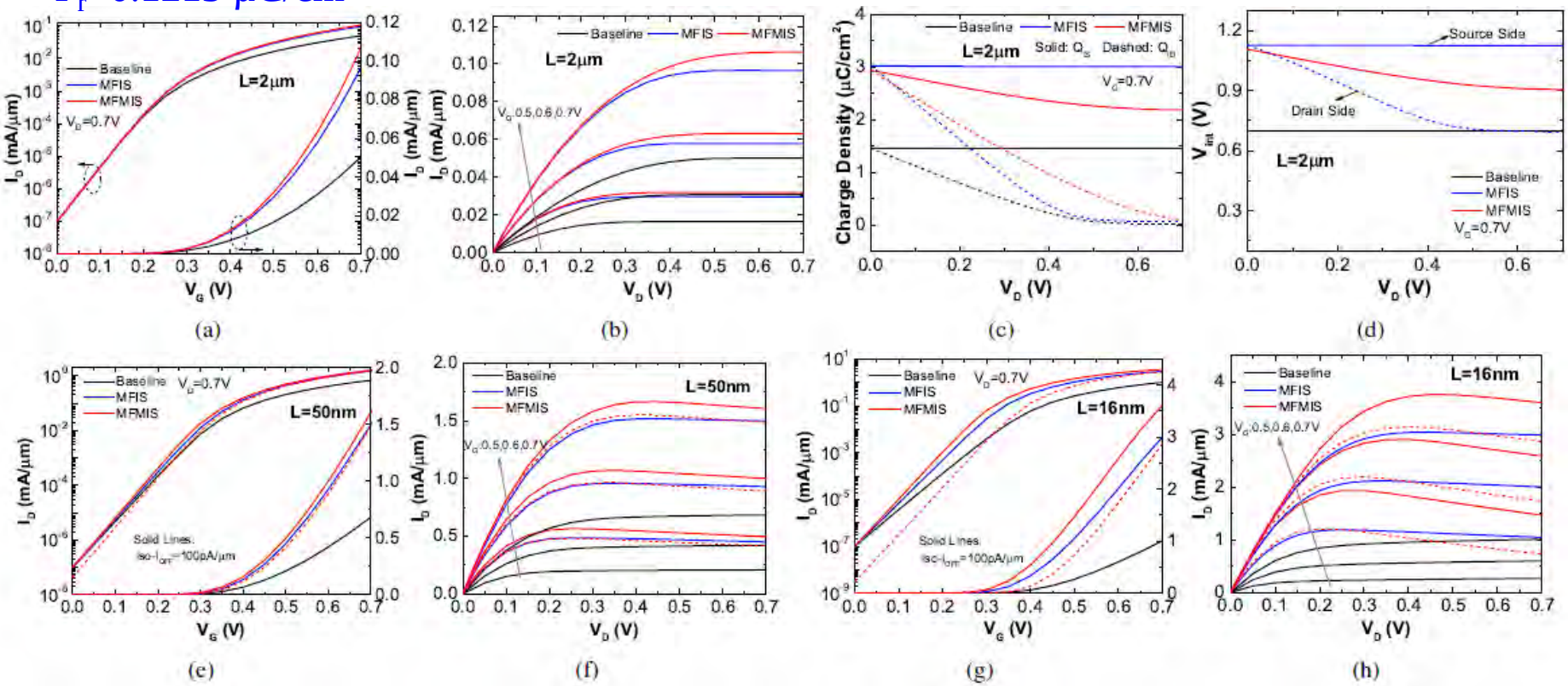


- The internal floating metal gate maintains a uniform electrical field distribution throughout the ferroelectric and a uniform potential (Vint) at ferroelectric-oxide interface.
- In the MFIS, however, electric field distribution and Vint at the interface are non-uniform.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above-Threshold Behavior", IEEE Transactions on Electron Devices, Vol. 66, Issue 3, pp. 1591–1598, Mar. 2019.

ON Regime: Electrical Characteristics

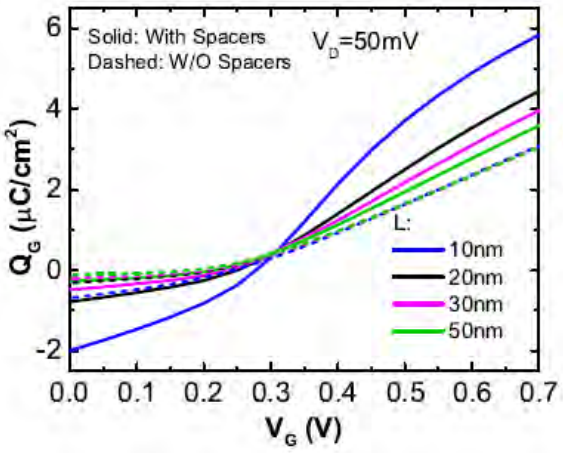
P_r=0.1213 μC/cm^2

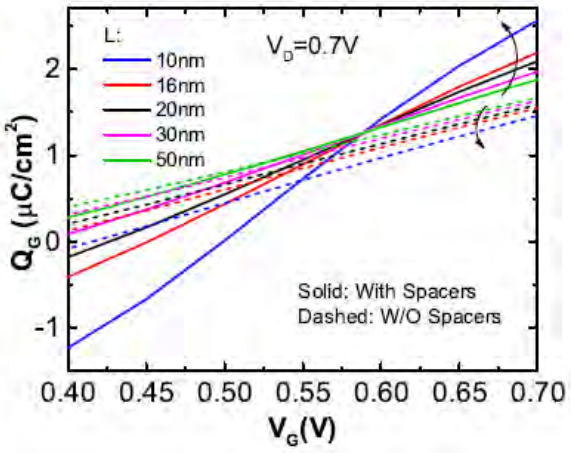


- Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling → lower V_{DSat} of MFIS results in lower I_{DS}.
- However, internal metal in MFMIS helps V_{DS} impact to easily reach source side→ Q_{IS} ↓ → Larger NDR effect in MFMIS than MFIS.
- In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former for iso-V_{FB} case only.

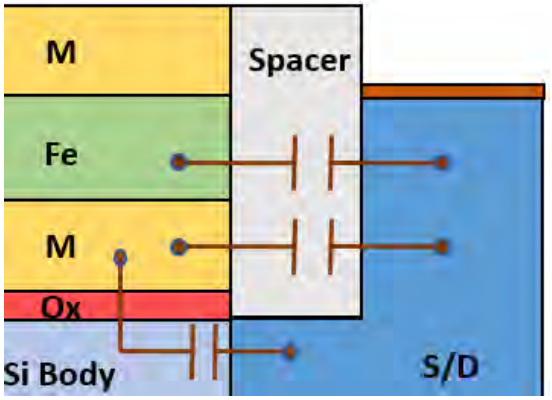
G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above-Threshold Behavior", IEEE Transactions on Electron Devices, Vol. 66, Issue 3, pp. 1591–1598, Mar. 2019.

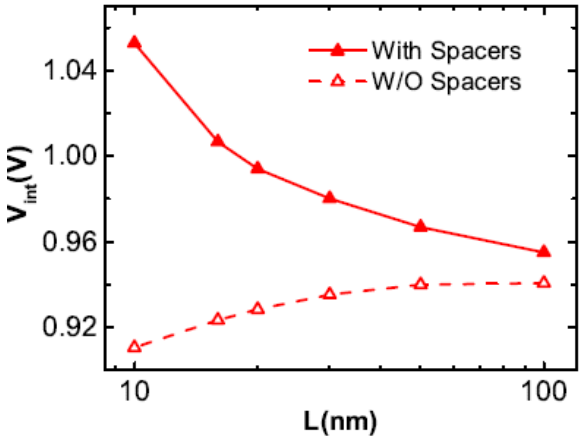
ON Regime: Impact of Spacers

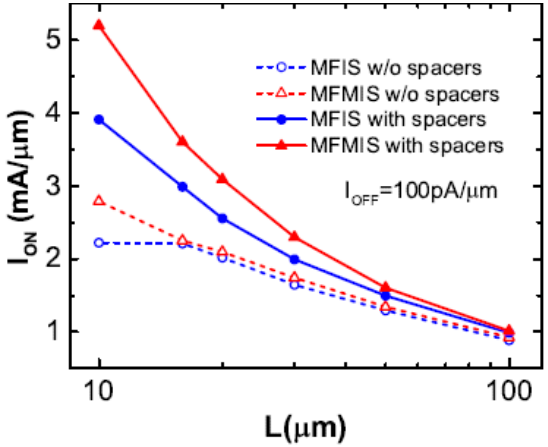




G. Pahwa et al., IEEE Transactions on Electron Devices, 2019.





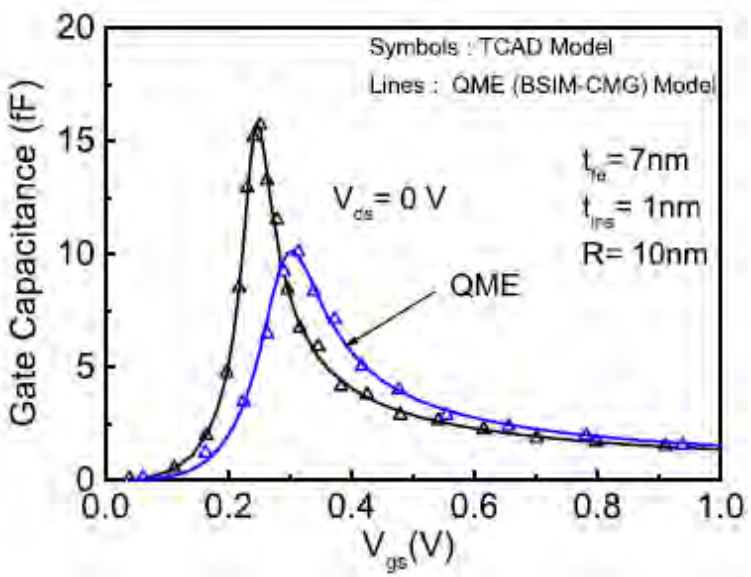


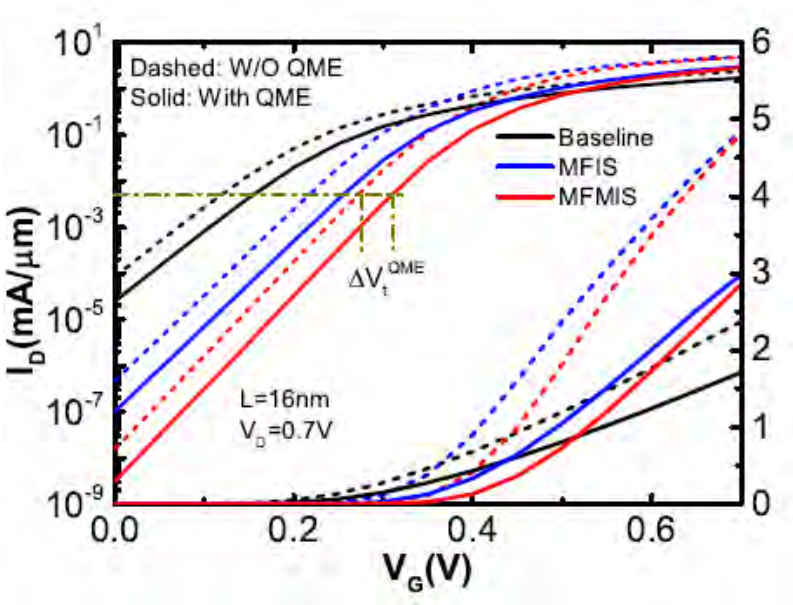
Without Spacers: Inner Fringing Only
With Spacers: Inner + Outer Fringing

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- C_{int} increases with scaling in NCFETs with spacers due to outer fringing capacitances→increases gain.
- For W/O spacers, V_{int} decreases due to absence of outer fringing, uncompensated drain side inner fringing, and increased drain to channel coupling.

Impact of Quantum Mechanical Effects



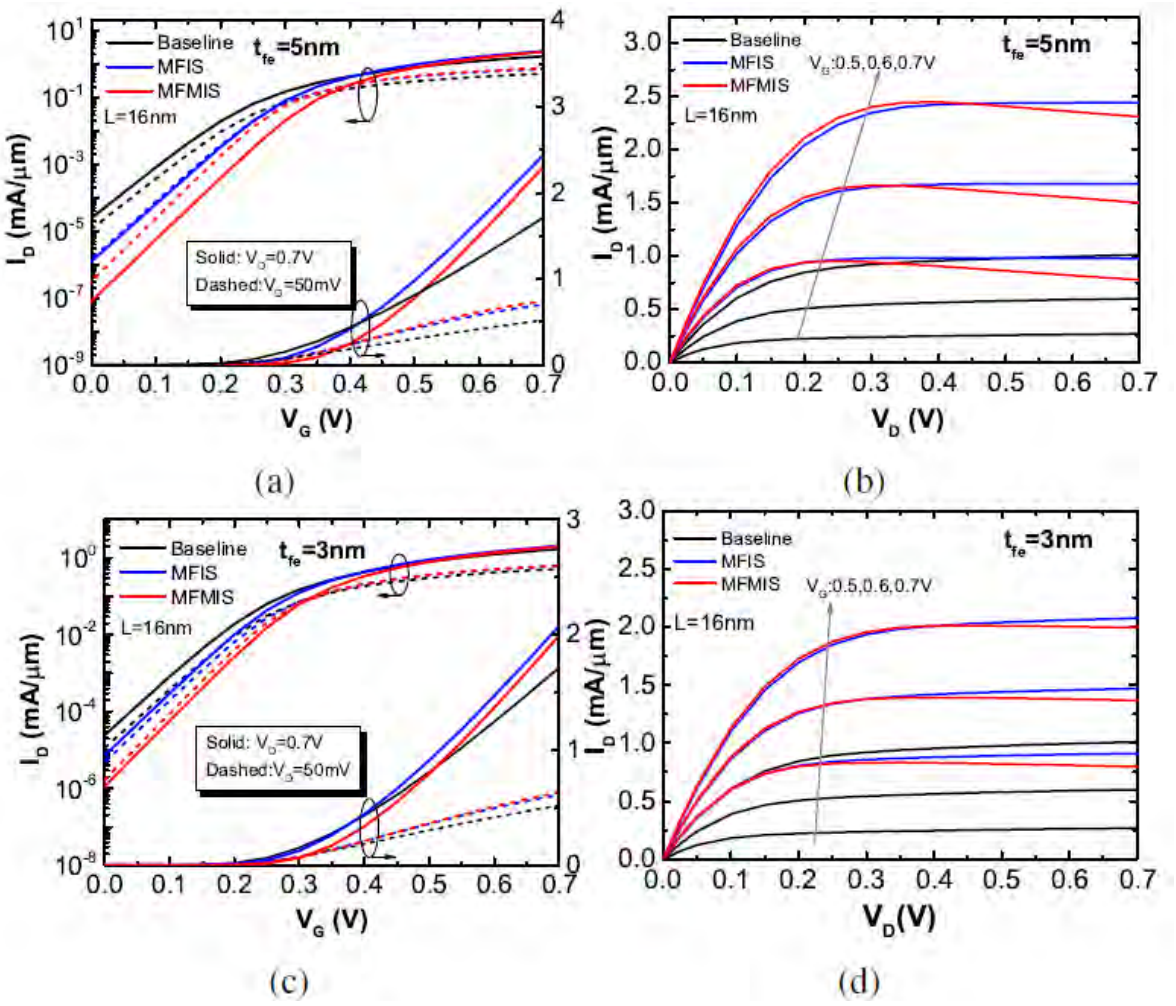


- The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.

A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", IEEE Transactions on Electron Devices, Vol. 65, Issue 5, pp. 2024-2032, May 2018.

G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above-Threshold Behavior", IEEE Transactions on Electron Devices, Vol. 66, Issue 3, pp. 1591–1598, Mar. 2019.

Impact of Ferroelectric Thickness



- NC influence decreases with t_{fe} which also starts to homogenise the internal gate potential.
- Thus, relative difference between MFIS and MFMIS diminishes as t_{fe} is decreased.

A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long Channel Gate-All-Around Negative Capacitance MFIS Transistor", IEEE Transactions on Electron Devices, Vol. 65, Issue 5, pp. 2024-2032, May 2018.

Does polarization damping really limit operating frequency of NC-FinFET based circuits?

Recent Demonstration by Global Foundries on 14nm NC-FinFET

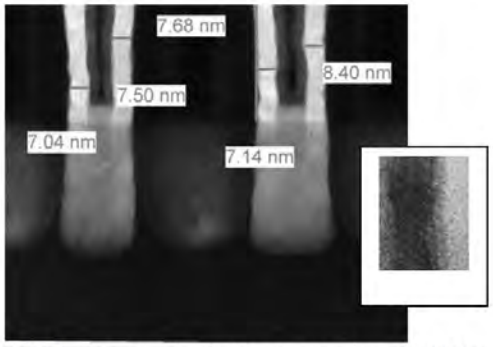


Fig. 3: TEM picture of minimum gate length RMG with 8nm FE. The inset shows the crystallinity of the FE film.

[1] Krivokapic, Z. et al., IEDM 2017

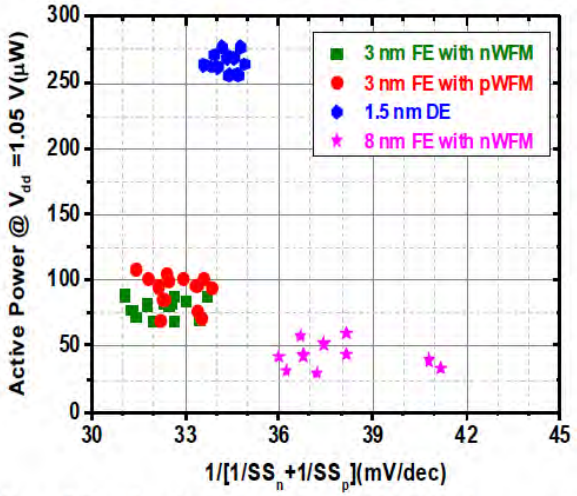


Fig. 13: Active power of FO3 inverter RO vs. effective SS for V_{dd}=1.05V.

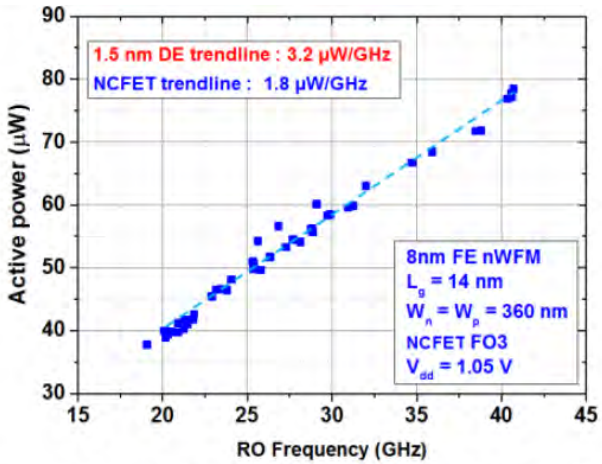
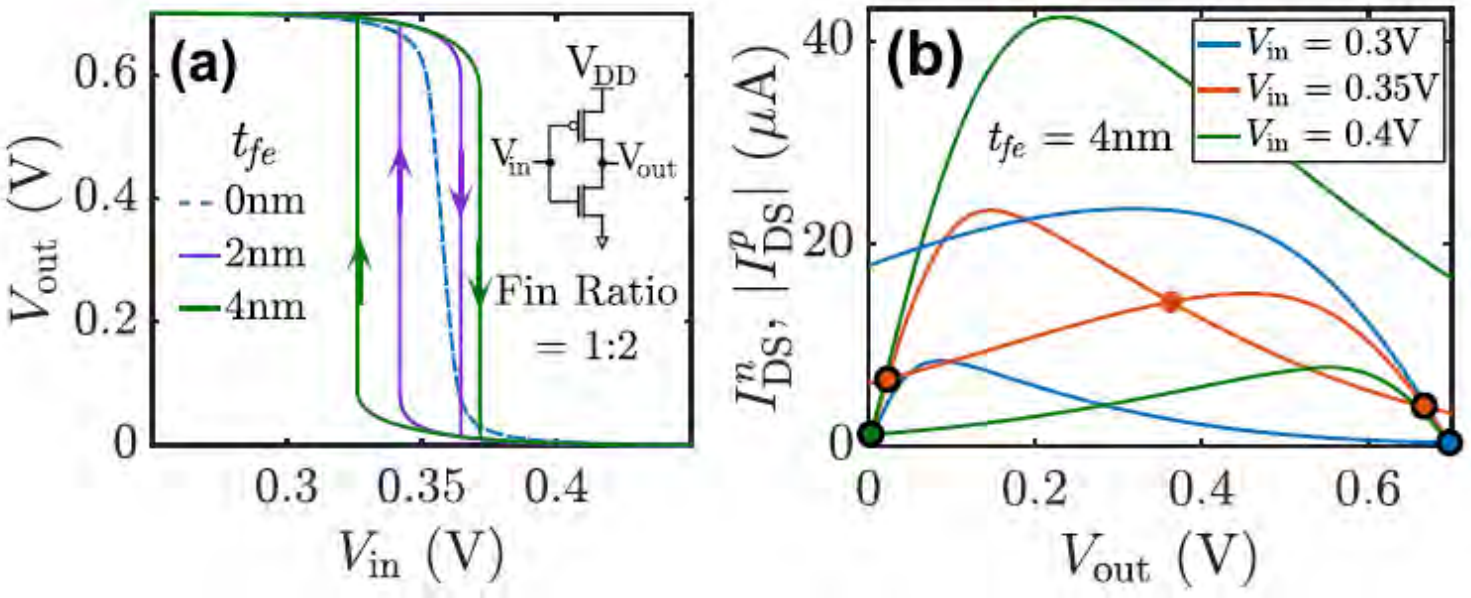


Fig. 14: Active power of NCFET FO3 inverter RO with W_n=W_p=360nm, L=14nm.

- Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power[1].
- Another theoretical study predicted intrinsic delay due to polarization damping in NCFET to be very small (270 fs)[2].

[2] Chatterjee, K., Rosner, A. J. & Salahuddin, IEEE Electron Device Letters 38, 1328–1330 (2017).

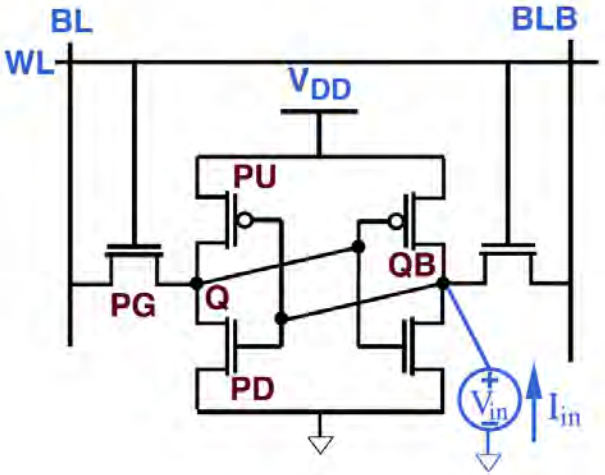
NC-FinFET based inverters

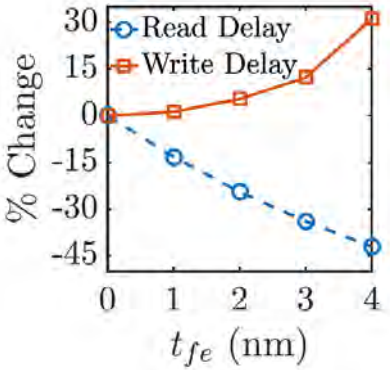


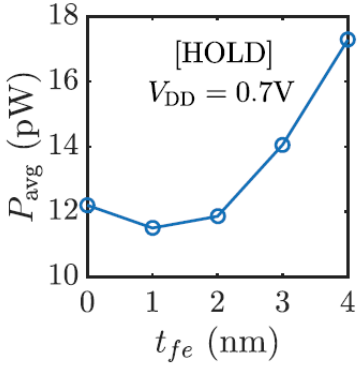
- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Vol. 38, Issue 8, pp. 1161-1164, Aug. 2017.

NC-FinFET based SRAM



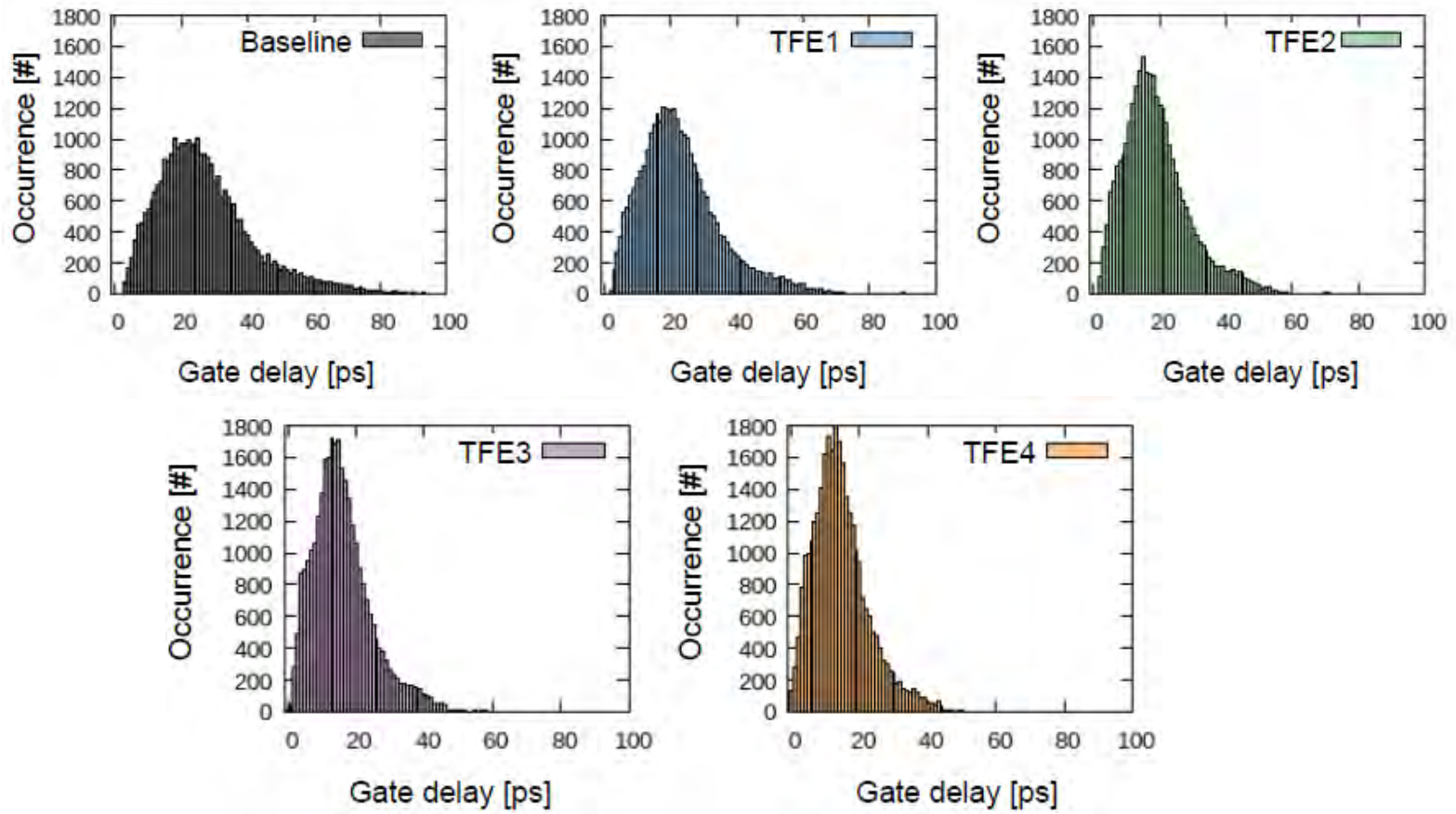




- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- P_{avg}: NC-SRAM performs better with lower standby leakage only at small t_{fe}, taking advantage of the lower subthreshold currents

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Vol. 38, Issue 8, pp. 1161-1164, Aug. 2017.

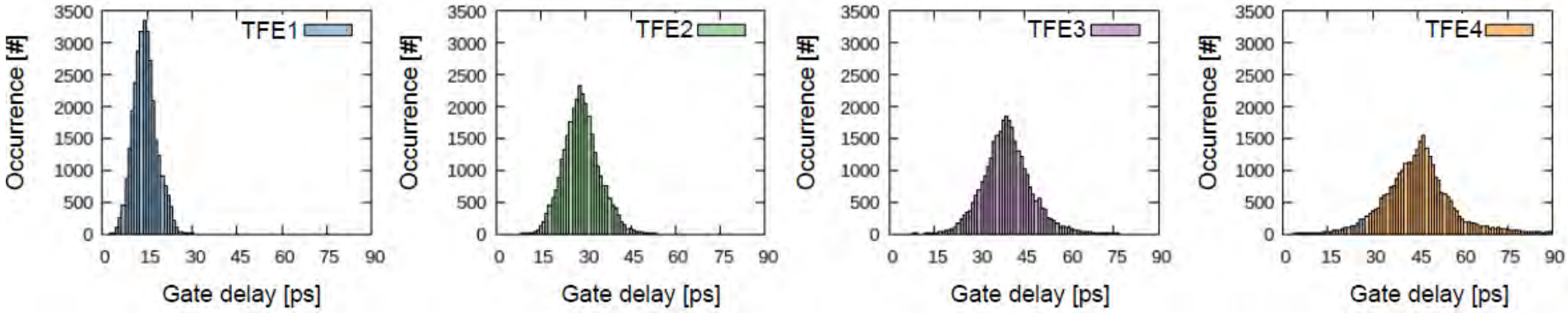
Effects of NCFET on standard cells: 7nm FinFET standard cell library



- Increasing t_{fe} – larger A_v in transistors (i.e., steeper slope and higher ON current) → Delay of cells become smaller.

H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance", IEEE Access, Vol. 6, Issue 1, pp. 52754-52765, Oct. 2018.

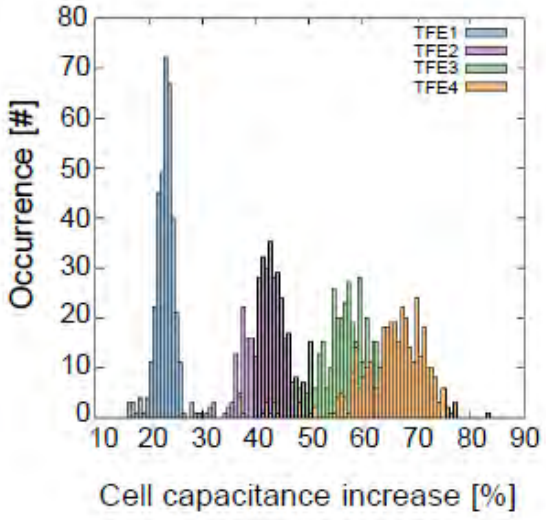
Effects of NCFET on standard cells: 7nm FinFET standard cell library

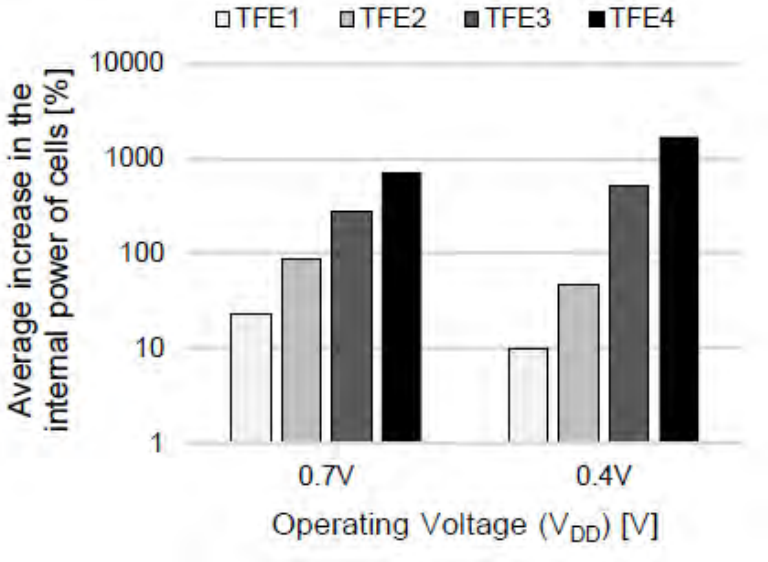


Using a ferroelectric with 1nm, 2nm, 3nm and 4nm thickness provides a speedup of around 15%, 30%, 40% and 45% respectively, in the delay of gates at the operating voltage of 0.7V.

- Quantifying the relative delay decrease/improvement of cells within the 7nm FinFET standard cell library due to NCFET **at V_{DD} = 0.7V**.

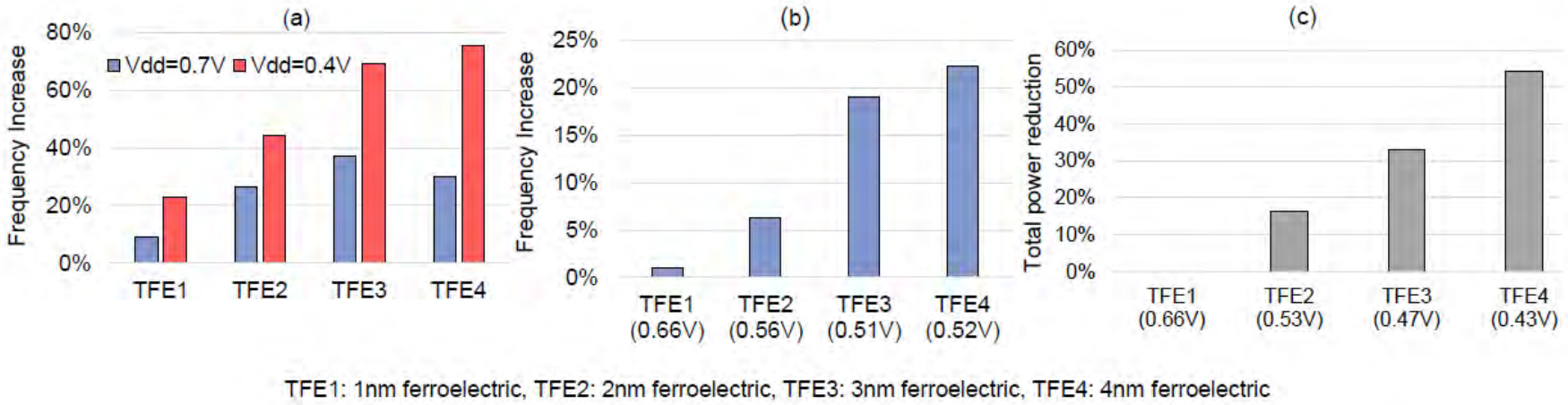
Effects of NCFET on standard cells: 7nm FinFET standard cell library





- Increase in t_{fe} leads to an increase in the total cells' capacitance which further increases internal power of the cells.
- Same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.

Effects of NCFET on future processor design



TFE1: 1nm ferroelectric, TFE2: 2nm ferroelectric, TFE3: 3nm ferroelectric, TFE4: 4nm ferroelectric

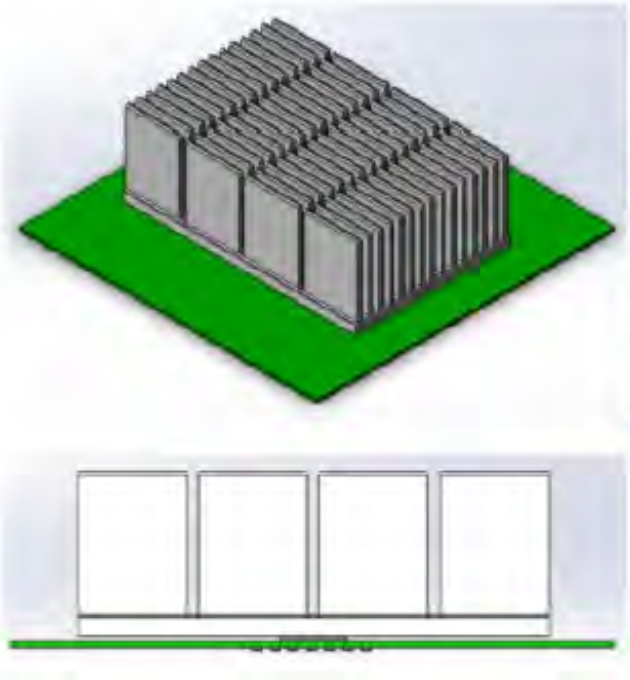
(a) What is the frequency increase due to NCFET under the same voltage constraint?

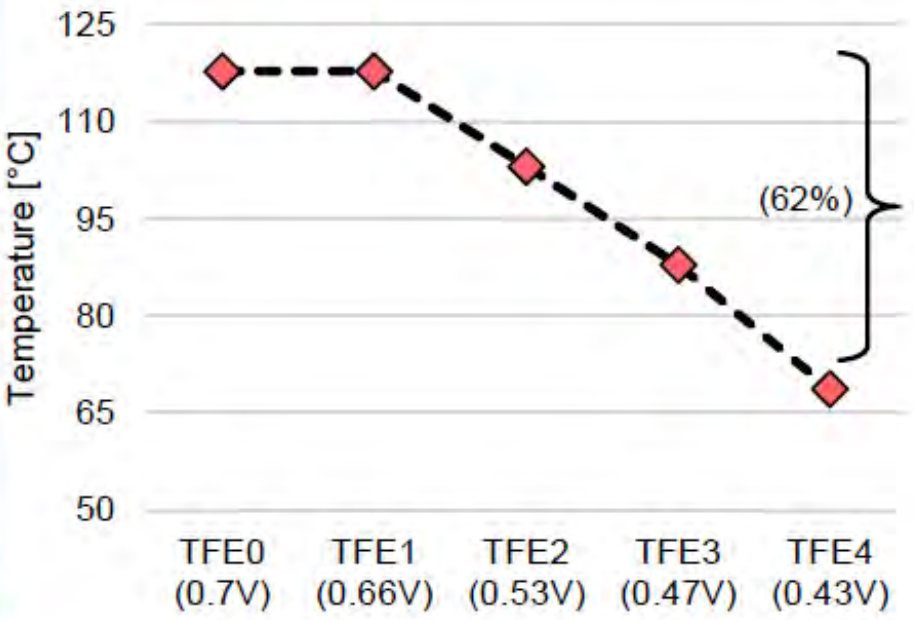
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?

(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance", IEEE Access, Vol. 6, Issue 1, pp. 52754-52765, Oct. 2018.

NC-FinFET based Processor Performance

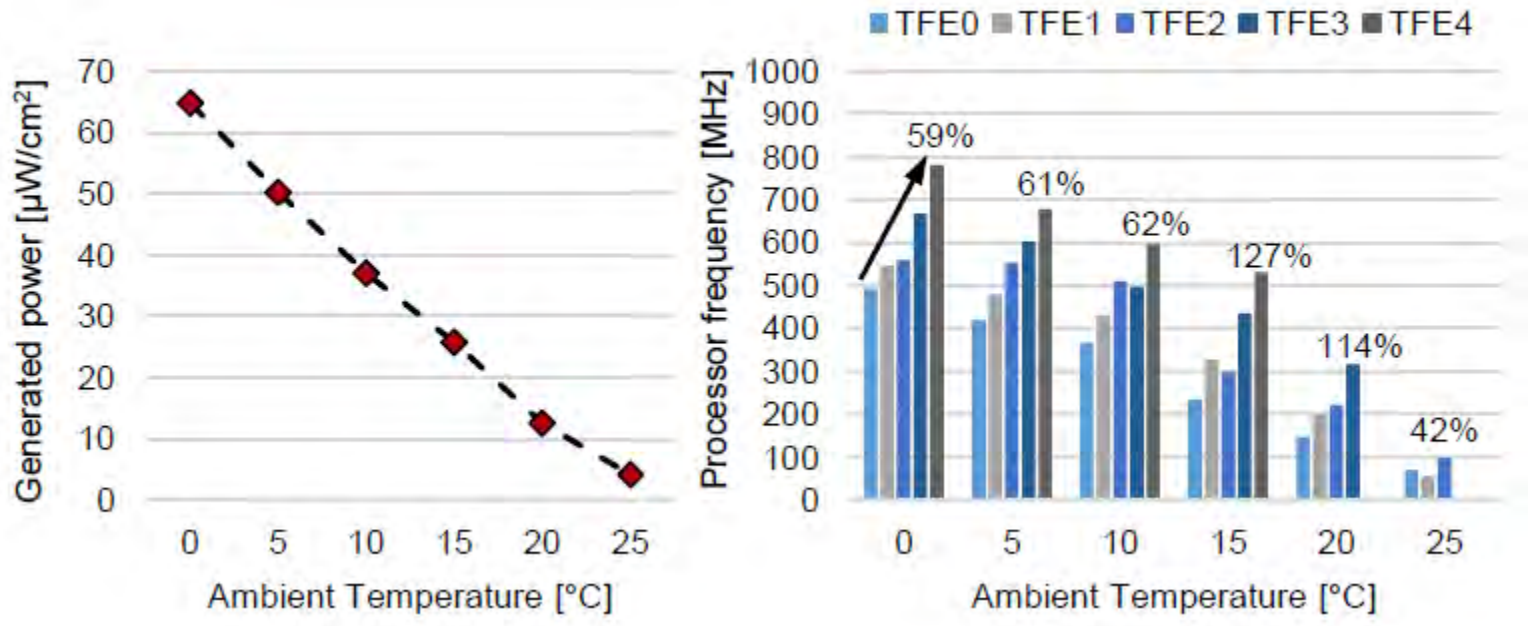




- NCFET with ferroelectric thickness more than 1nm leads to a noticeable temperature reduction, due to the decrease in the on-chip power density.

NC-FinFET based Processor Performance

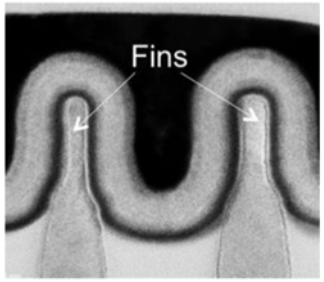
Energy harvesting and IOT

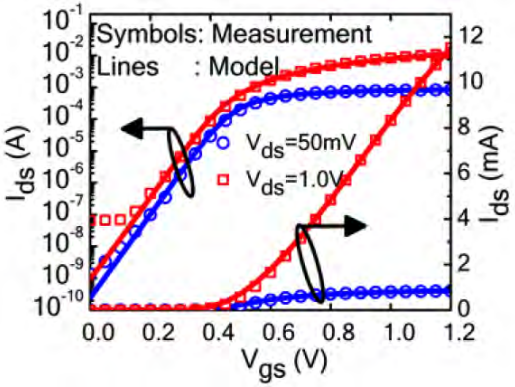


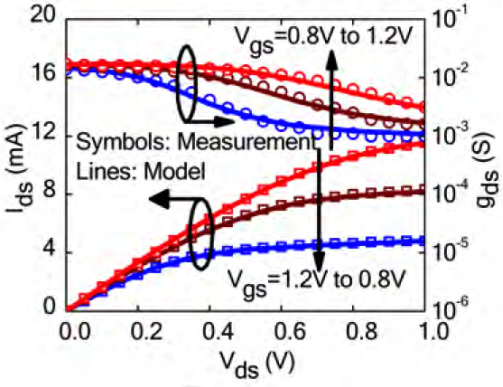
- Under very small power budgets harvested from body heat, NCFET technology enables the processor to operate at around 42-127% higher frequency compared to the conventional FinFET technology.

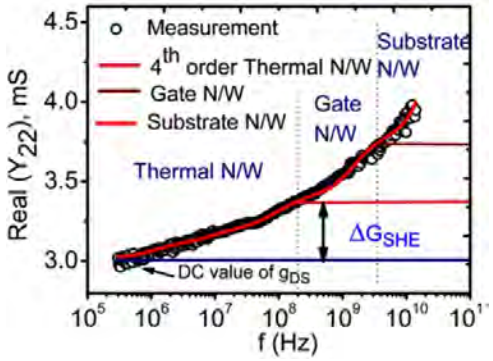
NC-FinFET RF Performance

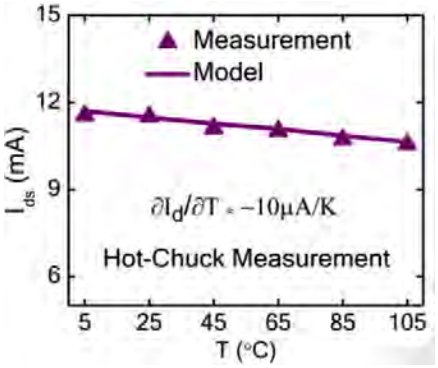
- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis

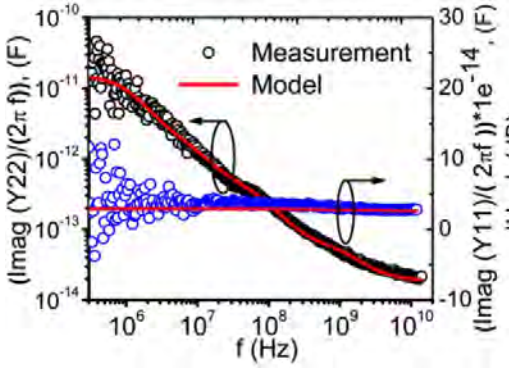


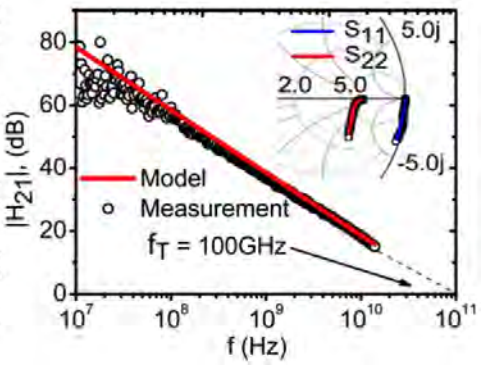






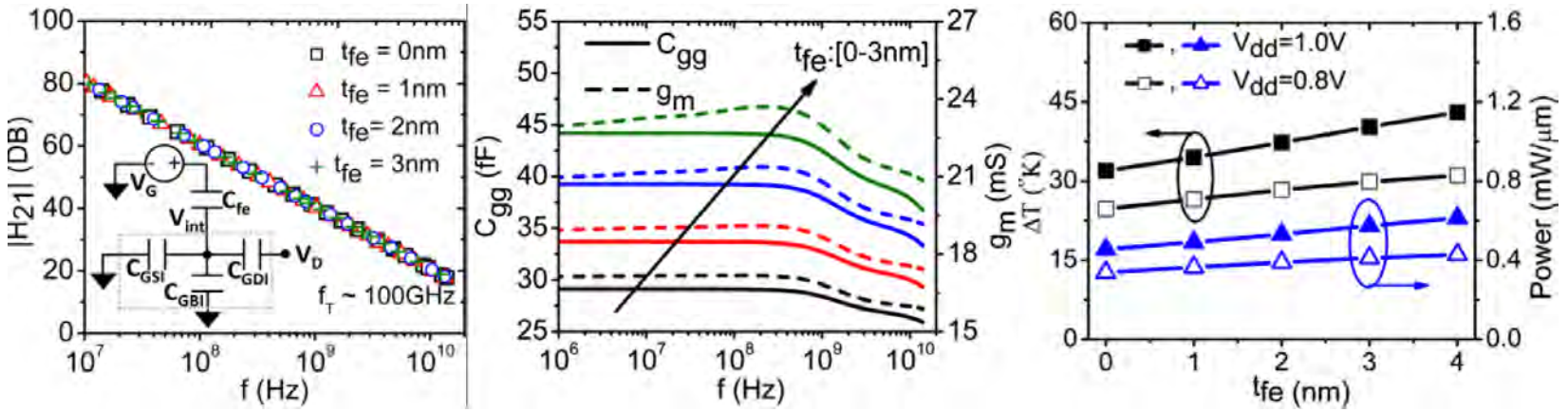






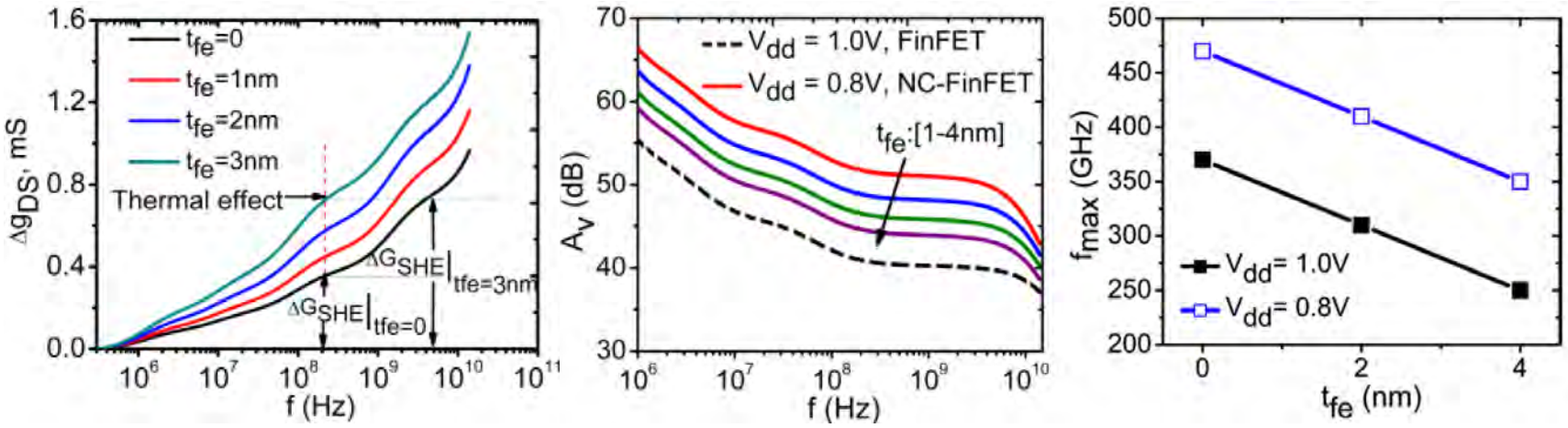
R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook, and A. Dixit, "Evaluation of 10nm Bulk FinFET RF Performance - Conventional vs. NC-FinFET", IEEE Electron Device Letters, Aug. 2018.

NC-FinFET RF Performance



- Current gain ($\propto {}^{g_m}/_{C_{gg}}$) is almost independent of t_{fe} as both the g_m and C_{gg} increase with t_{fe} almost at a constant rate.
  - Cut-off frequency (f_T) remains identical for both the Baseline and NC-FinFET.
- Temperature rise and Power consumption due to self-heating increase with t_{fe} as I_d increases. Reduce V_{dd} to achieve energy efficient performance.

NC-FinFET RF Performance

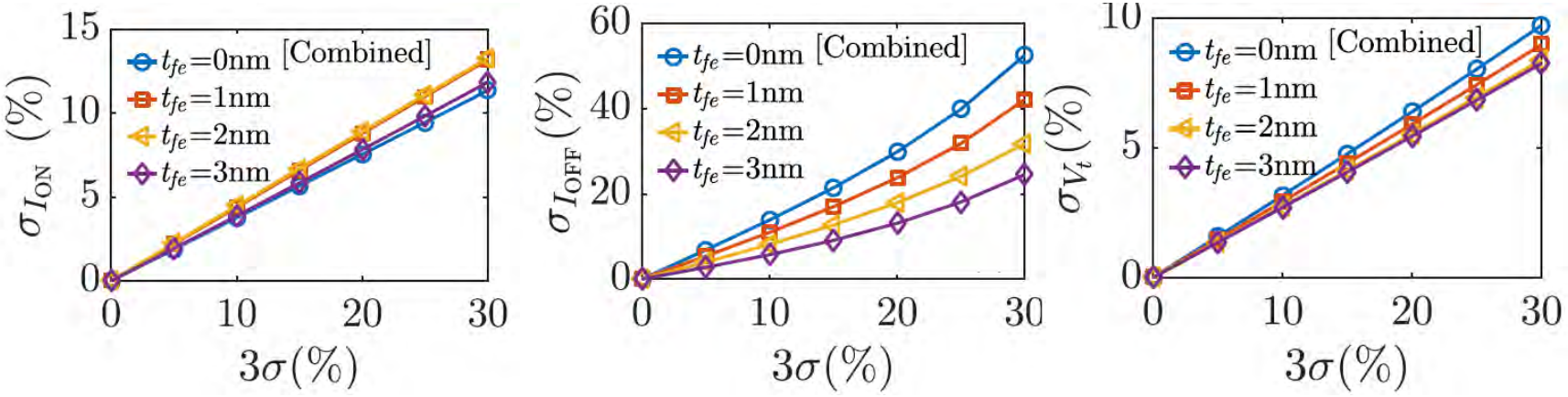


- g_{ds} and self heating ($\Delta G_{SHE} \propto g_{ds}(f) - g_{ds}(dc)$) both increase with t_{fe} due to increased capacitance matching between C_{fe} and C_{int}.

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\partial I_{ds}}{\partial V_{int}} * \frac{\partial V_{int}}{\partial V_{ds}} = g_m^{int} * A_V^D \quad \text{where} \quad A_V^D = \frac{-C_{GDI}}{|C_{fe}| - C_{int}}$$

- Voltage gain ($A_V = g_m/g_{ds} = C_{fe}/C_{GDI}$) decreases with t_{fe} due to decrease in C_{fe}.
- Maximum oscillation frequency (f_{max}) also reduces with t_{fe} which can be compensated by reducing V_{dd}.

Impact of Process Variations

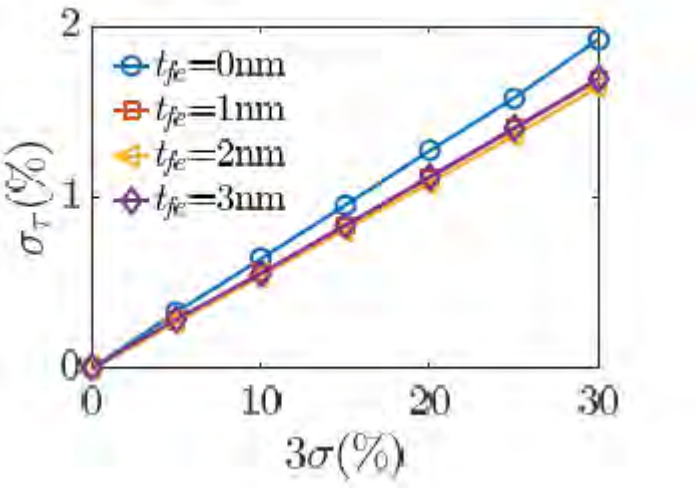


- Variability in I_{ON}, I_{OFF}, and V_t due to combined impact of variability in L_g, T_{fin}, H_{fin}, EOT, t_{fe}, E_c, and P_r
- I_{ON}: Improvement is non-monotonic with t_{fe}
- I_{OFF}: Decreases monotonically with t_{fe}
- V_t: Decreases monotonically with t_{fe}

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, Vol. 39, Issue 1, pp. 147-150, Jan. 2018.

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.



11-stage Ring-Oscillator: Variation in τ due to combined variation

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, Vol. 39, Issue 1, pp. 147-150, Jan. 2018.

Variability Analysis in a 3-D Multigranular Ferroelectric Capacitor

- A simulation-based study of the variability of P_r in a multigranular FE capacitor
- Poisson–Voronoitessellation (PVT) algorithm is used for the nucleation of grains in the FE region, which corresponds to the physical growth mechanism.
- The PVT algorithm implemented in MATLAB is coupled with TCAD simulations, to trace the FE hysteresis loop.
- The impact of both, area and thickness scaling on the variability of P_r, is considered.

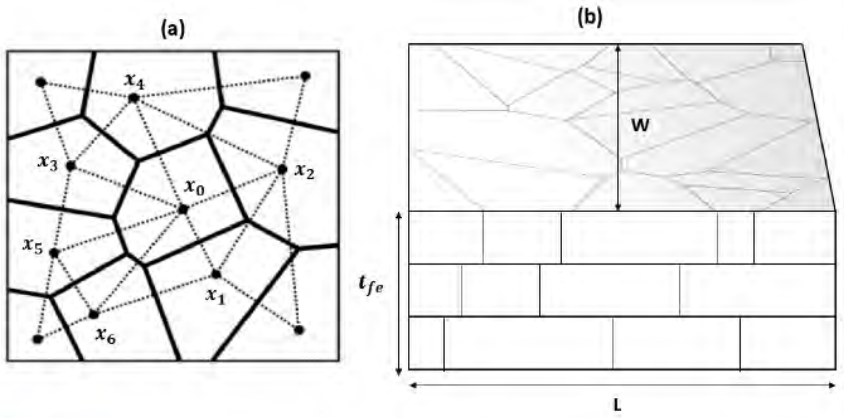


Fig. 1. (a) Grain distribution from PVT algorithm in a 2-D region where each polygon represents a grain of the FE material. (b) 3-D multigranular FE capacitor.

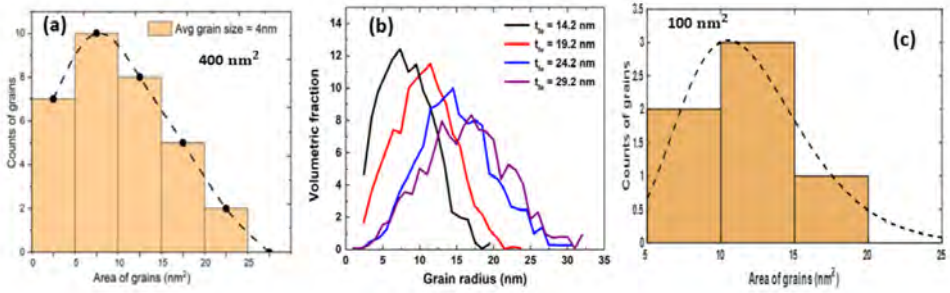


Fig. 2. (a) Distribution of grains with grain area follows the gamma distribution. The area of each grain is calculated by MATLAB and the count of the grains (n) are given as $n = 4(W \times L)/\pi(\text{grain size})^2$. (b) Demonstration of a gamma distribution in the experimentally observed FE grains [36]. (c) Grain distribution plot of a 100-nm^2 surface area FE memory.

N. Pandey, K. Qureshi and Y. S. Chauhan, "Variability Analysis in a 3-D Multi-Granular Ferroelectric Capacitor", IEEE TED, Aug. 2021.

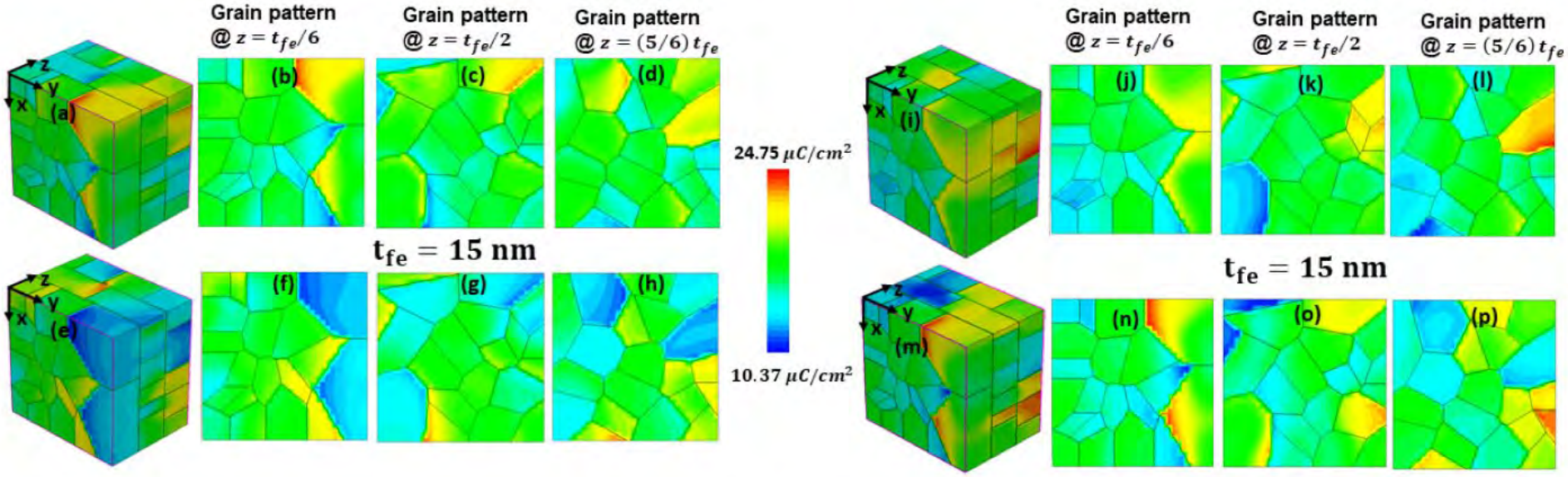


Fig. 3. (a) and (e) 3-D distribution of P_r with linearly increasing and decreasing profile with grain area respectively. (b)–(d) and (f)–(h) Surface plot of P_r with grain area in three distinct grain patterns for linearly increasing and decreasing profiles, respectively. (i) and (m) 3-D distribution of P_r with nested variability. (j)–(l) and (n)–(p) Illustration of nested variability for increasing/decreasing/increasing and increasing/decreasing/decreasing P_r profiles with grain area. The total number of simulations/models is needed: $125 \times 8 = 1000$.

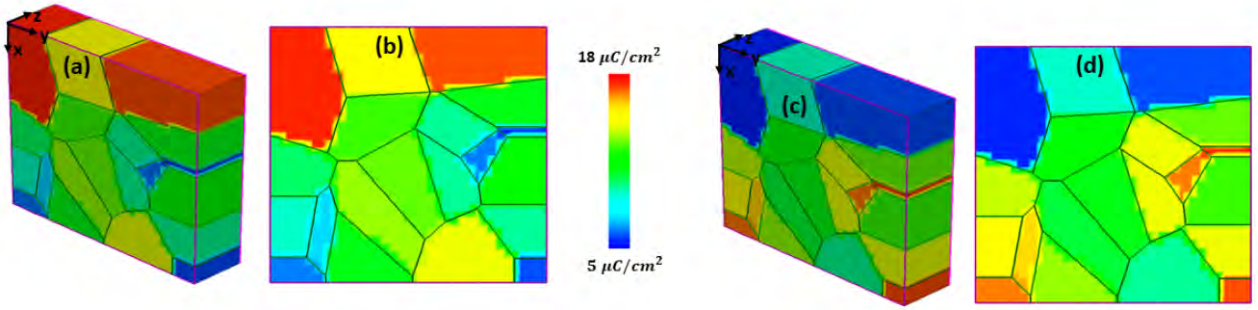


Fig. 5. (a) and (b) and (c) and (d) Distribution of P_r for linearly increasing and decreasing profiles with grain area, respectively. The net number of simulations/models needed: $125 \times 2 = 250$.

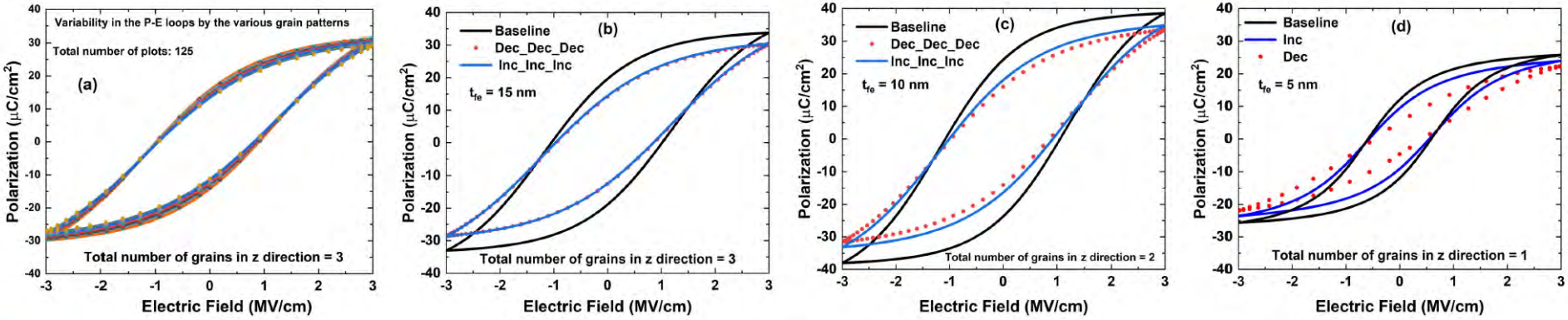


Fig. 6. Variability in the *P*–*E* hysteresis loop of a 400-nm^2 surface area FE capacitor. (a) Variability in the *P*–*E* loops with the distinct grain patterns. (b) Due to the gradual distribution of P_r in adjacent grains (see Fig. 3), the negligible difference between linearly increasing and decreasing P_r profiles is observed. (c) and (d) As FE thickness decreases, variability increases, due to the sharp variance in P_r of adjacent grains (see Fig. 5).

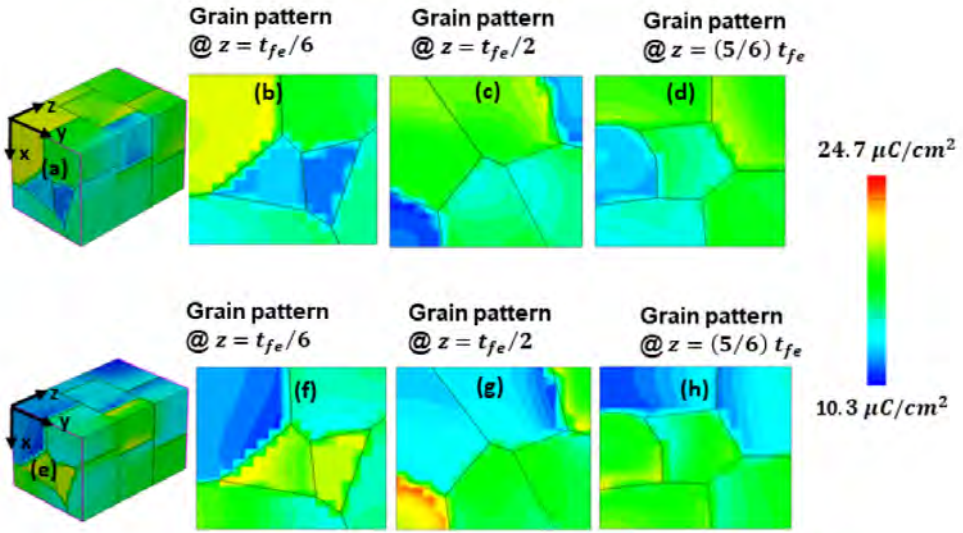


Fig. 7. Distribution of P_r in a 100-nm^2 surface area FE capacitor with $t_{fe} = 15$ nm. (a)–(d) and (e)–(h) Increasing and decreasing P_r with the grain area, respectively. The total number of simulations/models required to analyze variability: $40 \times 8 = 320$.

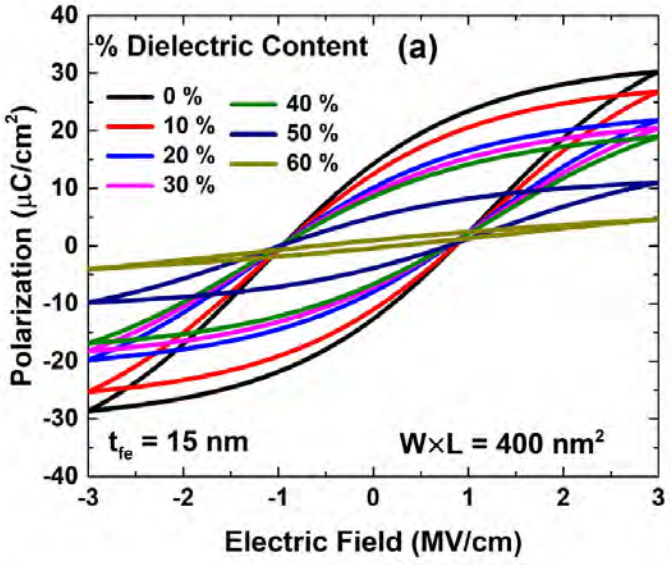


Fig. 11. (a) Impact of dielectric content on the variability of P–E hysteresis loops. As DE content increases the memory window of an FE capacitor decreases.

- Main Findings
  - Amount of variability in P_r increases as FE thickness decreases.
  - FE with the smaller surface area exhibits a higher variability in P_r compared to a larger surface area FE capacitor.
  - The dielectric grains cause a very large amount of variability in the FE hysteresis loop.
  - An increase in the dielectric grains also leads to a loss in the retentivity of the hysteresis loop.

Multi-domain switching dynamics in NCFET using SPICE model

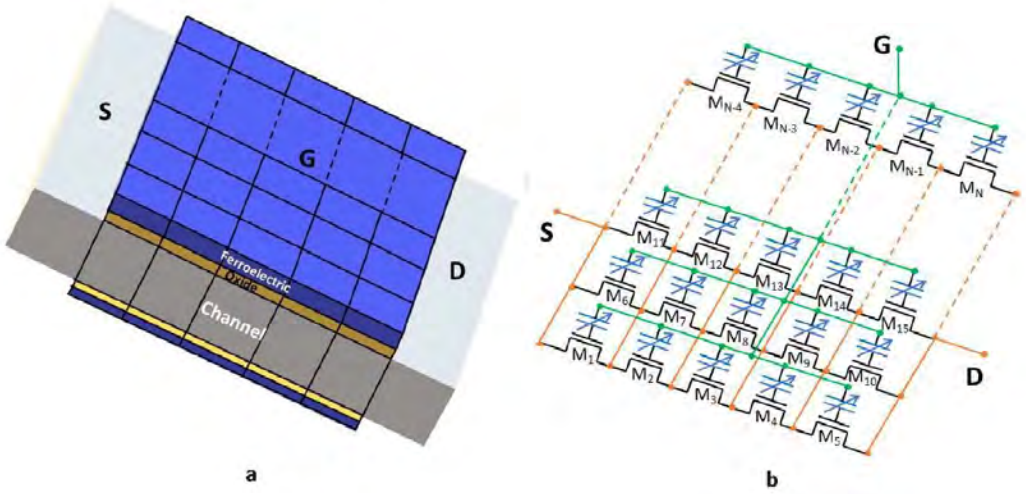


Fig. 1. (a) A schematic representation of Multi-domain Double Gate negative capacitance Field Effect Transistor. Each rectangular boxes in the ferroelectric material represents the individual domains. (b) An equivalent circuit representation for multi-domain NC-FinFET. Each individual domain present in the ferroelectric material is represented as a capacitor and the each divided region in the channel is represented as a separate transistor. *N* is the total number of domains present in the ferroelectric material.

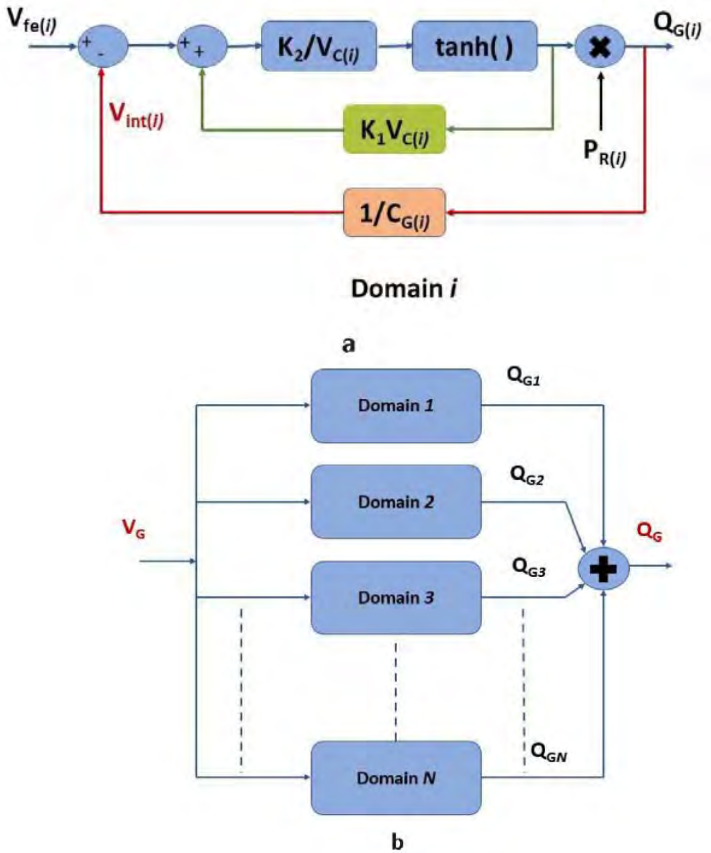
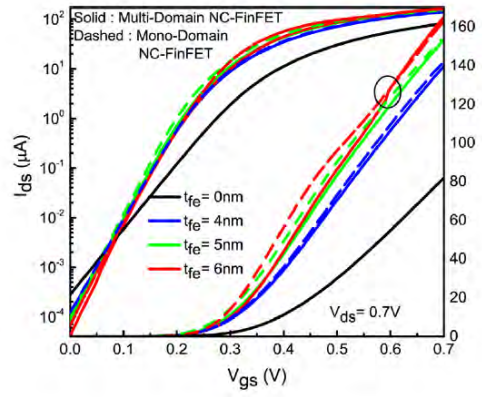


Fig. 2. (a) SPICE circuit model for single domain of NC-FinFET. (b) SPICE circuit model for multi-domain NC-FinFET.

A. D. Gaidhane, A. Verma and Y. S. Chauhan, "Study of Multi-Domain Switching Dynamics in Negative Capacitance FET using SPICE Model", Microelectronics Journal, 2021.



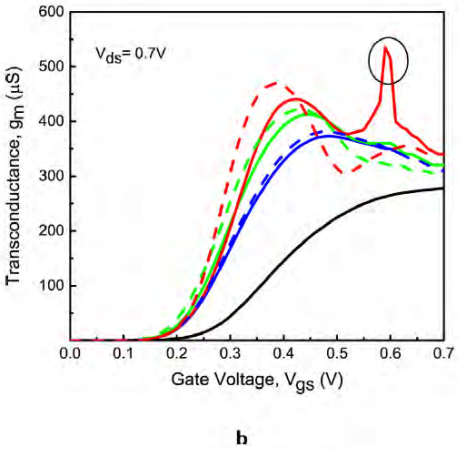
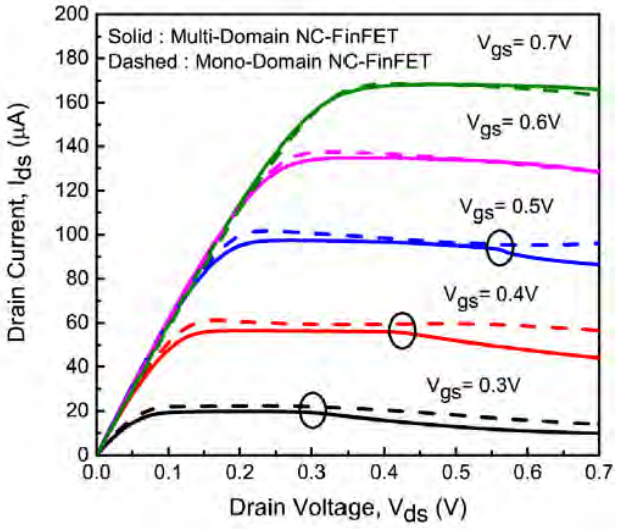


Fig. 5. (a) $I_{ds} - V_{gs}$ characteristics for different ferroelectric thickness of multi-domain NC-FinFET at V_{ds} = 0.7 V. The Multi-domain characteristic is compared with the baseline FinFET and mono-domain NC-FinFET. (b) Trans-conductance versus applied gate bias for different ferroelectric thicknesses at V_{ds} = 0.7 V.



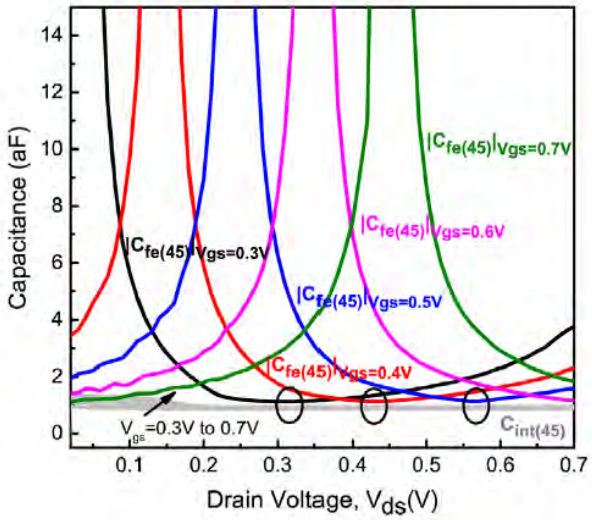


Fig. 7. (a) Comparison of $I_{ds} - V_{ds}$ characteristics of multi-domain NC-FinFET with mono-domain FinFET for different V_{gs}. The NDR effect is more pronounced in multi-domain FinFET compared to the mono-domain case. (b) Capacitance matching between the internal gate to drain capacitance $C_{int(45)}$ and $|C_{fe(45)}|$ with applied drain bias. The best capacitance matching results in kink in the drain current.

- Unlike the mono-domain case, switching of the individual domains in multi-domain scenario happens at different interval of gate bias since the switching depends on their individual domain parameters ($E_C(i)$ and $P_R(i)$).
- Amplification effect due to NC effect is lower in case of multi-domain compared to the mono-domain NC-FinFET.
- Lower drain current for the multi-domain NC-FinFET compared to mono-domain NC-FinFET.
- The kink in the drain current for t_{fe} = 6 nm → One of the domains does not satisfy the stability criteria i.e. $|C_{fe}(i)| > C\text{int}(i)$.

NC-DEMOS FET for High-Voltage Switching and Analog Applications

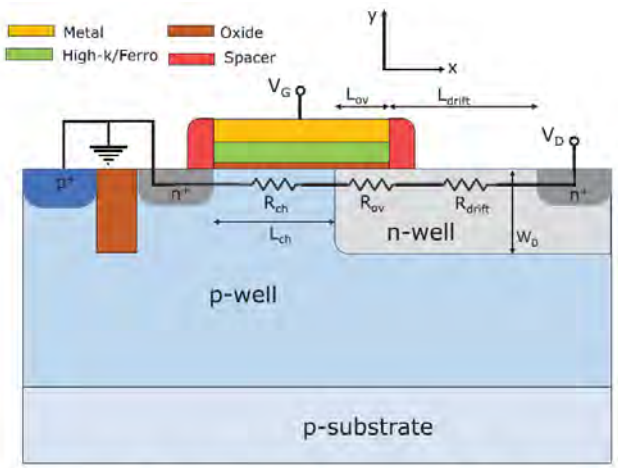


Fig. 1. Schematic of high-*k*/ferroelectric-based DEMOS.

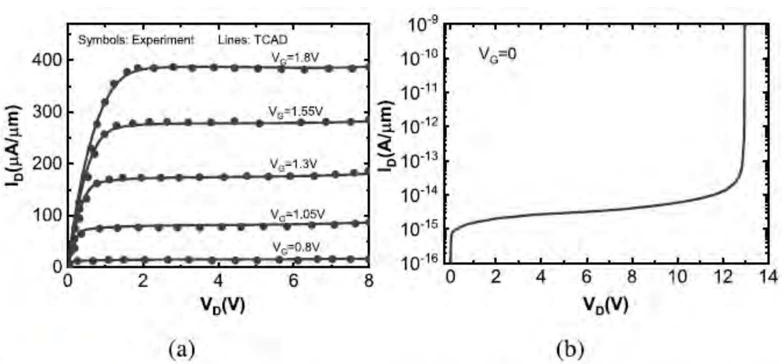
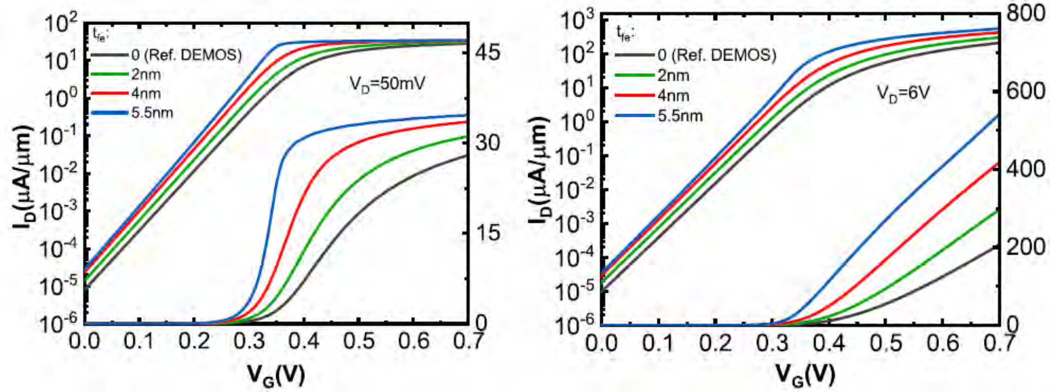
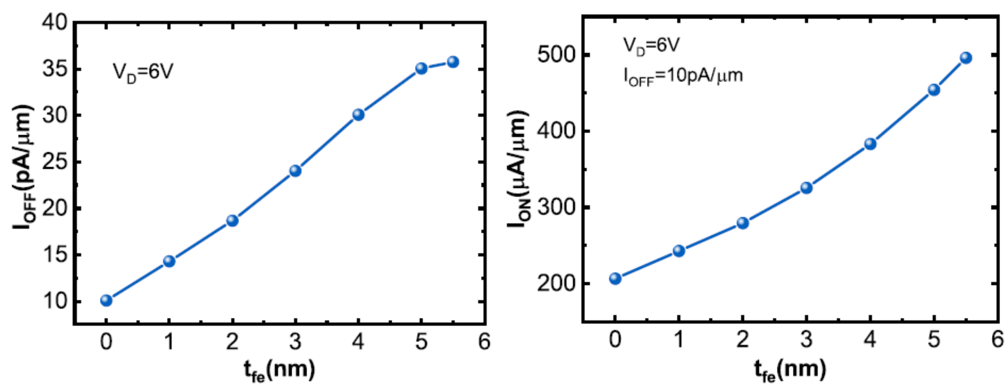


Fig. 2. (a) TCAD DEMOS calibration with experimental I_D–V_D data [2]. (b) Breakdown characteristics of the calibrated TCAD device with $I_{OFF} \approx 30$ fA/μm and $V_{Br} \approx 13$ V [2].





G. Pahwa, A. Gaidhane, A. Agarwal, and Y. S. Chauhan, "Assessing Negative-Capacitance Drain-Extended Technology for High-Voltage Switching and Analog Applications", IEEE Transactions on Electron Devices, Vol. 68, Issue 2, Feb. 2021.

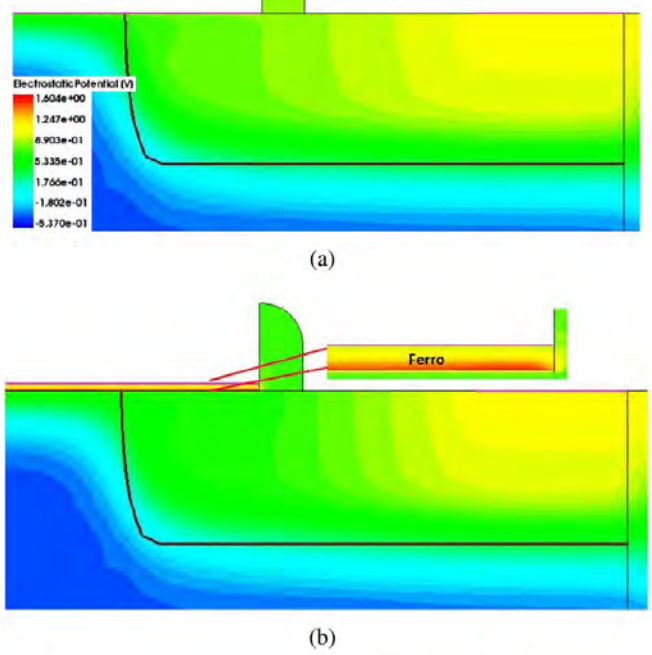


Fig. 6. Potential distribution in (a) DEMOS and (b) NC-DEMOS with $t_{fe} = 5.5$ nm at $V_G = 0.7$ V and $V_D = 0.6$ V. It can be seen that the gate voltage amplification caused by NC of ferroelectric lowers the potential near the gate edge in the overlap region and pushes its distribution toward the drain side.

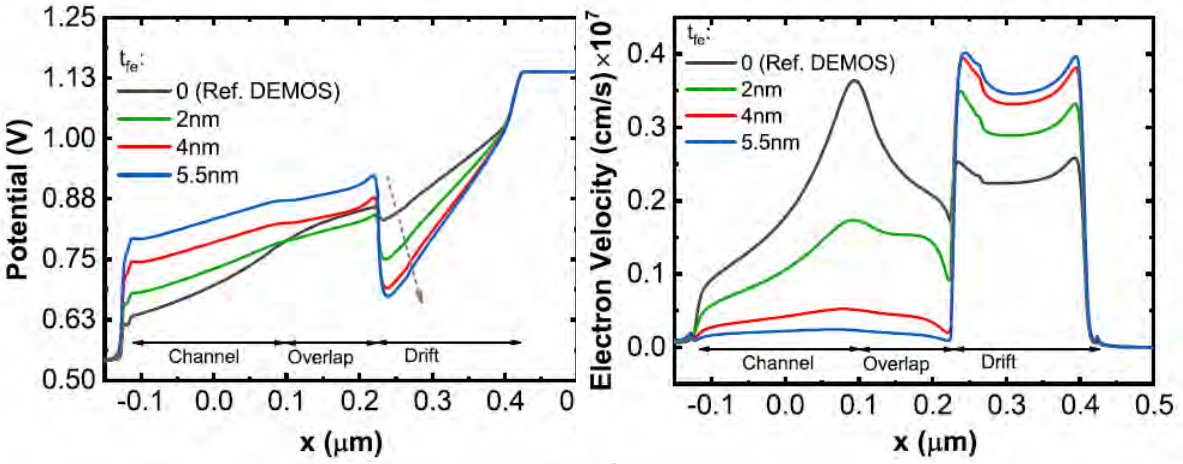


Fig. 7. (a) Potential and (b) electron velocity profiles along the silicon surface for reference DEMOS and NC-DEMOS at $V_G = 0.7$ V and $V_D = 0.6$ V. Increase in t_{fe} lowers the potential drop and electron velocity in the channel and, in turn, increases the potential drop across the drift regions causing velocity saturation of carriers there.

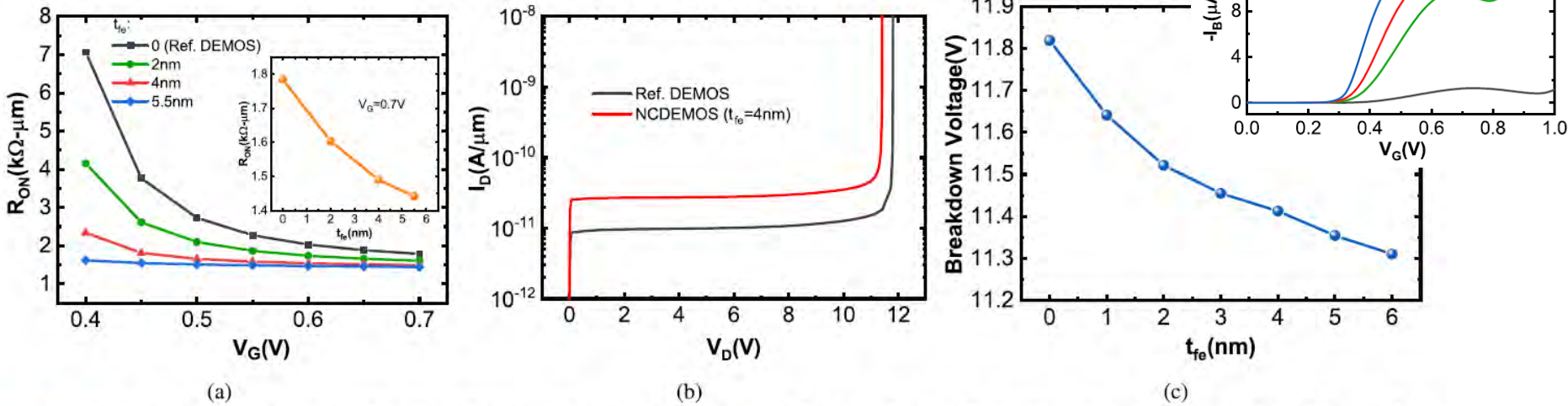


Fig. 11. (a) ON-resistance (R_{ON}) as a function of V_G for reference DEMOS and NC-DEMOS with different t_{fe} values. Inset: variation of R_{ON} with t_{fe} at $V_G = 0.7$ V. (b) Breakdown characteristics of DEMOS and NC-DEMOS. (c) Variation of the breakdown voltage of NC-DEMOS with t_{fe}.

Modeling of NC-FDSOI FET

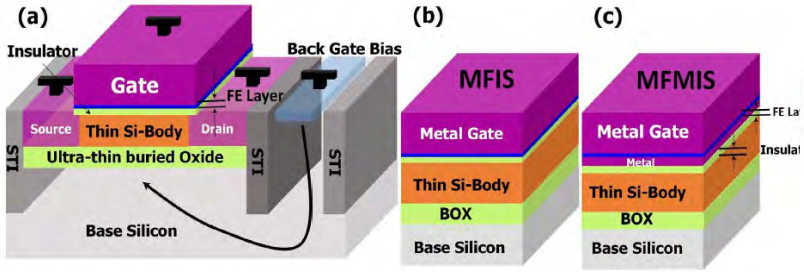


Fig. 1. (a) Schematic of NC MFIS FDSOI FET—FE layer is sandwiche between the oxide layer and the top gate. (b) Gate-stack of MFIS FDS FET. (c) Gate-stack of MFMIS FDSOI FET.

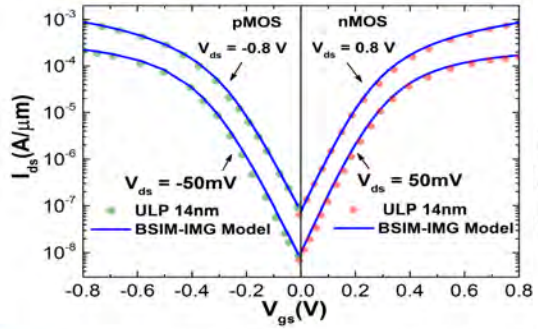
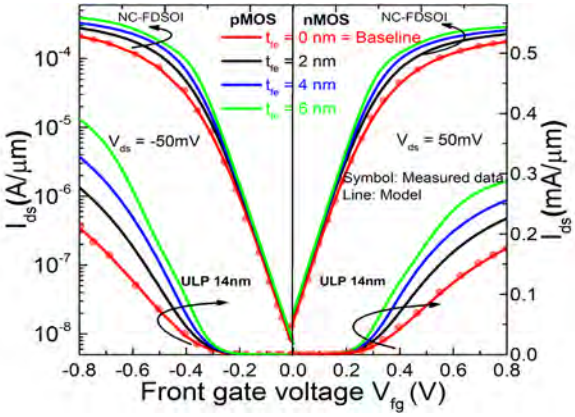
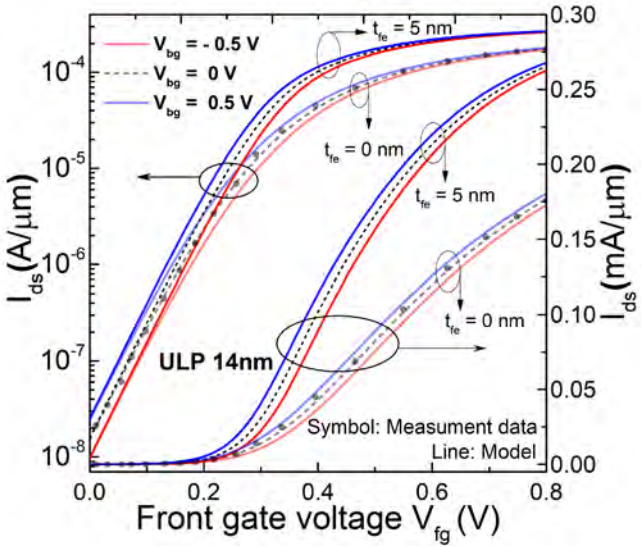
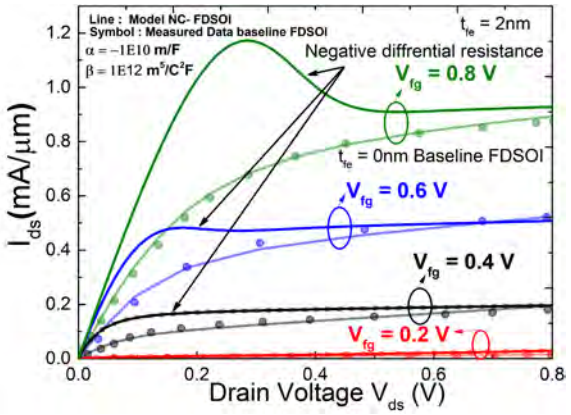
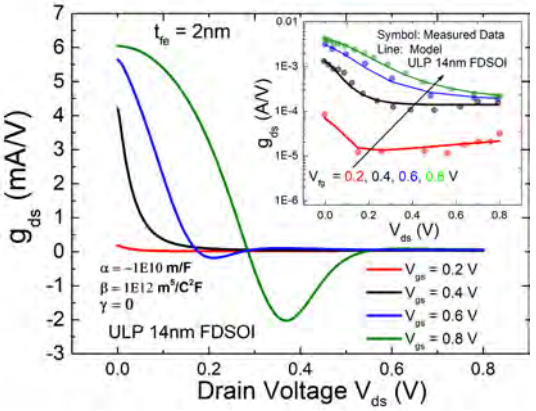


Fig. 2. 14-nm ULP FDSOI technology [23]. Measured data are fit agains the BSIM-IMG model as baseline FET (which is the same as developec model for t_{fe} = 0 nm).



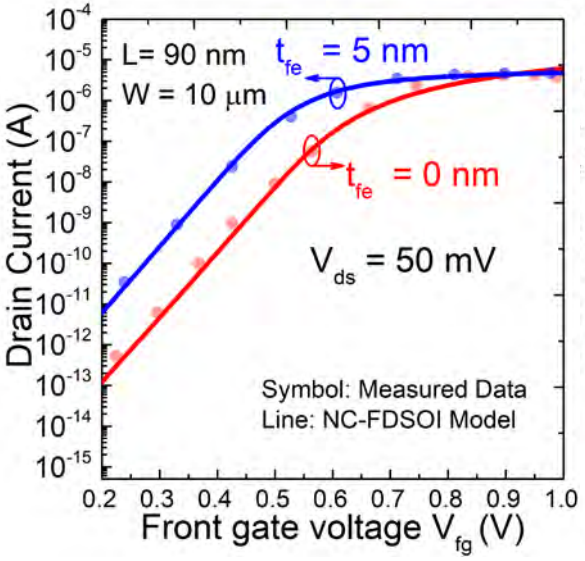


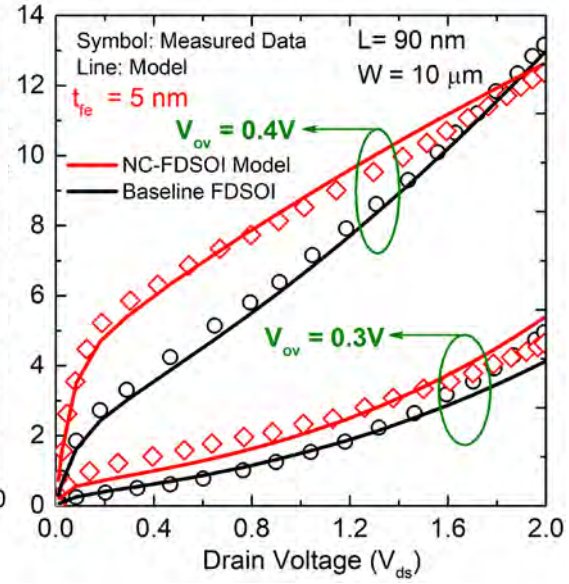


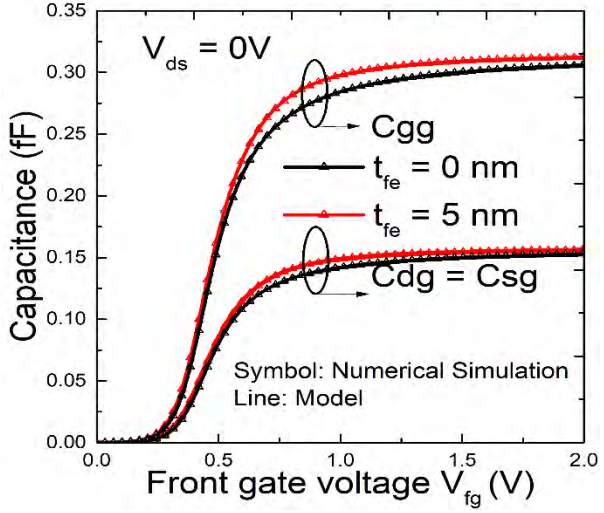


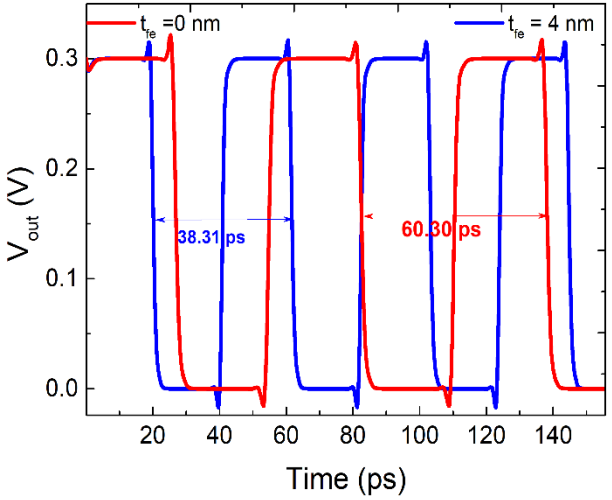
C. K. Dabhi, S. S. Parihar, A. Dasgupta, and Y. S. Chauhan, "Compact Modeling of Negative-Capacitance FDSOI FETs for Circuit Simulations", IEEE Transactions on Electron Devices, Vol. 67, Issue 7, July 2020.

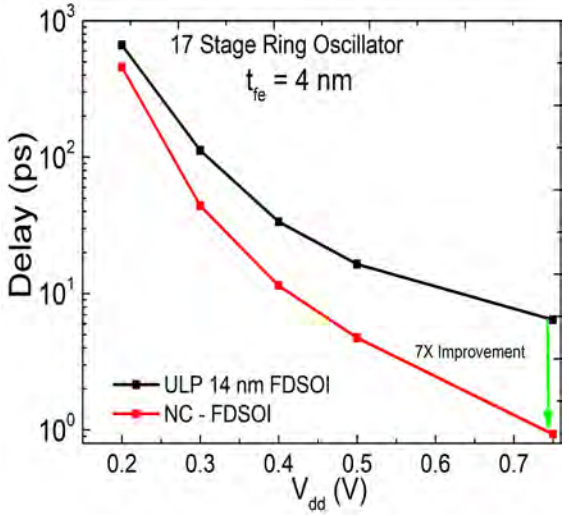
Expt. Validation and Circuit Performance











Open Questions

- Is NC a static or transient phenomenon?
- Physical explanation of NC effect
- Second order effects
  - Impact of grain boundaries and their sizes
  - Impact of multi-domain effects
  - Impact of traps
  - Impact of FE thickness
  - Reliability
- Impact of NDR/NDIBL on circuits

Conclusion

- Maintaining I_{ON}/I_{OFF} is the biggest challenge in new technology nodes
- Negative capacitance FET is one of the best choice
  - Need to find sweet material ($HfZrO_2$?)
  - Integration in conventional CMOS process remains a challenge (lot of progress)
- Compact (SPICE) Models are ready for circuit evaluation

Relevant Publications from our group

- A. D. Gaidhane, A. Verma and Y. S. Chauhan, "Study of Multi-Domain Switching Dynamics in Negative Capacitance FET using SPICE Model", Microelectronics Journal, 2021.
- O. Prakash, A. Gupta, G. Pahwa, Y. S. Chauhan, and H. Amrouch, "On the Critical Role of Ferroelectric Thickness for Negative Capacitance Device-Circuit Interaction", IEEE Journal of the Electron Devices Society, 2021.
- S. Salamin, G. Zervakis, Y. S. Chauhan, J. Henkel, and H. Amrouch, "PROTON: Post-synthesis ferROelectric Thickness OptimizatioN for NCFET Circuits", IEEE Transactions on Circuits and Systems I, 2021.
- D. Rajasekharan, A. Gaidhane, A. R. Trivedi, and Y. S. Chauhan, "Ferroelectric FET-based Implementation of FitzHugh-Nagumo Neuron Model", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.
- N. Pandey, K. Qureshi and Y. S. Chauhan, "Variability Analysis in a 3-D Multi-Granular Ferroelectric Capacitor", IEEE Transactions on Electron Devices, Vol. 68, Issue 8, Aug. 2021.
- S. Salamin, G. Zervakis, F. Klemme, H. Kattan, Y. S. Chauhan, J. Henkel, and H. Amrouch, "Impact of NCFET Technology on Eliminating the Cooling Cost and Boosting the Efficiency of Google TPU", IEEE Transactions on Computers, 2021.
- O. Prakash, G. Pahwa, C. K. Dabhi, Y. S. Chauhan, and H. Amrouch, "Impact of Self-Heating on Negative-Capacitance FinFET: Device-Circuit Interaction", IEEE Transactions on Electron Devices, Vol. 68, Issue 4, April 2021.
- G. Paim, G. Zervakis, G. Pahwa, Y. S. Chauhan, E. A. C. Costa, S. Bampi, J. Henkel, and H. Amrouch, "On the Resiliency of NCFET Circuits against Voltage Over-Scaling", IEEE Transactions on Circuits and Systems I, Vol. 68, Issue 4, April 2021.
- G. Zervakis, I. Anagnostopoulos, S. Salamain, Y. S. Chauhan, J. Henkel, and H. Amrouch, "Impact of NCFET on Neural Network Accelerators", IEEE Access, Vol. 9, pp. 43748 - 43758, 2021.
- G. Pahwa, A. Gaidhane, A. Agarwal, and Y. S. Chauhan, "Assessing Negative Capacitance Drain Extended Technology for High Voltage Switching and Analog Applications", IEEE Transactions on Electron Devices, 2021.
- O. Prakash, C. Dabhi, Y. Chauhan, and H. Amrouch, "Transistor Self-Heating: The Rising Challenge for Semiconductor Testing", IEEE VLSI Test Symposium (VTS’21), April 2021.
- V. M. V. Santen, S. Thomann, Y. Chauhan, J. Henkel, and H. Amrouch, "Reliability-Driven Voltage Optimization for NCFET-based SRAM Memory Banks", IEEE VLSI Test Symposium (VTS’21), April 2021.

Relevant Publications from our group

- O. Prakash, A. Gupta, G. Pahwa, Y. S. Chauhan, and H. Amrouch, "On the Critical Role of Ferroelectric Thickness for Negative Capacitance Transistor Optimization", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Chengdu, China, Mar. 2021.
- J. Knechtel, S. Patnaik, M. Nabeel, M. Ashraf, Y. S. Chauhan, J. Henkel, O. Sinanoglu, and H. Amrouch, "Power Side-Channel Attacks in Negative Capacitance Transistor (NCFET)", IEEE Micro, Vol. 40, Issue 6, Nov.-Dec. 2020.
- O. Prakash, G. Pahwa, Y. S. Chauhan and H. Amrouch, "Impact of Interface Traps on Negative Capacitance Transistor: Device and Circuit Reliability", IEEE Journal of Electron Devices Society, Vol. 8, Nov. 2020.
- K. Nandan, C. Yadav, P. Rastogi, A. T.-Lopez, A. M.-Sanchez, E. G. Marin, F. G. Ruiz, S. Bhowmick, and Y. S. Chauhan, "Compact Modeling of Multi-layered MoS2 FETs including Negative Capacitance Effect", IEEE Journal of Electron Devices Society, Vol. 8, Nov. 2020.
- A. D. Gaidhane, G. Pahwa, A. Dasgupta, A. Verma, and Y. S. Chauhan, "Compact Modeling of Surface Potential, Drain Current and Terminal Charges in Negative Capacitance Nanosheet FET including Quasi-Ballistic Transport", IEEE Journal of Electron Devices Society, Vol. 8, Nov. 2020.
- N. Pandey and Y. S. Chauhan, "Analytical Modeling of Short Channel Effects in MFIS Negative Capacitance FET including Quantum Confinement Effects", IEEE Transactions on Electron Devices, Vol. 67, Issue 11, Nov. 2020.
- D. Rajasekharan, P. Kushwaha, and Y. S. Chauhan, "Associative Processing using Negative Capacitance FDSOI Transistor for Pattern Recognition", Microelectronics Journal, Vol. 104, art. no. 104877, Oct. 2020.
- H. Amrouch, G. Pahwa, A. D. Gaidhane, C. K. Dabhi, F. Klemme, O. Prakash and Y. S. Chauhan, "Impact of Variability on Processor Performance in Negative Capacitance FinFET Technology", IEEE Transactions on Circuits and Systems I, Vol. 67, Issue 9, Sep. 2020.
- C. K. Dabhi, S. S. Parihar, A. Dasgupta, and Y. S. Chauhan, "Compact Modeling of Negative-Capacitance FDSOI FETs for Circuit Simulations", IEEE Transactions on Electron Devices, Vol. 67, Issue 7, July 2020.
- F. Bellando, C. K. Dabhi, A. Saeidi, C. Gastaldi, Y. S. Chauhan, and A. M. Ionescu, "Subthermionic Negative Capacitance Ion Sensitive Field-Effect Transistor", Applied Physics Letters, Vol. 116, Issue 17, April 2020.
- A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Gate Induced Drain Leakage in Negative Capacitance FinFETs", IEEE Transactions on Electron Devices, Vol. 67, Issue 3, March 2020.
- F. Klemme, Y. Chauhan, J. Henkel, and H. Amrouch, "Cell Library Characterization using Machine Learning for Design Technology Co-Optimization", IEEE International Conference on Computer-Aided Design (ICCAD), Paris, France, Nov. 2020.
- G. Bajpai, A. Gupta, O. Prakash, G. Pahwa, J. Henkel, Y. S. Chauhan, and H. Amrouch, "Impact of Radiation on Negative Capacitance FinFET", IEEE International Reliability Physics Symposium (IRPS), Grapevine-Texas, USA, Mar.-Apr. 2020.

Relevant Publications from our group

- A. D. Gaidhane, G. Pahwa, A. Dasgupta, A. Verma, and Y. S. Chauhan, "Compact Modeling of Negative Capacitance Nanosheet FET including Quasi-Ballistic Transport", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Penang, Malaysia, Mar. 2020.
- O. Prakash, A. Gupta, G. Pahwa, J. Henkel, Y. S. Chauhan and H. Amrouch, "Impact of Interface Traps Induced Degradation on Negative Capacitance FinFET", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Penang, Malaysia, Mar. 2020.
- H. Amrouch, V. M. Van Santen, G. Pahwa, Y. S. Chauhan, J. Henkel, "NCFET to Rescue Technology Scaling: Opportunities and Challenges", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), Beijing, China, Jan. 2020.
- H. Amrouch, S. Salamin, G. Pahwa, A. D. Gaidhane, J. Henkel, and Y. S. Chauhan, "Unveiling the Impact of IR-drop on Performance Gain in NCFET-based Processors", IEEE Transactions on Electron Devices, Vol. 66, Issue 7, pp. 3215-3223, July 2019.
- G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Numerical Investigation of Short Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above-Threshold Behavior", IEEE Transactions on Electron Devices, Vol. 66, Issue 3, pp. 1591–1598, Mar. 2019.
- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Evaluating Negative Capacitance Technology for RF MOS Varactors", IEEE SOI–3D–Subthreshold Microelectronics Technology Unified Conference (S3S), San Francisco, USA, Oct. 2019.
- K. Sharma, A. D. Gaidhane and Y. S. Chauhan, "Performance Enhancement of 4T-IFGC DRAM in 7nm NC-FinFET Technology Node", IEEE SOI–3D–Subthreshold Microelectronics Technology Unified Conference (S3S), San Francisco, USA, Oct. 2019.
- H. Amrouch, G. Pahwa, J. Henkel and Y. S. Chauhan, "NCFET-Aware Voltage Scaling", IEEE International Symposium on Low Power Electronics and Design (ISLPED), Lausanne, Switzerland, July 2019.
- M. Rapp, H. Amrouch, S. Salamin, G. Pahwa, J. Henkel and Y. S. Chauhan, "Performance, Power and Cooling Trade-Offs with NCFET-based Many-Cores", IEEE Design Automation Conference (DAC), Las Vegas, USA, June 2019.
- A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Modeling of Inner Fringing Charges and Short Channel Effects in Negative Capacitance MFIS Transistor", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Singapore, Mar. 2019.
- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Above Threshold Behavior," in IEEE Transactions on Electron Devices, 2019.
- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Modeling of Inner Fringing Charges and Short Channel Effects in Negative Capacitance MFIS Transistor", accepted in Electron Devices Technology and Manufacturing (EDTM), 2019.
- G. Pahwa, A. Agarwal and Y. S. Chauhan, "Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior," in IEEE Transactions on Electron Devices, Nov. 2018.
- Karishma Qureshi, G. Pahwa and Y.S. Chauhan, "Impact of Linear Intergranular Variation in Remnant Polarization on Negative Capacitance Field Effect Transistor", ICEE, 2018.

Relevant Publications from Our group

- A.D. Gaidhane, G. Pahwa and Y.S. Chauhan, "Compact Modeling of Drain Current in Double Gate Negative Capacitance MFIS Transistor", ICEE, 2018.
- H. Amrouch, G. Pahwa, A. D. Gaidhane, J. Henkel and Y. S. Chauhan, "Negative Capacitance Transistor to Address the Fundamental Limitations in Technology Scaling: Processor Performance," IEEE Access, Sep. 2018.
- A.D. Gaidhane, G. Pahwa, A. Verma, Y. S. Chauhan, "Compact Modeling of Drain Current, Charges, and Capacitances in Long-Channel Gate-All-Around Negative Capacitance MFIS Transistor," IEEE Transactions on Electron Devices, May 2018.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, “Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", IEEE Transactions on Electron Devices, Mar. 2018.
- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", IEEE Electron Device Letters, Jan. 2018.
- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan,"Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS Structure", IEEE Transactions on Electron Devices, Mar. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part I, Model description", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part II, Model validation", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", IEEE ICEE, Dec. 2016. (Best Paper Award)
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE ESSDERC, Switzerland, Sept. 2016. (Invited)
- G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Compact Modeling of Negative Capacitance Transistor with Experimental Validation", IWPSD, Dec. 2015.

Thank You