ASM-HEMT: Compact Modeling of GaN HEMTs for High Frequency and High Power Applications

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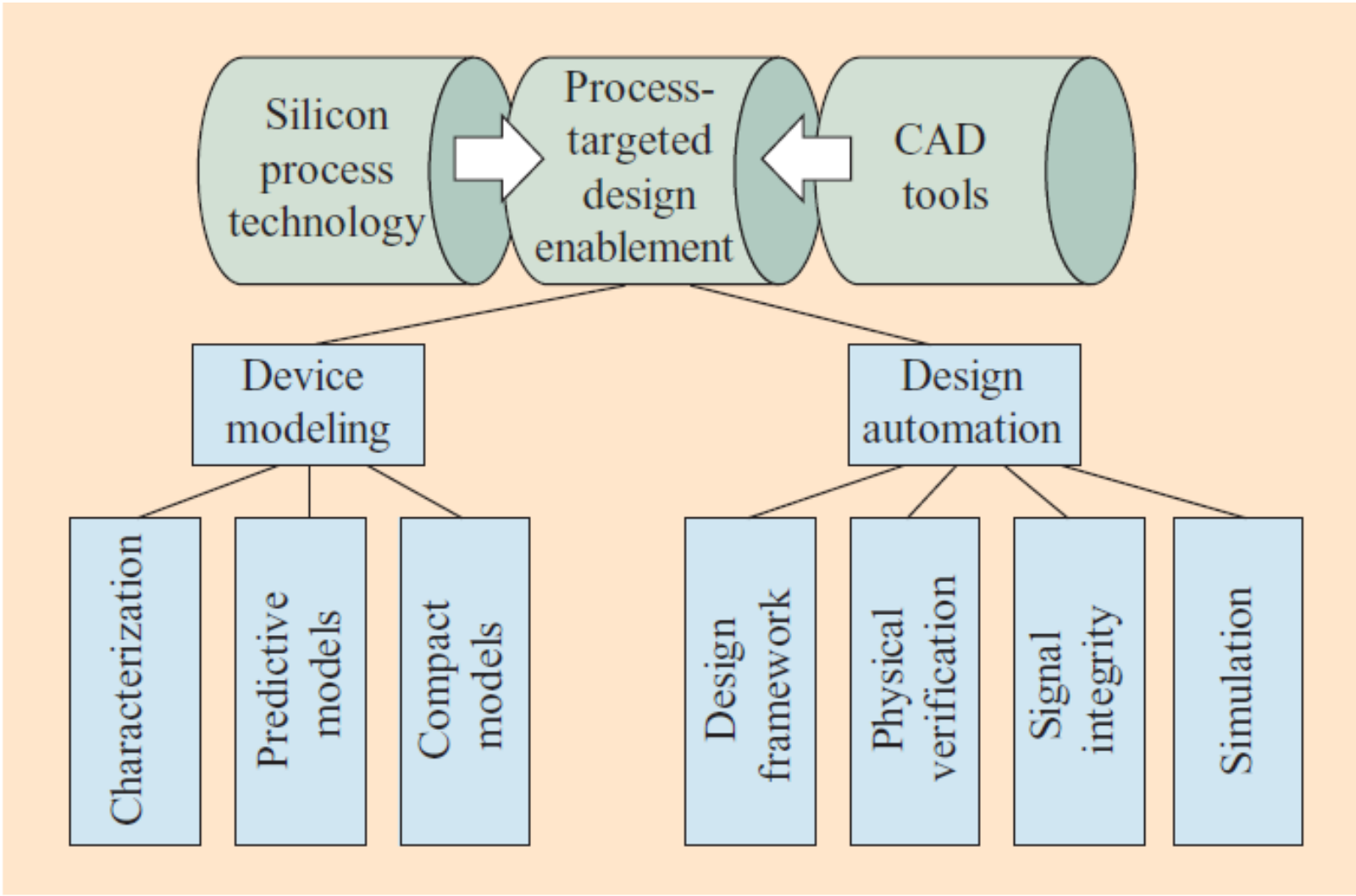
Outline

- Overview of Compact Modeling
- GaN HEMT
- ASM-HEMT Model Overview
- Model Validation

Joint Development & Collaboration

PDK and Compact Model

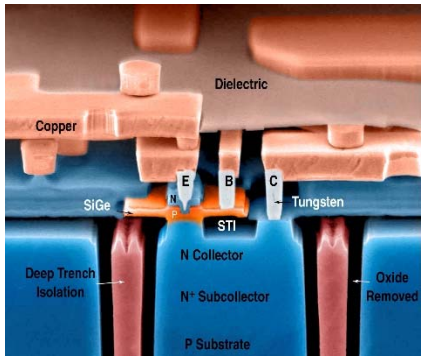
Enablers of a silicon chip design



Source: David HARAME at. al., IBM J. RES. & DEV. MARCH/MAY 2003

Goal of a PDK – The output of Enablement

Technology Innovation

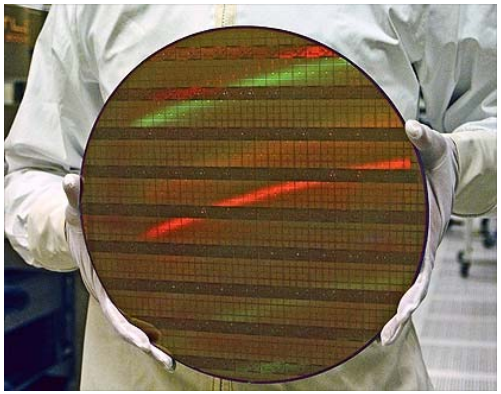


Enablement PDK
Key to Happy Designers!!

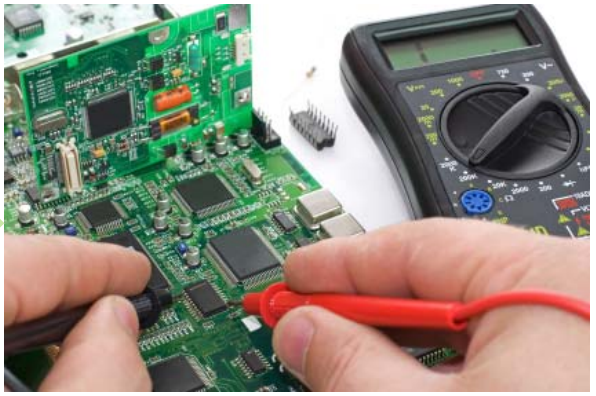
Circuit Designers

- Offer a circuit design environment that enables full exploitation of technology
  - Capture all device physics
  - Model impact of layout choices on device mean and variance
  - Include typical layout effects for simulation from schematic
  - Accurate modeling of layout effects for simulation from layout

Compact Modeling or SPICE Modeling



Medium of information exchange



- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~μ*sec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

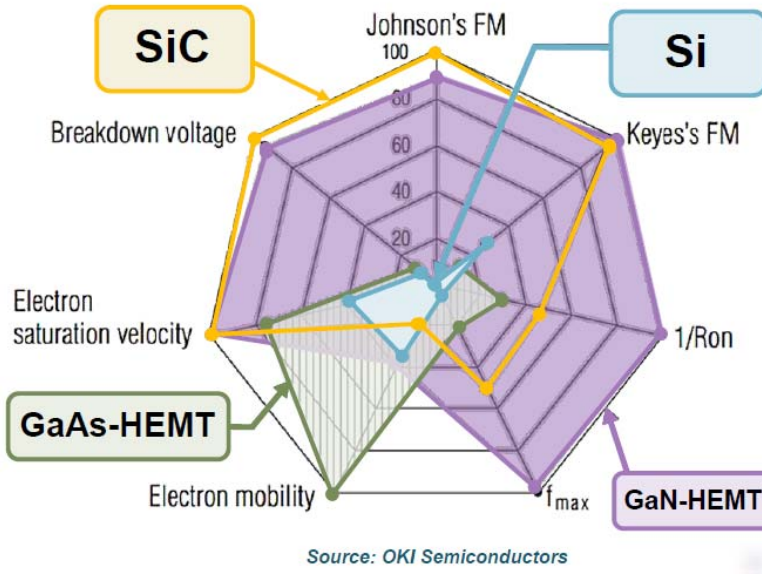
Industry Standard Compact Models

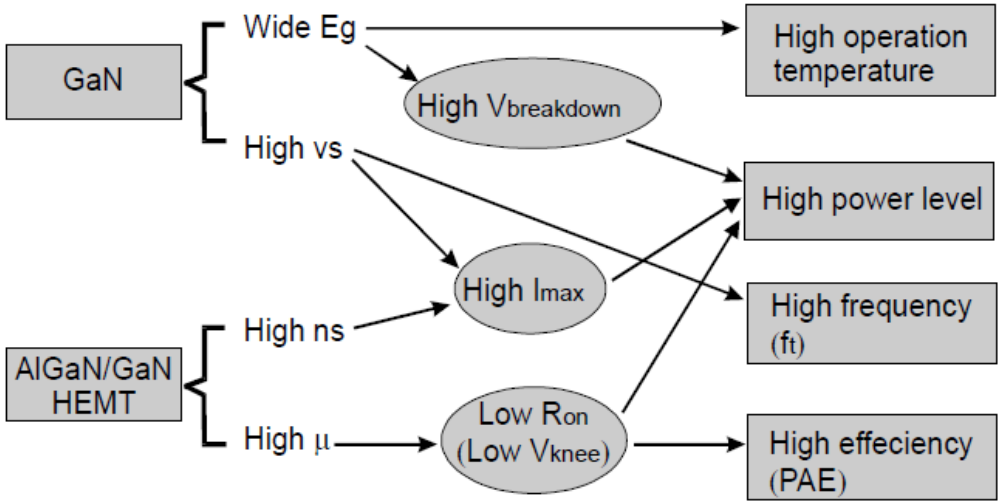
- Standardization Body – Compact Model Coalition
- CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia
- CMC is by the industry and for the industry

GaN Properties

	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.1	1.42	3.26	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0
μ_n (cm^2/Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)
v_{sat} (10^7cm/s)	1.0	1.0	2.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5

Johnson's figure of merit (rel. to Si)





Device characteristics:
- High Breakdown Voltage (V_{BR})
- Low ON Resistance (R_{ON})

[U. K. Mishra *et al.*, Proc. IEEE, **96 (2)**, 287 (2008)]

GaN HEMT: Advantages

600V FETs	Ron (mohm)	Ciss (nF)	FOM 1 (Ron*Ciss)	Coss (nF)@400V	FOM2 (Ron*Coss)	Qrr(uC)	FOM3 (Ron*Qrr)
Si SJ	37	7.24	267	0.38	14	36	1332
SiC MOS	120	1.2	144	0.09	10.8	0.053	6.3
GaN HFET	25	.52	13	0.13	3.25	0.113	2.8

Si SJ: Infineon IPW65R037C6. SiC MOSFET: Rohm SCT2120AF GaN HFET: GaNSystem GS66516T

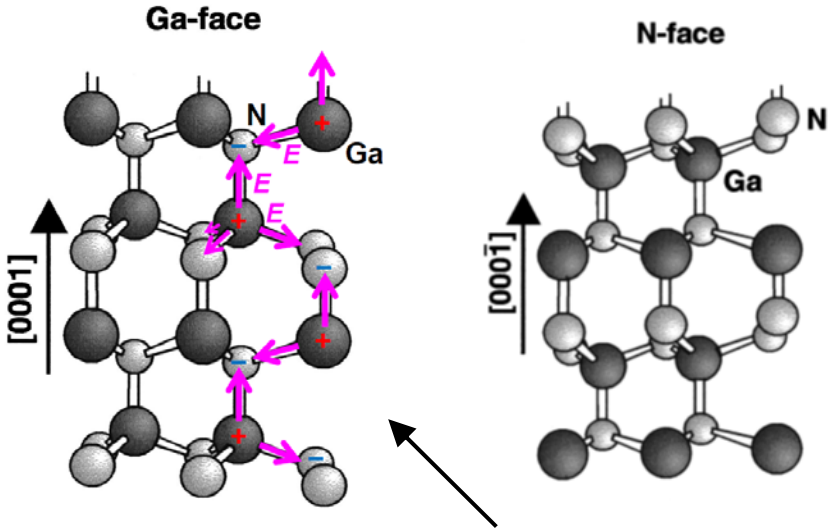
Alex Q. Huang pp. 528-531, IEDM 2016

advantage of fast gate driving capability

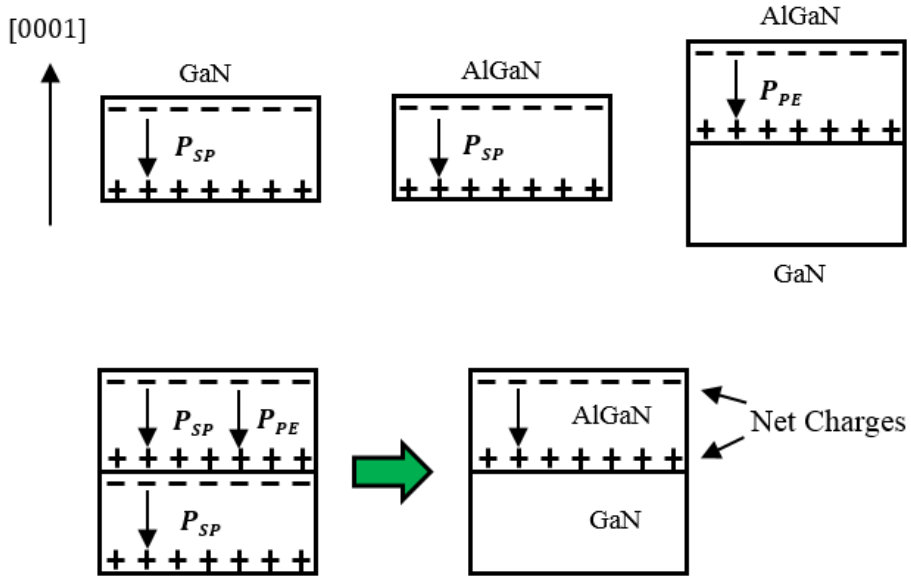
Reduction in switching loss in hard or soft switched converter

Reverse recovery loss reduction

Polarization



Polarization!

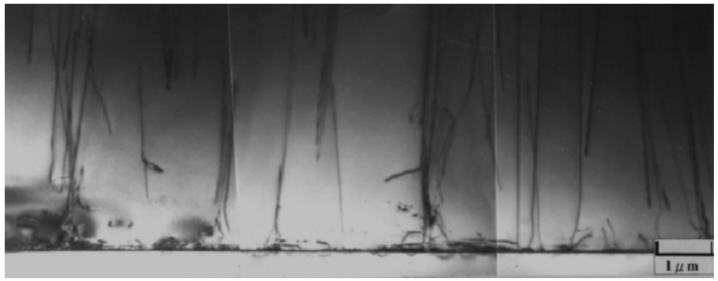


$$P_{\mathrm{PE}} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$$

Constant for a given x (Al fraction)

[O. Ambacher *et al.*, JAP, **85 (6)**, 3222 (1999)]

GaN Wafers



TEM Image of GaN on Sapphire

- **Sapphire (Al_2O_3)**

☺ Semi-insulating
☺ High growth temperatures
☺ Relatively cheap

☹ Low thermal conductivity
☹ Lattice mismatch
☹ CTE mismatch

- **Silicon (Si)**

☺ Low cost
☺ Large diameters
☺ Acceptable thermal conductivity
☺ Processing in standard silicon fabs

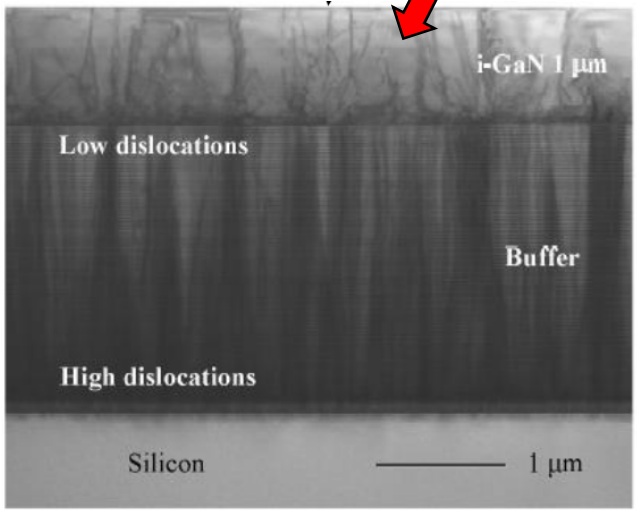
☹ Lattice mismatch
☹ CTE mismatch

- **Silicon Carbide (SiC)**

☺ High thermal conductivity
☺ Low Lattice mismatch
☺ Low CTE mismatch

☹ Highly costly
☹ Smaller Wafers

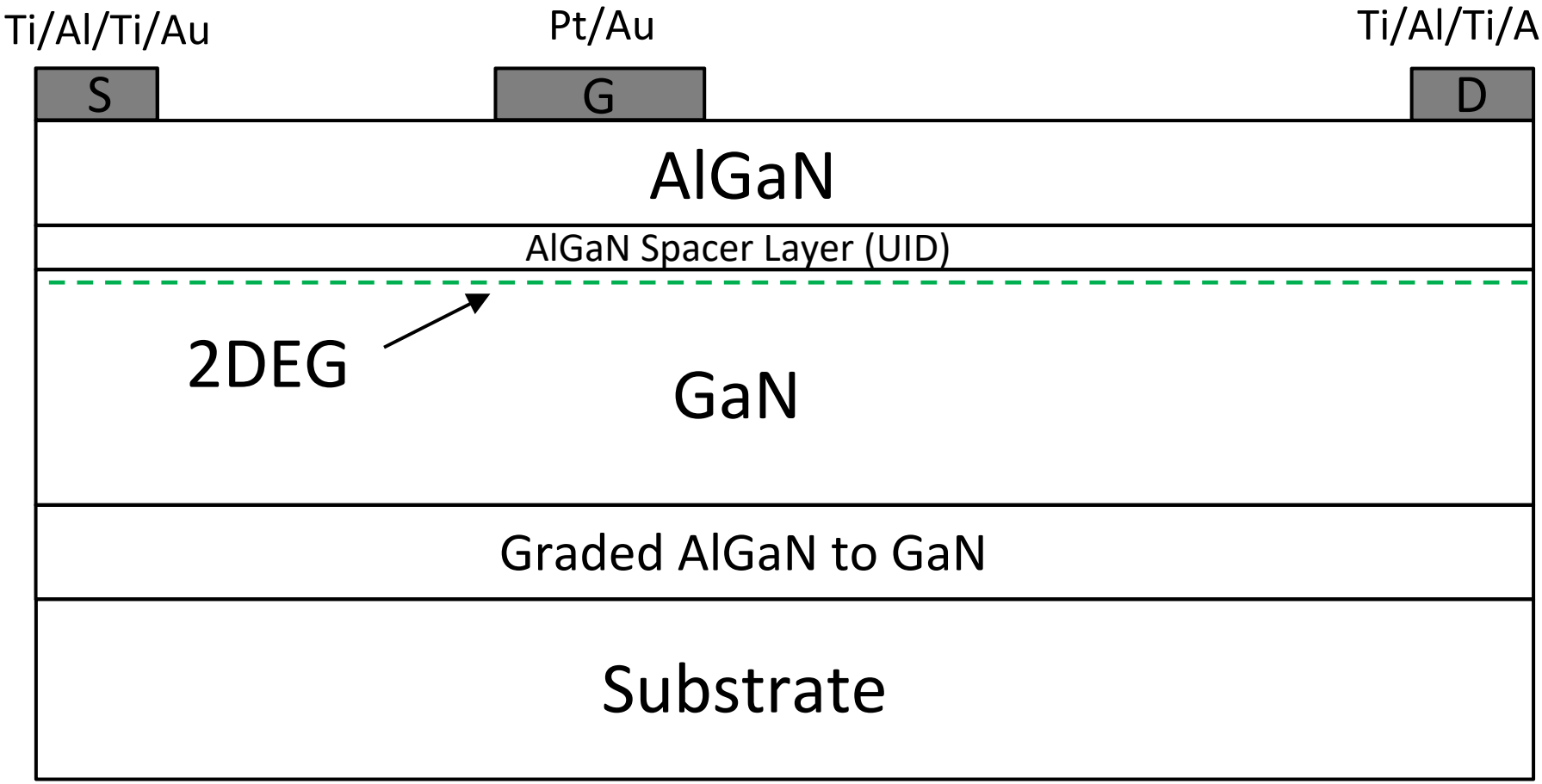
Dislocations ~ $10^9\ cm^{-2}$



[S. Huang, JJAP, 47 (10), 7998 (2008)]
[S. L. Selvaraj et al., Proc. DRC, 53 (2012)]

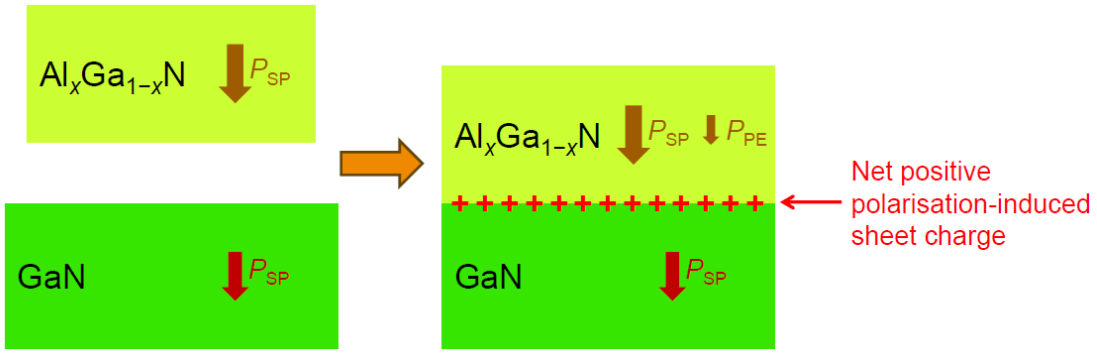
[U. K. Mishra et al., Proc. IEEE, 96 (2), 287-305 (2008)]

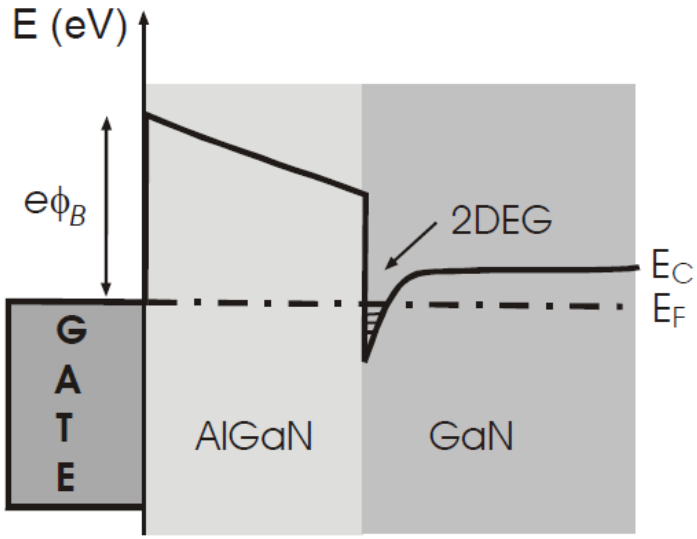
GaN HEMT Structure



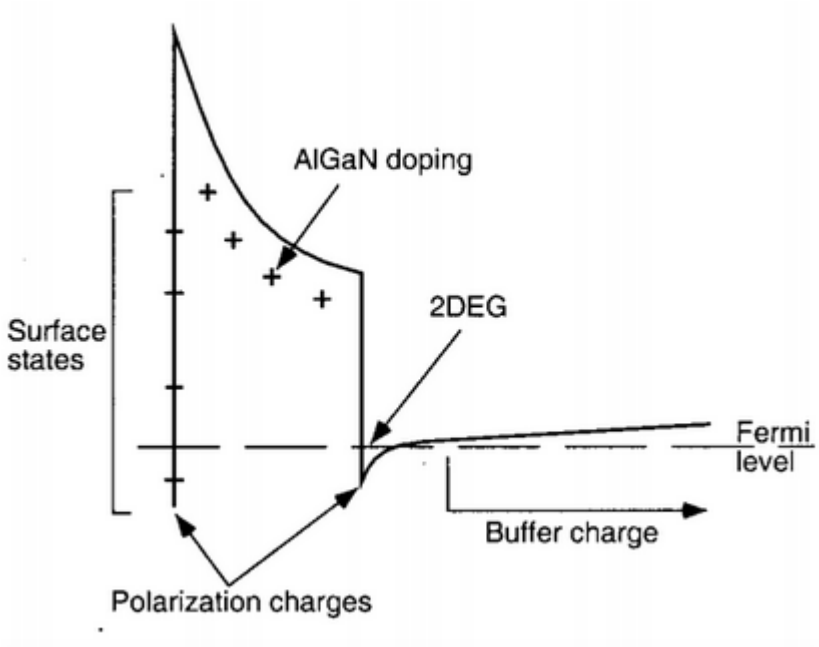
AlGaN/GaN Hetero-structure

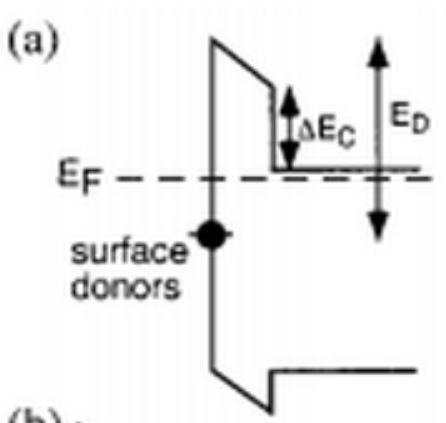
- The AlGaN/GaN hetero-structure is used to take advantage of the two dimensional electron gas (2-DEG)
- AlGaN/GaN materials create piezoelectric and spontaneous polarization effects using an un-doped hetero-interface

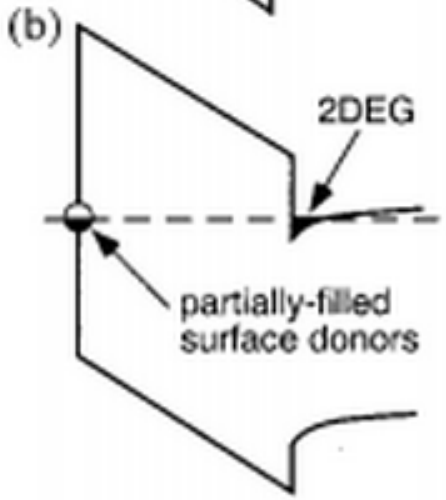


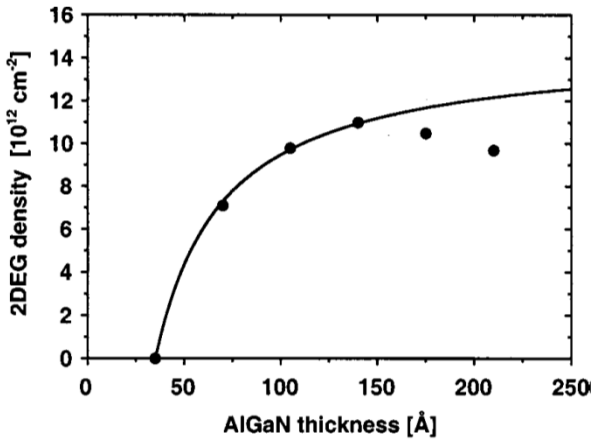


2DEG Source









$$qn_s = \sigma_{pz}\left(1 - \frac{t_{cr}}{t}\right)$$

[J. P. Ibbetson *et al.*, APL, **77 (2)**, 250 (2000)]

Design Rules – Materials Perspective

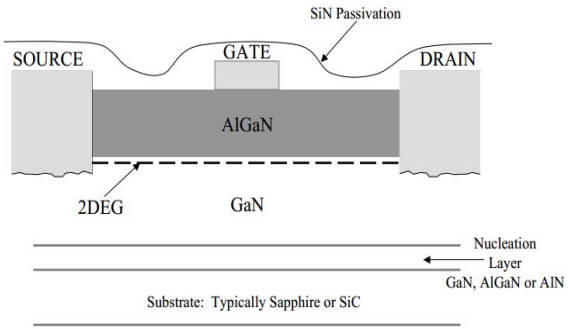
- Thickness of the barrier – 2DEG control
- Al Mole Fraction – 2DEG Concentration
- Nucleation and Buffer Layer – Dislocations
- Substrate – Thermal Properties

GaN HEMT

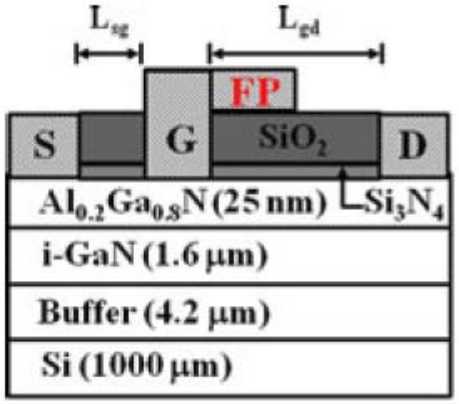
Some interesting features of III-nitride system:

- Wide bandgap
- High 2-DEG charge density
- High electron mobility
- High breakdown voltage
- Excellent thermal conductivity
- High power density per mm of gate periphery

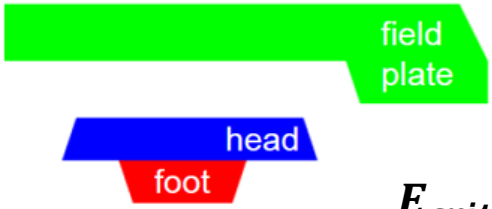
- GaN based HEMTs are able to operate in high frequency, high power as well as high temperature device applications



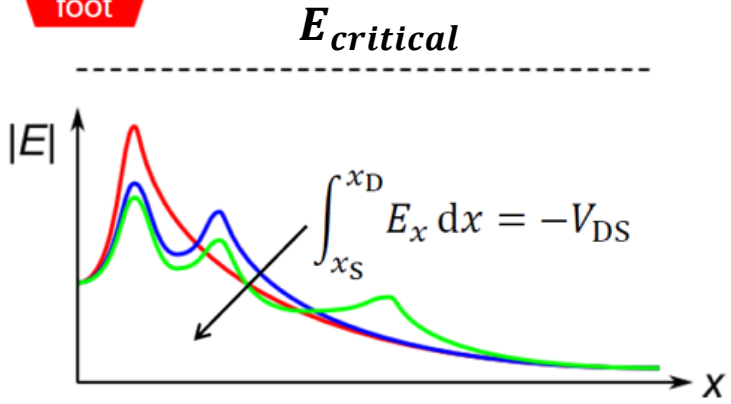
Field Plates



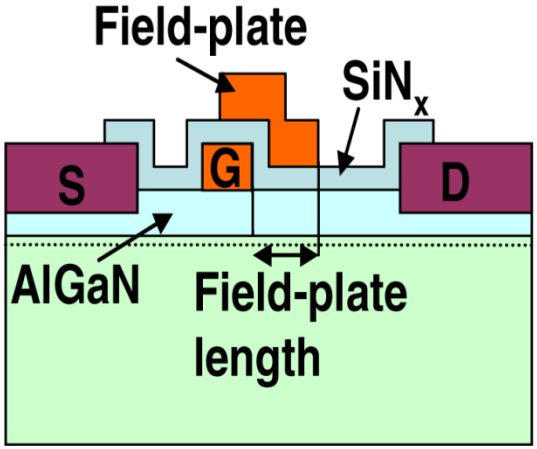
Field Plated Structure



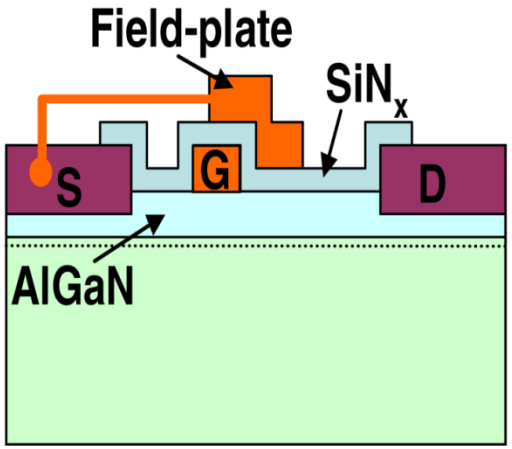
Distribution of *E*



C_{gd} and C_{ds}



(a)

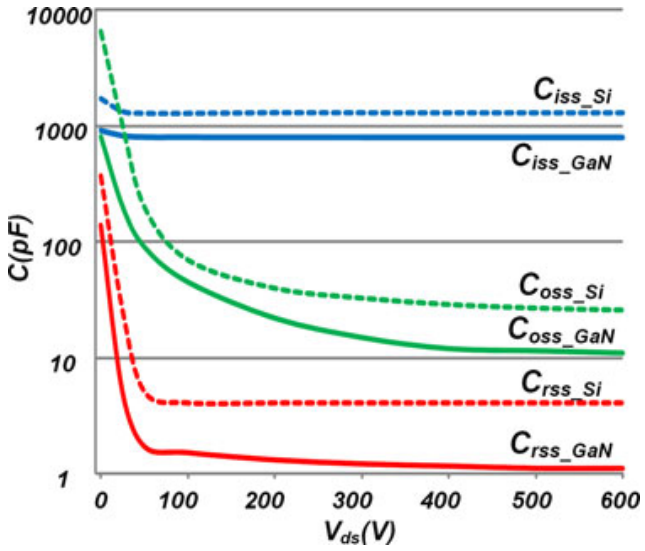


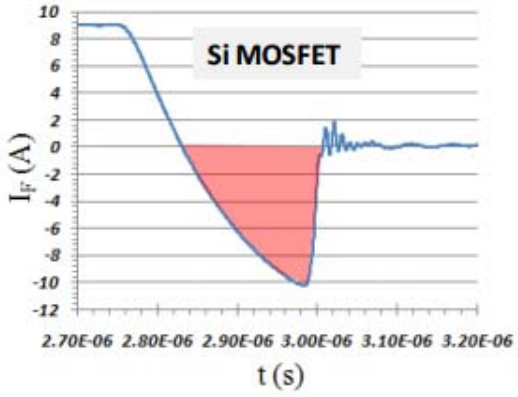
(b)

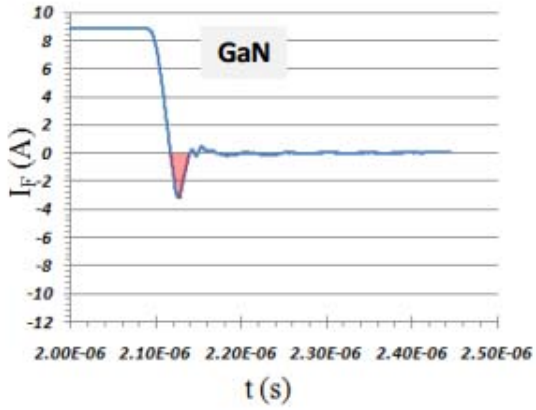
[H Huang, *et al.*, IEEE TPEL, **29 (5)**, 2164 (2014)]

[W. Saito *et al.*, IEEE TED, **50 (12)**, 2528 (2003)]

Switching applications



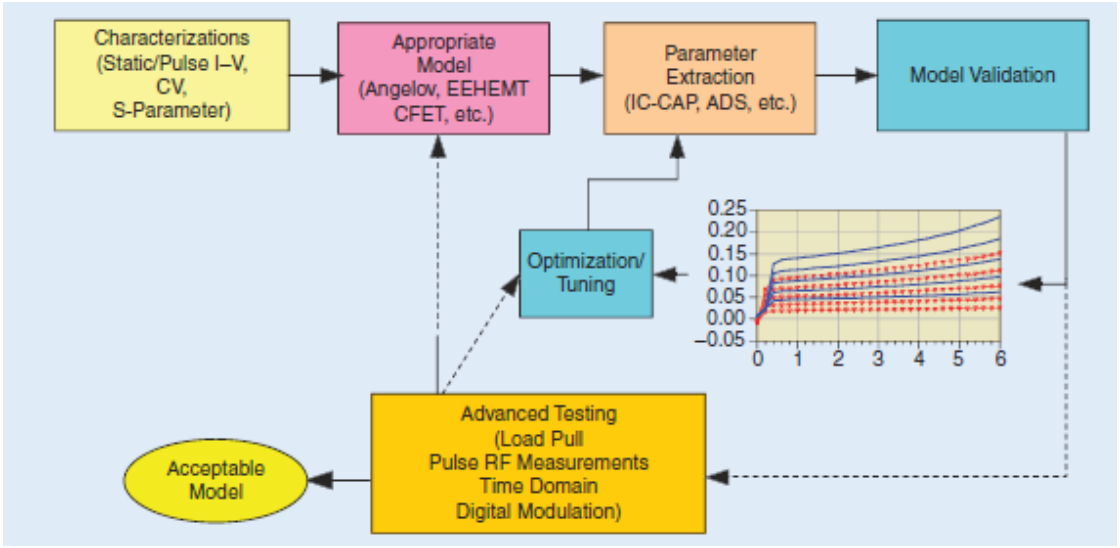




- Small terminal capacitances
- Less reverse recovery charge
- Power loss is low

[X. Huang, *et al.*, IEEE TPEL, **29 (5)**, 2453 (2014)]

Modeling GaN!



Modeling Strategy

Existing Models

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

[L. Dunleavy *et al.*, Microwave Magazine **11 (6)**, 82 (2010)]

Modeling Continued…

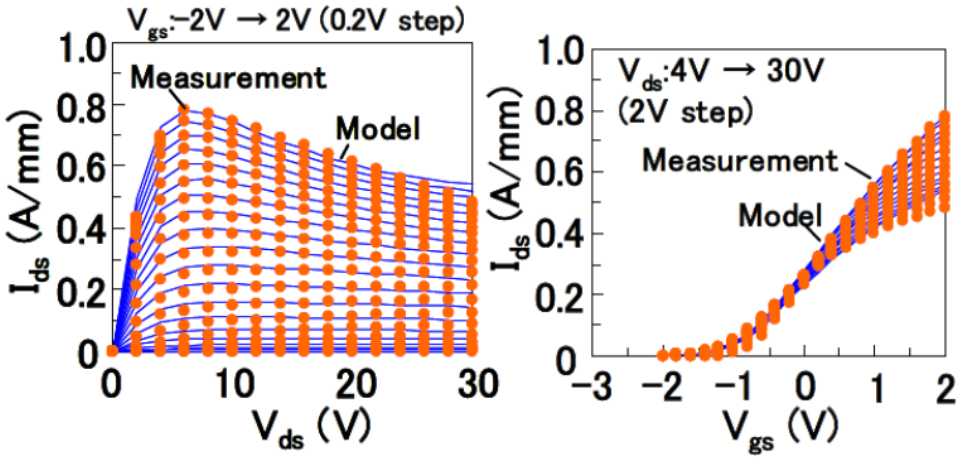
Angelov model

$$g_m = g_{mpk}\left(1 - tanh^2[p_{1m}\,(V_{gs} - V_k)]\right)$$

$$I_{ds} = I_{pks}\,(1 + tanh(\psi_p))\,tanh(\alpha V_{ds})\,(1 + \lambda V_{ds})$$

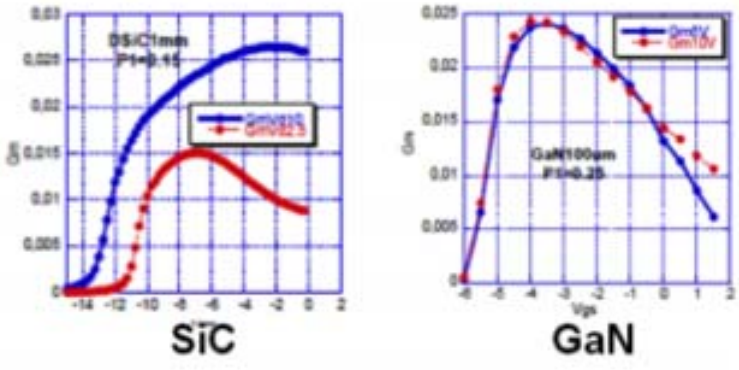
$$\psi_p = P_{1m}\,(V_{gs} - V_{pk0}) + P_2\,(V_{gs} - V_{pks})^2 + P_3\,(V_{gs} - V_{pksm})^3$$

$$C_{gs} = C_{gsp} + C_{gso}\,(1 + tanh(\psi_1))\,(1 + tanh(\psi_2))$$



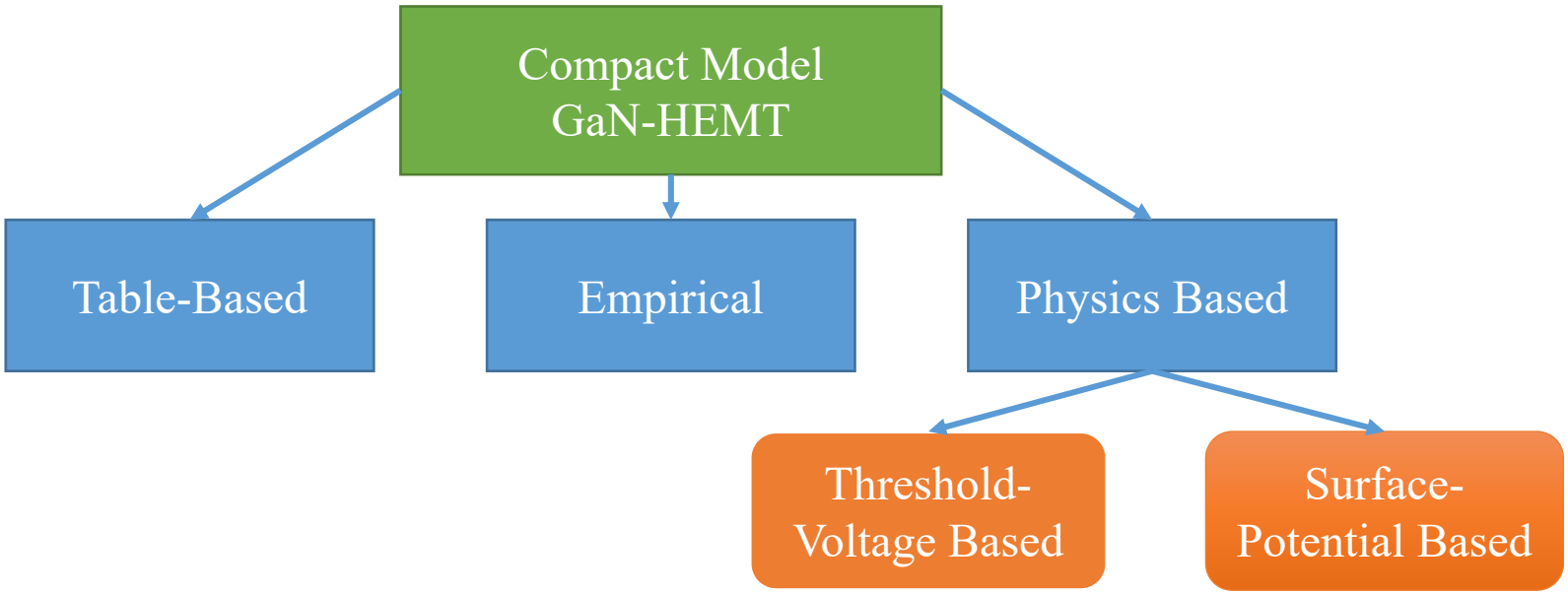
Angelov Model Deficiencies

- Emperical model with ~ 90 parameters
- Fails to capture non-linear behaviour and harmonic accuracy in power circuits
- Challenging to use for multiple device dimensions



[I. Angelov *et al.*, IEEE T-MTT, **44 (10)**, 1664 (1996)] [I. Angelov *et al.*, IEEE T-MTT, **40 (12)**, 2258 (1992)]

Status of Compact Model – GaN HEMT



Advanced SPICE Model for GaN HEMT device

CMC candidate models for industry standardization

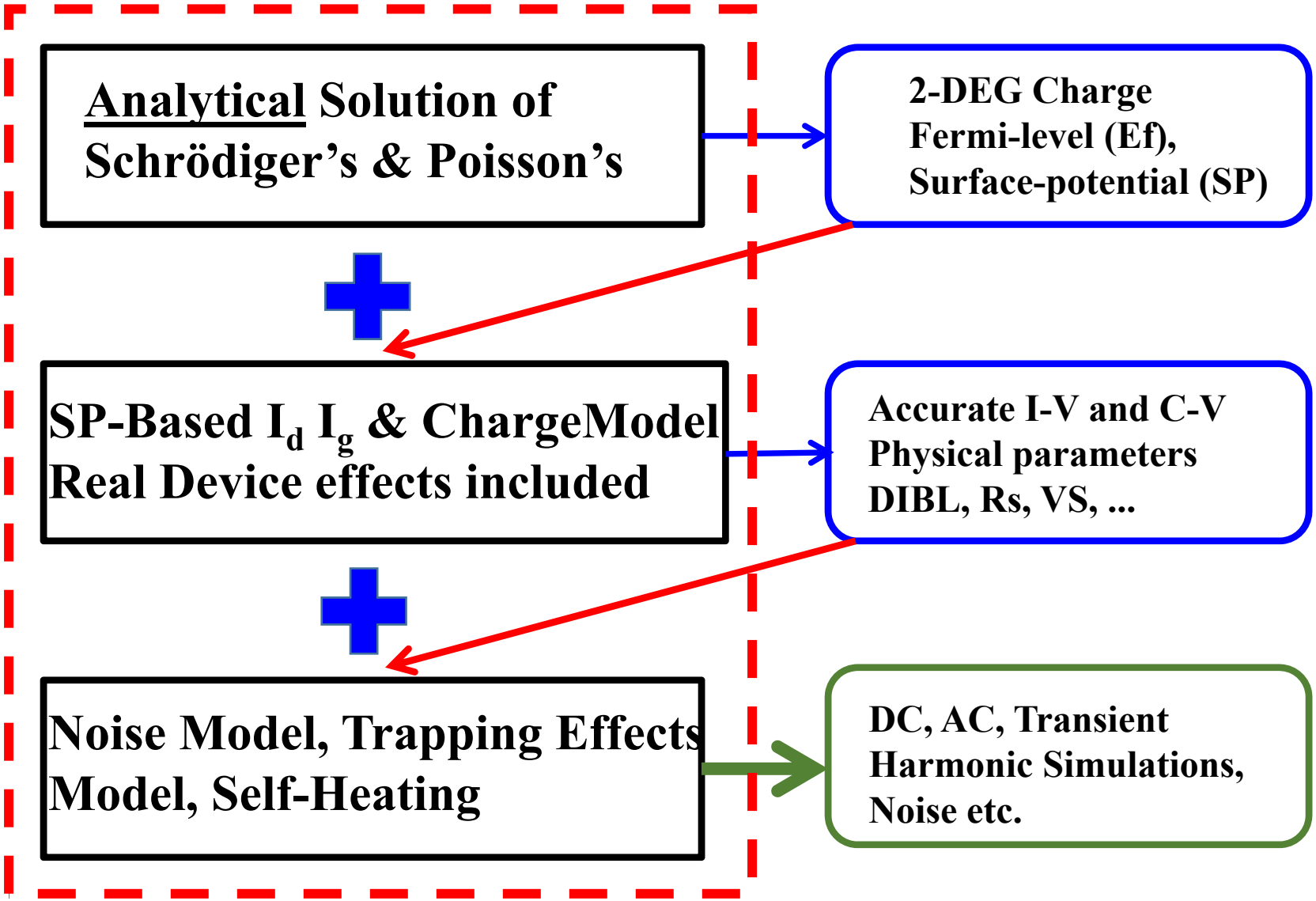
(Two models are in final phase)

- ASM-HEMT model: Our model
- MIT Unified VS GaNFET (MVSG) model: MIT, Prof. D. Antoniadis

Advantages of SP-Based Model

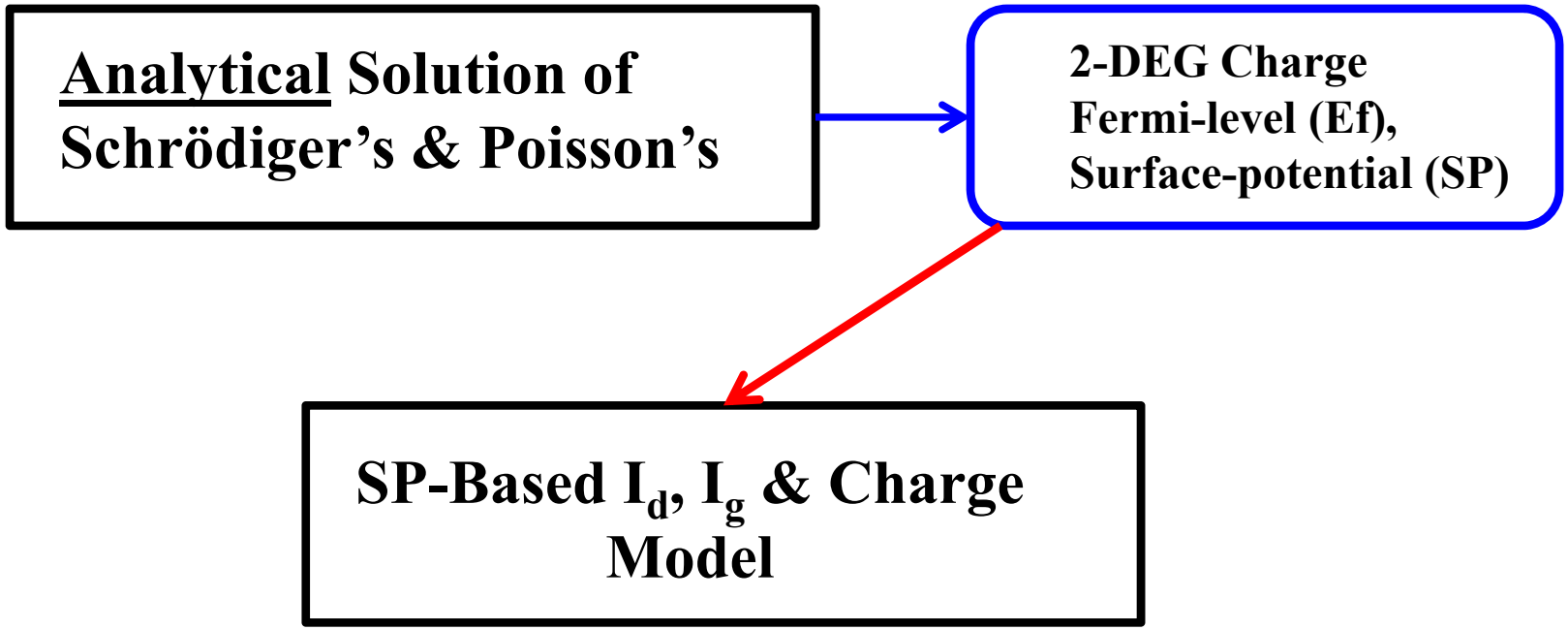
- Better Model Scalability
- Device Insight
- Better Statistical Behavior
- Accurate Charges and Capacitances
- Better Temperature Scalability
- Less number of parameters
- Easier parameter extraction
- Uses a single expression for all regions
- Inherent Model Symmetry

ASM-HEMT Model Overview



ASM-HEMT Model Overview

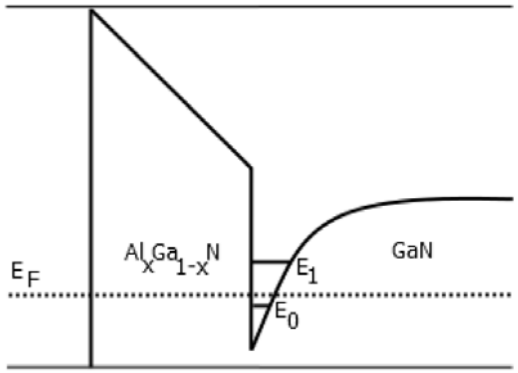
Core Model



Surface-Potential Calculation

Assumptions:

- Quasi-constant electric field in the potential well (triangular well approximation)
- Only the contribution of the first two sub-bands are important



$$n_s = DV_{th}\left\{\ln\left[\exp\left(\frac{E_f - E_0}{V_{th}}\right) + 1\right] + \ln\left[\exp\left(\frac{E_f - E_1}{V_{th}}\right) + 1\right]\right\}$$

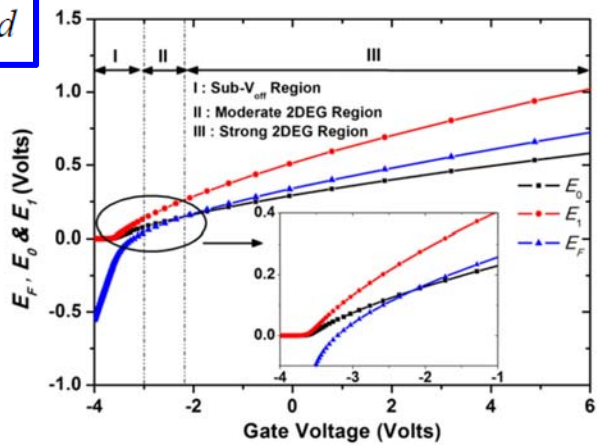
Quasi-Fermi-potential and SP

$$E_{f,\text{unified}} = V_{\text{go}} - \frac{2V_{\text{th}} \ln\left(1 + e^{\frac{V_{\text{go}}}{2V_{\text{th}}}}\right)}{1/H(V_{\text{go},p}) + (C_g/qD)e^{\frac{-V_{\text{go}}}{2V_{\text{th}}}}}$$

$$E_{f1} = E_{f,\text{unified}} - \frac{p}{q}\left(1 + \frac{pr}{2q^2}\right)$$

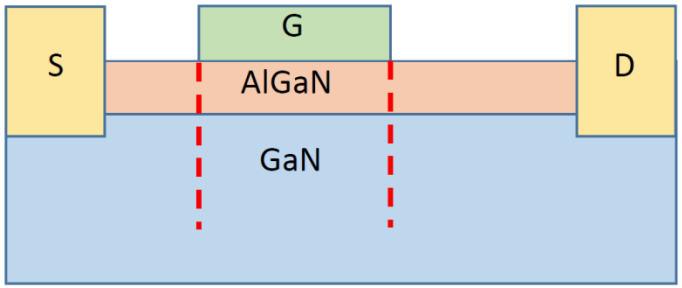
$$\psi_{s/d} = E_{f,s/d} + V_{s/d}$$

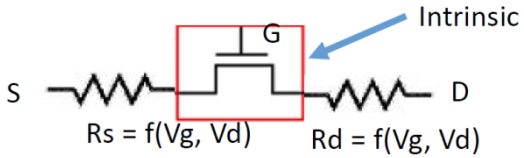
- Basic device equations are transcendental in nature
- We divide variation of E_f with V_g into regions to develop fully analytical expression
- Regional models are combined in one analytical expression
- No fitting parameters introduced, accuracy (order of nano-Volts)



S. Khandelwal, TED, VOL. 59, NO. 10, OCTOBER 2012

ASM-HEMT Model Overview





CLM

Mobility Degradation

Temperature Dependence

Bias Dependent Series Resistance

Self-Heating

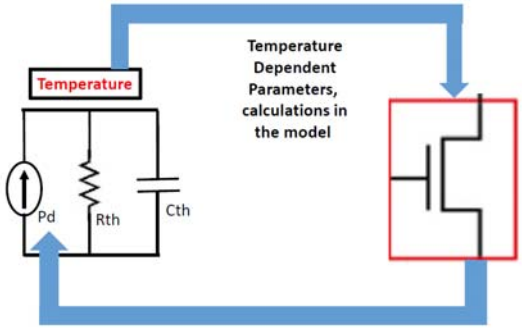
Core Drain Current Model

Complete Drain Current Model

DIBL

Velocity Saturation

Sub-threshold Slope



SPICE Model including Self-Heating

Drain-Current Model and Intrinsic Charges

- We apply the drift-diffusion framework for carrier transport
- An analytical and continuous expression for the core drain-current is developed including the velocity-field relation and mobility degradation
- Core Drain Current Model:

$$\int I_d .dx = \int \mu_{eff} W \tilde{Q}_{ch} d\psi$$

$$\tilde{Q}_{ch} = V_{th} \frac{dQ_{ch}}{d\psi} - Q_{ch}$$

$$I_{ds} = \frac{\mu_{eff} C_g}{\sqrt{1 + \theta_{sat}^2 \psi_{ds}^2}} \frac{W}{L} \left(V_{go} - \psi_m + V_{th}\right) \left(\psi_{ds}\right) \left(1 + \lambda V_{ds}\right)$$

- Velocity-Field relation and mobility-degradation:

$$\psi_{ds} = \psi_d - \psi_s \qquad \psi_m = \left(\psi_d + \psi_s\right)/2 \qquad \theta_{sat} = \mu_{eff} / v_{sat} L$$

$$\mu_{eff} = \frac{\mu_0}{1 + UA \left(V_{go} - \psi_m\right) + UB \left(V_{go} - \psi_m\right)^2}$$

λ is the CLM parameter

- Ward-Dutton Partitioning for S/D charges
- Capacitances are calculated as derivatives of the terminal charges: $C_{ij}=-dQ_i/dV_j$ $(i\neq j)$, $C_{ii}=dQ_i/dV_i$ $(i=j)$

Charge conservation

$$Q_g = \int_0^L W q n_s \left(V_g, V_x\right).dx$$

$$Q_d = \int_0^L \frac{x}{L} W q n_s \left(V_g, V_x\right).dx$$

$$Q_s = \int_0^L \left(1 - \frac{x}{L}\right) W q n_s \left(V_g, V_x\right).dx$$

Temperature Dependence

$$\mu_0(T) = U0 \cdot \left(\frac{T}{TNOM}\right)^{UTE} \qquad V_{sat}(T) = VSAT \cdot [1 + AT(T - TNOM)]$$

$$V_{off}(T) = VOFF + KT1 \cdot \left(\frac{T}{TNOM} - 1\right)$$

$$R_{source}(T) = \frac{R_{sc}(T)}{W \cdot NF} + R_{s,bias}(T)$$

$$I_{sat,acc}(T) = W \cdot NF \cdot q_{s,acc}(T) \cdot V_{sat,accs}(T)$$

$$q_{s,acc}(T) = q \cdot n_{s0}(T)$$

$$n_{s0}(T) = NSOACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

$$V_{sat,accs}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

$$R_{drain}(T) = \frac{R_{dc}(T)}{W \cdot NF} + R_{d,bias}(T)$$

$$R_{sc}(T) = RSC \cdot \left(1 + KRSC\left(\frac{T}{TNOM} - 1\right)\right)$$

$$R_{dc}(T) = RDC \cdot \left(1 + KRDC\left(\frac{T}{TNOM} - 1\right)\right)$$

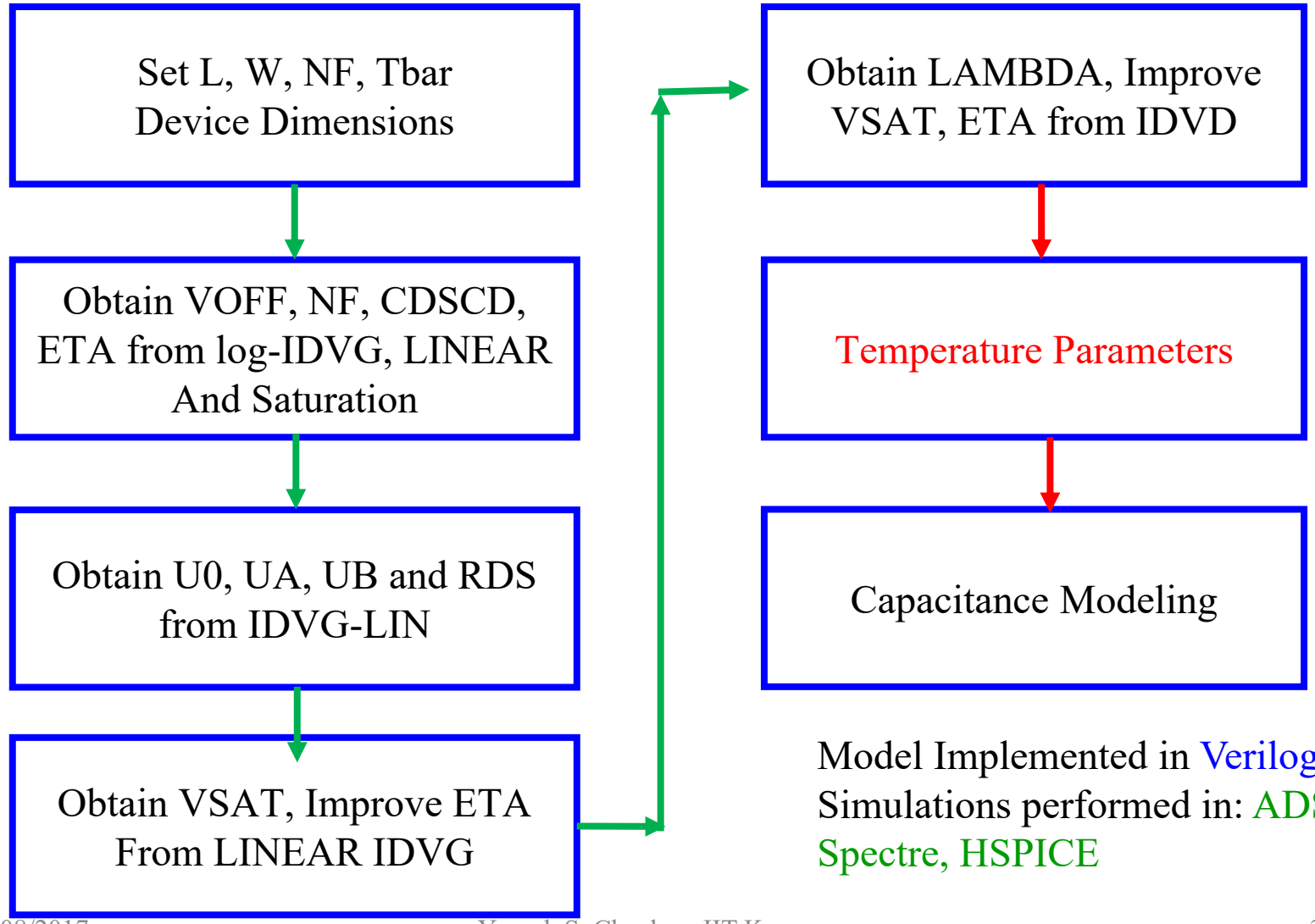
$$R_{s0}(T) = \frac{LSG}{W \cdot NF \cdot q_{s,acc}(T) \cdot \mu_{0,accs}(T)}$$

$$R_{d0}(T) = \frac{|LDG}{W \cdot NF \cdot q_{s,acc}(T) \cdot \mu_{0,accd}(T)}$$

$$R_{s,bias}(T) = \frac{R_{s0}(T)}{\left[1 - \left(\frac{I_{ds}}{I_{sat,acc}(T)}\right)^{MEXPACCS}\right]^{\frac{1}{MEXPACCS}}}$$

$$R_{d,bias}(T) = \frac{R_{d0}(T)}{\left[1 - \left(\frac{I_{ds}}{I_{sat,acc}(T)}\right)^{MEXPACCD}\right]^{\frac{1}{MEXPACCD}}}$$

Model Parameter Extraction



Model Implemented in Verilog-A
Simulations performed in: ADS, Spectre, HSPICE

List of Main Parameters

- Physical Constants
- Simulation Conditions
- Device dimensions
- Physically-Linked Parameters

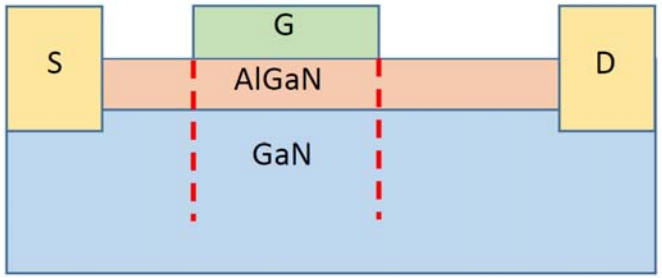
Parameters	Physical Meaning
U0	Low field Mobility
UA	Mobility degradation parameter
UB	Mobility degradation parameter
VOFF	Cut-off Voltage of Device
VSAT	Saturation Velocity
RTH	Thermal Resistance
DIBL	DIBL effect parameter
LAMBDA	Channel length modulation
VOFFT	Temperature dependence of Voff
UTE	Mobility dependence of mu0
RS	Source Side Resistance
RD	Drain Side Resistance
…..	…..

Importance of $R_{d/s}$ Model

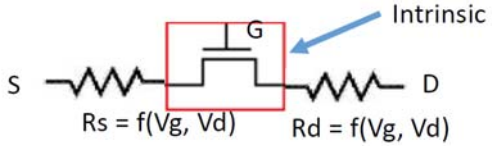
- Aggressive lateral scaling of source-drain access regions improve the RF performance of GaN HEMT but at the cost of breakdown voltage (BV)
  - Too short L_{gd} increases electric field which is responsible for lowering of BV
  - Scaling of L_{gd} also affects the f_{max} due to increasing C_{gd} and g_{ds} of device
- As a trade-off, a short L_{gs} and optimized L_{gd} is required to achieve high f_T , f_{max} and BV altogether

- In GaN HEMT, gate-to-drain/source access region works as nonlinear resistance ($R_{d/s}$) which limits maximum drain current
- Accurate model of $R_{d/s}$ is of great importance to predict the I_d and g_m for high power as well as high frequency GaN HEMTs

Nonlinear source/drain access region resistance model



$$R_J = \frac{L_J}{q\mu_n n_{s0}} \qquad J = S, D$$



$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R/V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

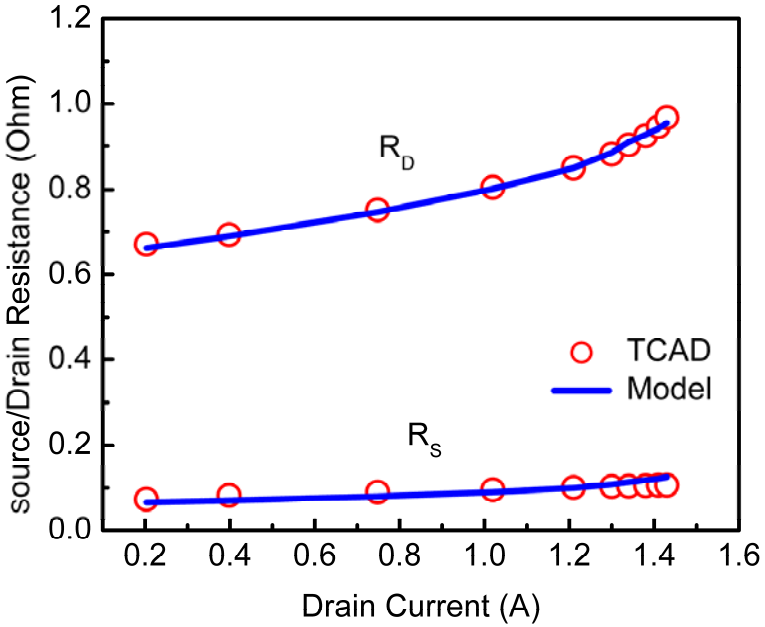


Fig. 1: Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

$R_{d/s}$ Model Validation with Measurement

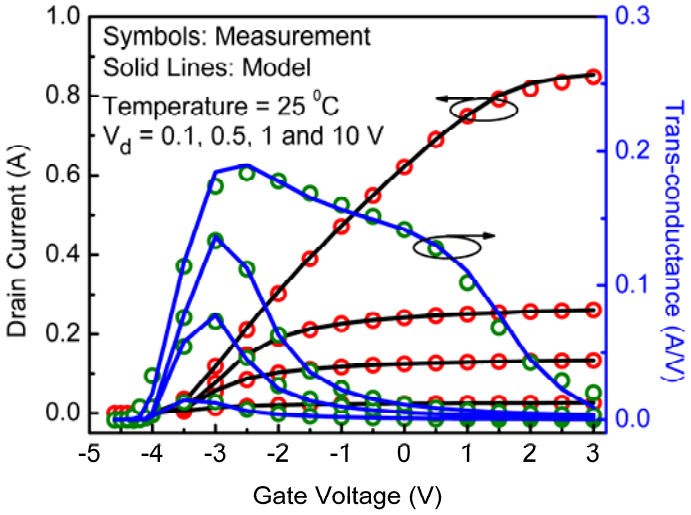


Fig. 2: I_d - V_g and trans-conductance for the Toshiba power HEMT. Different slopes above V_{off} in g_m-V_g: self-heating governs the first slope while velocity saturation in access region affects second slope.

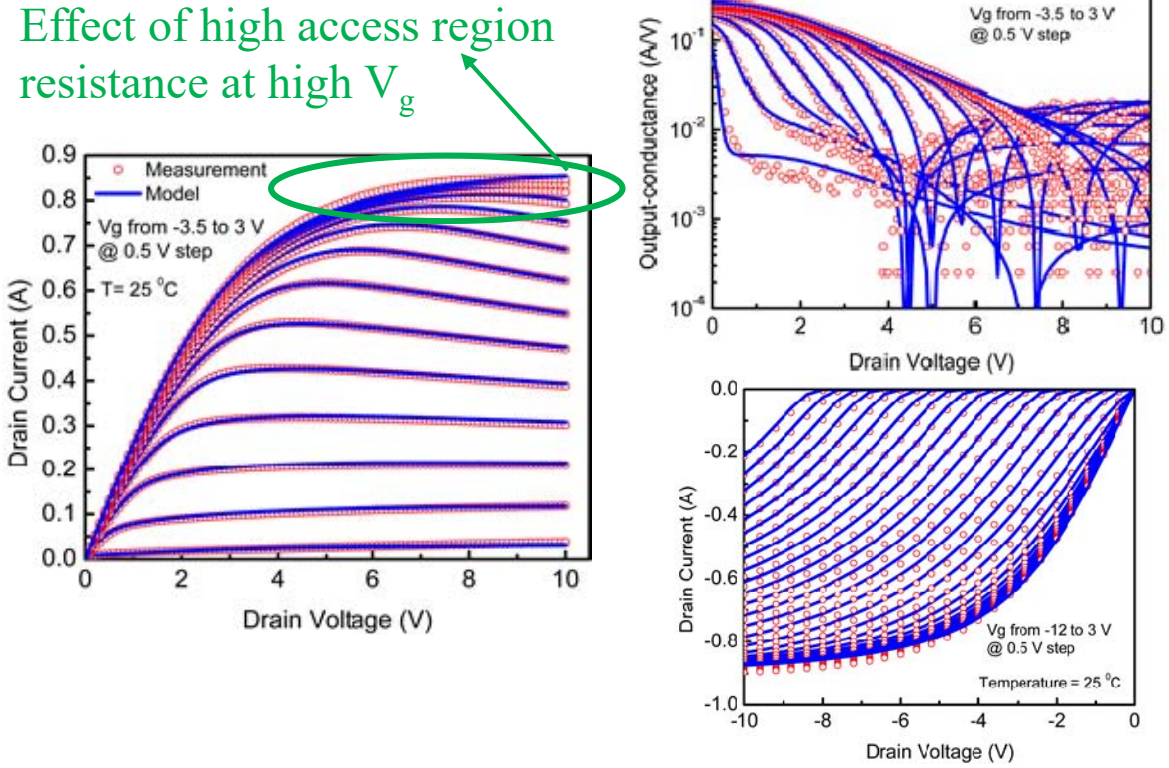


Fig. 3: (a) Ids-Vds, (b) g_{ds} and (c) reverse Ids-Vds fitting with experimental data. The non-linear $R_{s/d}$ model shows correct behavior for the higher Vg curves in the Id - Vd plot; the S-P based model can accurately capture the reverse output characteristics.

Modeling of Temperature dependence

The temperature dependence of $R_{d/s}$ model is extremely important as it increases significantly with increasing temperature

Temperature dependence of 2-DEG charge density in the drain or source side access region:

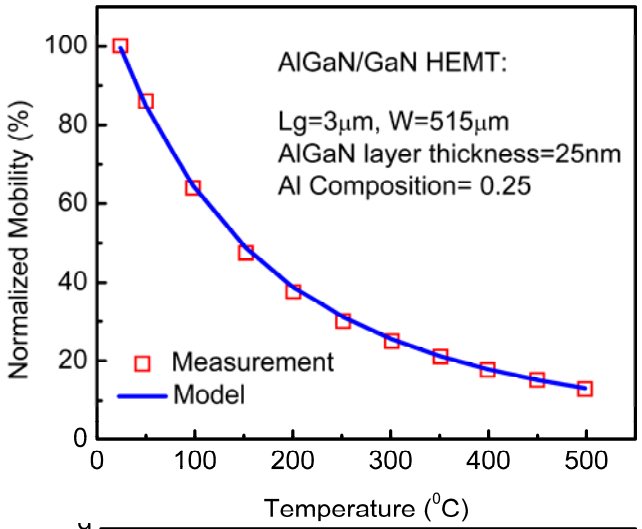
$$n_{s0}(T) = NS0ACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

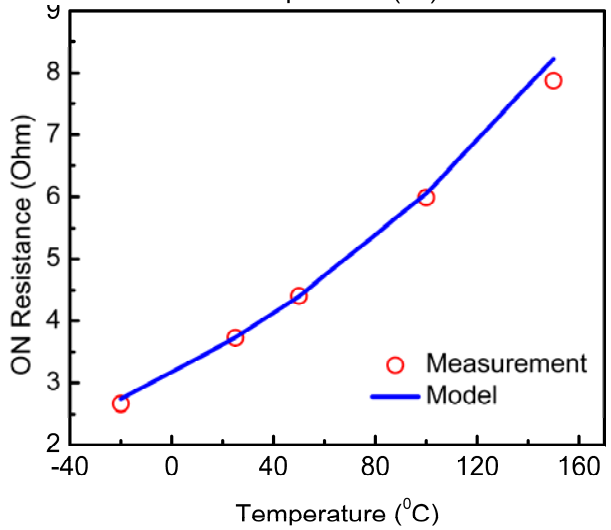
Temperature dependence of Saturation Velocity:

$$V_{sat}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

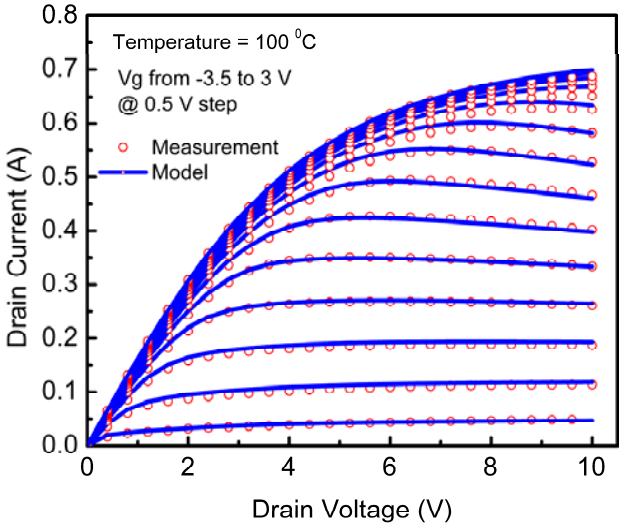
Temperature dependence of electron Mobility:

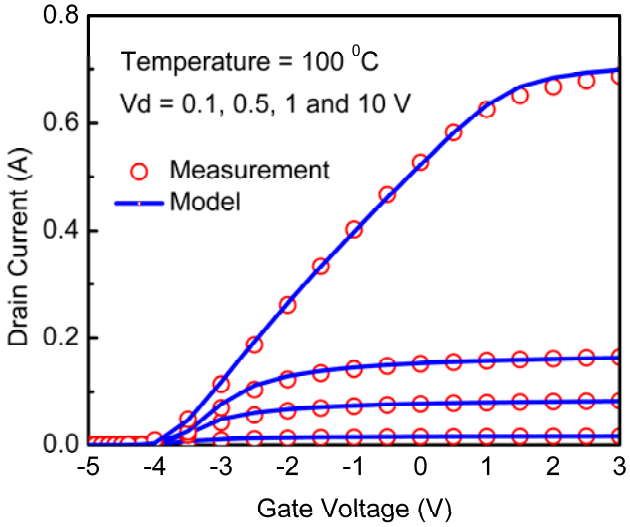
$$\mu_{acc}(T) = U0ACC \cdot \left(\frac{T}{TNOM}\right)^{UTEACC}$$

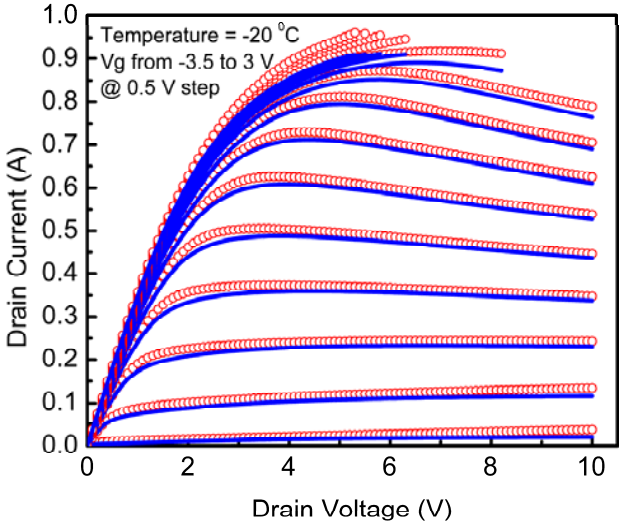


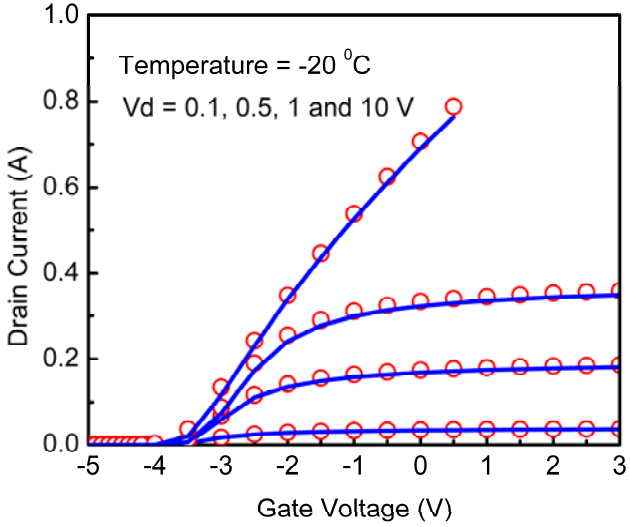


Temperature Model Validation







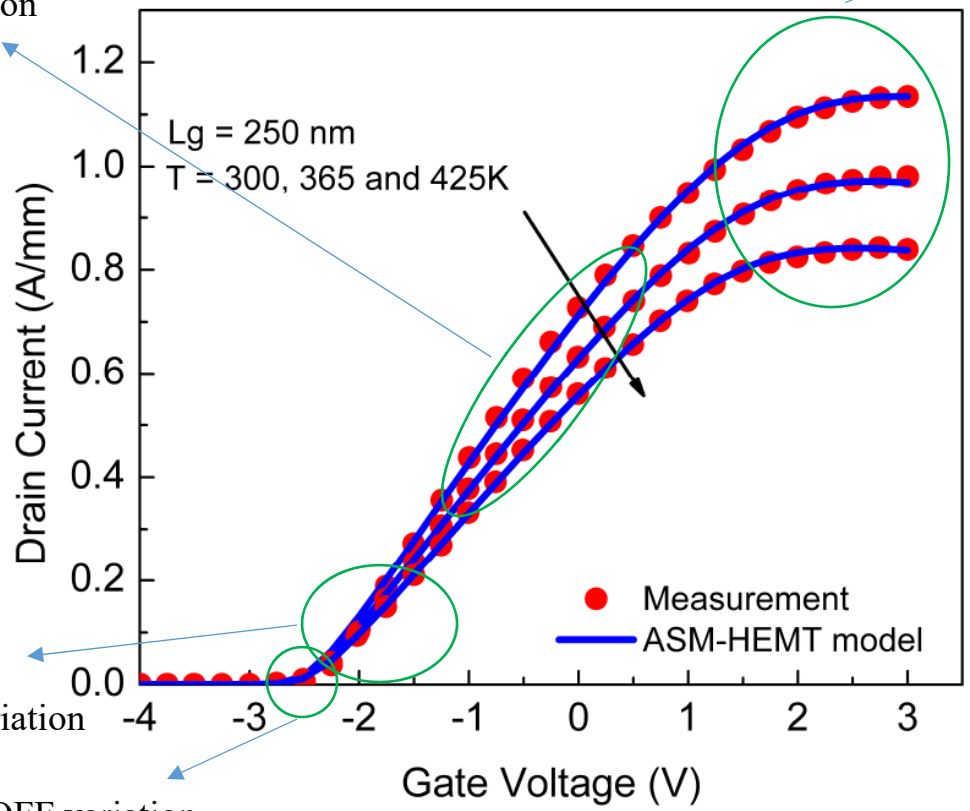


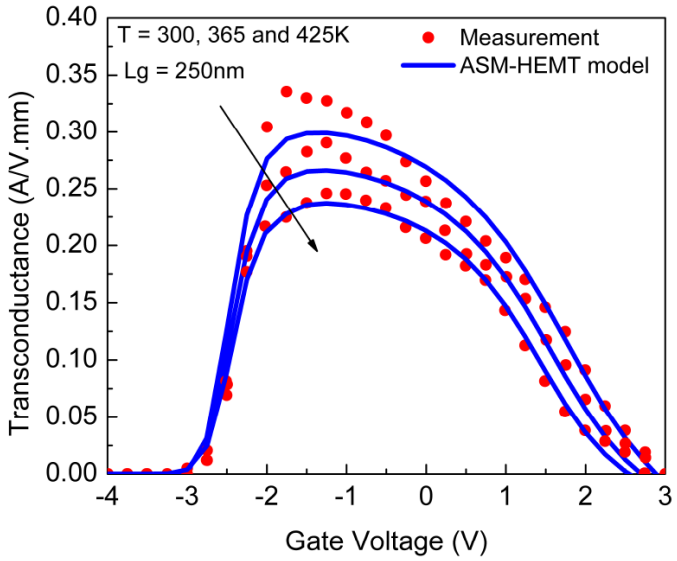
Temperature Model Validation

Id-Vg at three different temperatures 300, 365 and 425 K

RDS variation

VSAT variation



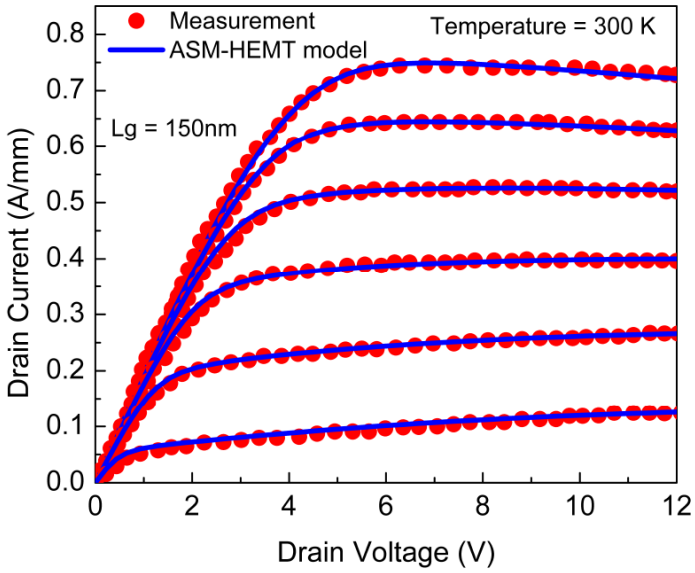


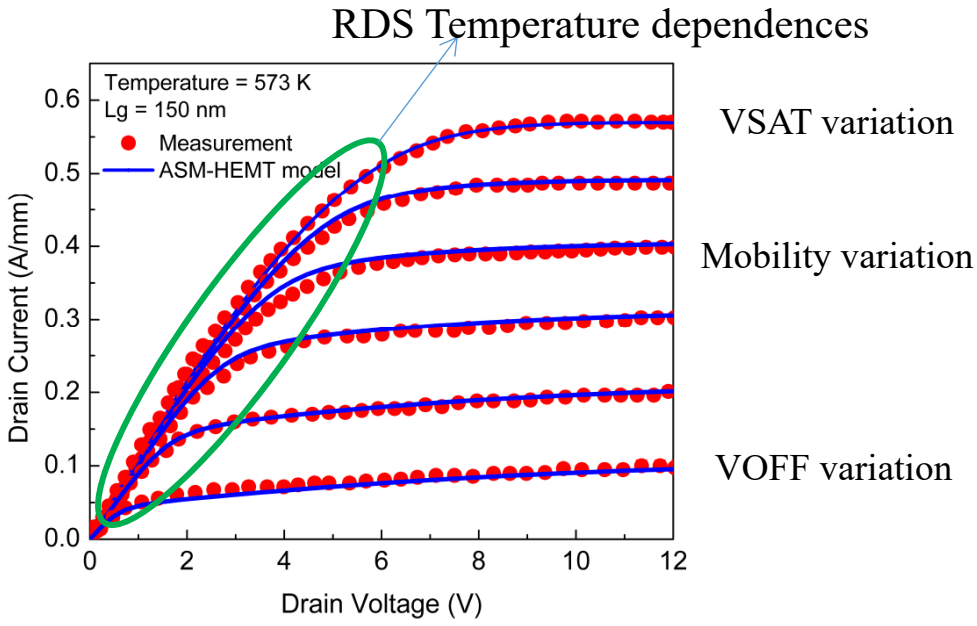
Mobility variation

VOFF variation

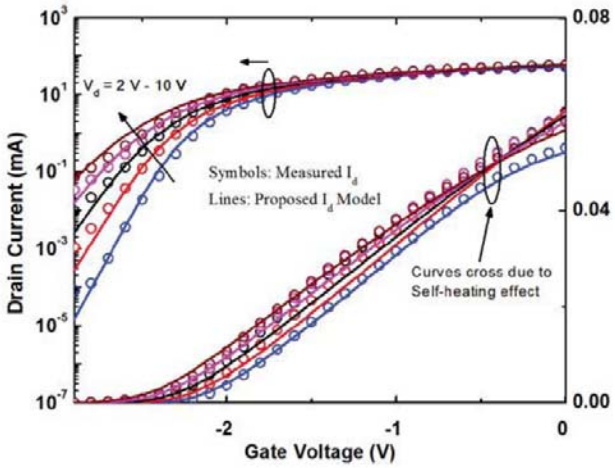
Temperature Model Validation

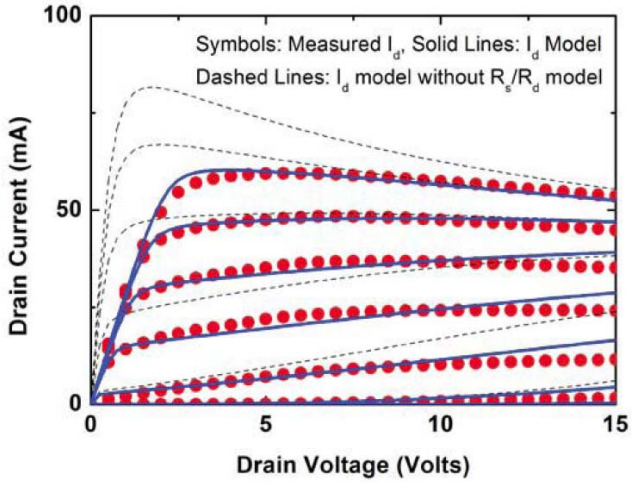
- **Id-Vd at two different temperatures 300 and 573K**

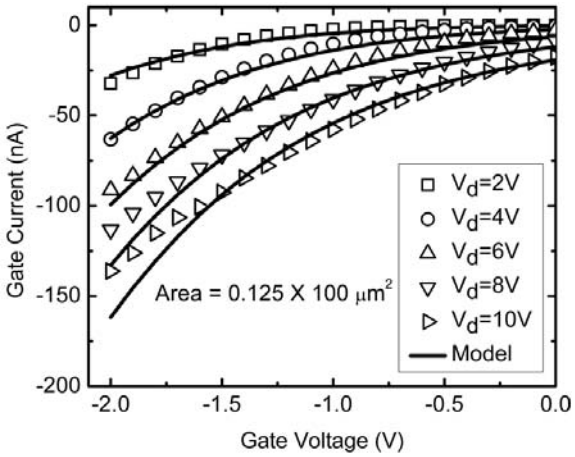




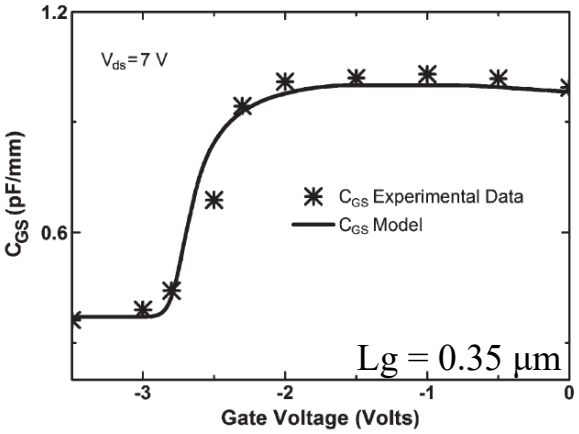
Model Validation – IEMN France data

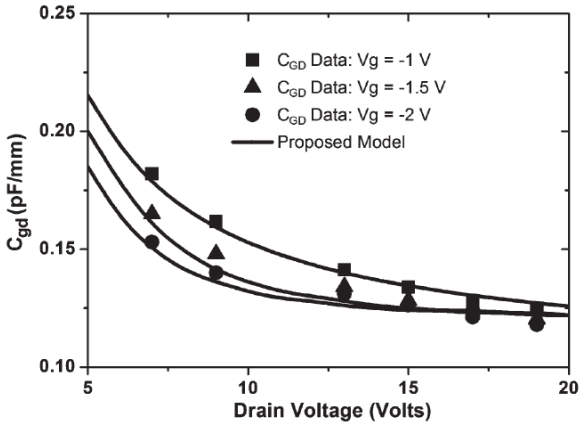


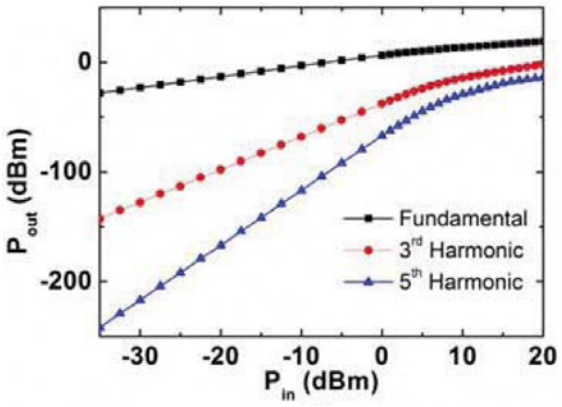




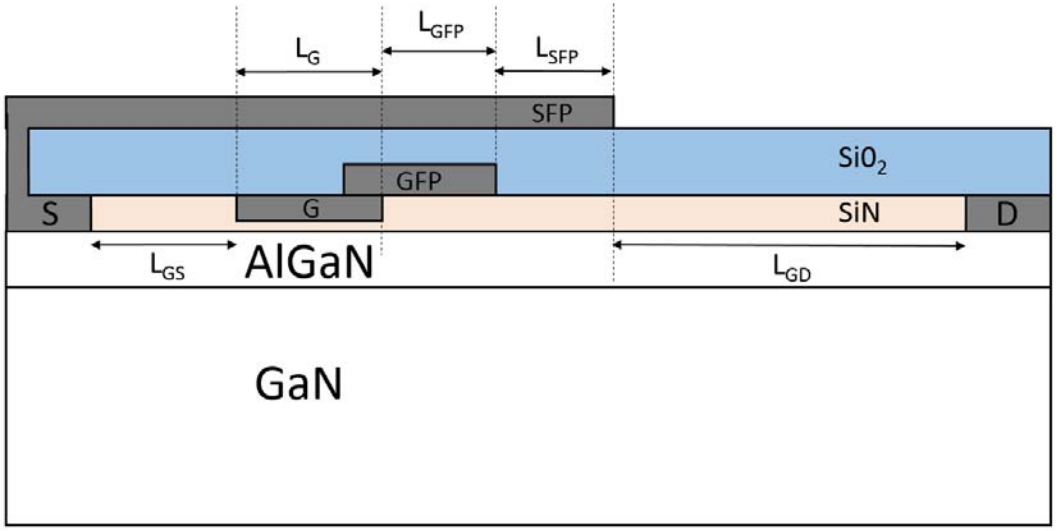
Lg = 0.125 μm, W=100 μm

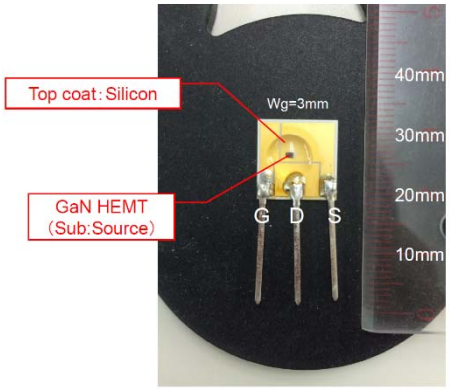


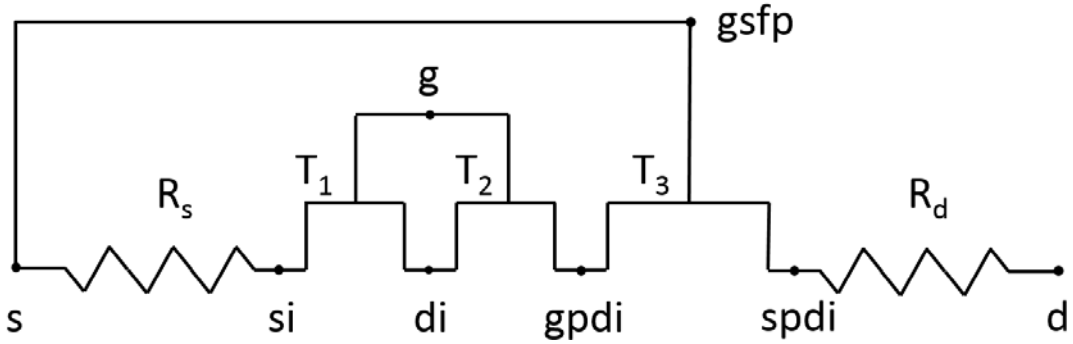




Modeling of Field-Plates in HEMTs

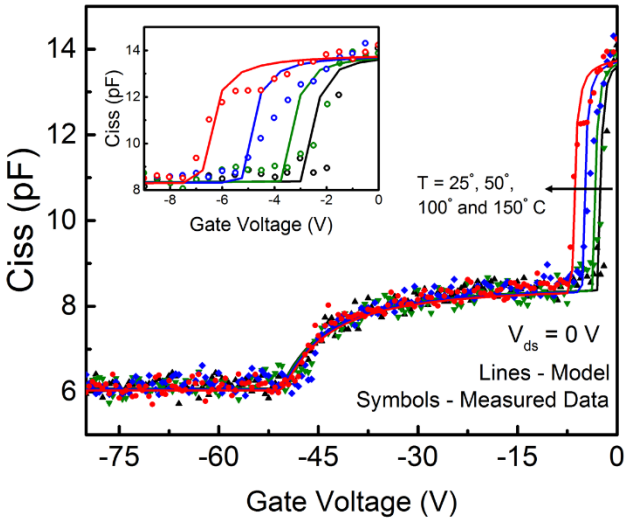


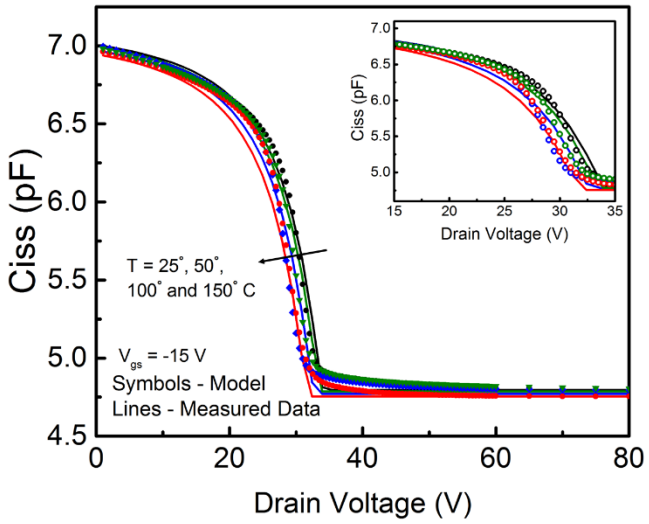


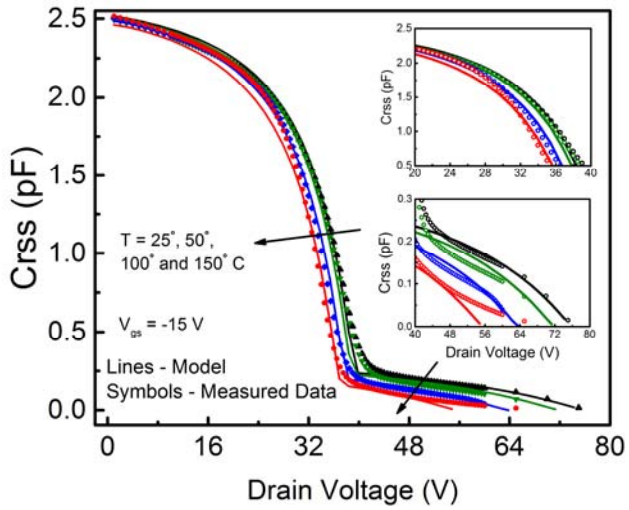


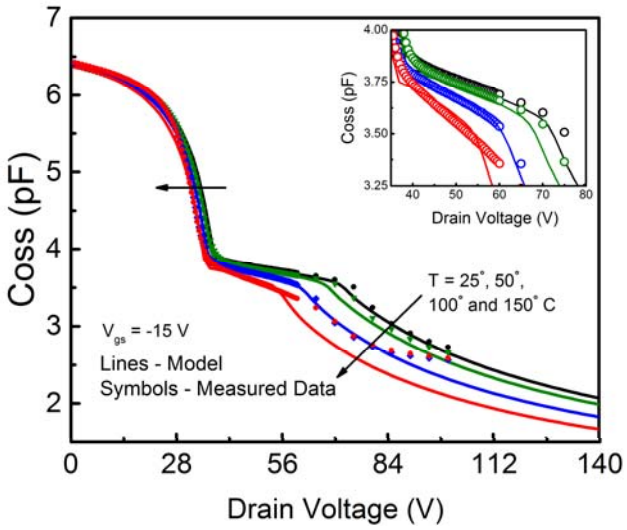
Affects capacitance and breakdown behavior.

Field-Plate Capacitance Modeling

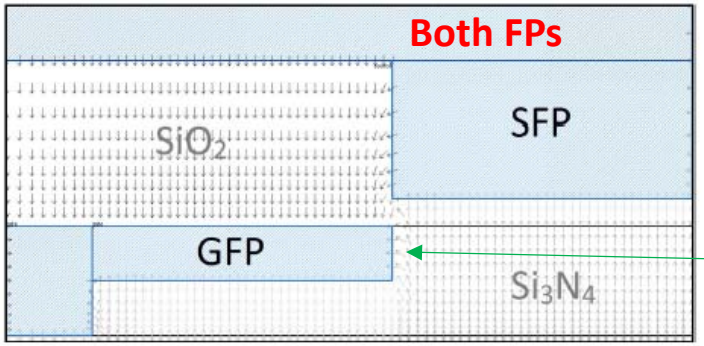




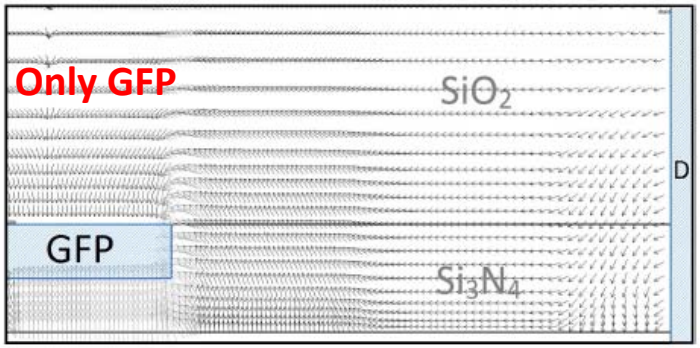




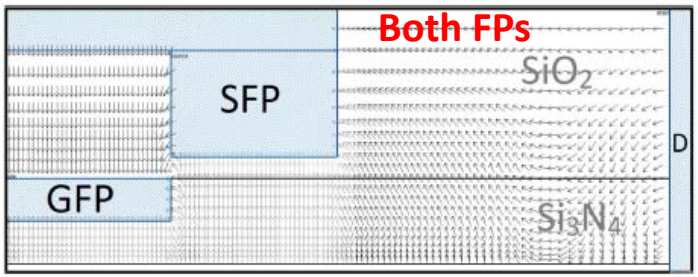
Cross-Coupling Capacitance



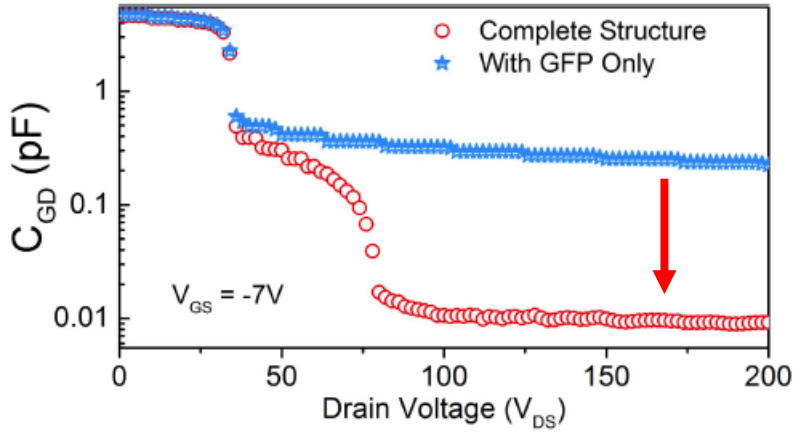
(a)



(b)



(c)



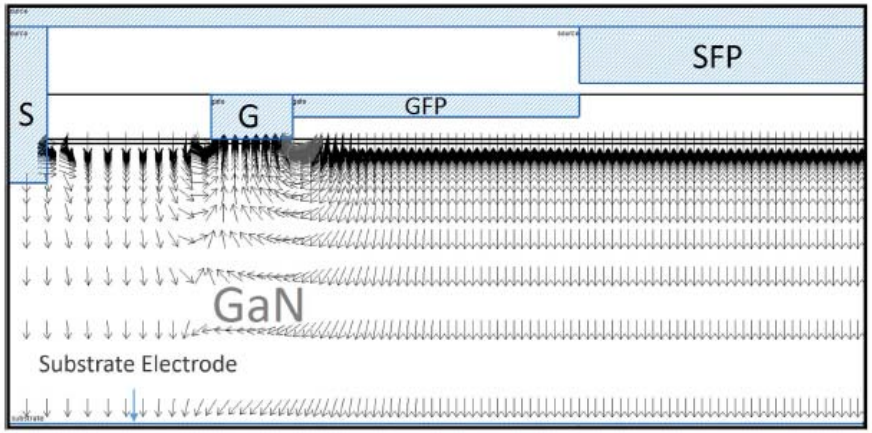
Appearance of fringing electric field between the vertical wall of the GFP and the 2-DEG$_{SFP}$ causes the cross-coupling effect giving rise to the second plateau

Significant number of fringing field lines reach the GFP through the insulator stack in the absence of SFP causing more fringing capacitance

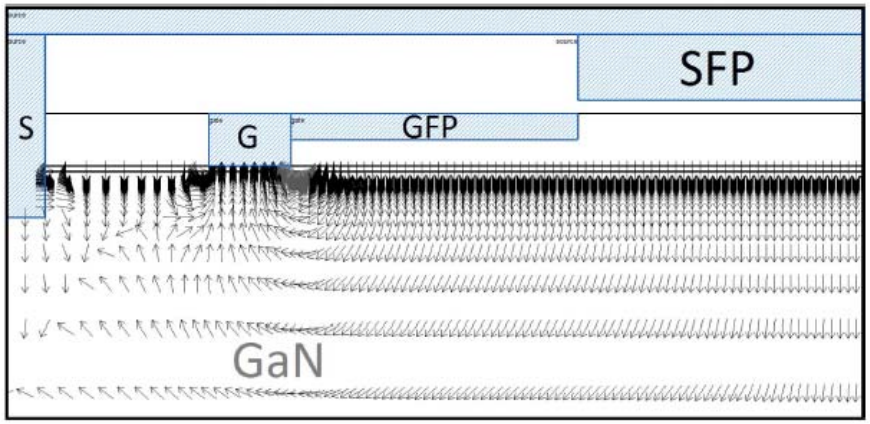
In the presence of the SFP, most of them end up at the SFP leading to a reduced fringing capacitance component in C_{gd}

Substrate Capacitance

Vgs = −7 V Vds = 20 V



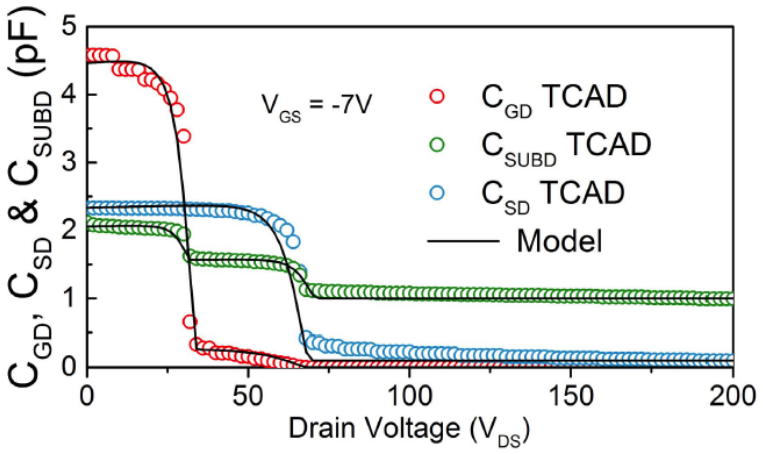
(a)



(b)

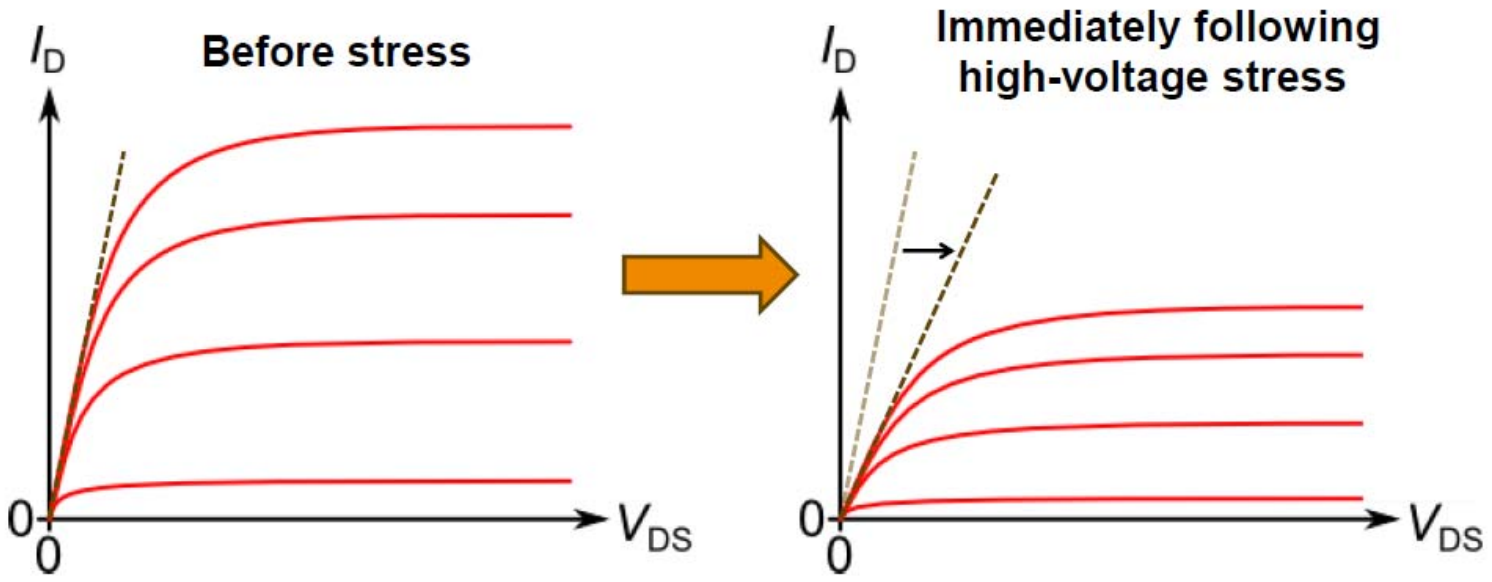
(a) Field lines originating from the 2-DEG reach the substrate electrode leading to the existence of C_{SUBD}

(b) whereas without substrate node, field lines from the drain side of the 2-DEG terminate at the 2-DEG on the source side through the GaN buffer



Current Collapse

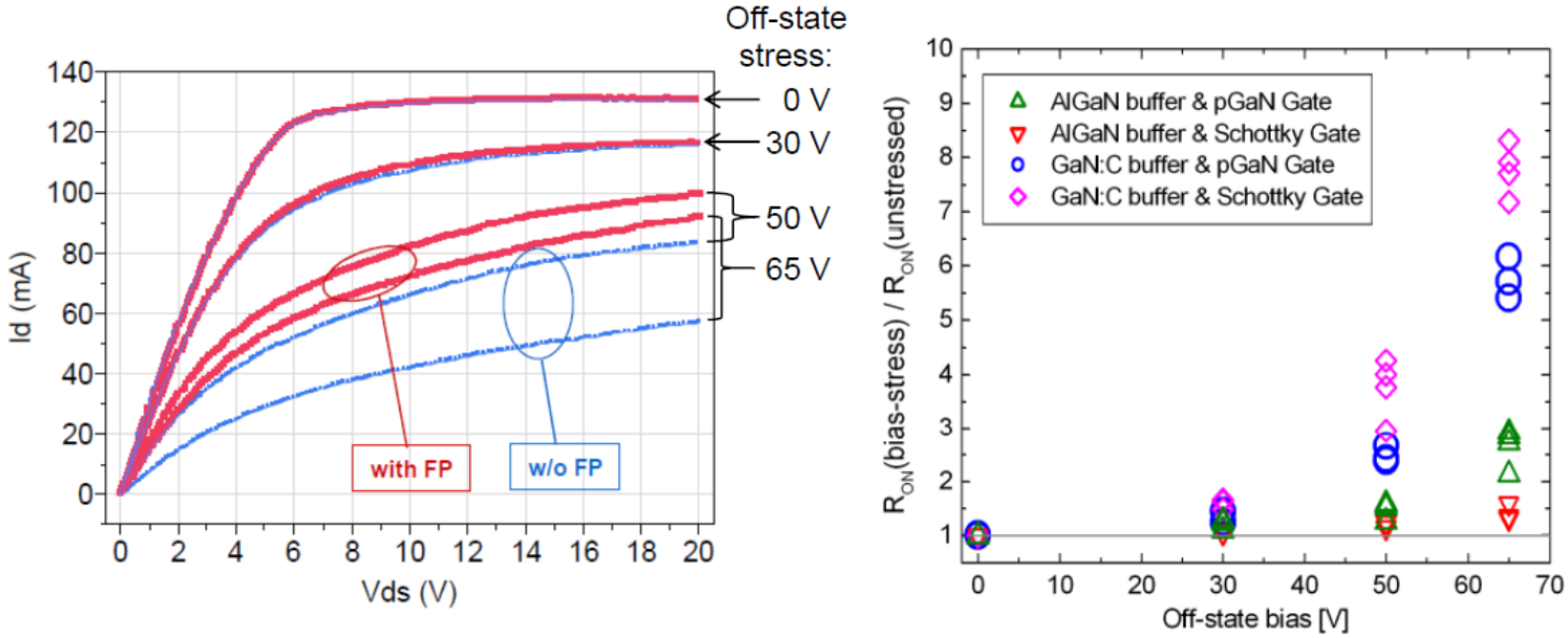
- On-state current temporarily reduced following off-state stress



- Also known as **dynamic R_{on}**
  - On-state resistance depends on recent history of device biasing

Current Collapse

- Device design and substrate composition can have a strong influence on the magnitude of current collapse (dynamic-R_{on} increase)

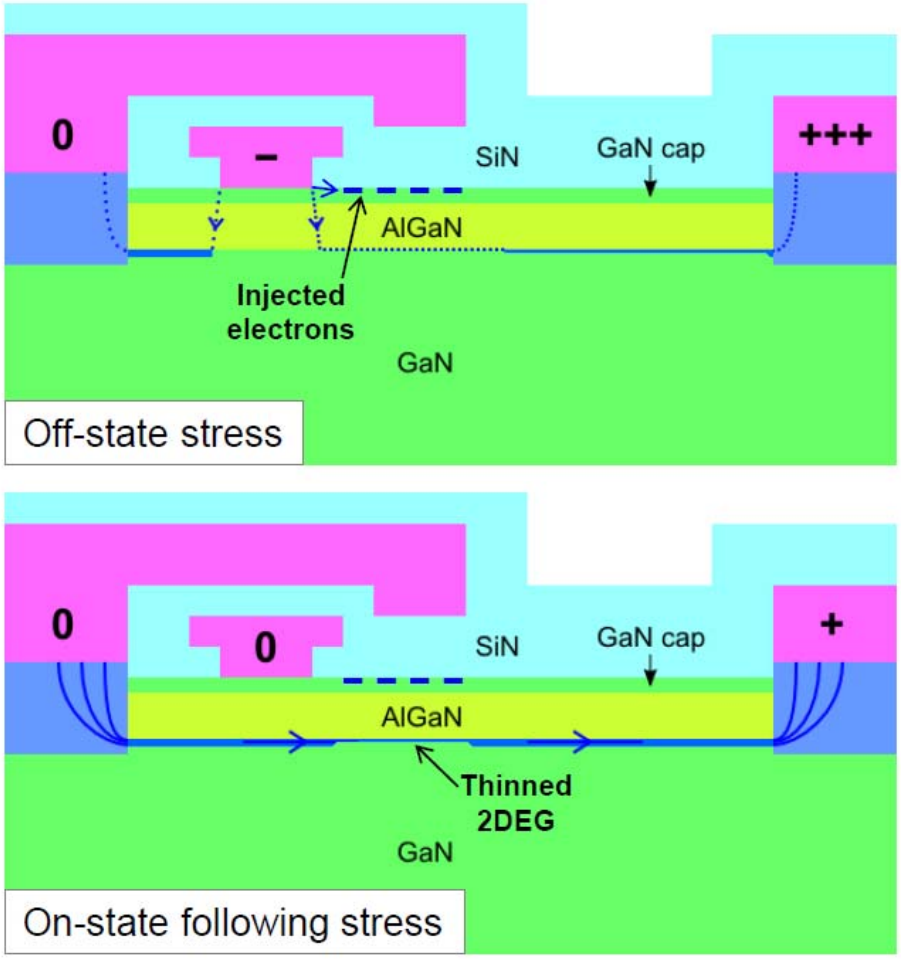


[O. Hilt *et al.*, Proc. ISPSD 2012, 345 (2012)]

[S. DasGupta et al., Appl. Phys. Lett. 101 (24), 243506 (2012)]

Issues-Virtual-gate effect

- **Off-state stress:**
  - Electrons from gate injected into trap states next to gate
- **On-state after stress:**
  - Trapped electrons act like a negatively biased gate
  - 2DEG partially depleted underneath ⇒ increased R_{on}
- **Later (~seconds):**
  - Electrons de-trap, 2DEG current restored

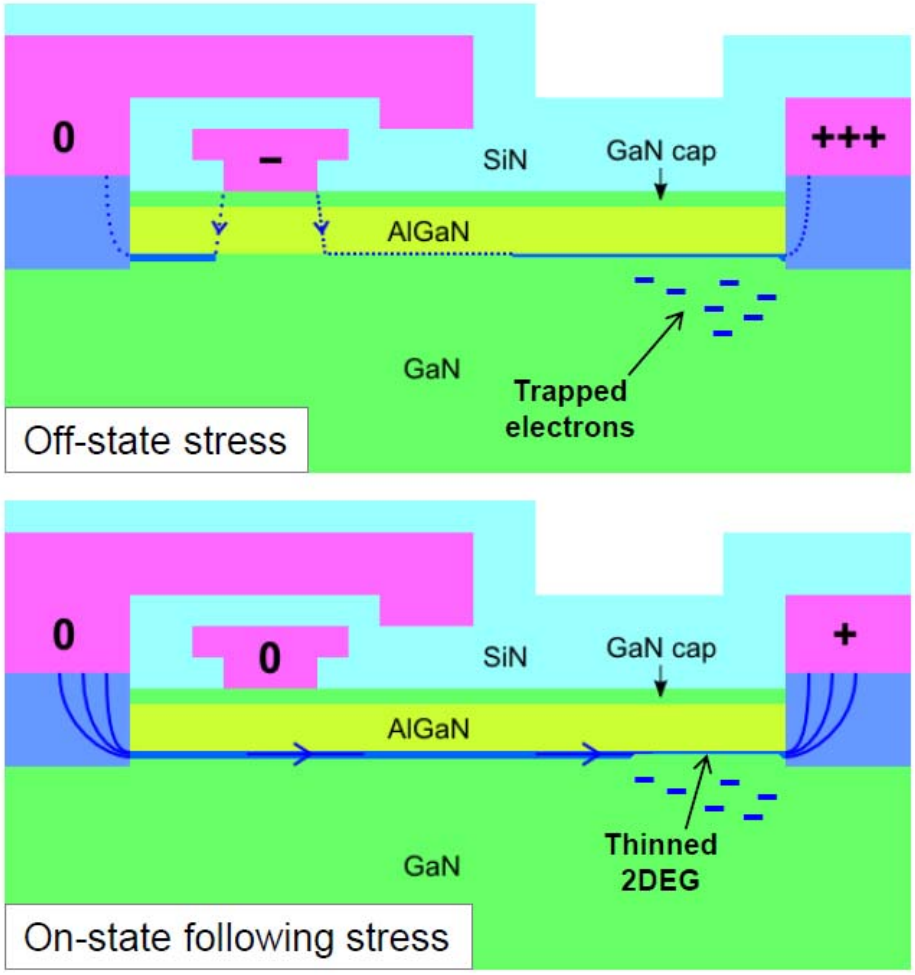


[R. Vetury *et al.*, Trans. Elec. Dev. **48 (3)**, 560 (2001)]
[T. Mizutani *et al.*, TED **50**, 2015 (2003)]

Issues-Buffer trapping

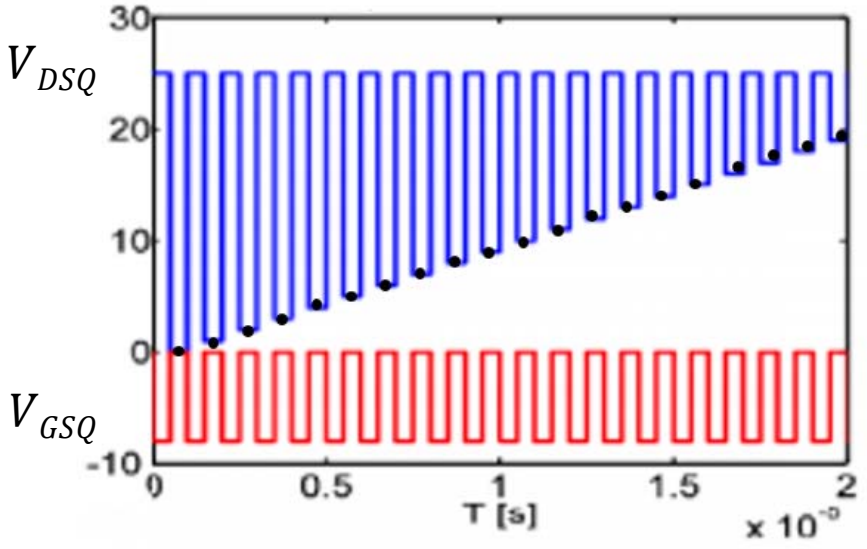
- **Off-state stress:**
  - Electrons trapped in bulk (deep donors/acceptors?)
- **On-state after stress:**
  - Trapped electrons partially deplete the 2DEG above ⇒ increased R_{on}
- **Later (~minutes):**
  - Electrons de-trap, 2DEG current restored

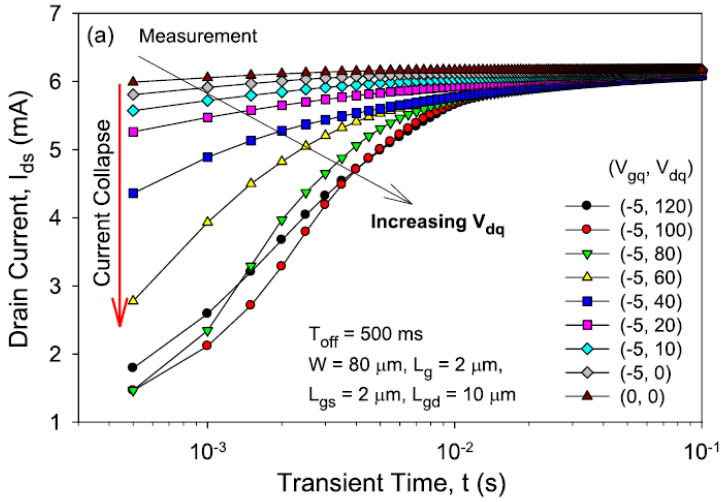
[M. J. Uren *et al.*, Trans. Elec. Dev. **59 (12)**, 3327 (2012)] and refs. therein

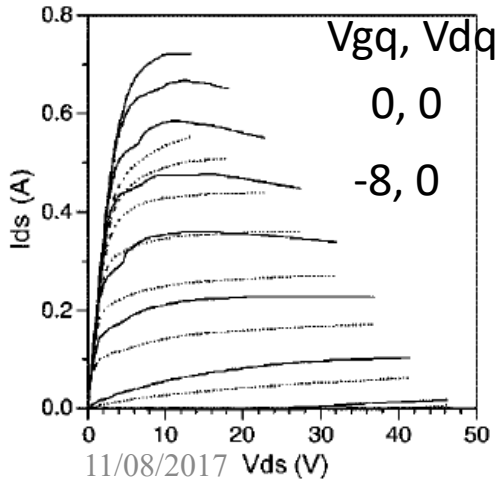


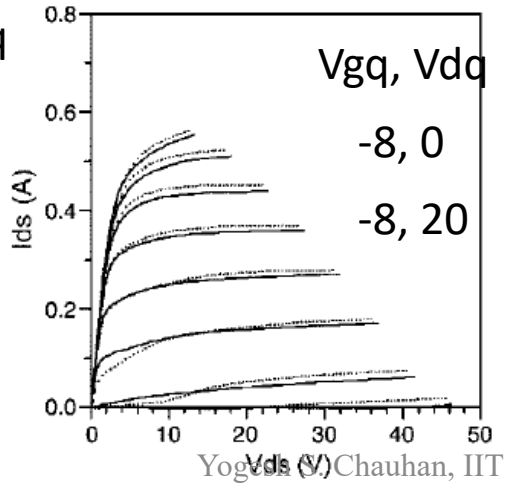
[E. Kohn et al., Trans. Microw. Theory Tech. 51 (2), 634 (2003)]

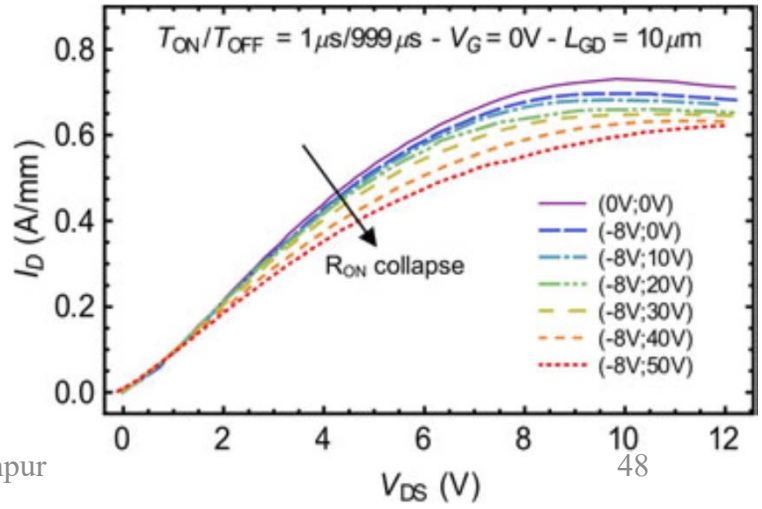
Pulsed IV Measurements



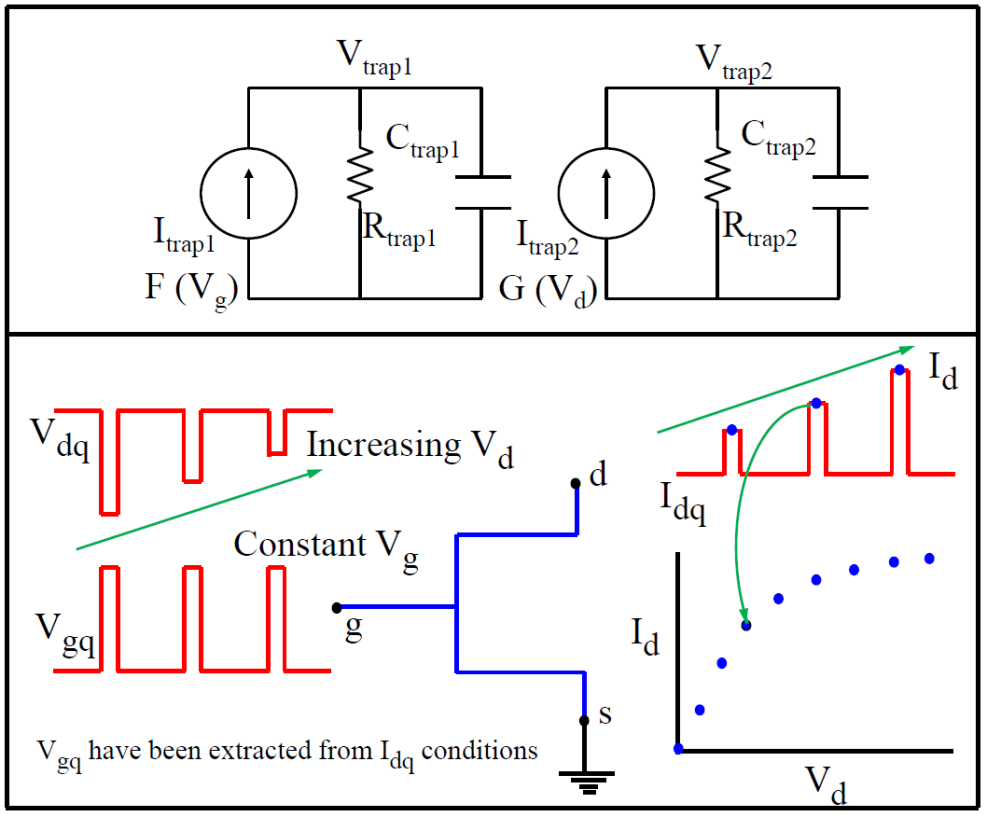








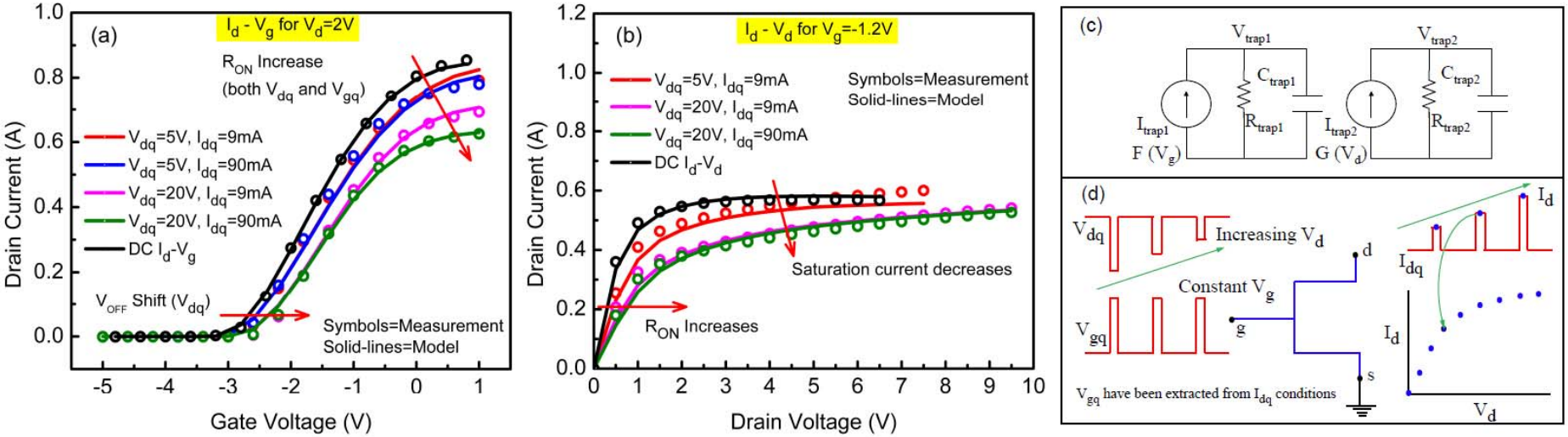
Trap Model and Pulsed IV Scheme



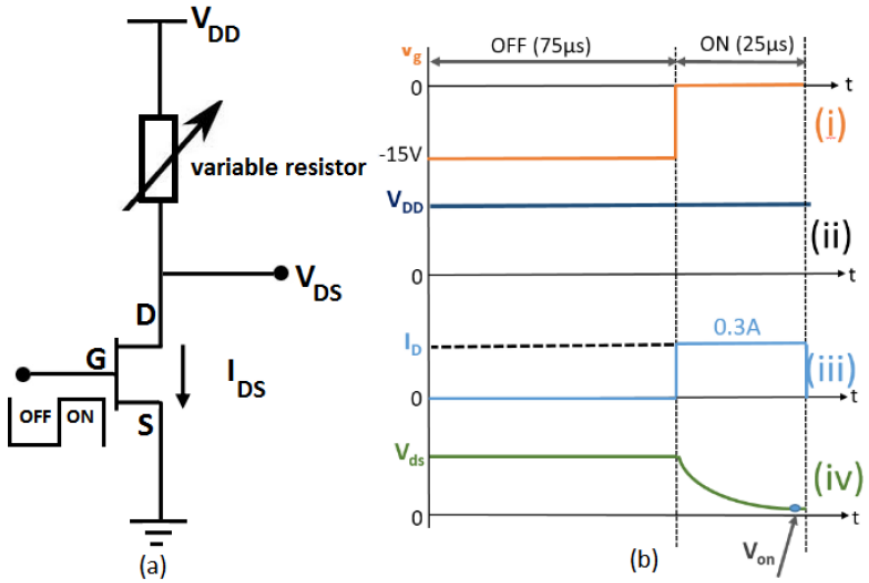
The trapping effects are modeled with the help of two R-C sub-circuits. The generated trap voltages V_{trap1} and V_{trap2} are fed back into the model which update parameters like the cut-off voltage, sub-threshold slope, source and drain-resistances to capture the effects of traps.

Modeling of Trapping effect

Traps in GaN HEMTs play huge role in determining the performance of the device, especially in high frequency operations



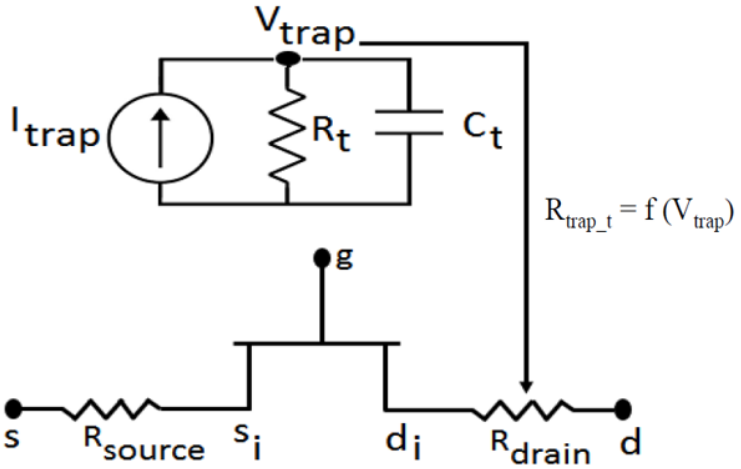
Switching Collapse Setup



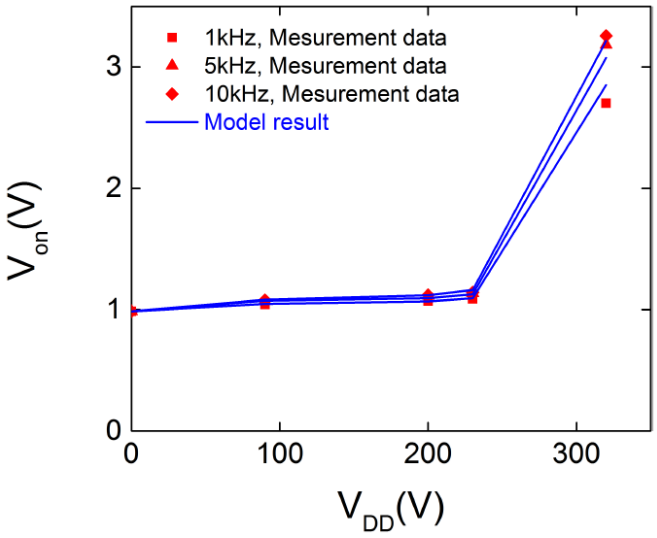
Signal generator at gate terminal switches device from high negative stress voltage (Vgsq) to some value higher than Voff . Variable resistor is used to make device working in linear region of operation.

- Waveform (i) is the input at the gate, which is switching the device from ON to OFF-state and vice versa. Waveform (ii) is the constant input applied at drain terminal via a variable resistor.
- Waveform (iii) is showing the output drain current with time. The drain current is kept fixed at 0.3A with the help of variable resistor.
- Waveform (iv) is the value of Vds which is equal to VDD when device is in OFF-state and becomes Von when device is in ON-state.
- Waveform (iv) illustrates the fact that, as the device is turning ON, capacitor assumed for the trap-states start to discharge and due to reduction in depletion of 2-DEG, Von of the device recovers with time.

Switching Collapse Model



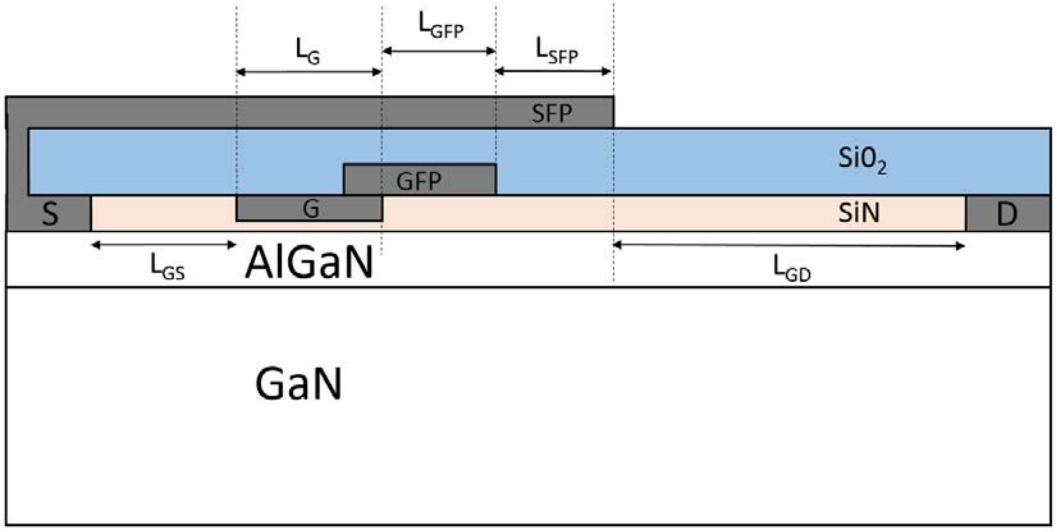
Strategy for implementation of surface trapping effect using an RC network

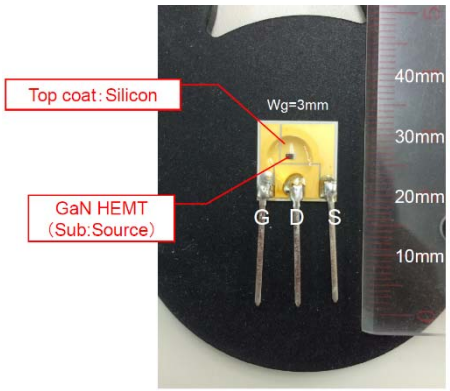


- Modeling of trapping effect by using RC network with different time constant. This RC network is contributing to drain-access region resistance as Rtrap (as a function of Vtrap) to capture the trapping effect on device ON-resistance (Ron)

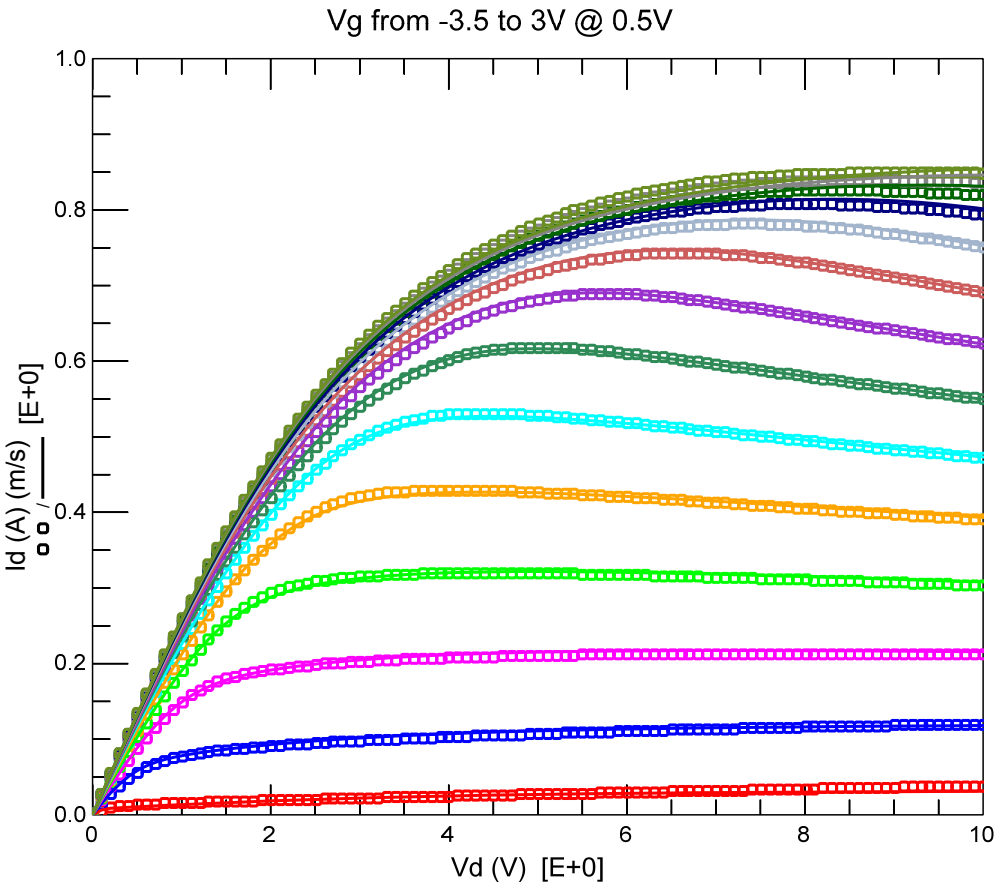
- Model-Hardware correlation for pulsed I-V, Von data for 1, 5 and 10 kHz input applied at gate terminal for various Vds. Von is the value of Vds at which the value of drain current is 0.3A. As VDD is increasing, Ron of the device increases which results in switching collapse. Measured data is from Toshiba for CMC standardization.

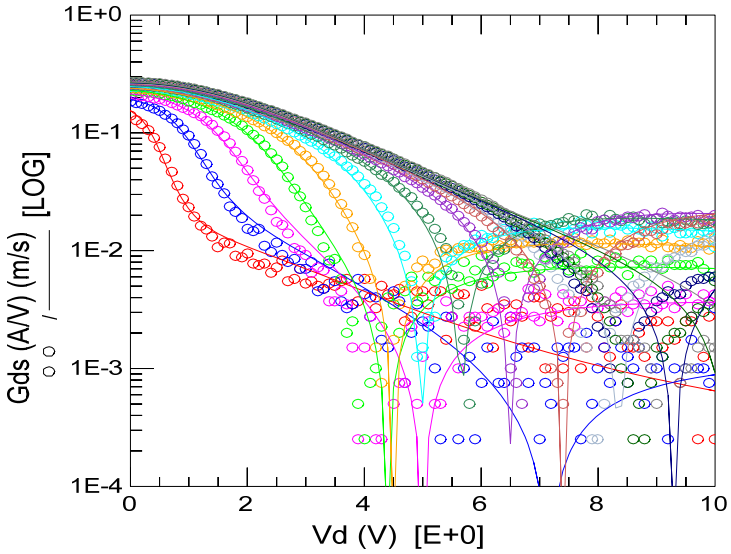
Toshiba DC I-V Results for High Power HEMT

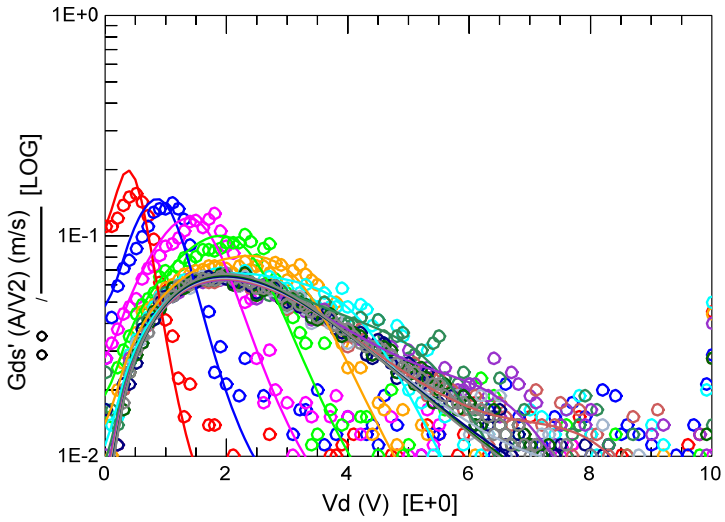




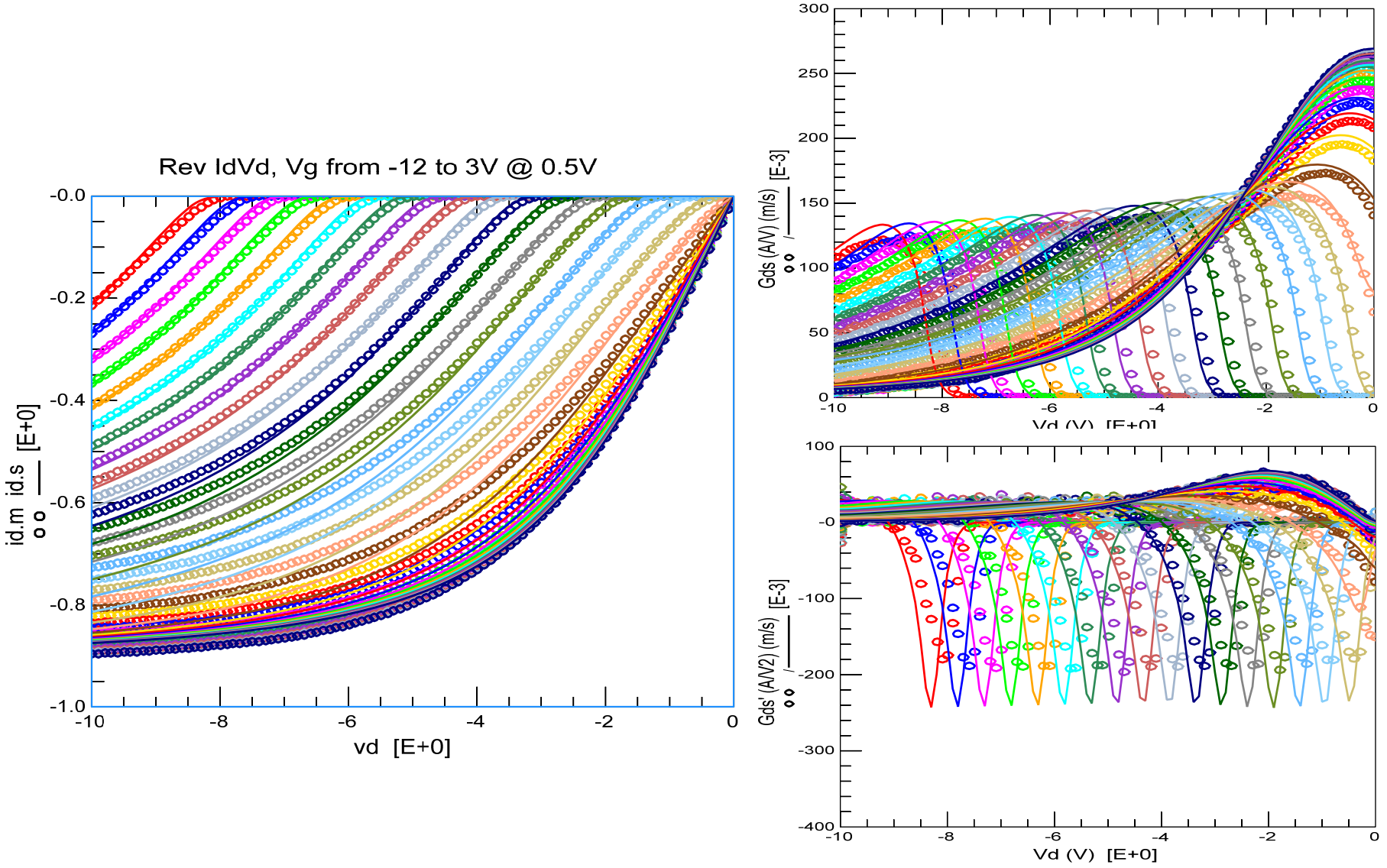
Room Temperature I-V



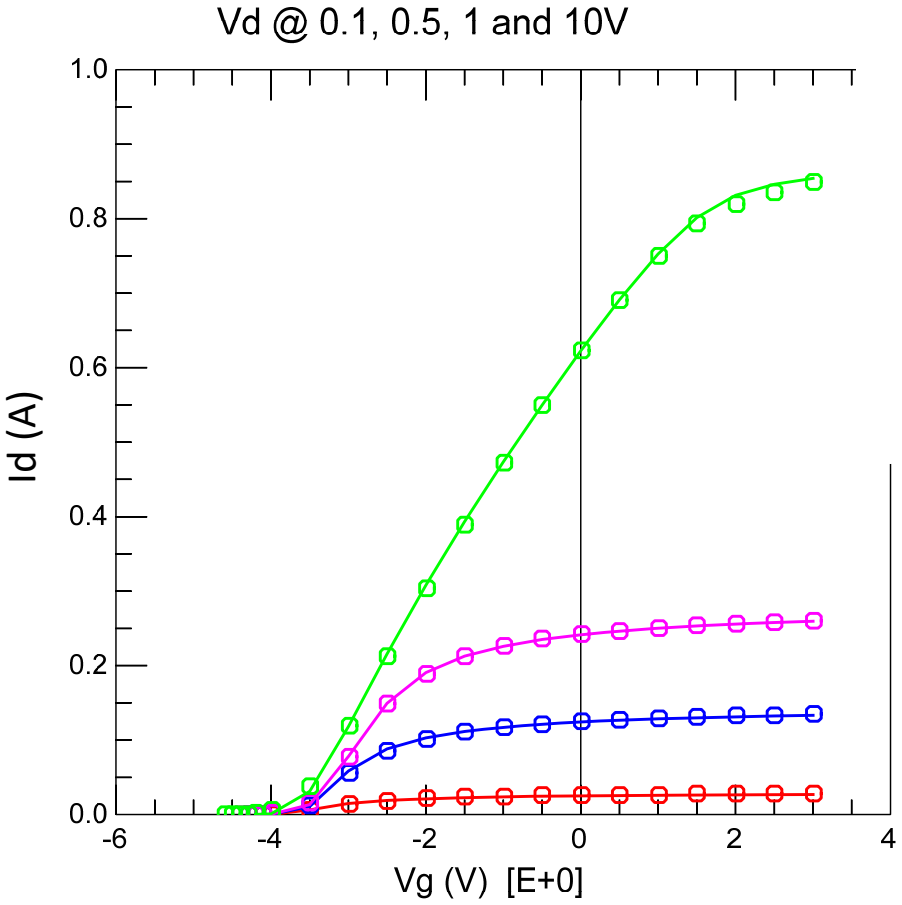


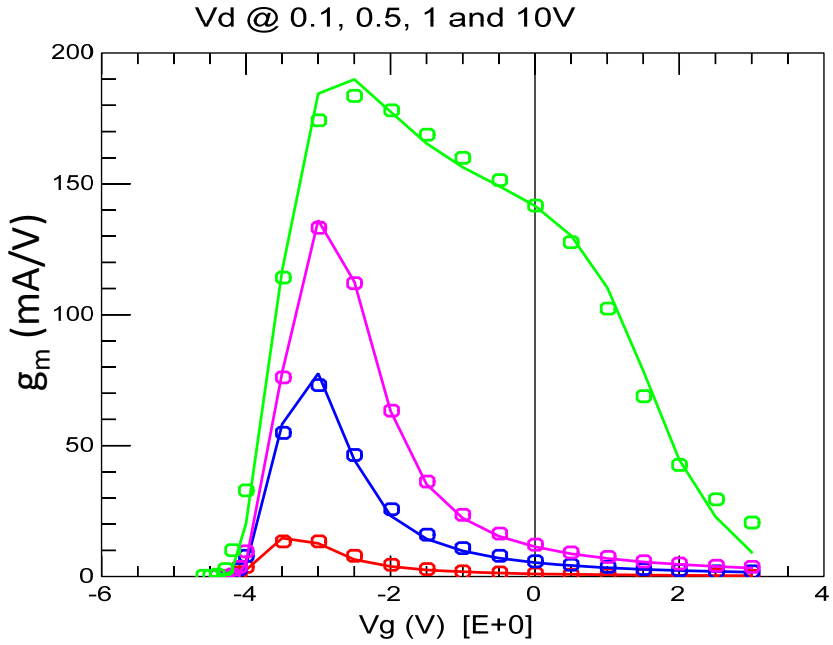


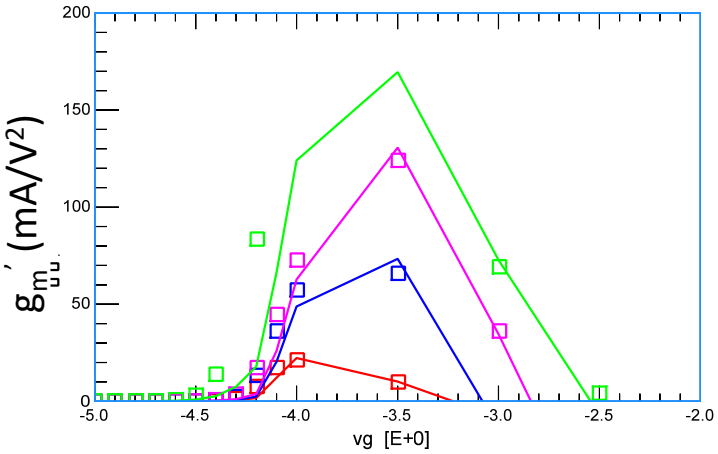
Reverse IdVd @ room temperature



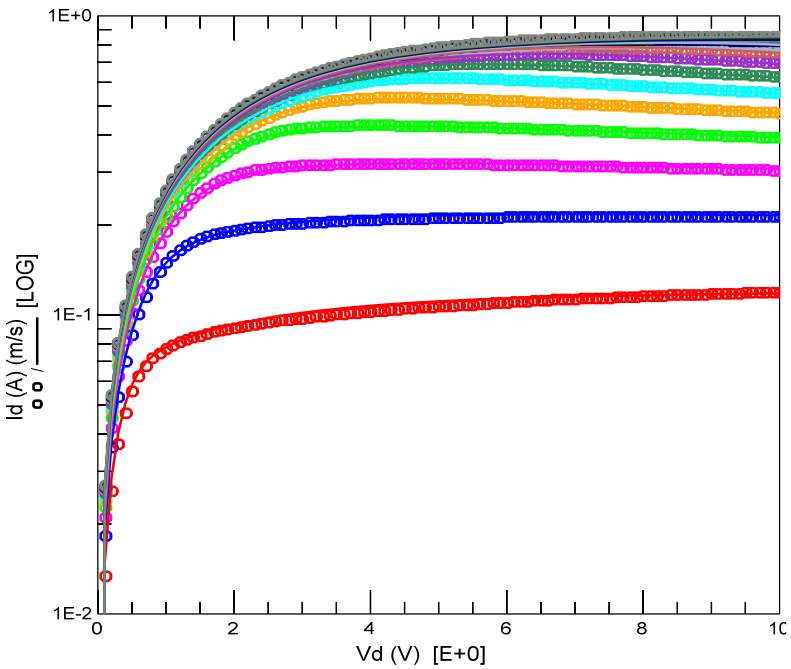
Room Temperature I-V



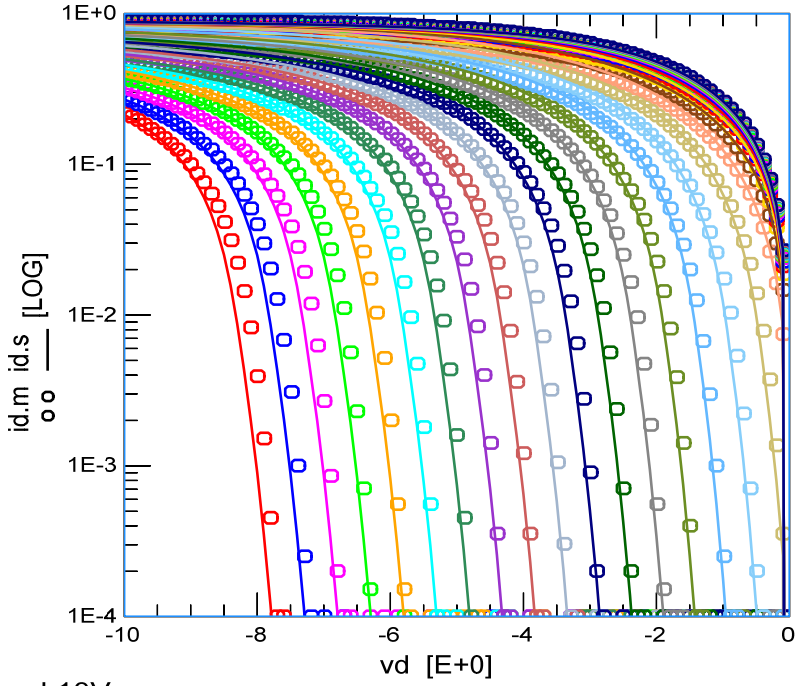


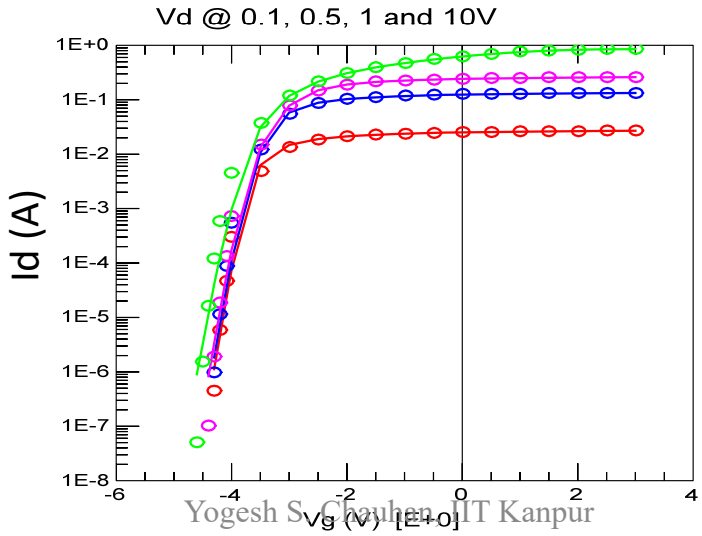


Log (Id) - Vds (Vd>0) T=25



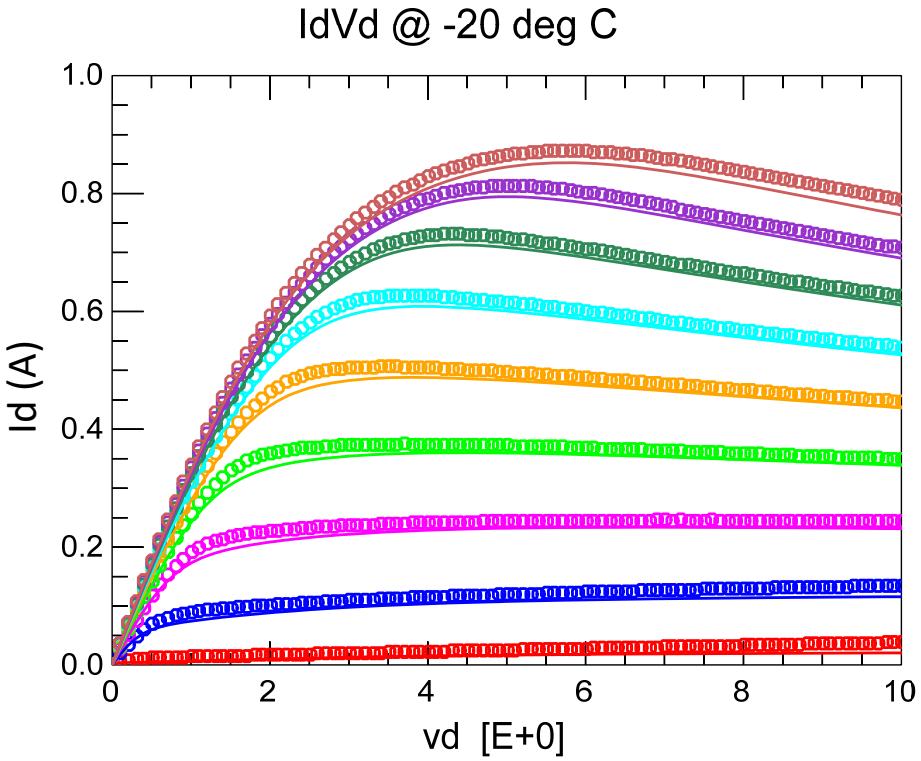
Log (Id) - Vds (Vd<0) T=25

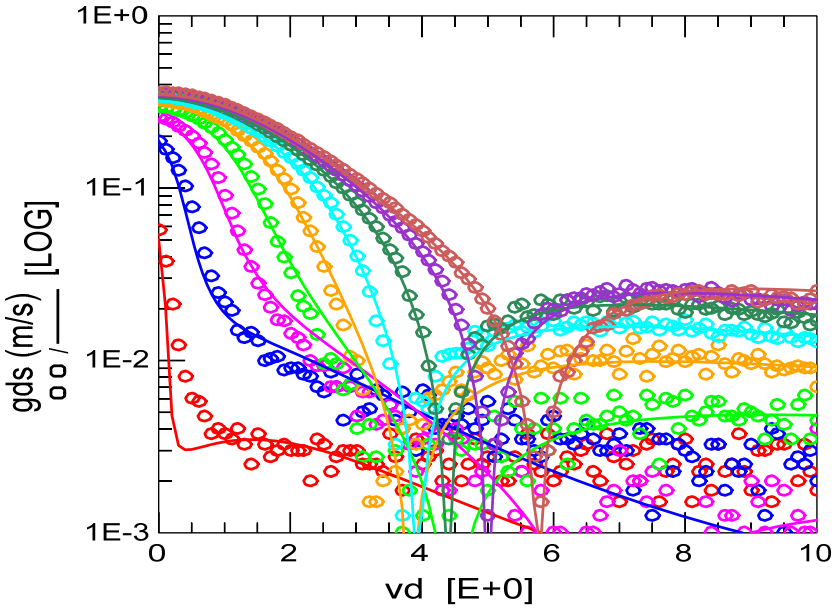


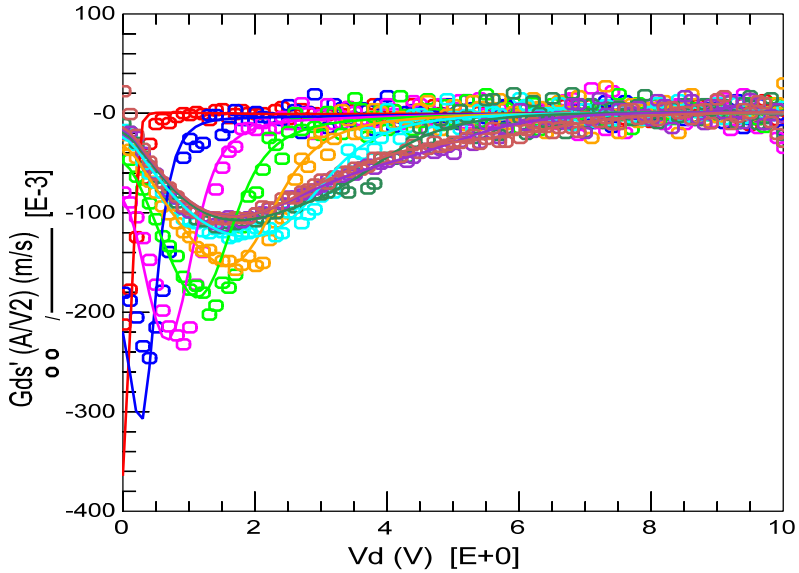


Log (Id) - Vgs T=25

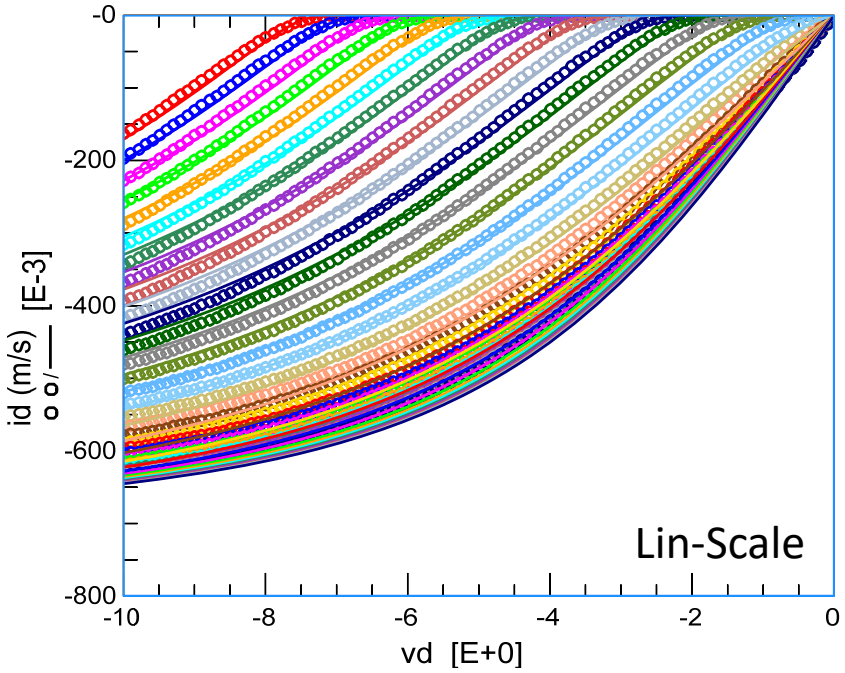
I-V @ -20 deg C

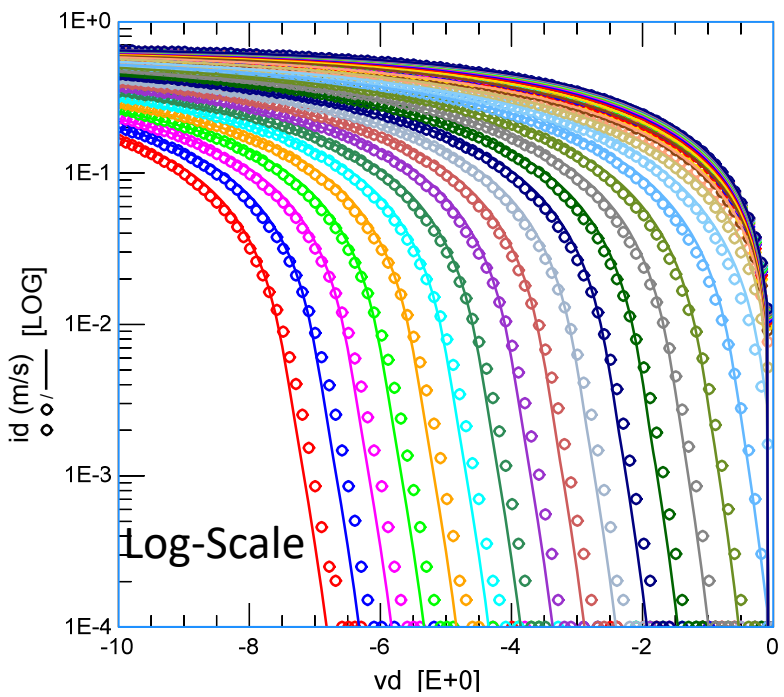

IdVd @ -20 deg C
Id (A)
vd [E+0]
1.0
0.8
0.6
0.4
0.2
0.0
0
2
4
6
8
10

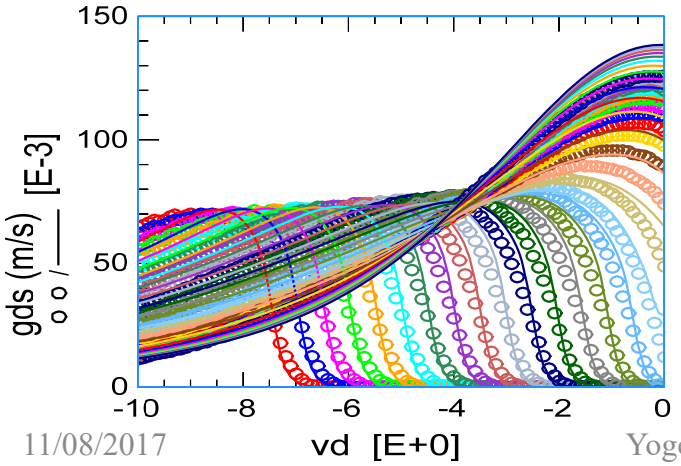

gds (m/s) / oo [LOG]
vd [E+0]
1E+0
1E-1
1E-2
1E-3
0
2
4
6
8
10

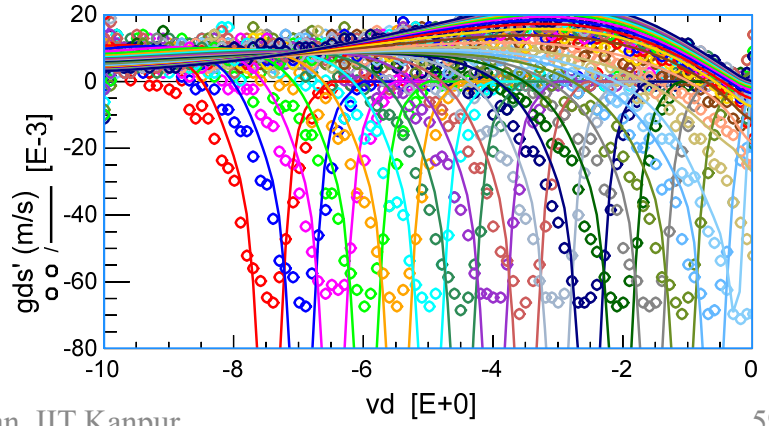

Gds' (A/V2) (m/s) / oo [E-3]
Vd (V) [E+0]
100
-0
-100
-200
-300
-400
0
2
4
6
8
10

Rev IdVd @ T=150 C



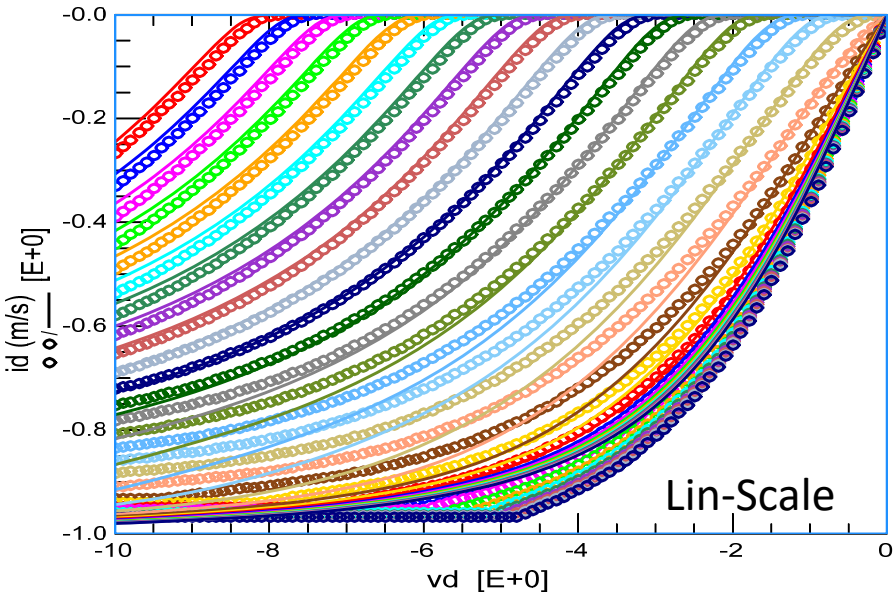


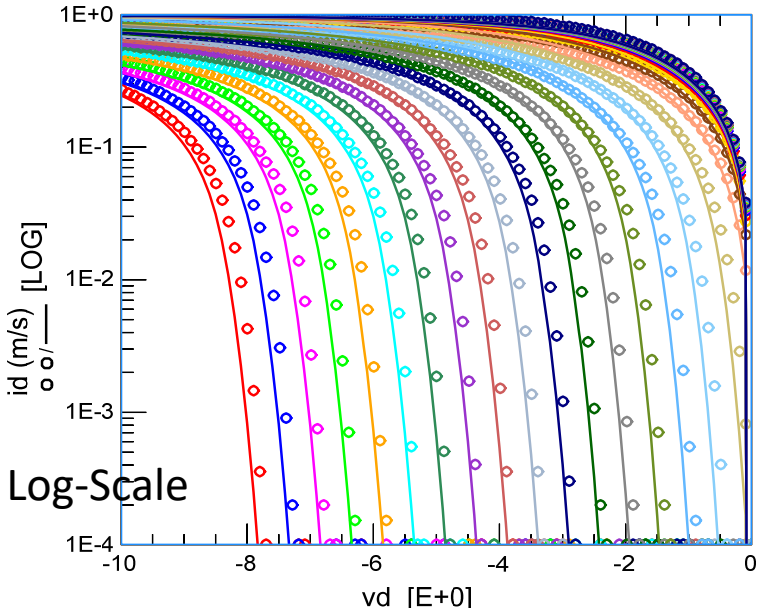


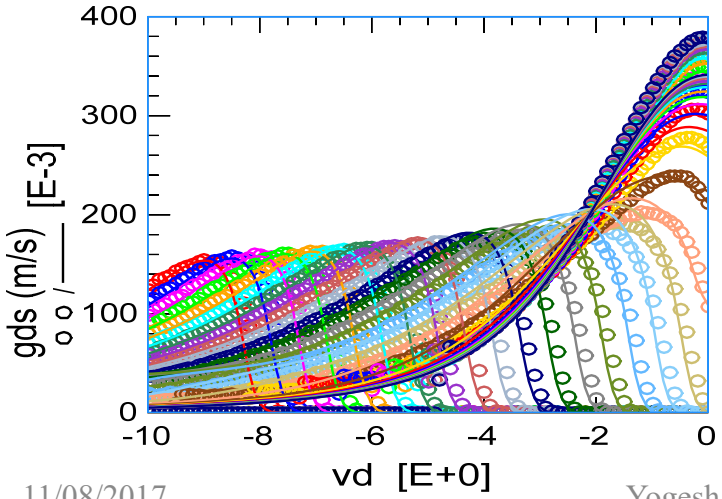


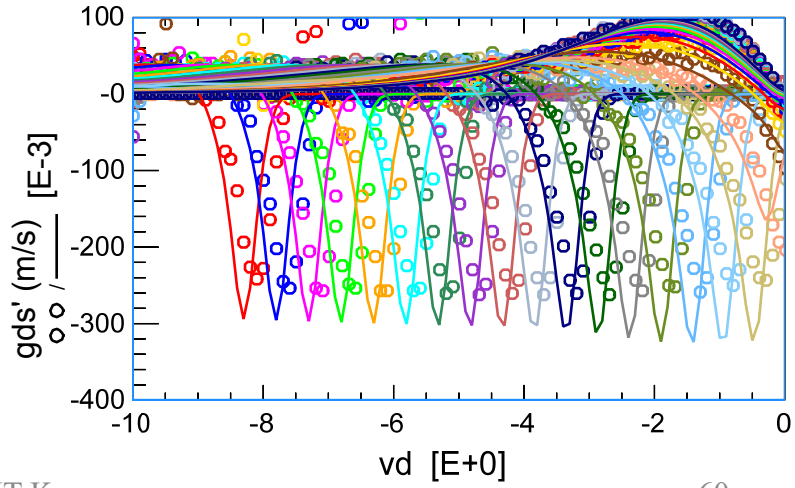
Rev IdVd @ T=-20 C

Vg from -12 to 6 V @ 2.5V step

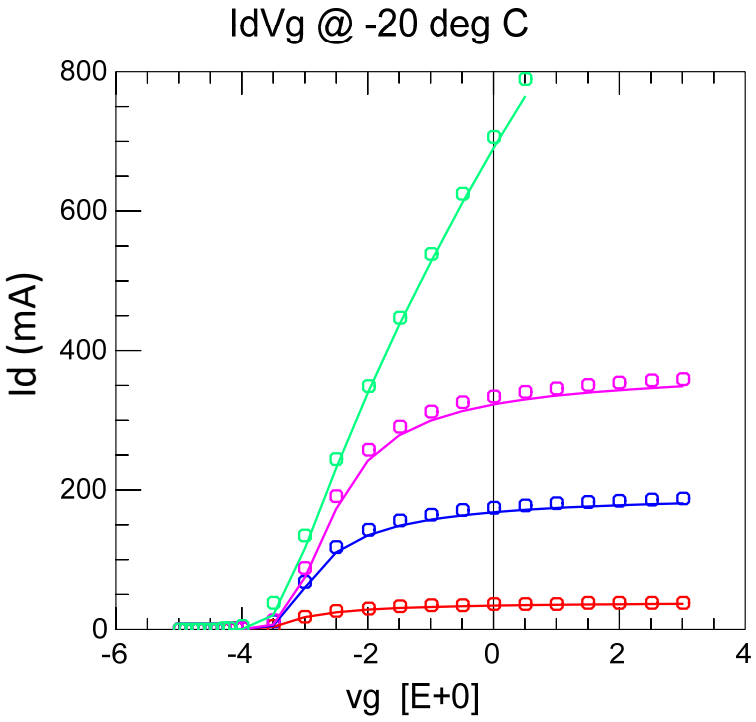


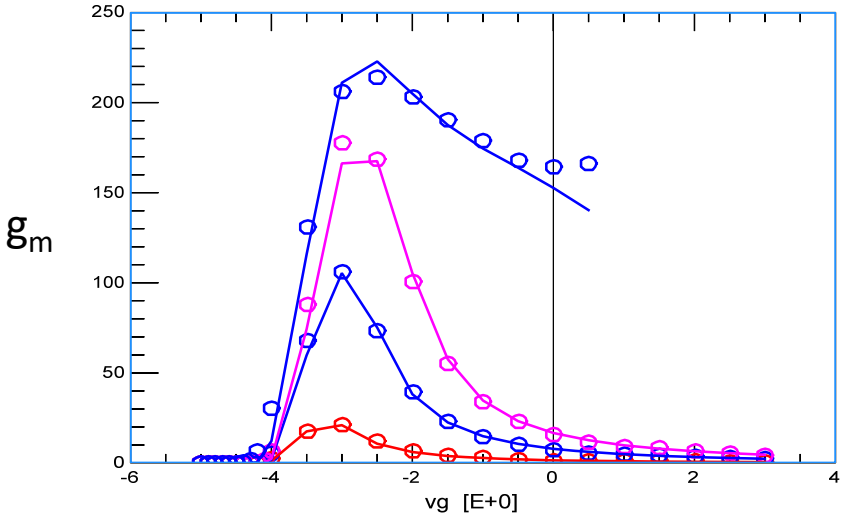


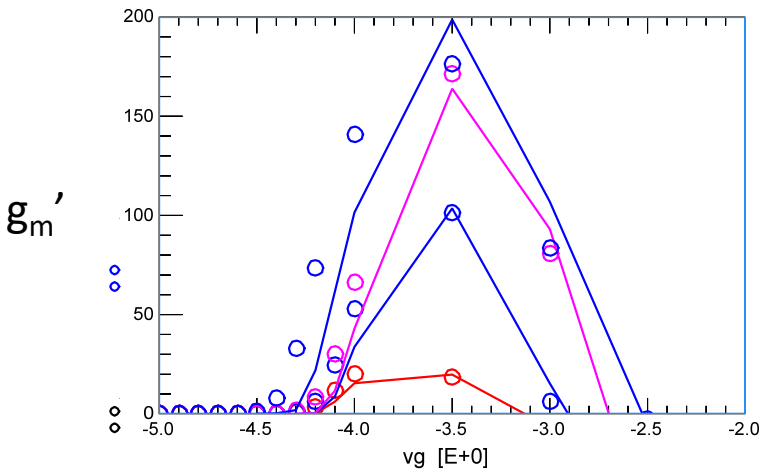




I-V @ -20 deg C

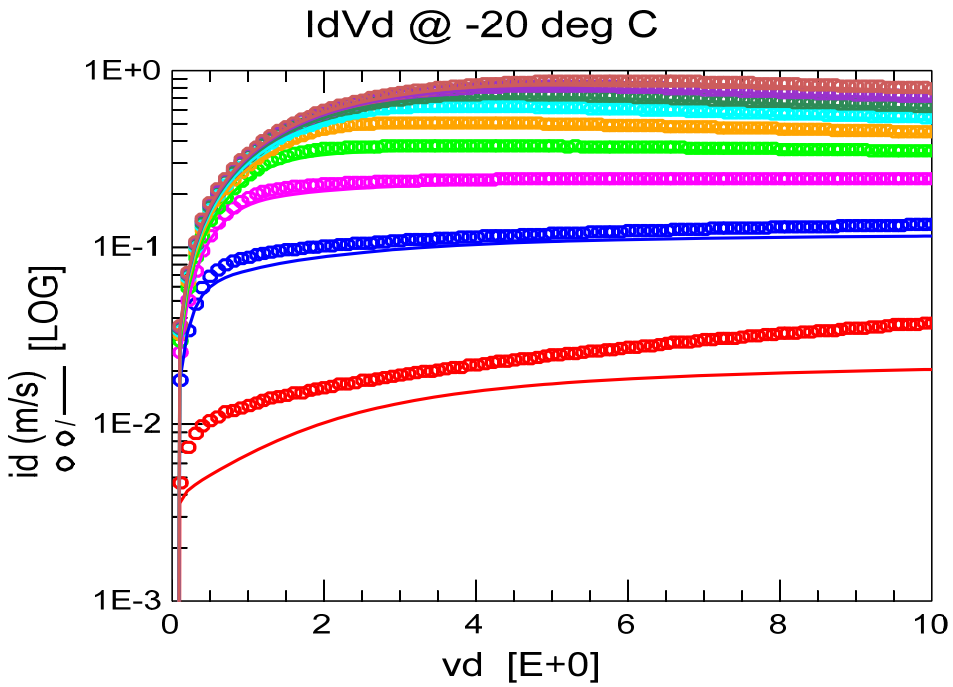

IdVg @ -20 deg C
Id (mA)
800
600
400
200
0
-6
-4
-2
0
2
4
vg [E+0]

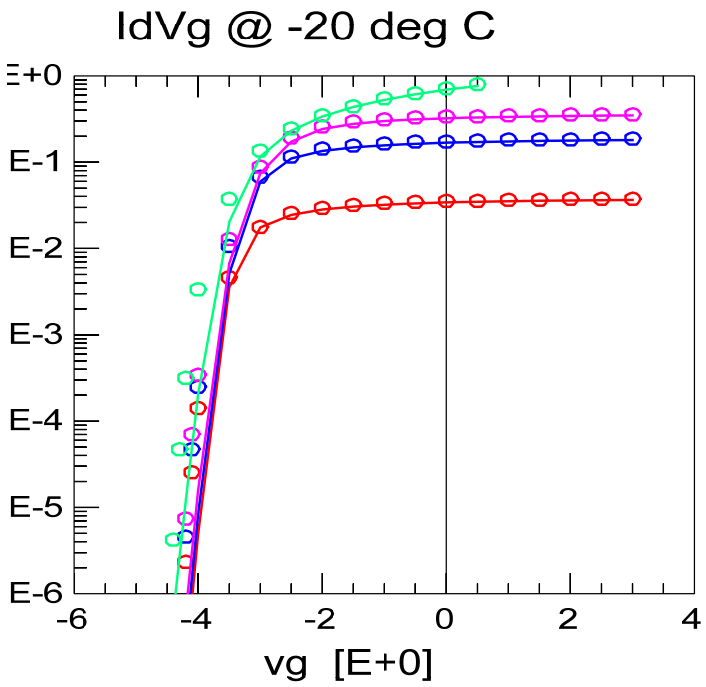

g_m
250
200
150
100
50
0
-6
-4
-2
0
2
4
vg [E+0]


g_m'
200
150
100
50
0
-5.0
-4.5
-4.0
-3.5
-3.0
-2.5
-2.0
vg [E+0]

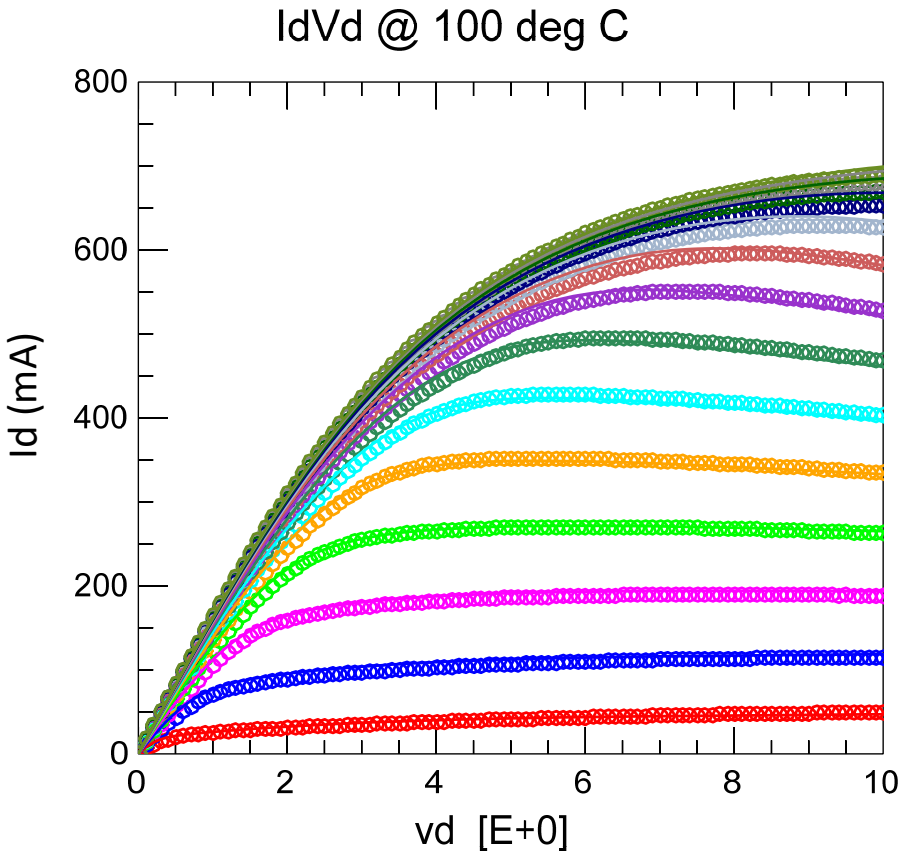
I-V @ -20 deg C

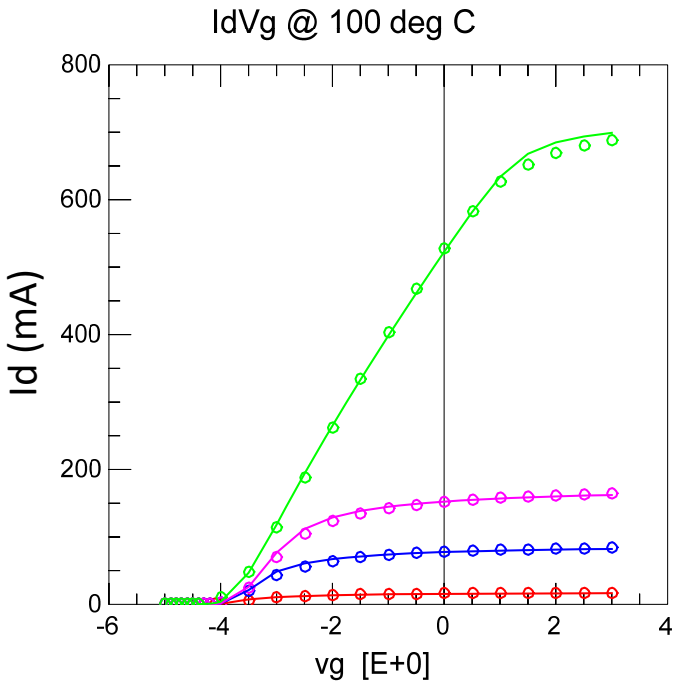
Log -Scale

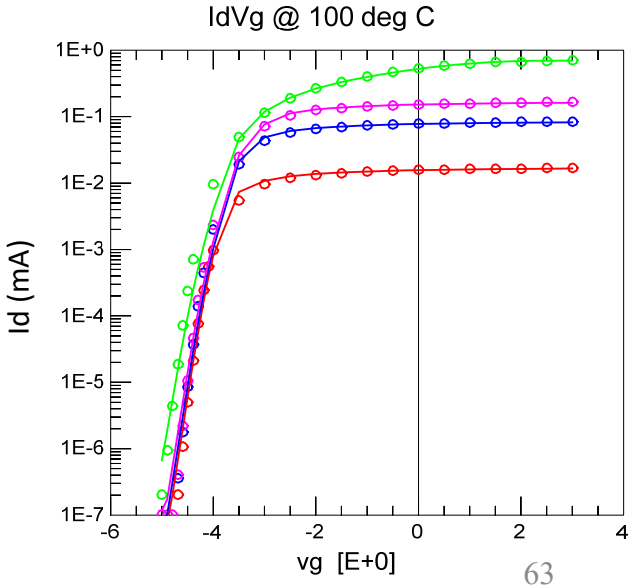




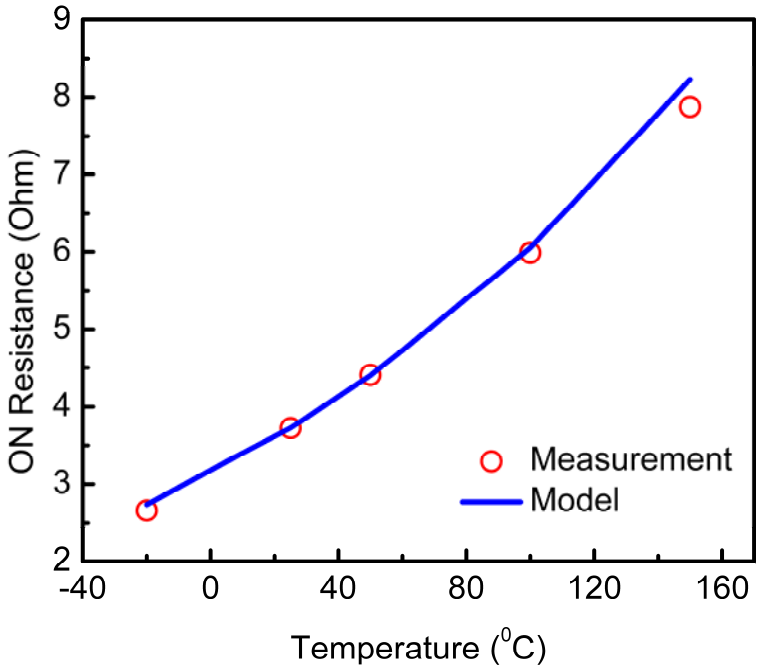
I-V @ 100 deg C

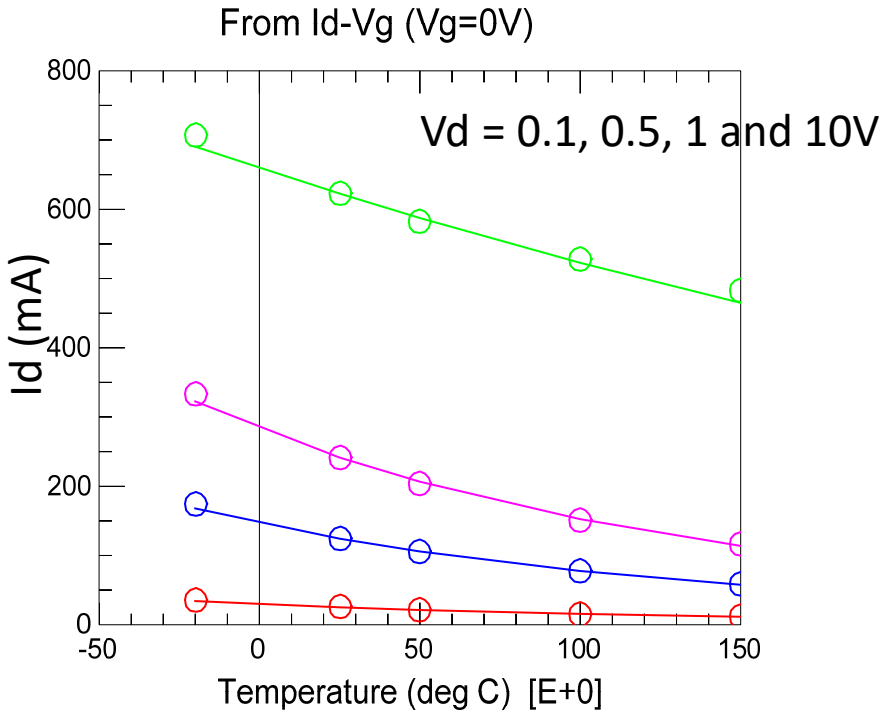

IdVd @ 100 deg C
Id (mA)
vd [E+0]
0
200
400
600
800
0
2
4
6
8
10


IdVg @ 100 deg C
Id (mA)
vg [E+0]
0
200
400
600
800
-6
-4
-2
0
2
4


IdVg @ 100 deg C
Id (mA)
vg [E+0]
1E+0
1E-1
1E-2
1E-3
1E-4
1E-5
1E-6
1E-7
-6
-4
-2
0
2
4

Temperature Scaling

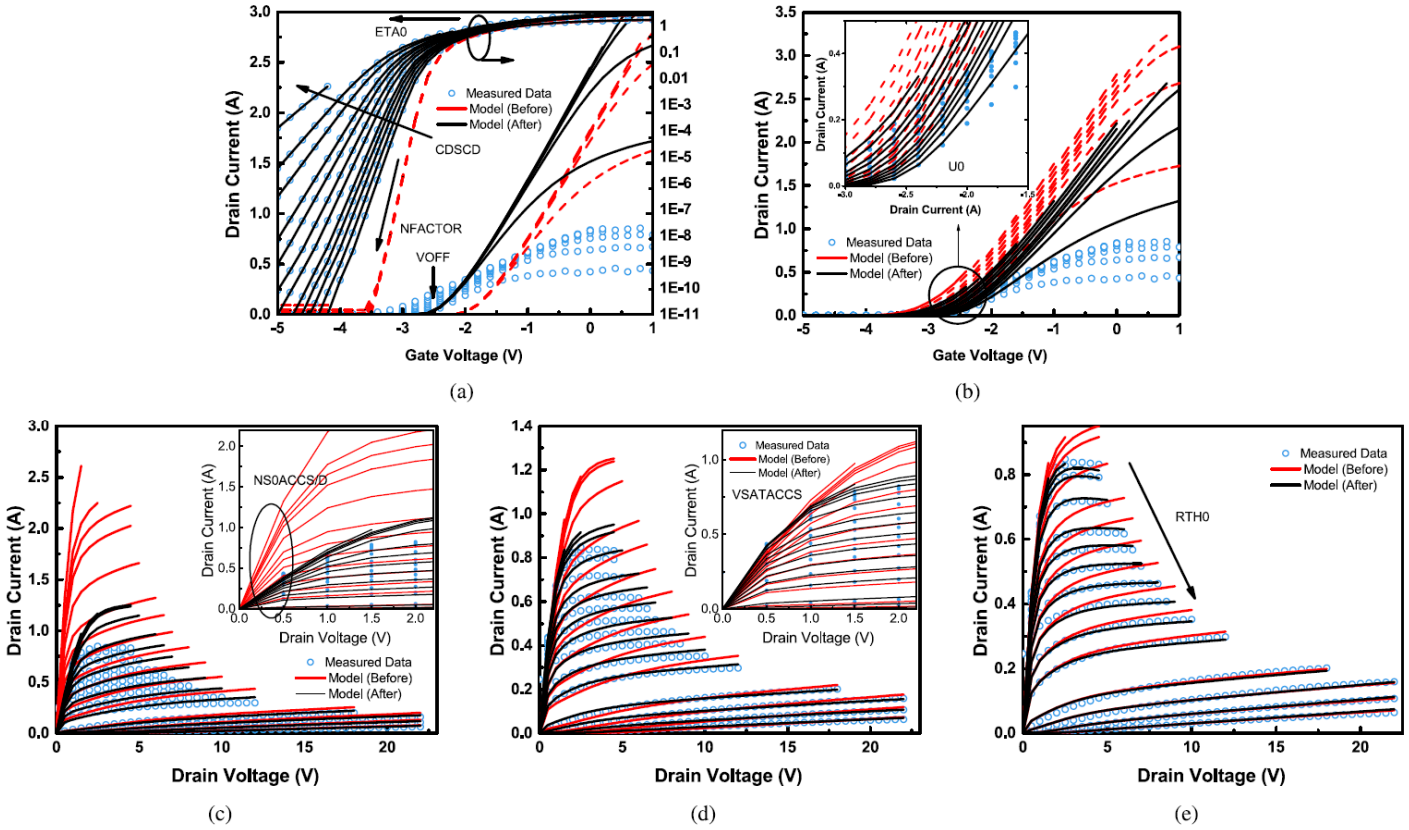




DC I-V Results of Multifinger RF HEMT

Lg = 125 nm, Wg = 10 × 90 µm, Lsg = 200 nm, Ldg = 1.7 µm

DC Parameter Extraction Flow



S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Multi-bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow", IEEE Journal of the Electron Devices Society, Sept. 2017.

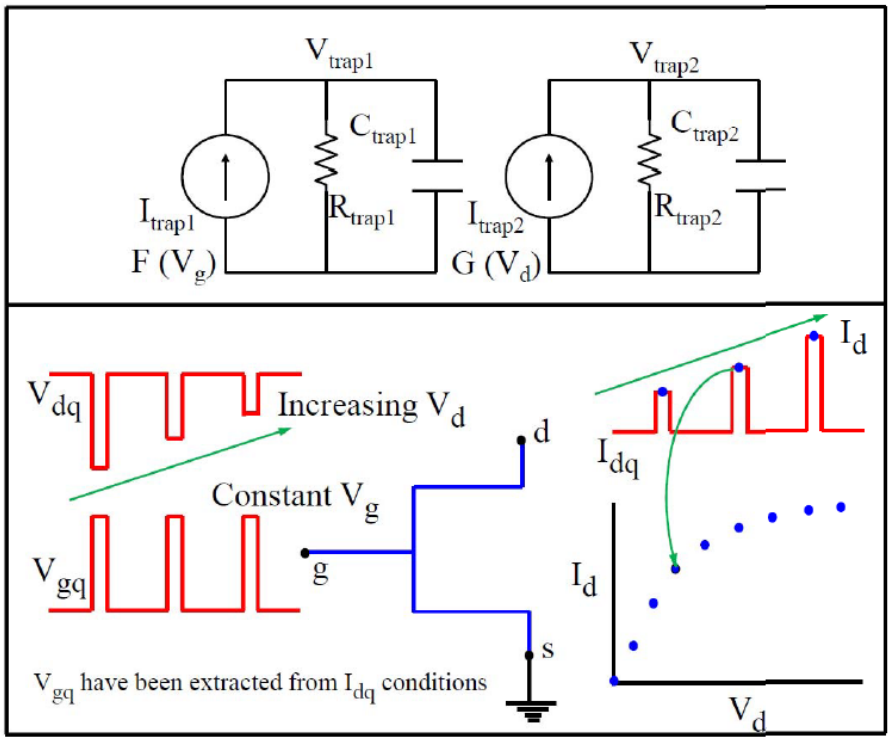


FIGURE 4. **(I) Two R – C sub-circuits used for modeling trapping effects, one each for gate-lag and drain-lag. The voltages $V_{trap1,2}$ are fed back into the compact model to update its key parameters as shown in (5). (II) The dual-pulsed scheme to do the pulsed-IV simulation.**

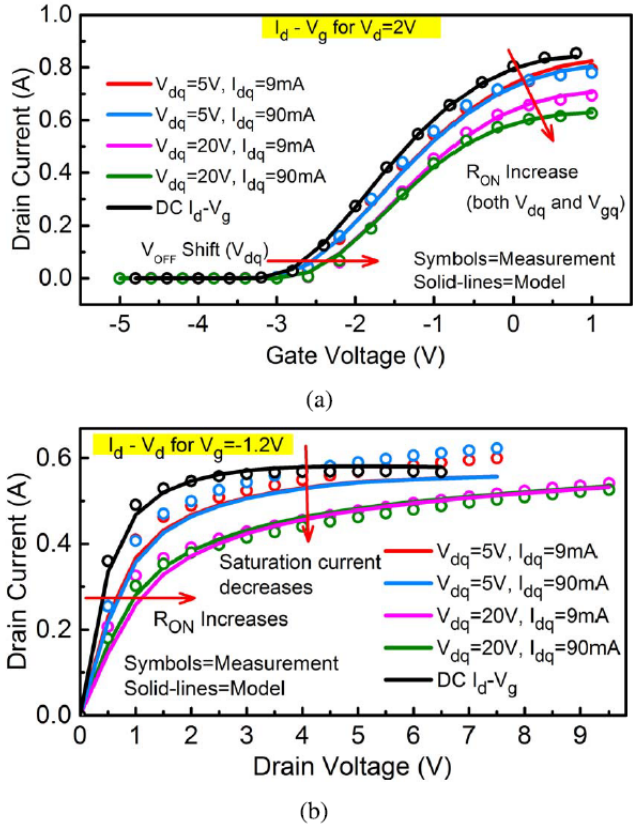
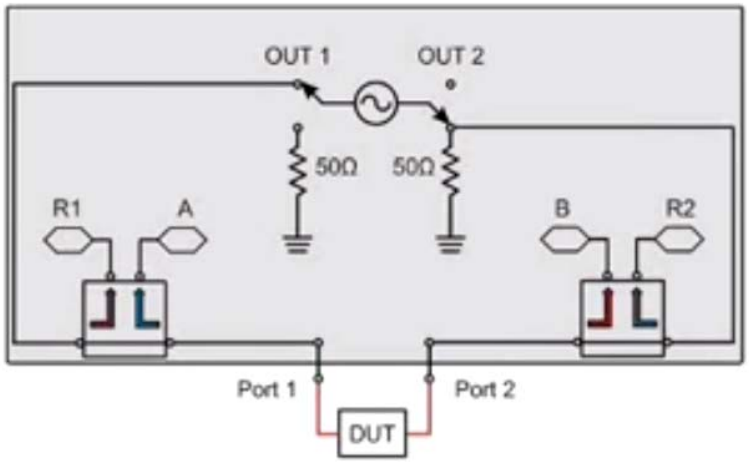


FIGURE 5. **Correlation between measured and modeled (a) Pulsed $I_d - V_g$ and (b) Pulsed $I_d - V_d$ characteristics using the trap model. Accurate fits are seen for multiple quiescent bias conditions (V_{dq} = 5, 20 V and I_{dq} = 10, 100 mA/mm), which is essential for the non-linear RF behavior of the model.**

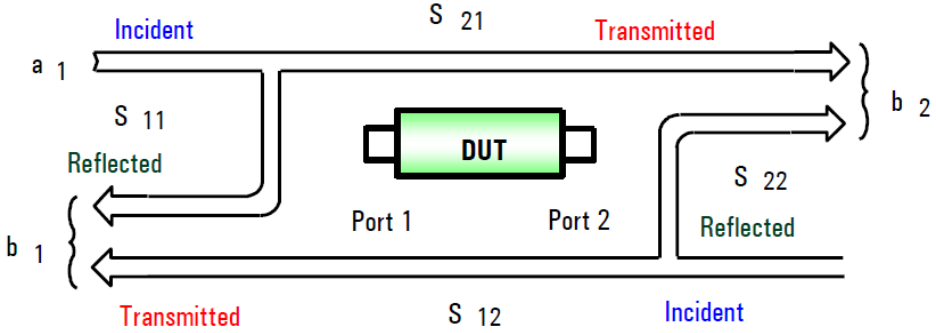
RF Measurements

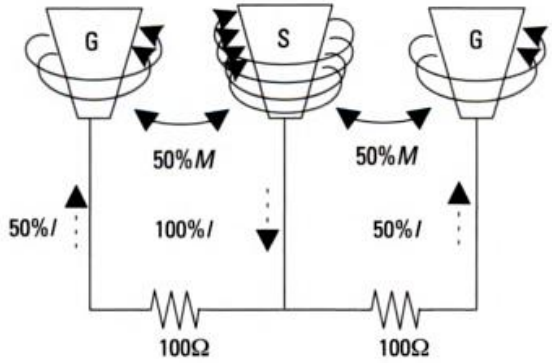
S-Parameters

- Easy for high frequencies (hard to do open/short for Z/Y)
- Calculate other quantities
- Cascadable
- Transformation
- Compatibility with simulation tools



VNA Architecture





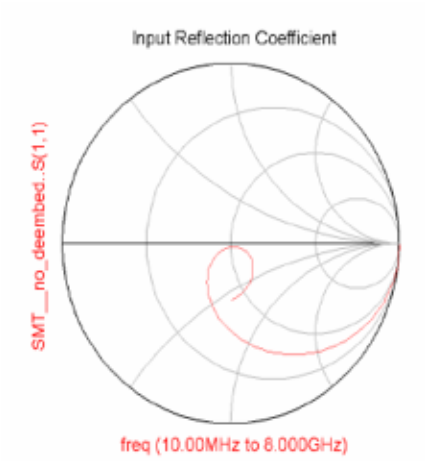
[Advanced Design System, Design Guide]

De-embedding

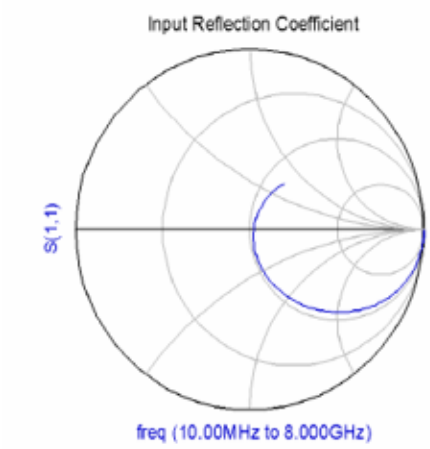
De-embedding : Negating effects of unwanted portion

"Real" DUT SP= Measured SP–Fixture Characteristic

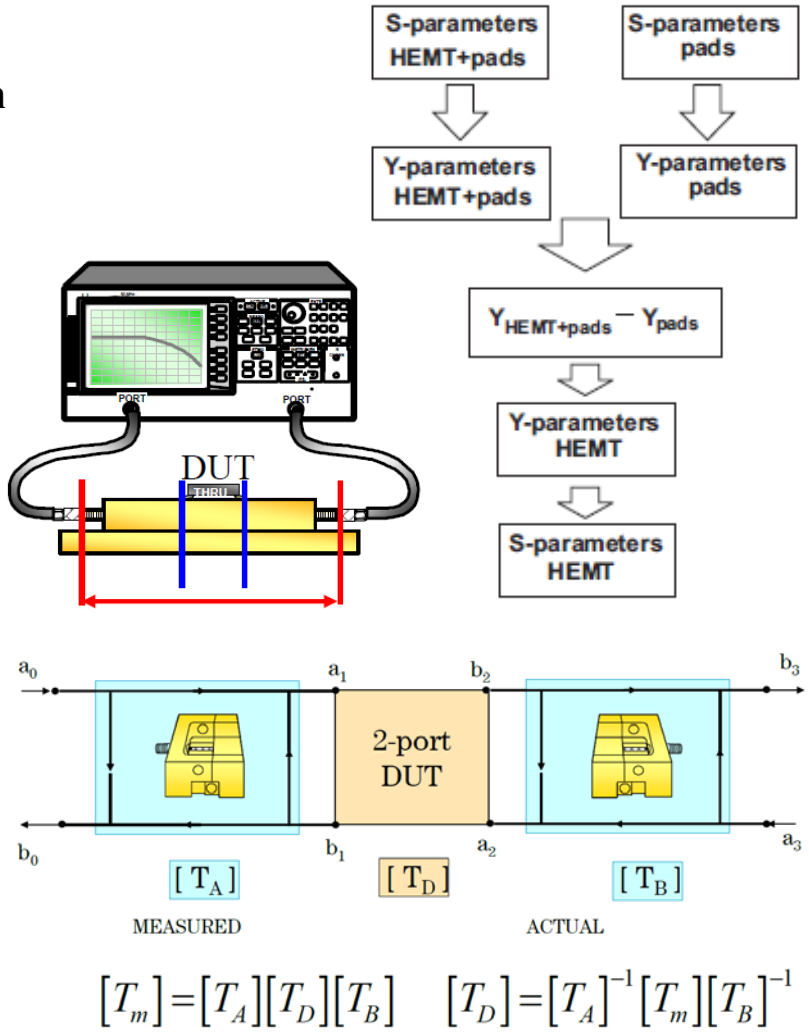
De-embedding is a mathematical process that removes the effects of unwanted embedded portions of the structure in the measured data by subtracting their contribution.



Before De-embedding



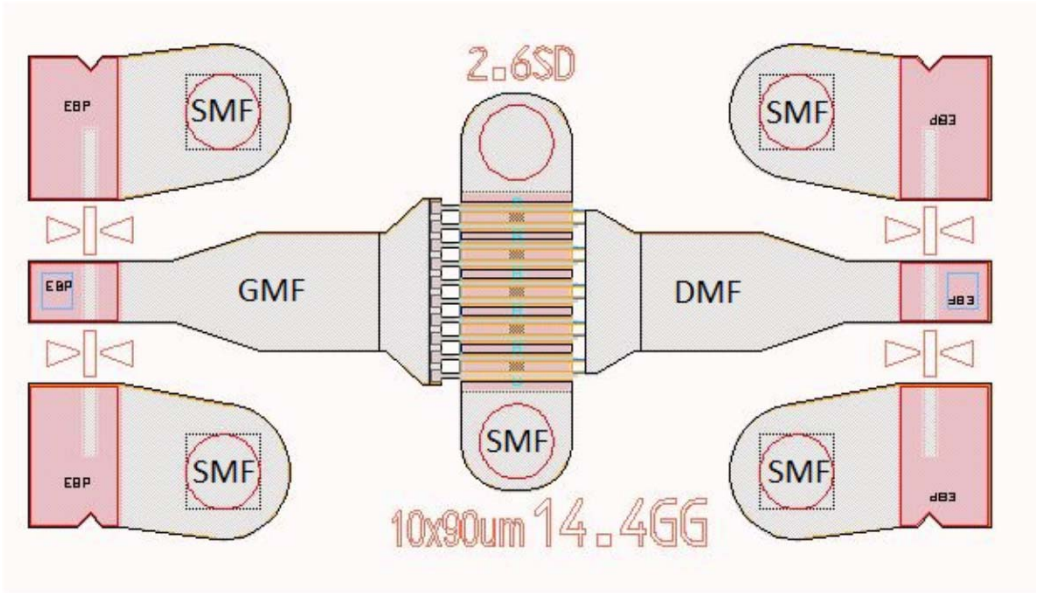
After De-embedding

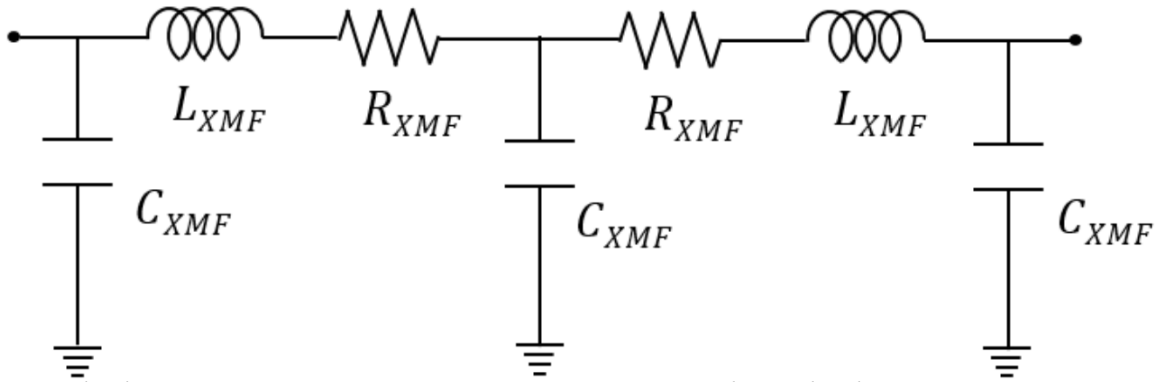


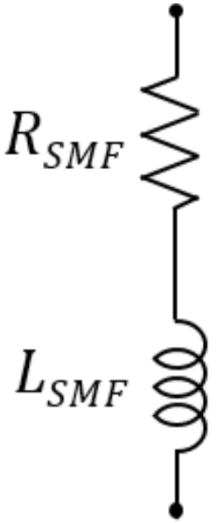
$$[T_m]=[T_A][T_D][T_B] \qquad [T_D]=[T_A]^{-1}[T_m][T_B]^{-1}$$

[De-embedding Techniques in Advanced Design System, Agilent Manual]

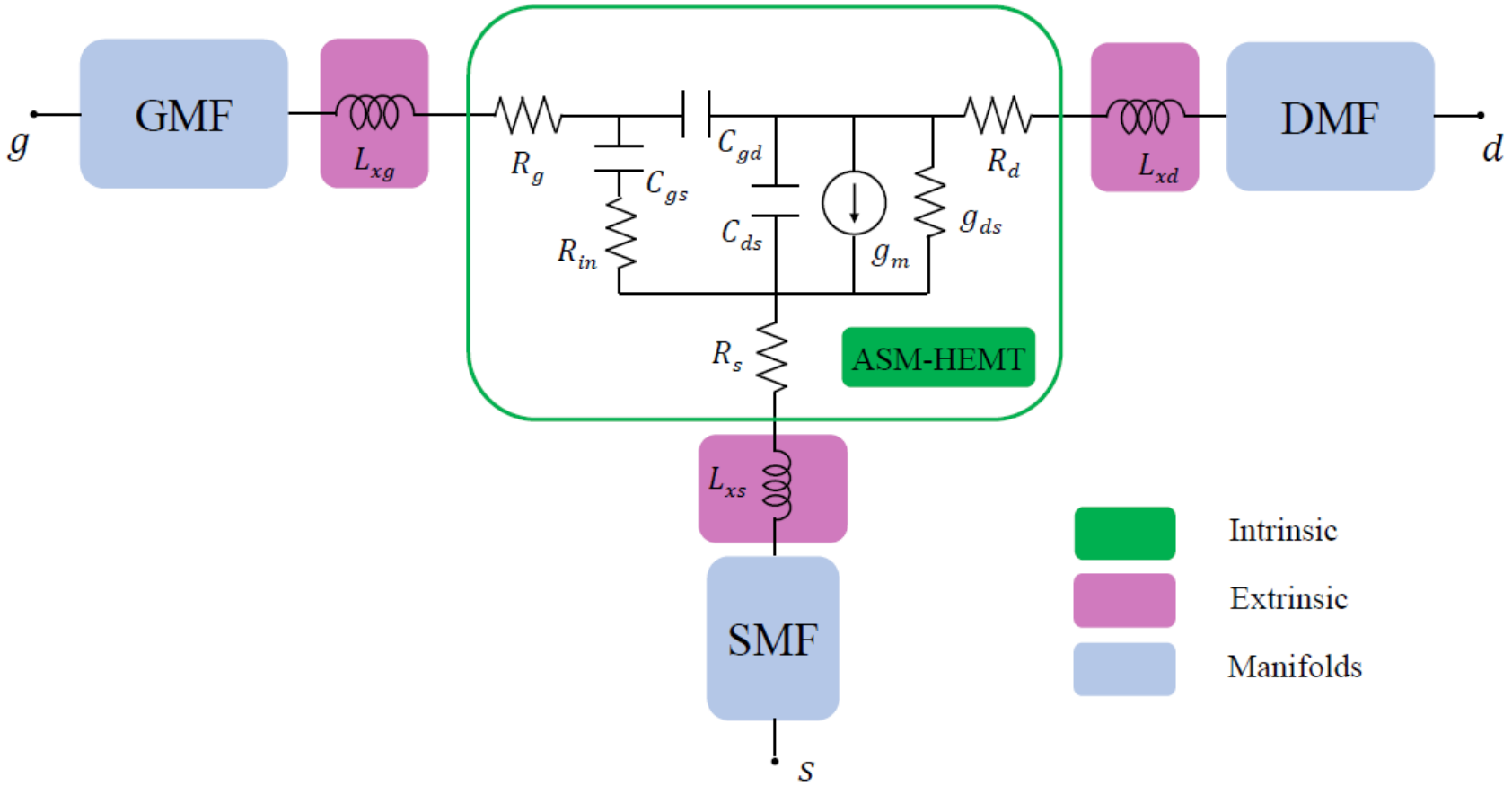
Device Layout and Manifolds







Equivalent Circuit Model at RF



$$\begin{bmatrix} C_{gs} & C_{gd} & C_{ds} \\ g_m & g_{ds} & R_g \end{bmatrix} = \begin{bmatrix} (\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}])/\omega & -\mathrm{Im}[Y_{12}]/\omega & \mathrm{Im}[Y_{22}]/\omega - C_{gd}(1 + g_m R_g) \\ \mathrm{Re}[Y_{21}] & \mathrm{Re}[Y_{22}] & \mathrm{Re}[Y_{11}]/(\omega^2 C_{gg}^2) \end{bmatrix}$$

Small Signal Modeling

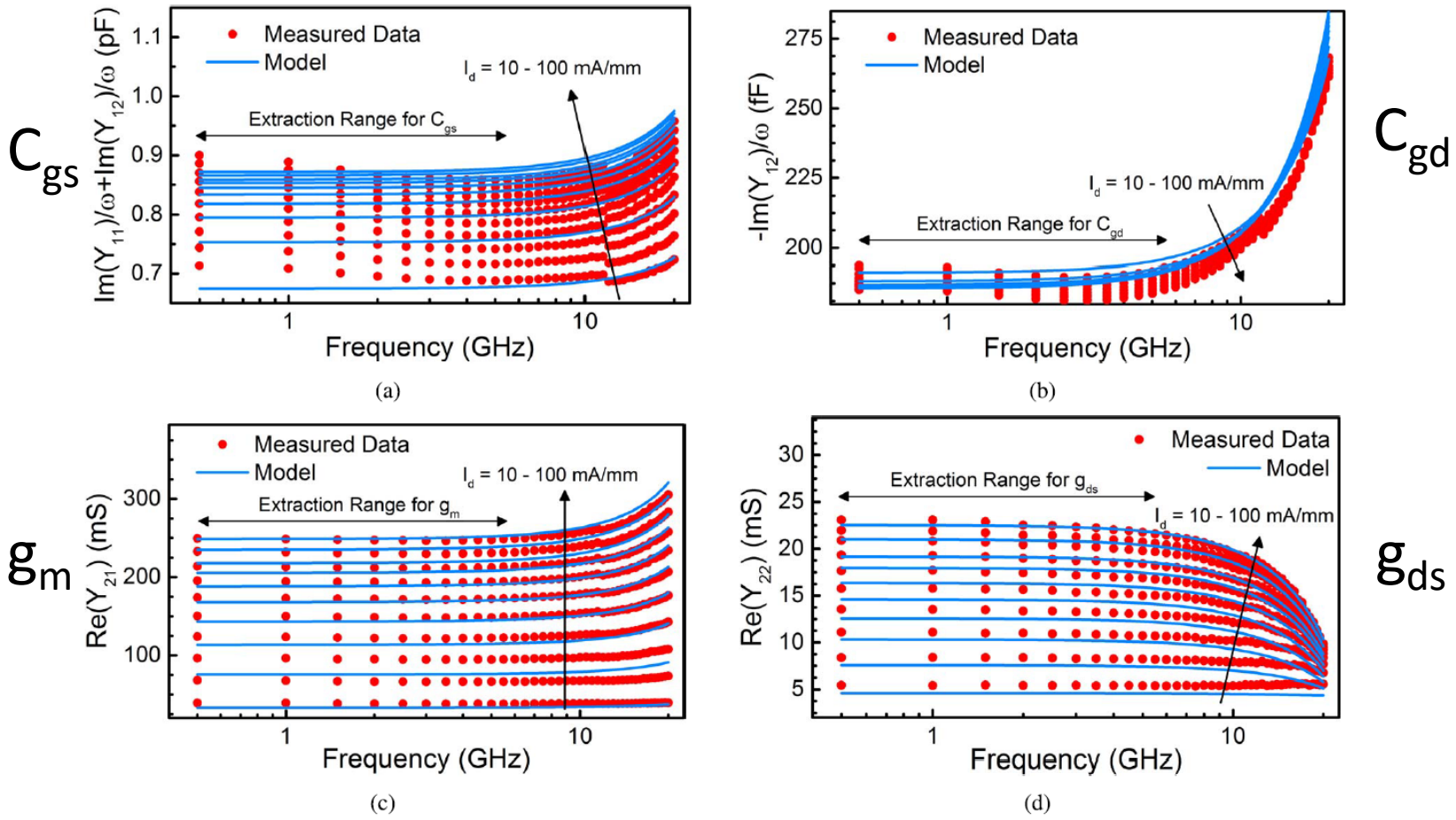
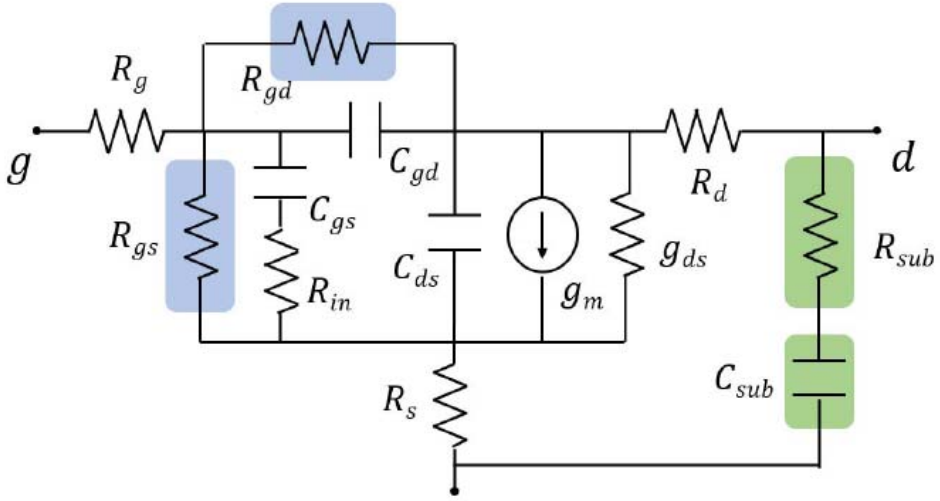


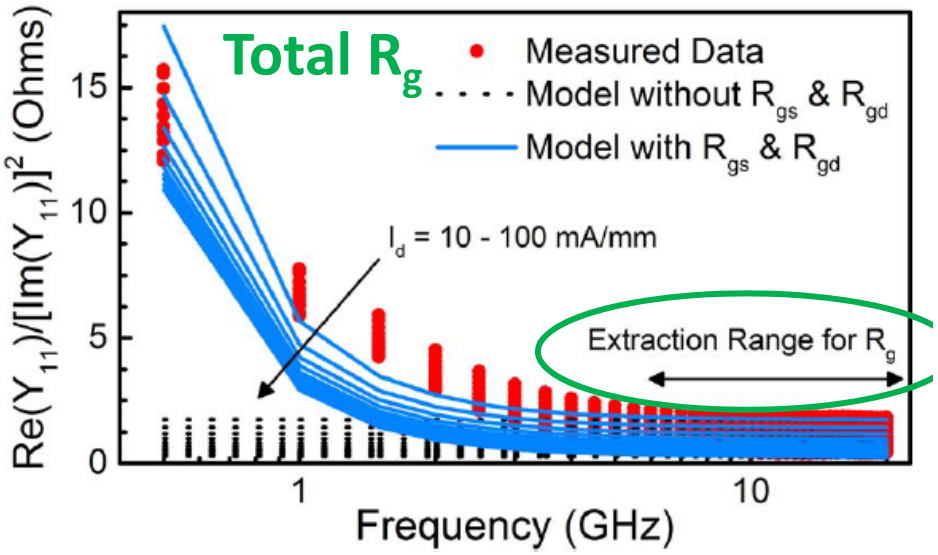
FIGURE 7. Extracted SS – EC (a) C_{gs} (b) C_{gd} (c) g_m and (d) g_{ds} for V_d = 5 V and 10 gate bias conditions. Parasitic capacitances are adjusted to values given in Table 2 to fit model and measured data for (a–b). A sufficiently broad frequency range (≈ 10 GHz) is observed for extraction for which frequency-independent behavior of SS – EC elements is seen after which inductive effects dominate.

S. A. Ahsan, ..,Y. S. Chauhan, IEEE Journal of the Electron Devices Society, Sept. 2017.

Impact of Gate Resistance

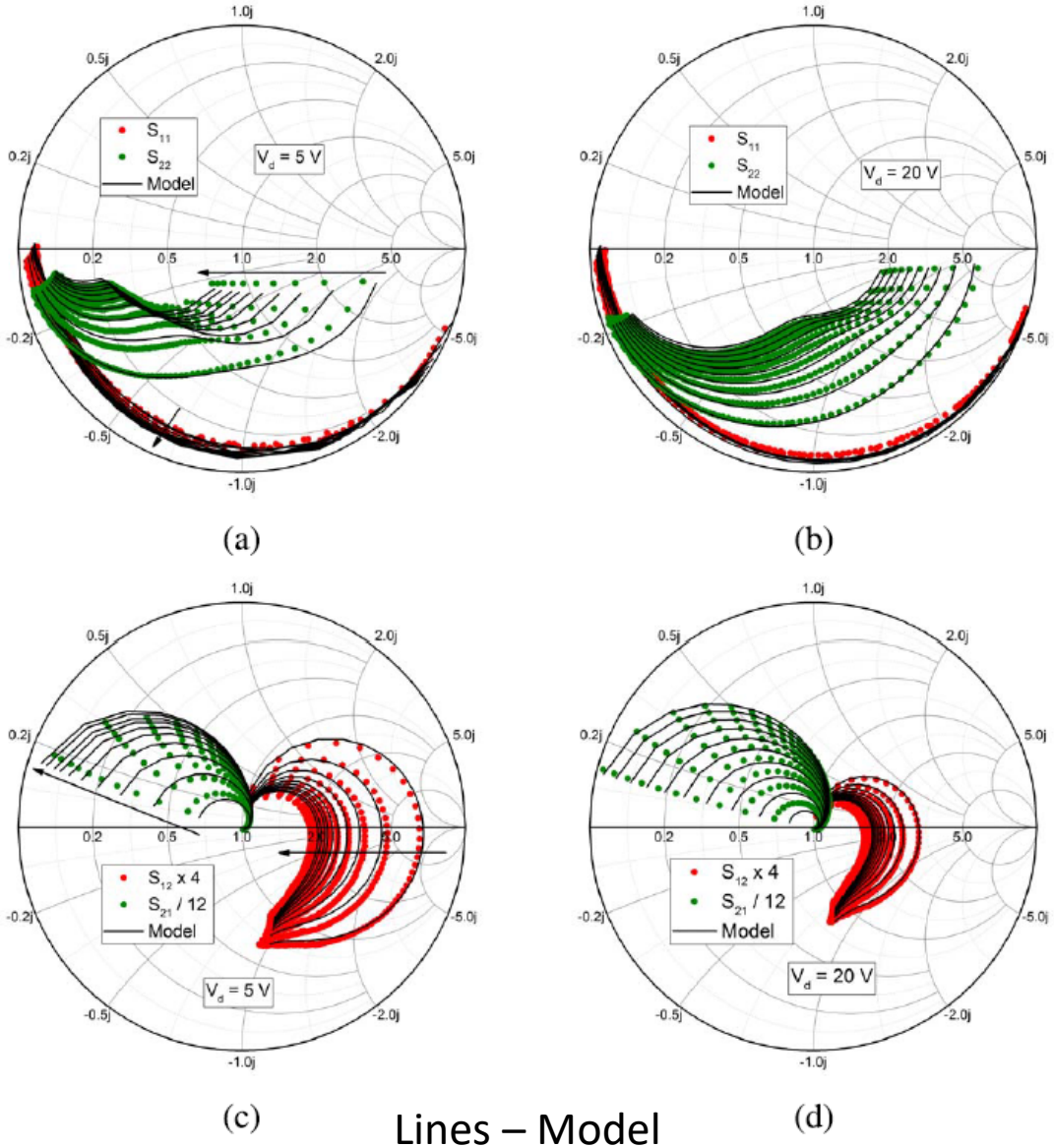
- Large resistors R_{gs} and R_{gd} – Capture the differential gate resistance for current flowing through the gate-source and gate-drain Schottky diodes.
- Their inclusion significantly impacts the overall gate resistance (R_g) at low frequencies as shown in Fig.
- R_{sub} and C_{sub} – Capture the substrate loss at the output port.





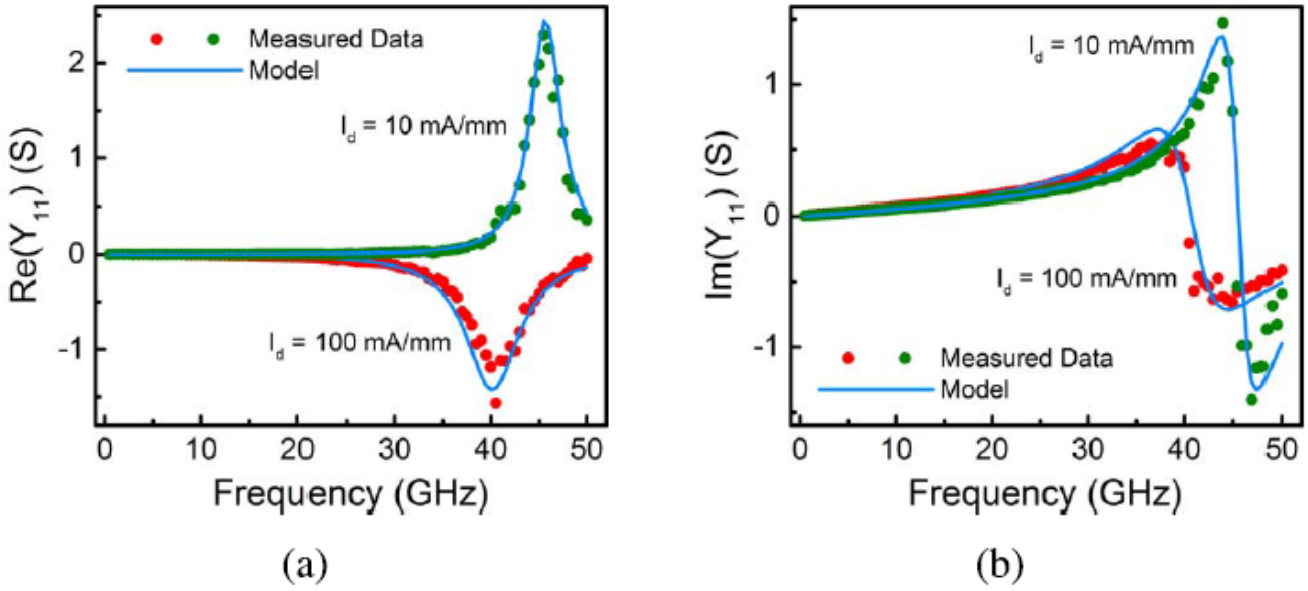
S-Parameters

- Frequency: 0.5 – 50 GHz
- 2 different drain-bias conditions, with 10 different gate biases (Id = 10 – 100 mA/mm)



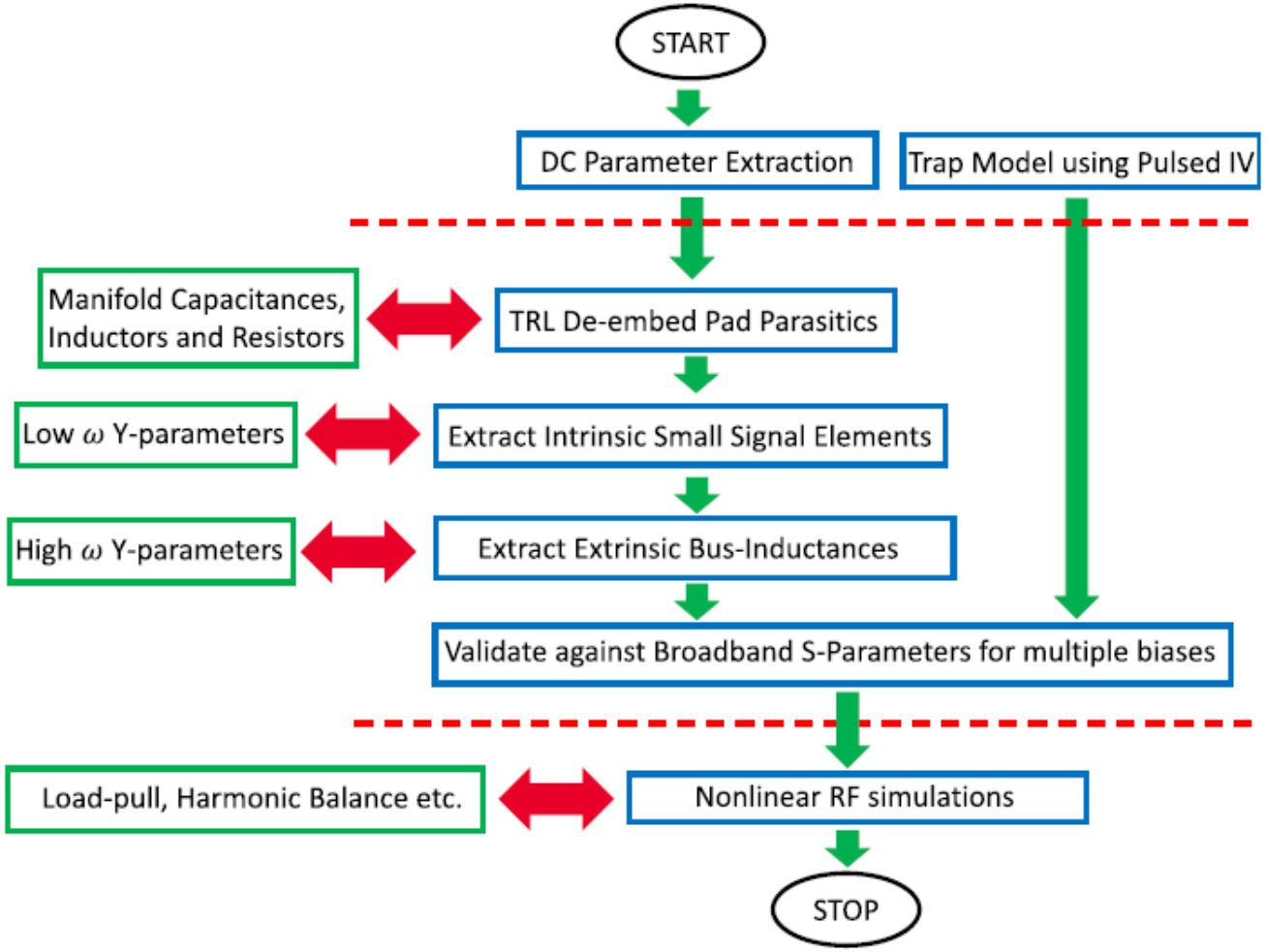
Lines – Model
Symbols – Measured Data

Y-Parameters

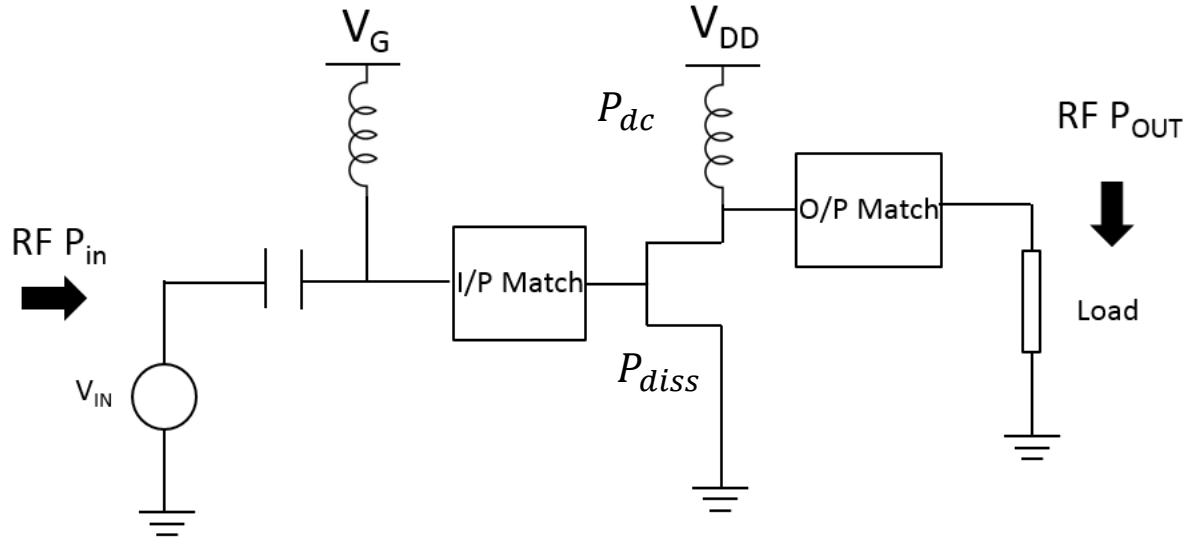


- The peaks and dips and their bias dependence is a manifestation of the interaction between the intrinsic capacitances and the extrinsic inductances.
- The values of bus-inductances can be fine-tuned to fit the peaks/dips in measured and modeled extrinsic-level Y-parameters.

RF Parameter Extraction Flow



Power Amplifier Design Goals



$$Gain = \frac{P_{out}}{P_{in}}$$

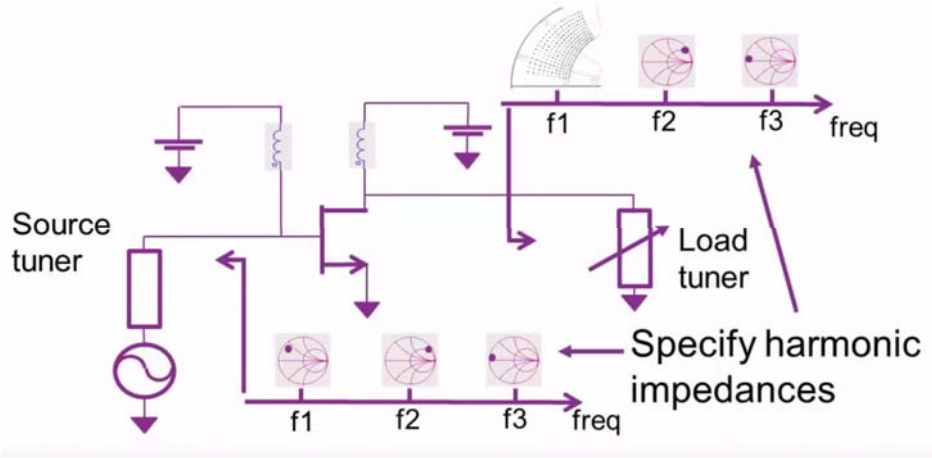
$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}$$

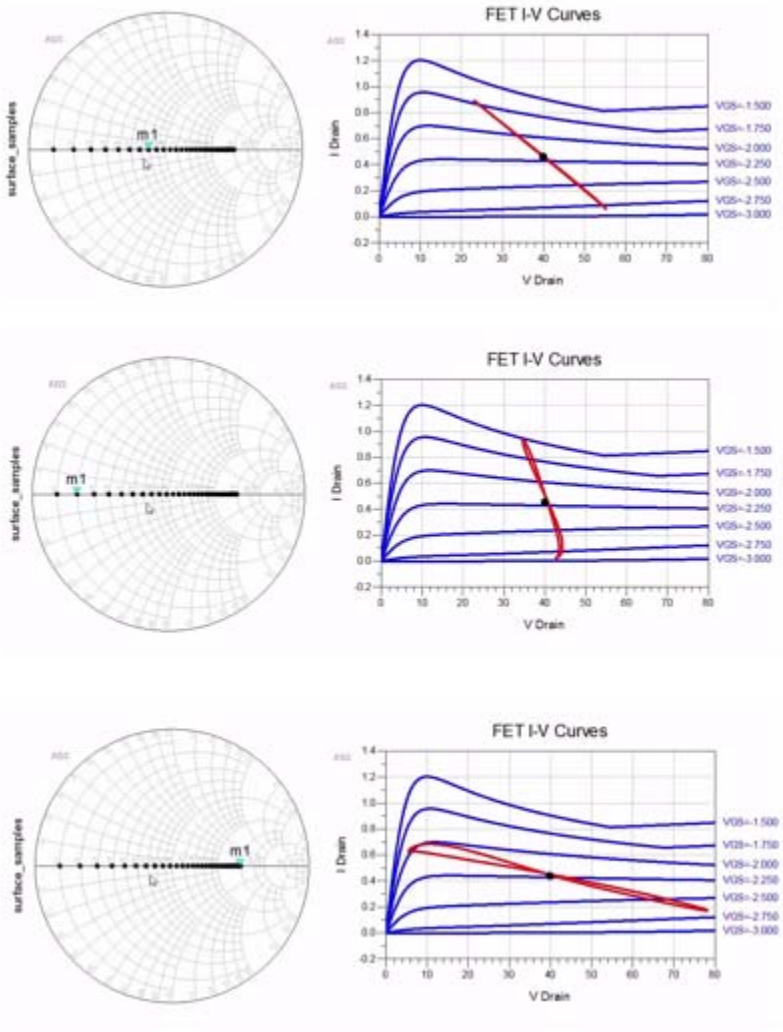
$$Drain\ Efficiency = \frac{P_{out}}{P_{dc}}$$

Load Pull Technique

Helps us:

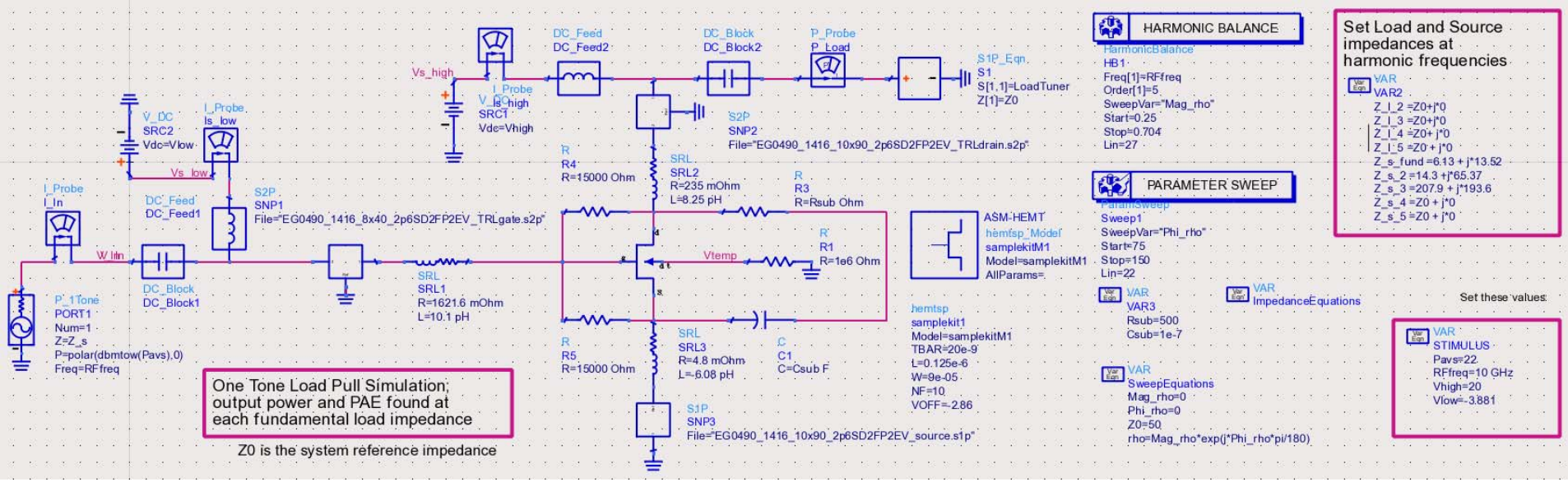
- Determine Optimum load impedance for maximum Pout and PAE performance
- Matching networks
- Understand tradeoffs!

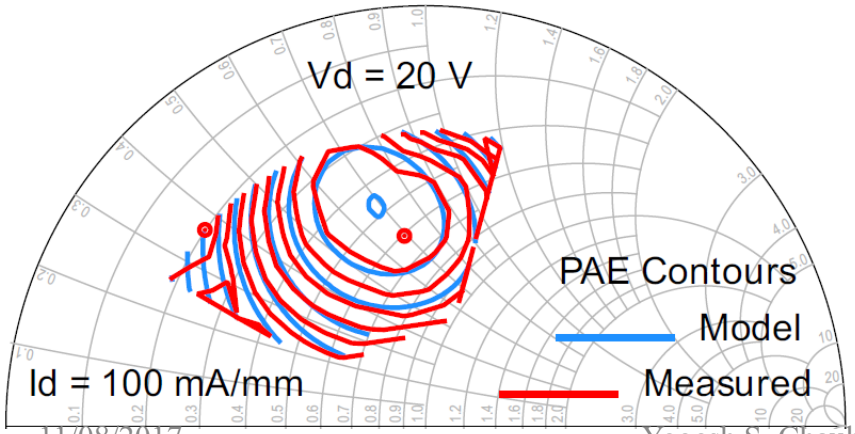


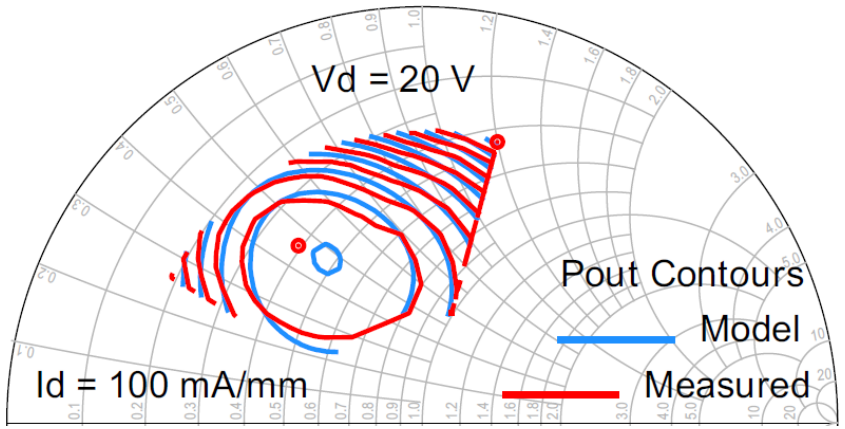


[M. S. Hashmi *et. al*, *IEEE Instrum. Meas. Mag.*, **16 (2)**, Feb., (2013)]

Load-Pull Schematic & Overlays







S. A. Ahsan, et. al, *IEEE Trans. Microwave Theory Tech,* 2017.

Load Pull Contours

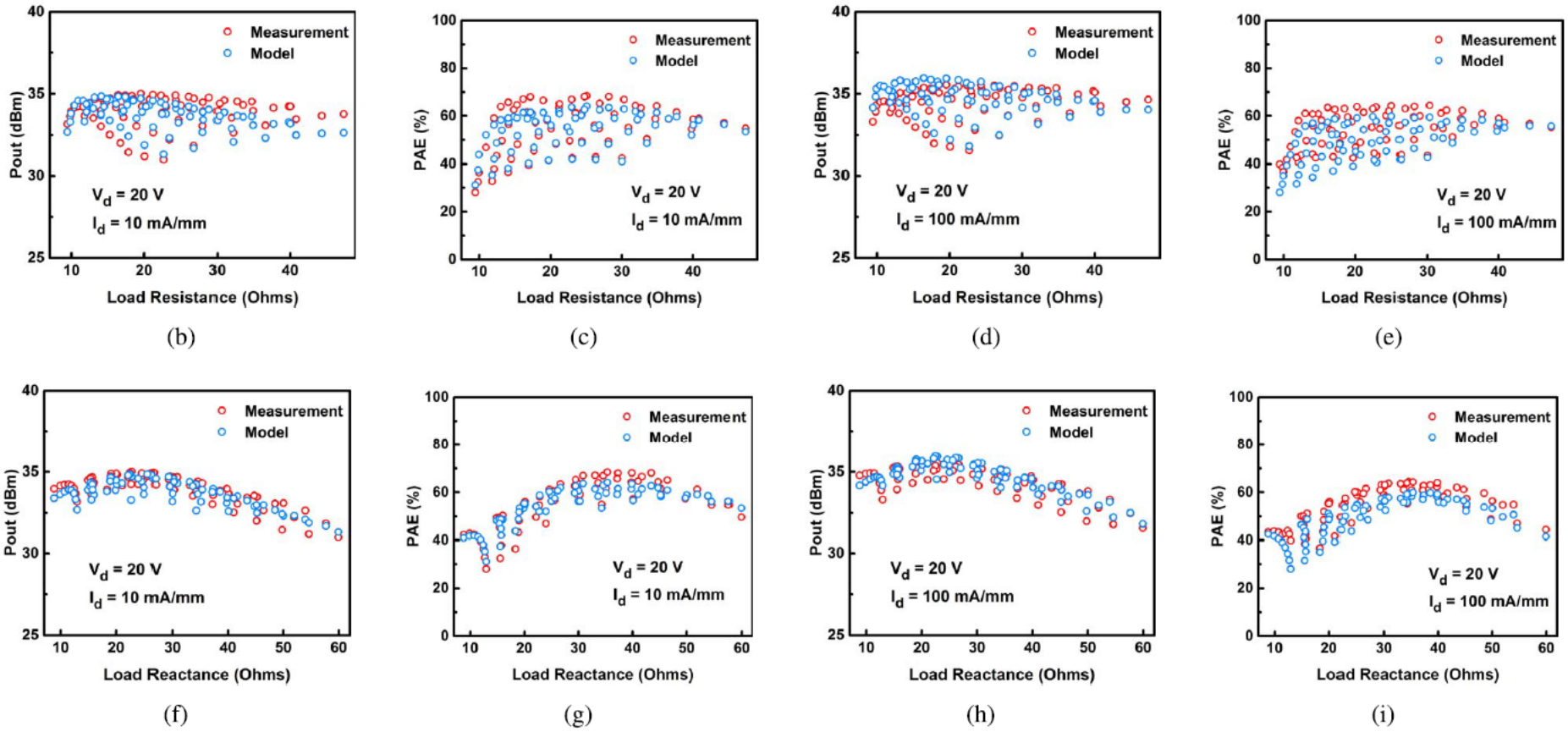
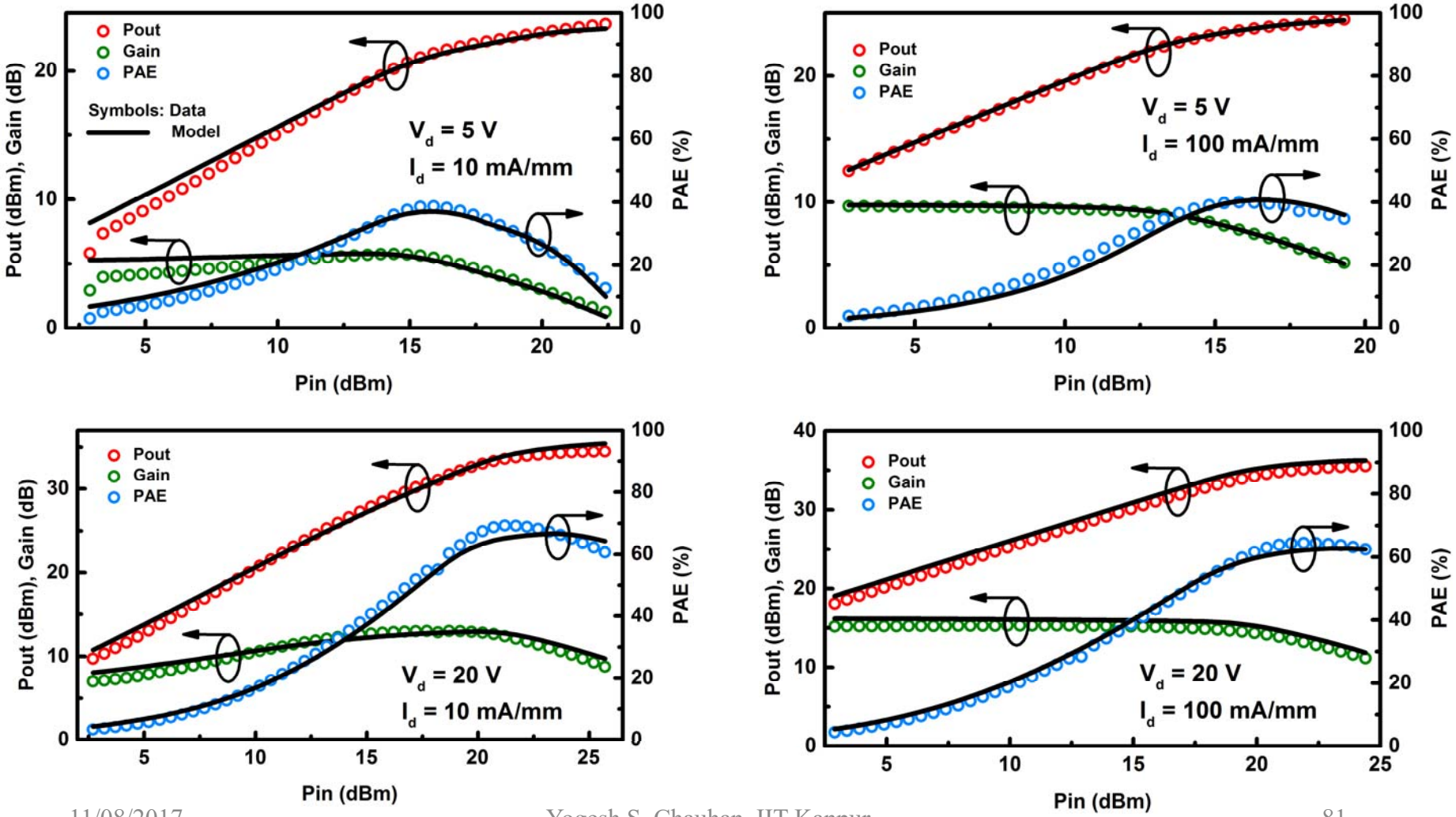


FIGURE 12. **(a) ADS schematic for simulating load-pull contours using the embedded model. Pad level parasitics in the form of 2-port S-parameter components are added. Right in the centre is the DUT which is governed by the ASM-GaN-HEMT PDK. (b-i) Discrete load-sweeps for P_{OUT} and PAE against real and imaginary loads for multiple bias conditions, at 10 GHz signal frequency. The model accurately predicts the P_{OUT} and PAE maxima as well as their mutual tradeoffs upon varying the load resistance/reactance.**

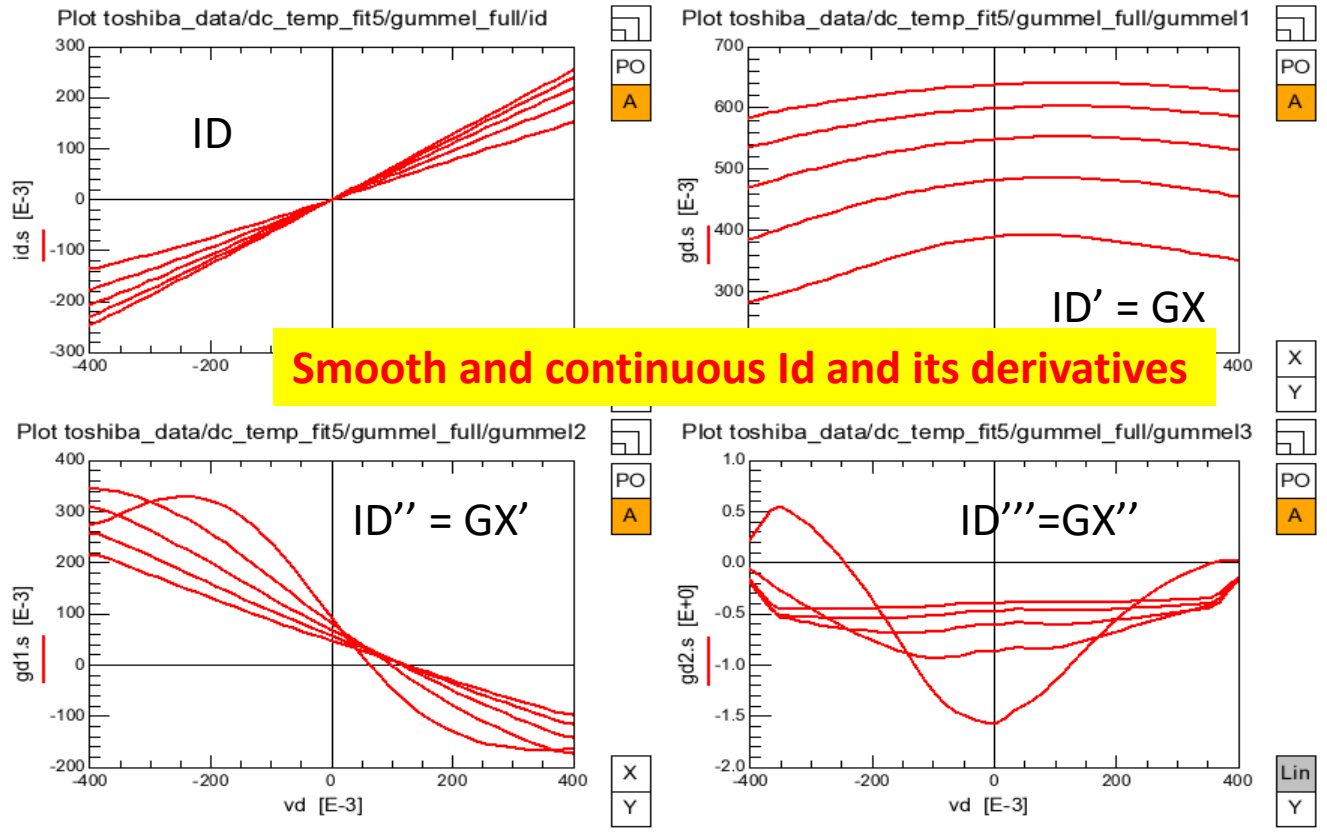
Harmonic Balance Power Sweeps



S. A. Ahsan, et. al, *IEEE Trans. Microwave Theory Tech,* 2017.

Model Quality

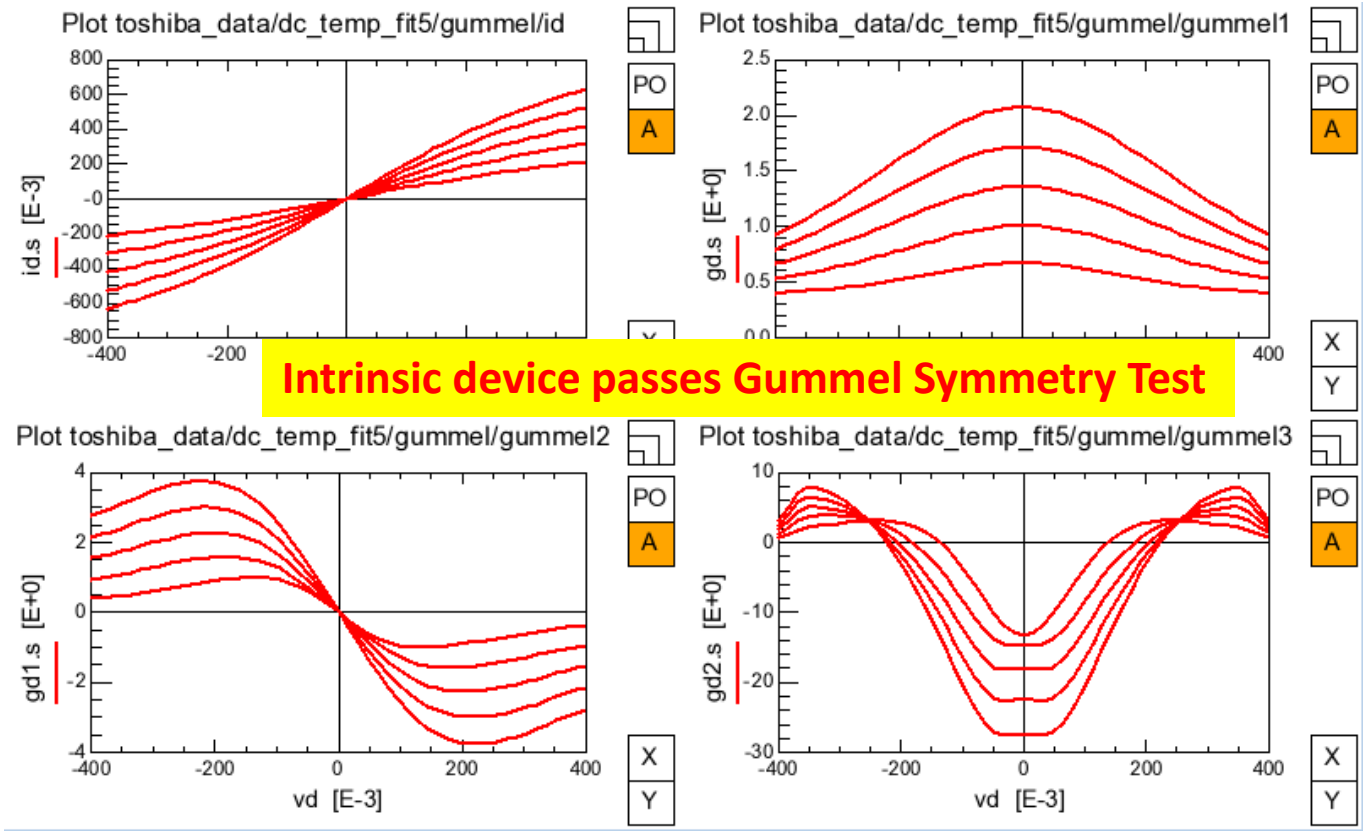
Toshiba device Id and derivatives



Full device (simulation)

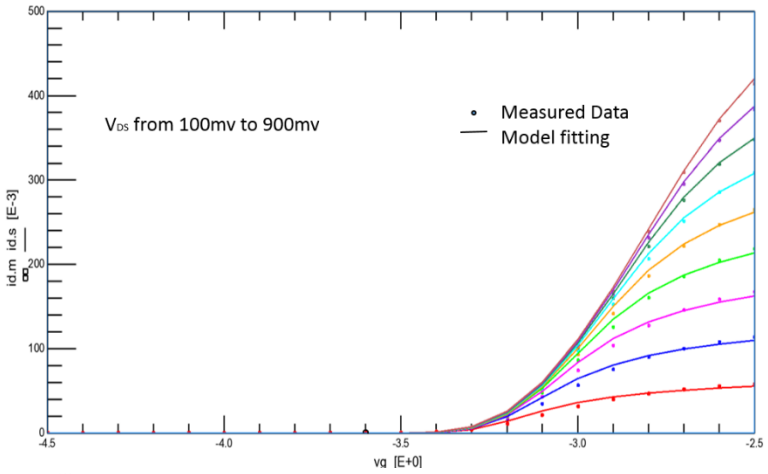
Toshiba device

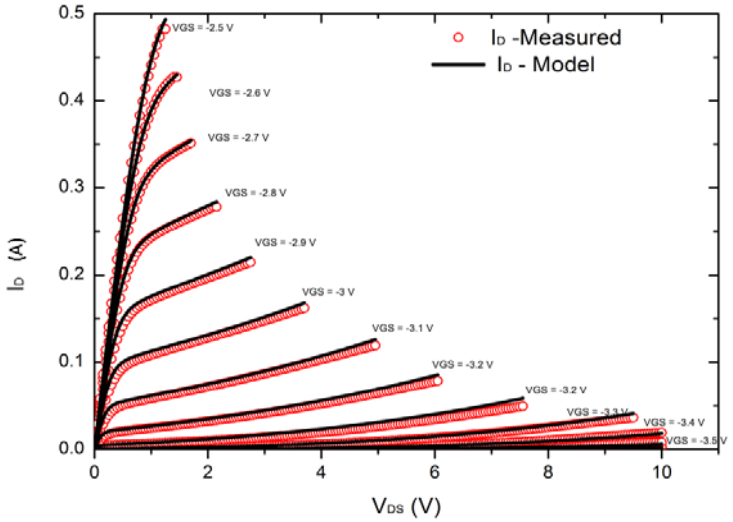
Intrinsic device (simulation)

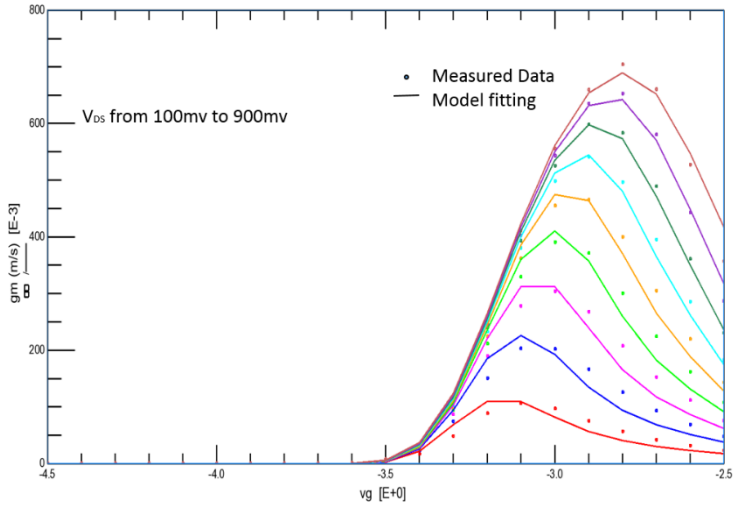


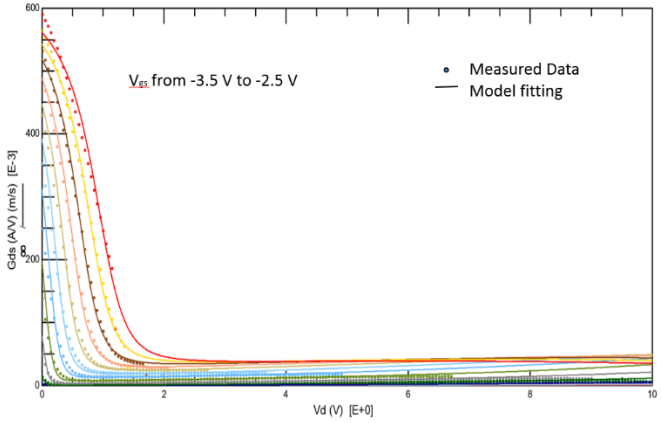
Characterization and Parameter Extraction for RFMD RF 3931 Device

(Devices received from ISRO)









Summary

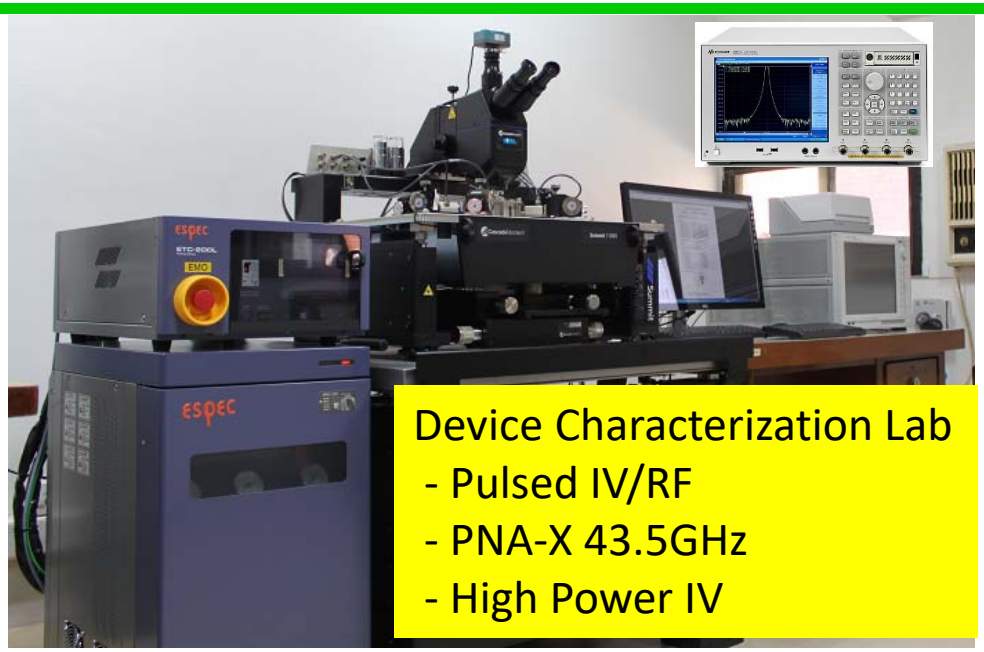
- Physics-based fully analytical model for the GaN HEMTs
- Excellent agreement with the measured data at different temperatures for different channel length devices
- Model is implemented in the **Verilog - A** code
- Tested on Agilent ADS, Synopsys HSPICE and Cadence's Spectre **simulators**
- In final phase of industry standardization at CMC

My Group and Nanolab

Current members – 30

- Postdoc – 5
- Ph.D. – 17
- Three PhD graduated
  - Postdocs in UC Berkeley and U. Bordeaux France

	2017	2016	2015	2014	2013	2012
Books	1		1			
Journal	20	18	9	5	3	3
Conference	8	30	30	8	4	6



Device Characterization Lab
- Pulsed IV/RF
- PNA-X 43.5GHz
- High Power IV

Funding in last 5 years:
> Rs. 8.5 Crore

GaN-HEMT Journal Publications

1. S. A. Ahsan, A. Pampori, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "A New Small-signal Parameter Extraction Technique for large gate-periphery GaN HEMTs", in IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 10, Oct. 2017.
2. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Multi-bias RF Large-Signal GaN HEMT Modeling and Parameter Extraction Flow", in IEEE Journal of the Electron Devices Society, Vol. 5, Issue 5, Sept. 2017.
3. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Pole-Zero Approach to Analyze and Model the Kink in Gain-Frequency Plot of GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 3, Mar. 2017.
4. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Cross-Coupling and Substrate Capacitance in GaN HEMTs for Power-Electronic Applications", IEEE Transactions on Electron Devices (Special Issue), Vol. 64, Issue 3, Mar. 2017.
5. A. Dasgupta and Y. S. Chauhan, "Modeling of Induced Gate Thermal Noise in HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 26, Issue 6, June 2016.
6. S. A. Ahsan, S. Ghosh, A. Dasgupta, K. Sharma, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling in Dual Field Plate Power GaN HEMT for Accurate Switching Behaviour", IEEE Transactions on Electron Devices, Vol. 63, Issue 2, Feb. 2016.
7. A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Surface potential based Modeling of Thermal Noise for HEMT circuit simulation", IEEE Microwave and Wireless Components Letters, Vol. 25, Issue 6, June 2015.
8. S. Ghosh, A. Dasgupta, S. Khandelwal, S. Agnihotri, and Y. S. Chauhan, "Surface-Potential-Based Compact Modeling of Gate Current in AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 62, Issue 2, Feb. 2015.
9. A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Compact Modeling of Flicker Noise in HEMTs", IEEE Journal of Electron Devices Society, Vol. 2, Issue 6, Nov. 2014.
10. S. Khandelwal, C. Yadav, S. Agnihotri, Y. S. Chauhan, A. Curutchet, T. Zimmer, J.-C. Dejaeger, N. Defrance and T. A. Fjeldly, "A Robust Surface-Potential-Based Compact Model for GaN HEMT IC Design", IEEE Transactions on Electron Devices, Vol. 60, Issue 10, Oct. 2013.
11. S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, "Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices", IEEE Transactions on Electron Devices, Vol 59, Issue 8, Oct. 2012.

GaN-HEMT Conference Publications

1. S. Khandelwal, S. Ghosh, S. A. Ahsan and Y. S. Chauhan, "Dependence of GaN HEMT AM/AM and AM/PM Non-Linearity on AlGaN Barrier Layer Thickness", IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpur, Malaysia, Nov. 2017.
2. S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Surface-potential-based Gate-periphery-scalable Small-signal Model for GaN HEMTs", IEEE Compound Semiconductor IC Symposium (CSICS), Miami, USA, Oct. 2017.
3. S. Ghosh, S. A. Ahsan, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "GaN HEMT Modeling for Power and RF Applications using ASM-HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
4. S. Ghosh, A. Dasgupta, A. K. Dutta, S. Khandelwal, and Y. S. Chauhan, "Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
5. S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Statistical Simulation for GaN HEMT Large Signal RF performance using a Physics-based Model", IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, Dec. 2016.
6. A. Dasgupta, S. Ghosh, S. A. Ahsan, S. Khandelwal, N. Defrance, and Y. S. Chauhan, "Modeling DC, RF and Noise behavior of GaN HEMTs using ASM-HEMT Compact Model", IEEE International Microwave and RF Conference (IMaRC), Delhi, India, Dec. 2016.
7. S. A. Ahsan, S. Ghosh, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "ASM-HEMT: Advanced SPICE Model for Gallium Nitride High Electron Mobility Transistors", International Conference of Young Researchers on Advanced Materials (ICYRAM), Bangalore, India, Dec. 2016.
8. S. Ghosh, S. A. Ahsan, S. Khandelwal and Y. S. Chauhan, "Modeling of Source/Drain Access Resistances and their Temperature Dependence in GaN HEMTs", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
9. S. A. Ahsan, S. Ghosh, S. Khandelwal and Y. S. Chauhan, "Modeling of Kink-Effect in RF Behaviour of GaN HEMTs using ASM-HEMT Model", IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, Aug. 2016.
10. R. Nune, A. Anurag, S. Anand and Y. S. Chauhan, "Comparative Analysis of Power Density in Si MOSFET and GaN HEMT based Flyback Converters", IEEE International Conference on Compatibility and Power Electronics, Bydgoszcz, Poland, June 2016.
11. S. Agnihotri, S. Ghosh, A. Dasgupta, A. Ahsan, S. Khandewal, and Y. S. Chauhan, "Modeling of Trapping Effects in GaN HEMTs", IEEE India Conference (INDICON), New Delhi, India, Dec. 2015.
12. S. Ghosh, S. Agnihotri, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Analysis and Modeling of Trapping Effects in RF GaN HEMTs under Pulsed Conditions", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
13. S. Agnihotri, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Impact of Gate Field Plate on DC, C-V, and Transient Characteristics of Gallium Nitride HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
14. K. Sharma, S. Ghosh, A. Dasgupta, S. A. Ahsan, S. Khandelwal, and Y. S. Chauhan, "Capacitance Analysis of Field Plated GaN HEMT", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
15. S. A. Ahsan, S. Ghosh, J. Bandarupalli, S. Khandelwal, and Y. S. Chauhan, "Physics based large signal modeling for RF performance of GaN HEMTs", International Workshop on Physics of Semiconductor Devices (IWPSD), Bangalore, India, Dec. 2015.
16. S. Khandelwal, S. Ghosh, Y. S. Chauhan, B. Iniguez, T. A. Fjeldly and C. Hu, "Surface-Potential-Based RF Large Signal Model for Gallium Nitride HEMTs", IEEE Compound Semiconductor IC Symposium (CSICS), New Orleans, USA, Oct. 2015.
17. S. A. Ahsan, S. Ghosh, K. Sharma, A. Dasgupta, S. Khandelwal, and Y. S. Chauhan, "Capacitance Modeling of a GaN HEMT with Gate and Source Field Plates", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015.
18. A. Dasgupta and Y. S. Chauhan, "Surface Potential Based Modeling of Induced Gate Thermal Noise for HEMTs", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015.
19. S. Khandelwal, Y. S. Chauhan, B. Iniguez, and T. Fjeldly, "RF Large Signal Modeling of Gallium Nitride HEMTs with Surface-Potential Based ASM-HEMT Model", IEEE International Symposium on Compound Semiconductors (ISCS), Santa Barbara, USA, June 2015. (Invited)
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