BSIM: Industry Standard Compact MOSFET Models

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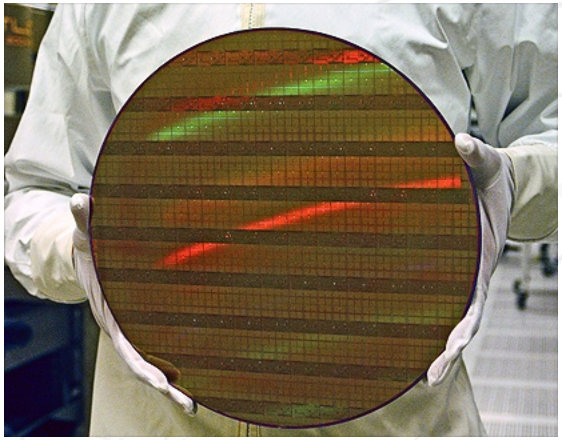
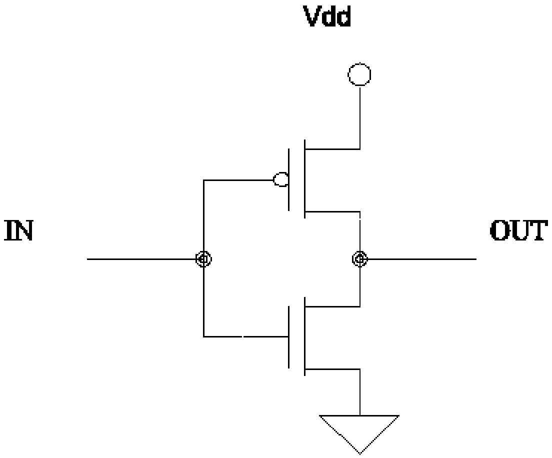
ESSDERC Bordeaux, France

SPICE Transistor Modeling



Medium of information exchange

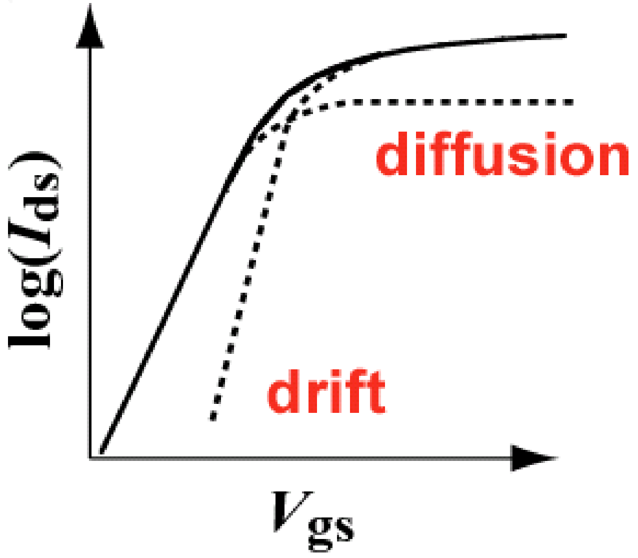


- Simulation Time
  - ~ 10µs per DC data point
  - No complex numerical method allowed
- Accuracy requirements
  - ~ 1% RMS Error after fitting
- Excellent Convergence
- Example: BSIM-CMG
  - 5,000 lines of VA code
  - 50+ parameters
  - Open-source software implemented in major EDA tools

Compact MOSFET Modeling Approaches

- Threshold Voltage based Models (e.g. BSIM3, BSIM4)
  - Fully Analytical solution (easy to implement) – Fast
  - Currents expressed as functions of Voltages

$$I_{ds} = \mu \frac{W}{L} C_{ox} \left[\left(V_{gs} - V_{th} \right) V_{ds} - \frac{1}{2} V_{ds}^{2} \right]$$



- Different equations for
  - Sub-threshold and above-threshold
  - Linear/saturation regions
  - Use interpolation function to get smc

Compact MOSFET Modeling Approaches

- Surface Potential based Models (e.g. PSP, HiSim, BSIM-CMG, BSIM-IMG)

$$V_G - V_{FB} - \Psi_S = -\frac{Q_{si}}{C_{ox}}, Q_{si} = -sign(\Psi_S)\Gamma C_{ox}\sqrt{V_t\left(e^{-\frac{\Psi_S}{V_t}} - 1\right) + V_t e^{-\frac{2\Phi_F + V_{CH}}{V_t}}\left(e^{\frac{\Psi_S}{V_t}} - 1\right) + \Psi_S}$$

  - Implicit equation is solved either iteratively or analytically
  - Might be slower than threshold voltage based models
- Charge based Models (e.g. BSIM5, BSIM6, EKV)
  - Solve for charge instead of surface potential
  - No iterations
  - Faster than Surface Potential based approach with similar accuracy in charge/current

Outline

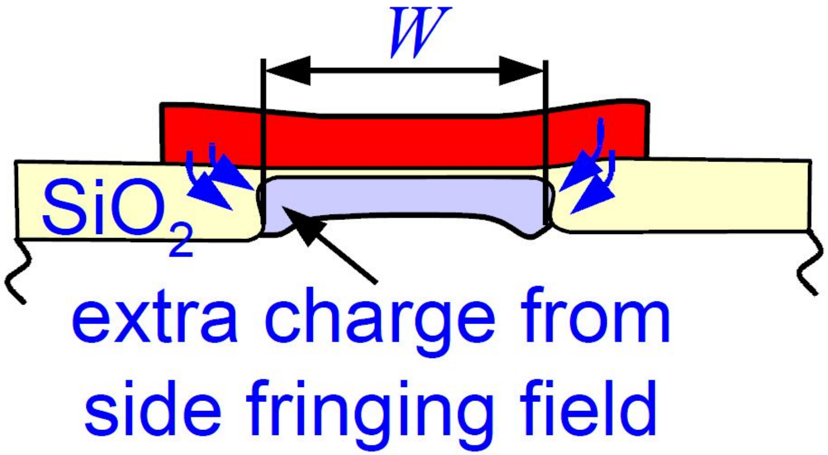
- History of BSIM Models
- BSIM6 Model
- BSIM-CMG Model
- BSIM-IMG Model

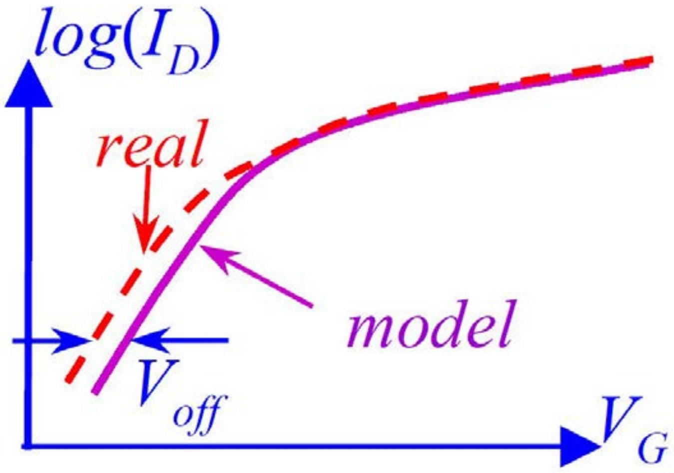
History of BSIM Models

- BSIM1 Model
  - Defined as an engineering model (vs a purely physical model)
  - Focus on the implementation in circuit simulator
  - Only a fast demonstration for DC simulation (no attention on derivatives)
- BSIM2 Model
  - A semi-physical (semi-empirical) model
  - Improvement over BSIM1 to include better fitting to output resistance and other first order derivatives
  - Huge attention placed on parameter extraction methodology
  - Still being used in many companies as internal model due to its fitting ability and simple parameter extraction

History of BSIM Models

- BSIM3 Model
  - Starts as a simple physical model with very few parameters
  - First time – Continuous *I*-*V* and derivatives for fast convergence
  - The 3rd version (BSIM3v3) becomes industry standard
  - Need to fit many technologies from different foundries – many new parameters added
    - Example – Need to have fitting parameters
    - Due to difficult to describe structural detail





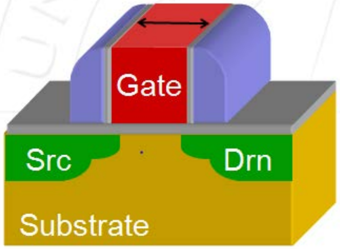
History of BSIM Models

- BSIM4 model
  - Started as model for statistical simulation
  - Priority on physical effects (gate current, mobility models etc.)
  - Added gate and body resistance networks to emphasize accuracy on RF simulation
  - Industry standard in 2000 and most widely used model by semiconductor industry
  - Provides better fitting with more number of parameters
- BSIM-SOI
  - Parallel work went on SOI modeling – PD/FD/DD
  - Real device effects same as BSIM3/BSIM4
  - Industry standard in 2002

BSIM Family of Compact Device Models

1990 1995 2000 2005 2010

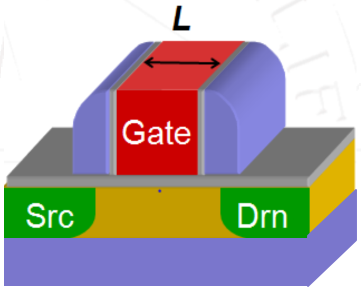
BSIM1,2 **BSIM3**



Bulk MOSFET

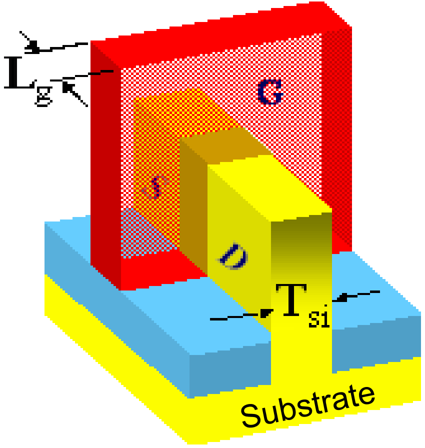
BSIM4

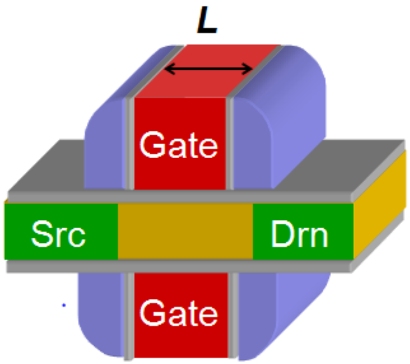
BSIM5 **BSIM6** **New**



Silicon on Insulator MOSFET

BSIMSOI





BSIM-MG

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model

BSIM6: Charge based MOSFET model

- BSIM6 – Next BSIM Bulk MOSFET model
  - Charge based core derived from Poisson’s solution
  - Real device effects (SCE, CLM etc.) from BSIM4
  - *Parameter names matched to BSIM4*
- Physical Capacitance model
  - Short channel CV–Velocity saturation & CLM
- *Symmetry*
  - Currents & derivatives are symmetric @ VDS=0
  - Capacitances & derivatives are symmetric @VDS=0
  - Provide accurate results in Harmonic Distortion simulation
- Continuous in all regions of operations
- Better Statistical Modeling using physical parameters

Physics of BSIM6 Model

- Gauss’ Law

$$V_G - V_{FB} - \Psi_S = -\frac{Q_{si}}{C_{ox}} = -\frac{Q_i + Q_b}{C_{ox}}$$

- Poisson’s solution for long channel MOSFET

$$\frac{Q_{si}}{\Gamma C_{ox}\sqrt{V_t}} = \mp\sqrt{e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1 + e^{-\frac{2\Phi_F + V_{ch}}{V_t}}\left(e^{\frac{\Psi_S}{V_t}} - \frac{\Psi_S}{V_t} - 1\right)}$$

- Bulk charge density is given by

$$\frac{Q_b}{\Gamma C_{ox}\sqrt{V_t}} = \mp\sqrt{e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1}$$

- Combining these, we have

$$V_G - V_{FB} - \Psi_S = -\frac{Q_i}{C_{ox}} \pm \Gamma\sqrt{V_t\left(e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1\right)}$$

Physics of BSIM6 Model

- Defining Pinch-off potential $\Psi_P = \Psi_S$, when $Q_i = 0$

$$V_G - V_{FB} - \Psi_P = sign(\Psi_P)\Gamma\sqrt{V_t\left(e^{-\frac{\Psi_P}{V_t}} + \Psi_P - 1\right)}$$

Ψ_P is evaluated from implicit equation

$$-\frac{Q_i}{\Gamma C_{ox}\sqrt{V_t}} = \sqrt{\frac{\Psi_S}{V_t} + e^{\frac{\Psi_S - 2\Phi_F - V_{ch}}{V_t}}} - \sqrt{\frac{\Psi_S}{V_t}}$$

- For $\Psi_S >$ few V_t, we have

$$-\frac{Q_i}{C_{ox}} = n_q(\Psi_P - \Psi_S)$$

n_q is the slope factor

- Inversion Charge linearization

*Ref.: Tsividis book & J.M. Sallese et al., Solid State Electronics

Physics of BSIM6 Model

- Using linearization approach and normalization

ACM/EKV/BSIM5 ignored the circled term

$$\ln(q_i)+\ln\left[\frac{2n_q}{\gamma}\left(\frac{2n_q}{\gamma}q_i+2\sqrt{-2q_i+\psi_p}\right)\right]+2q_i=\psi_p-2\phi_f-v_{ch}$$

- No approximation to solve the charge equation compared to other models.

- Solved the charge equation analytically

Drain current with velocity saturation

- Drain current

$$I_D = I_{drift} + I_{diff} = \mu W\left(-Q_i \frac{d\Psi_S}{dx} + V_T \frac{dQ_i}{dx}\right)$$

- Mobility model (ensures symmetry)

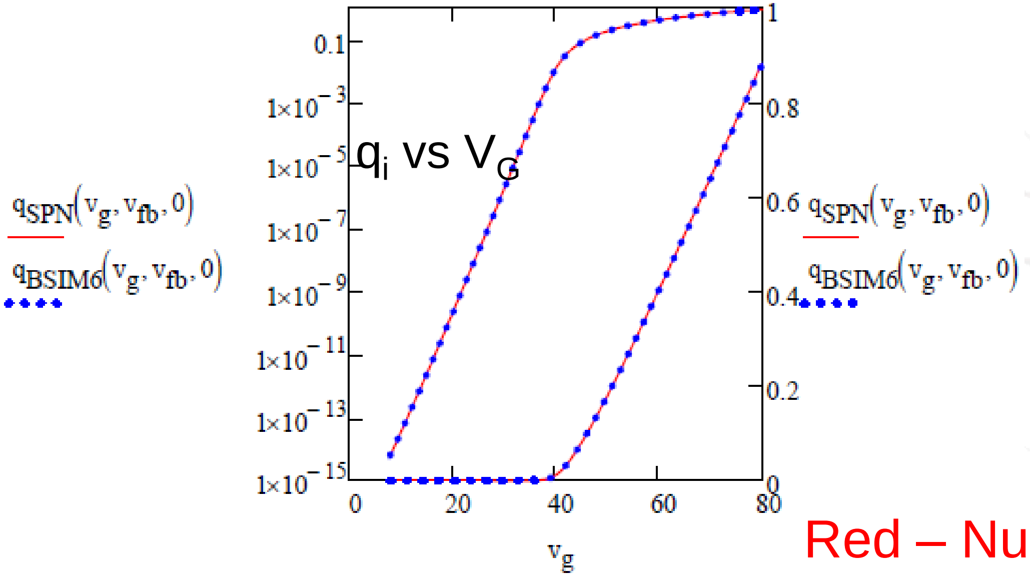
$$I_D = \frac{\mu_v}{\sqrt{1+\left(\frac{\mu_v}{v_{sat}}\left|\frac{d\Psi_S}{dx}\right|\right)^2}} W\left(-Q_i \frac{d\Psi_S}{dx} + V_T \frac{dQ_i}{dx}\right)$$

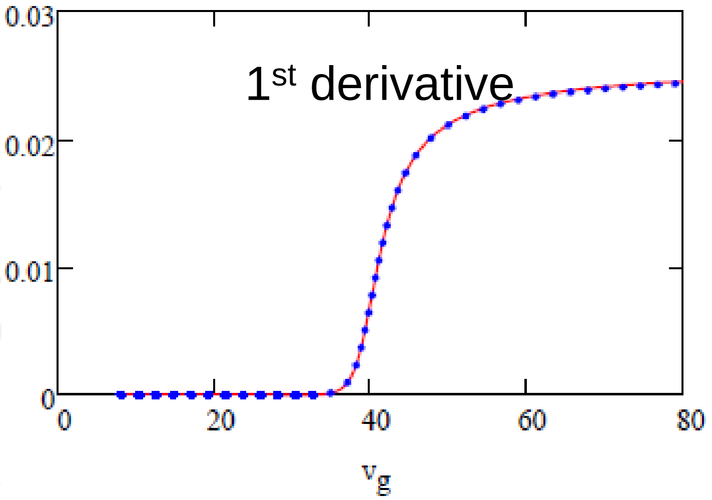
$$-\frac{Q_i}{C_{ox}} = n_q\left(\Psi_P - \Psi_S\right), q = \frac{-Q_i}{2n_q C_{ox} V_T}, i_d = \frac{I_D}{2n_q \frac{W}{L} \mu_v C_{ox} V_t^2}, \lambda_c = \frac{2\mu_v V_t}{v_{sat} L}$$

- Using charge linearization & normalization

$$\boxed{i_d = \frac{\left(q_s^2 + q_s\right) - \left(q_d^2 + q_d\right)}{\frac{1}{2}\left(1 + \sqrt{1 + \left[\lambda_c\left(q_s - q_d\right)\right]^2}\right)}}$$

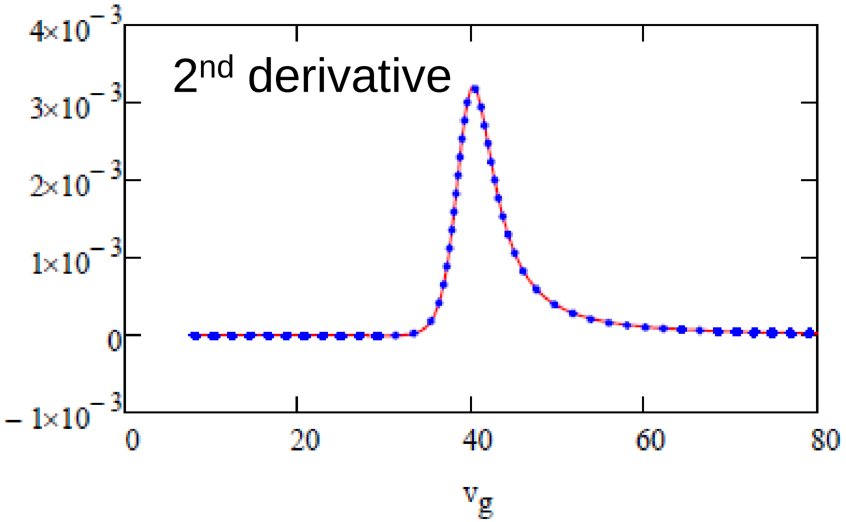
Normalized Q_i-V_G & derivatives

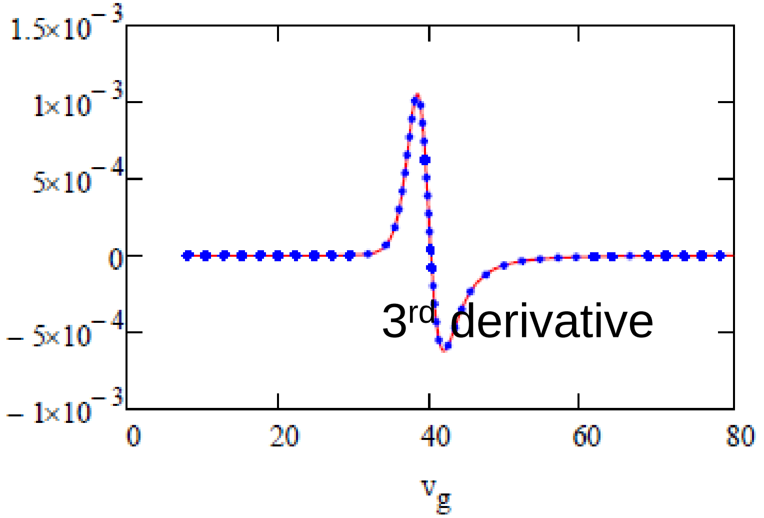




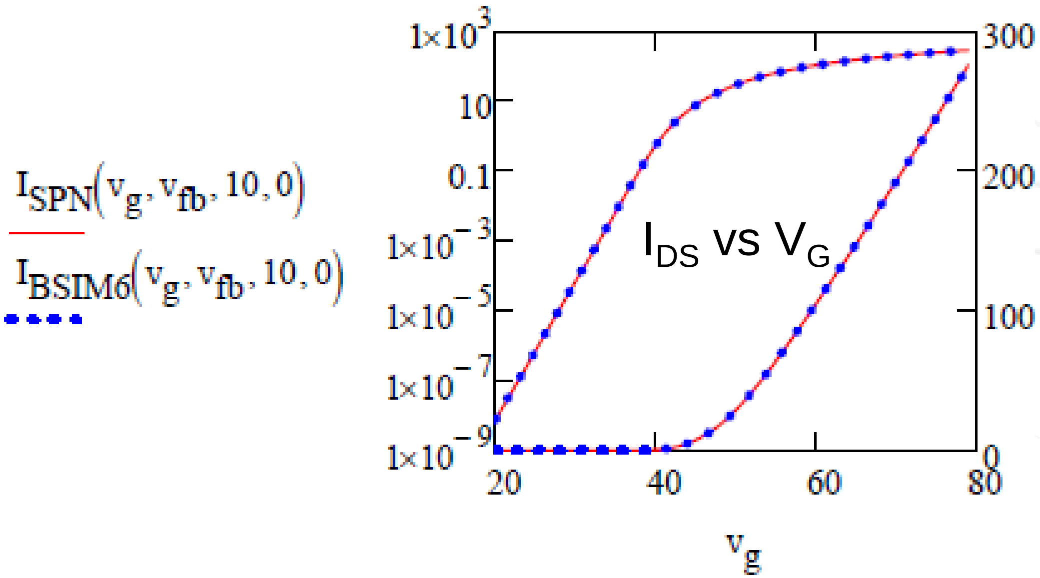
Red – Numerical Surf. Pot. model

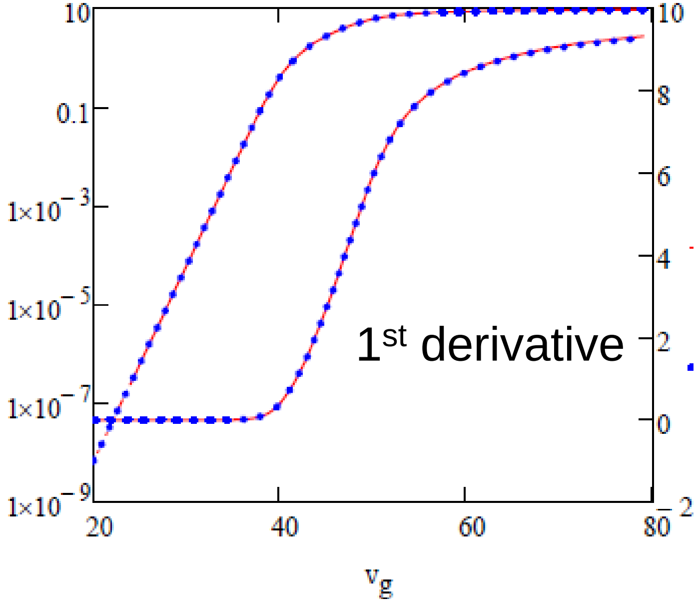
Blue – BSIM6 model

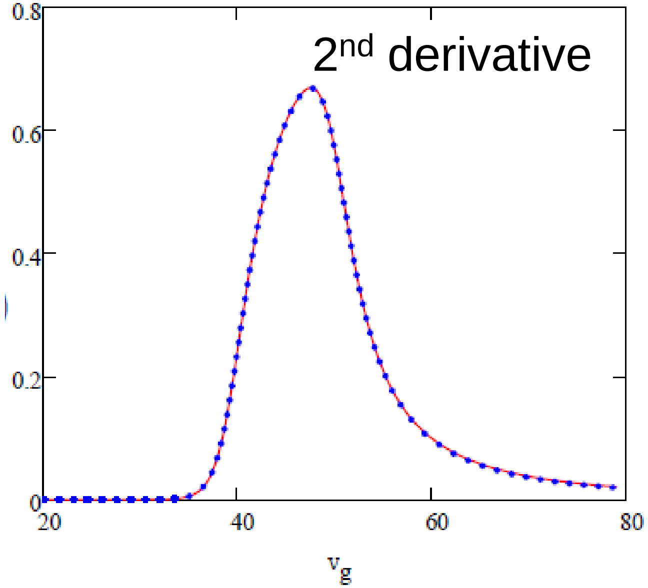




Normalized I_{DS}-V_{GS} & derivatives







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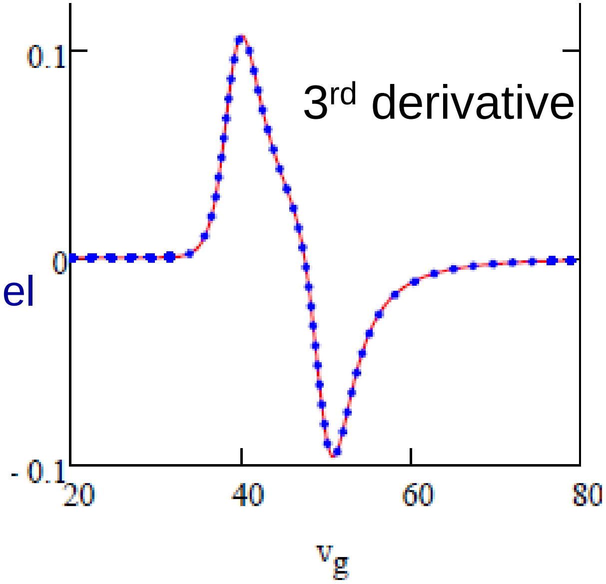


Mobility Model

- Mobility model has been adopted from BSIM4

BSIM4

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left[\frac{V_{gsteff} + C_0 \cdot (VTHO - VFB - \Phi_s)}{TOXE} \right]^{EU} + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)}$$

BSIM6

$$\mu_{eff} = \frac{U0}{1 + (UA + UC \cdot V_{bsx}) \cdot E_{eff}^{EU} + \frac{UD}{\left[\frac{1}{2}\left(1 + \frac{q_{is}}{q_{bs}}\right) \right]^{UCS}}}$$

where

$$\eta = \begin{cases} \frac{1}{2} \cdot ETAMOB & \text{for NMOS} \\ \frac{1}{3} \cdot ETAMOB & \text{for PMOS} \end{cases}$$

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01} - 0.1$$

$$V_{bsx} = -\left[V_s + \frac{1}{2}(V_{ds} - V_{dsx}) \right]$$

$$E_{effs} = 10^{-8} \cdot \left(\frac{q_{bs} + \eta \cdot q_{is}}{\epsilon_{ratio} \cdot Tox} \right)$$

MV/cm

Saturation Voltage V_{dsat}

- V_{ds} to V_{dsat} – BSIM4 formulation causes asymmetry

$$V_{BSIM4}(V_{ds}, V_{dsat}, \delta_0) := V_{dsat} - \frac{1}{2}\cdot\left[(V_{dsat} - V_{ds} - \delta_0) + \sqrt{(V_{dsat} - V_{ds} - \delta_0)^2 + 4\cdot\delta_0\cdot V_{dsat}}\right]$$

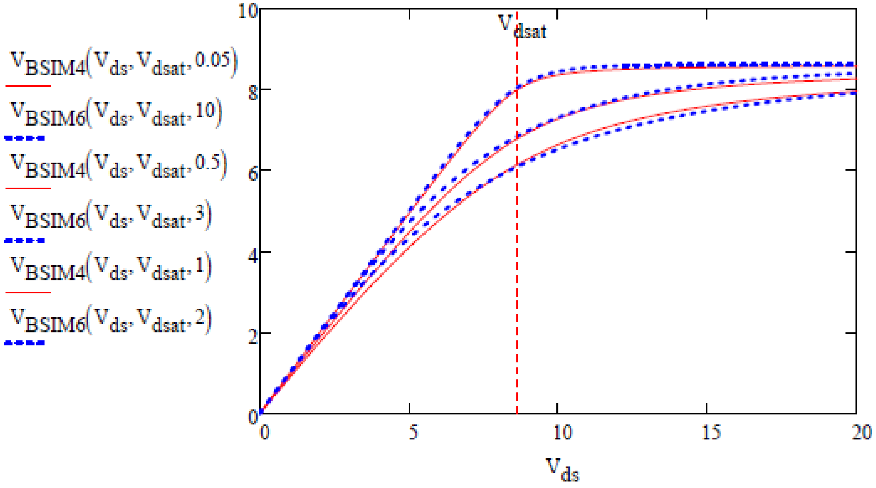
- New V_{dsat} evaluation:

$$\lambda_c = \frac{2\mu_{effs} V_t}{VSAT \bullet L_{eff}}$$

$$q_{dsat} = \frac{1}{2} KSATIV \bullet \lambda_c \bullet \frac{q_s^{\ 2} + q_s}{1 + \frac{1}{2}\lambda_c (1 + q_s)}$$

$$v_{dsat} = \frac{V_{dsat}}{V_t} = \psi_p - 2\varphi_f - 2q_{dsat} - \ln\left[\frac{2q_{dsat}\cdot n_q}{\gamma}\left(\frac{2q_{dsat}\cdot n_q}{\gamma} + \frac{\gamma}{n_q - 1}\right)\right]$$

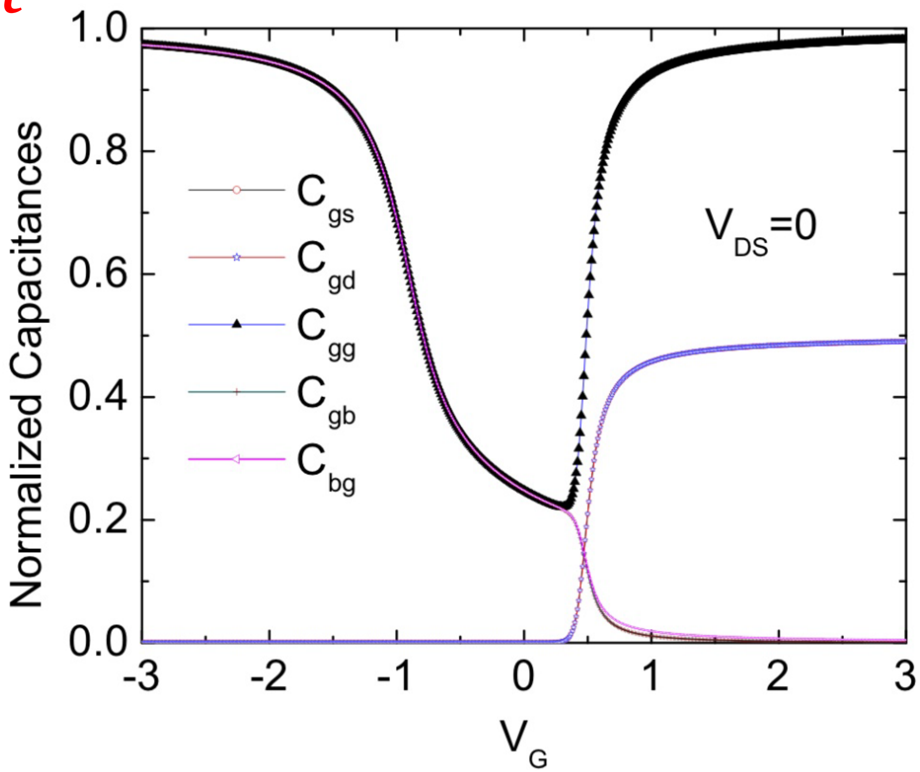
$$V_{dseff} = \frac{V_{ds}}{\left[1 + \left(\frac{V_{ds}}{V_{dsat} - V_s}\right)^{1/DELTA}\right]^{DELTA}}$$



CV Model

- Physical Capacitance Model
- Poly-depletion & *Quantum Mechanical Effect*
- Channel Length Modulation
- *Velocity Saturation Effect*

- Charge conservation



Junction capacitance model

- BSIM4 junction capacitance model gave asymmetry
- Updated diode junction capacitance model for AC symmetry

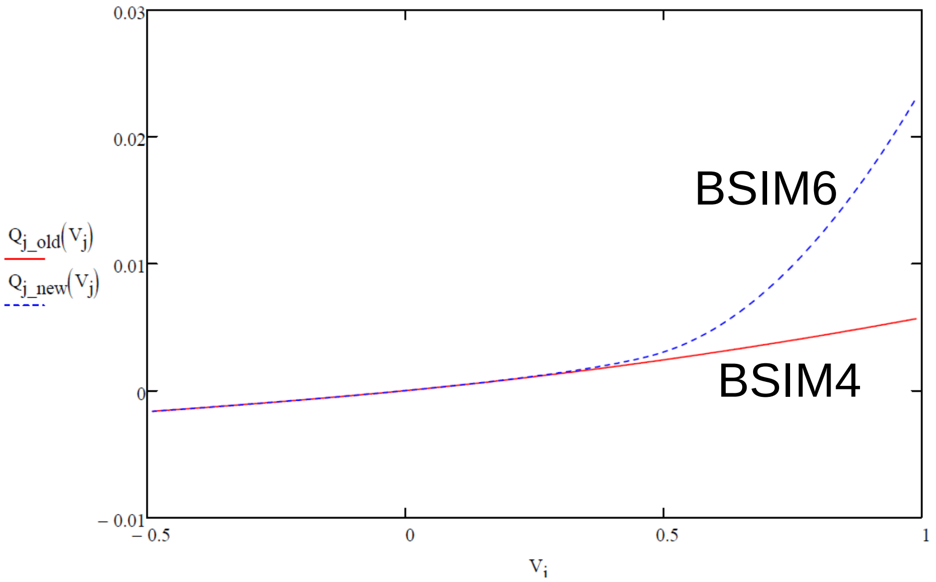
$$Q_{j\_old}(V_j) := \begin{cases} C_j \cdot PBS \cdot \dfrac{1 - \left(1 - \dfrac{V_j}{PBS}\right)^{1-MJS}}{1 - MJS} & \text{if } V_j < 0 \\ 0 & \text{if } V_j = 0 \\ V_j \cdot C_j + V_j^2 \cdot \dfrac{MJS \cdot C_j}{2 \cdot PBS} & \text{if } V_j > 0 \end{cases}$$

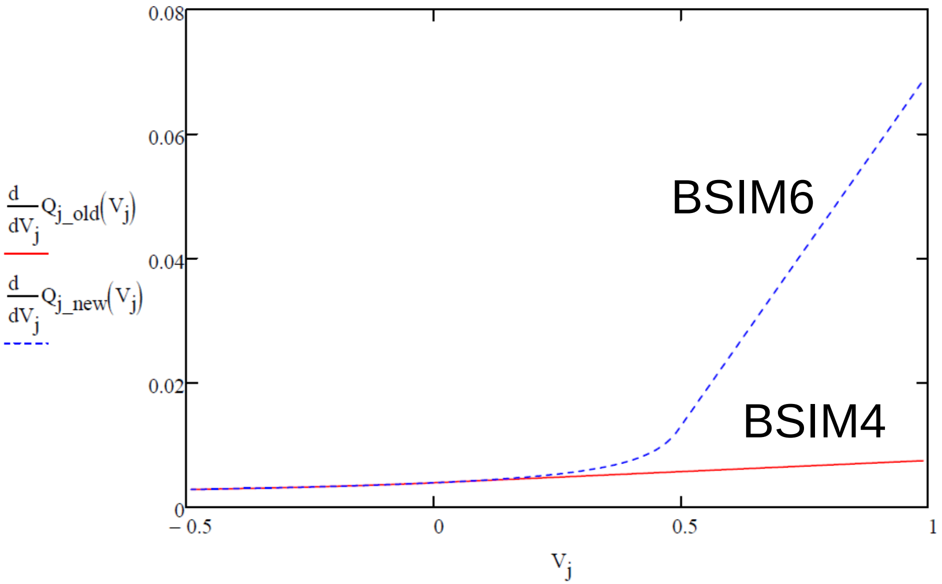
Transition point is at $V_j=0$

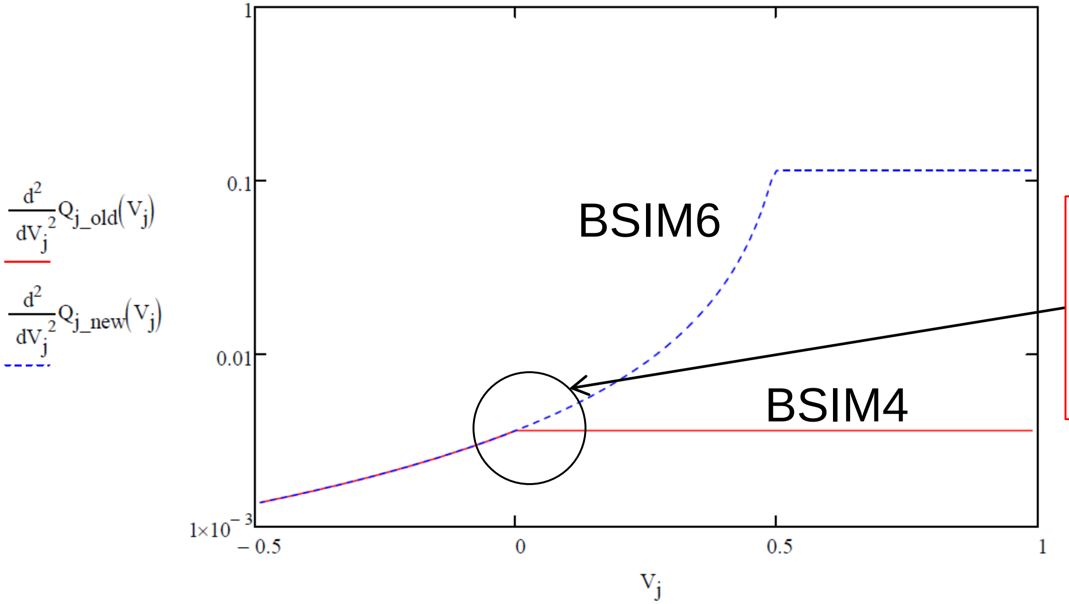
$$Q_{j\_new}(V_j) := \begin{cases} x_0 \leftarrow 0.9 & \\ C_j \cdot PBS \cdot \dfrac{1 - \left(1 - \dfrac{V_j}{PBS}\right)^{1-MJS}}{1 - MJS} & \text{if } \dfrac{V_j}{PBS} < x_0 \\ C_j \cdot PBS \cdot \dfrac{1}{(1 - x_0)^{MJS}} \cdot \left(1 - \dfrac{V_j}{PBS}\right) \cdot \left[\dfrac{1}{2} \cdot MJS \cdot \dfrac{1}{(1 - x_0)} \cdot \left(1 - \dfrac{V_j}{PBS}\right) - (1 + MJS)\right] + C_j \cdot \dfrac{PBS}{1 - MJS} \cdot \left[1 - \dfrac{MJS}{2} \cdot (1 + MJS) \cdot (1 - x_0)^{1-MJS}\right] & \text{otherwise} \end{cases}$$

Transition point is at $V_j=0.9V$ (pushed to strong forward bias)

Junction capacitance model



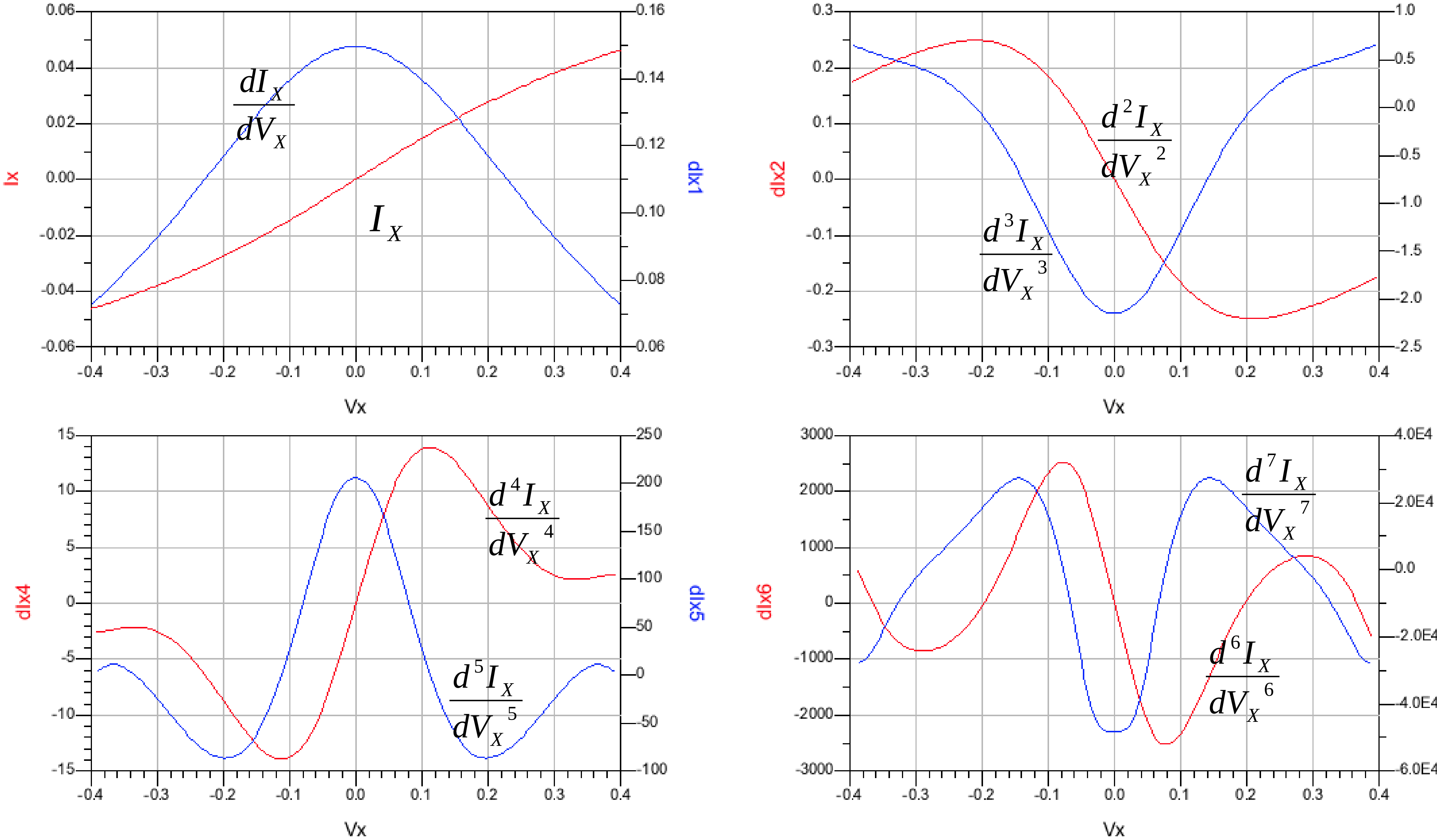




- Symmetry problem using old Q_j
- New model is infinitely differentiable @ V_{DS}=0

I_X vs V_X ($V_D=V_X$ & $V_S=-V_X$)

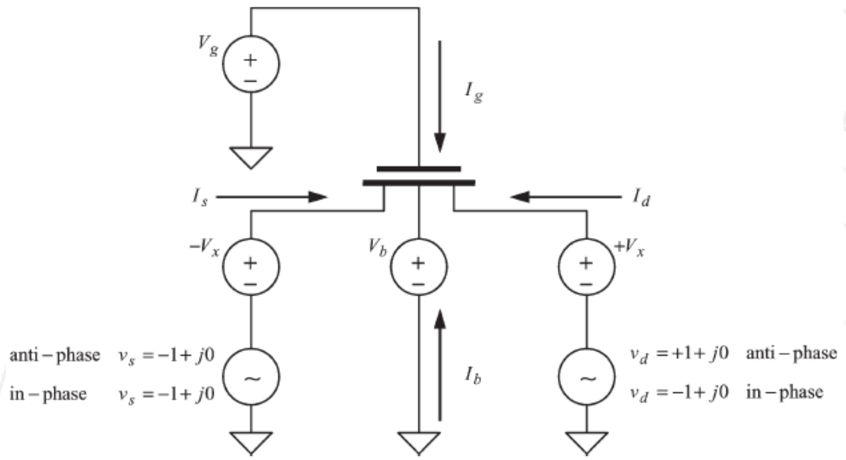
I_{DS}-V_X Gummel Symmetry



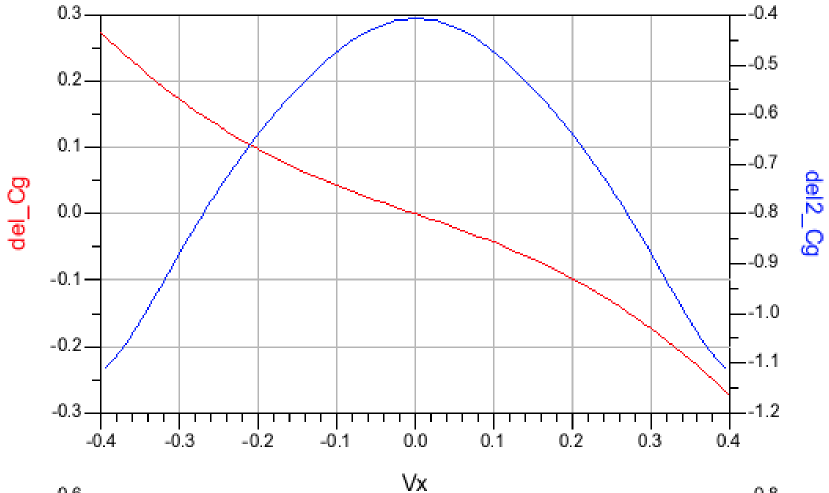
All derivatives are continuous at $V_{DS}=0$

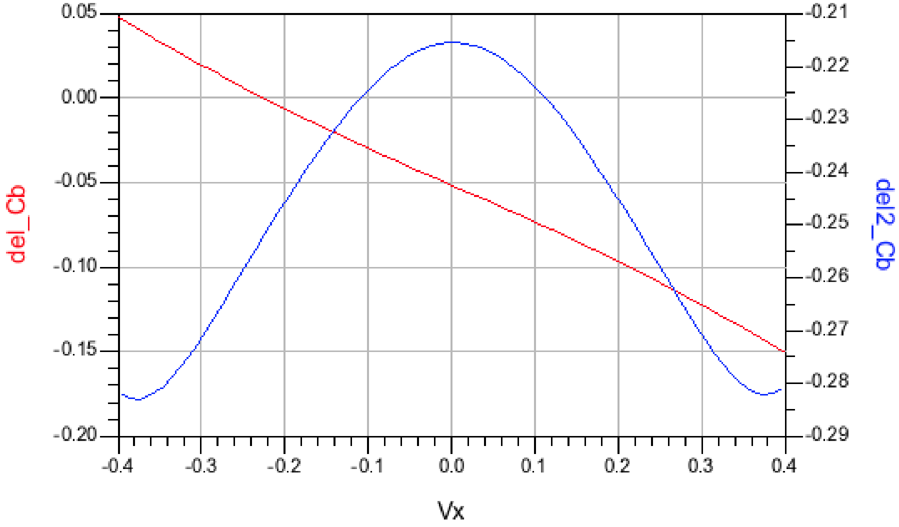
AC Symmetry test

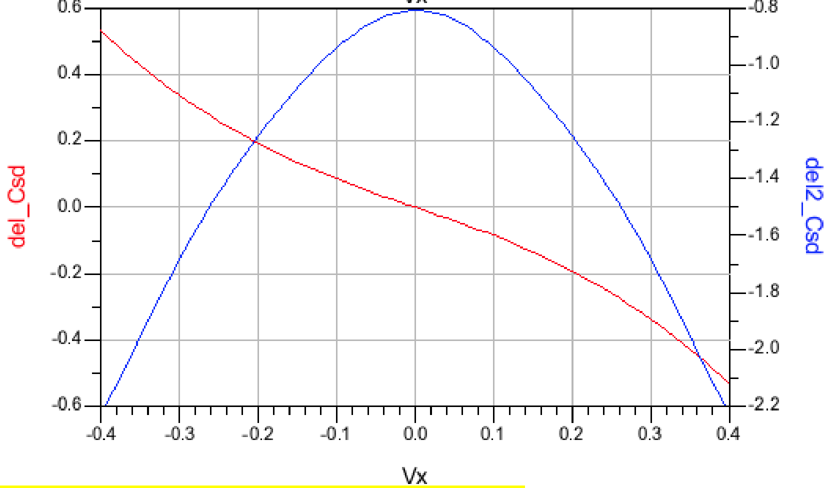
(C. McAndrew, IEEE TED, 2006)



Capacitance & derivatives are symmetric

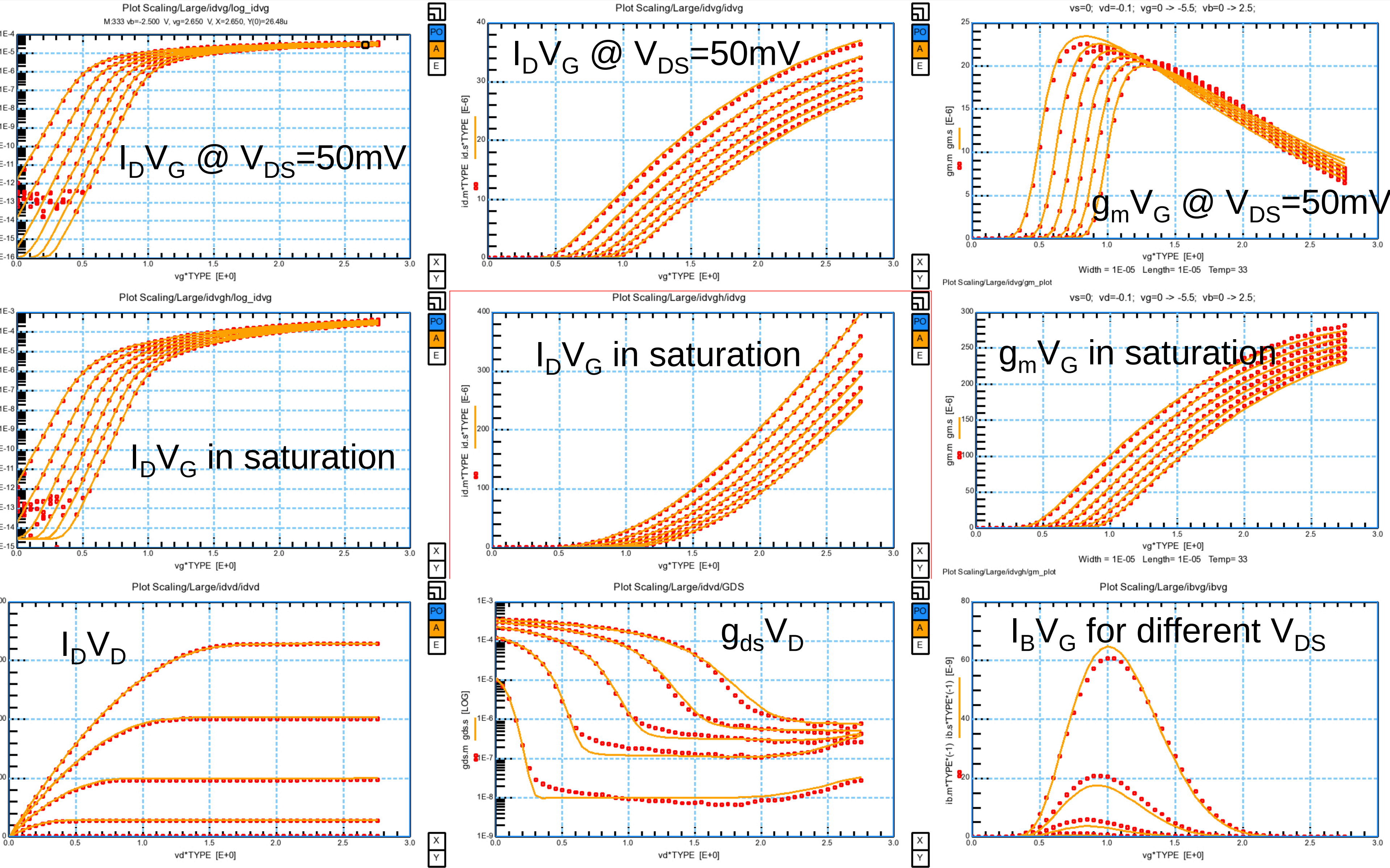




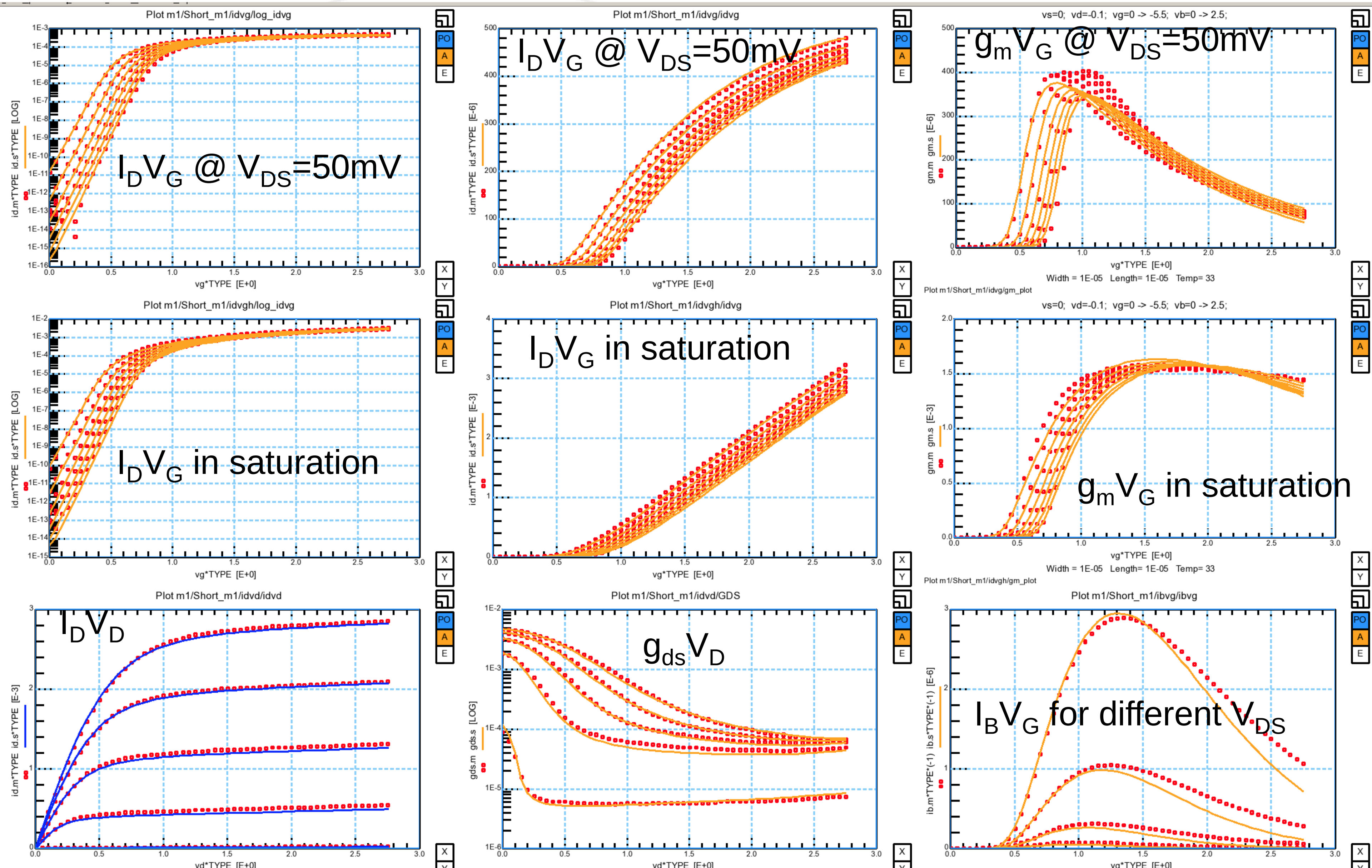


Capacitances and derivatives are continuous at V_{DS}=0

Validation on Measured Data (Large device)



Validation on Measured Data (Short device)



I_DV_G @ V_{DS}=50mV

I_DV_G @ V_{DS}=50mV

g_mV_G @ V_{DS}=50mV

I_DV_G in saturation

I_DV_G in saturation

g_mV_G in saturation

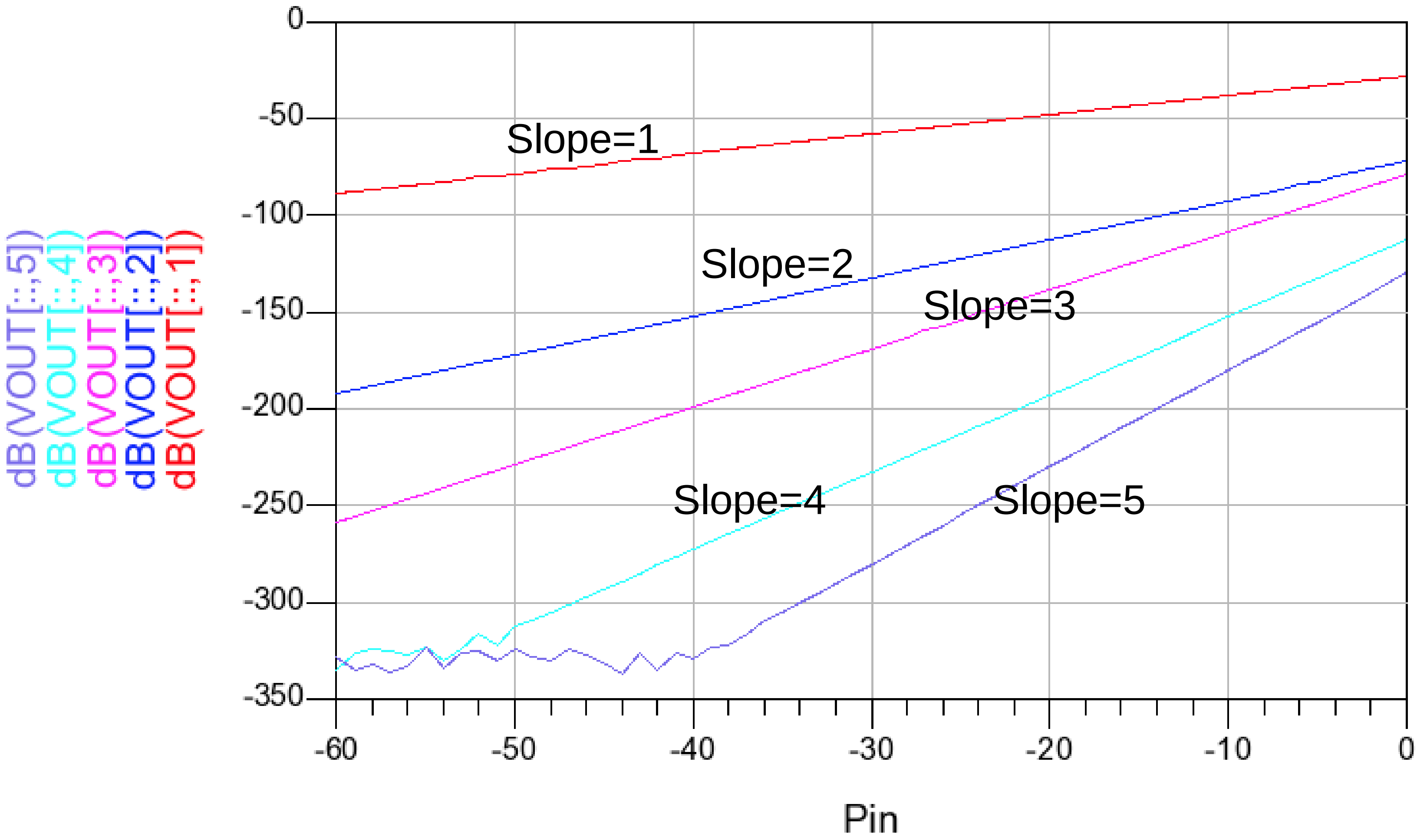
I_DV_D

$g_{ds}V_D$

I_BV_G for different V_{DS}

Harmonic Balance Simulation

- BSIM6 gives correct slope for all harmonics



BSIM6 model summary

- Rapid development: Released **BSIM6.0.0-beta8 in Aug. 2012**
- Charge based physical compact model
  - Physical effects & Parameter names matched to BSIM4
  - Smooth charge/current/capacitance & derivatives
- Symmetric and continuous around $V_{DS}=0$
  - Fulfills Gummel symmetry and AC symmetry
  - Shows accurate slope for harmonic balance simulation
- BSIM4's extraction methodology can be easily used for BSIM6 – fast deployment & lower cost
- Under standardization review in CMC

Outline

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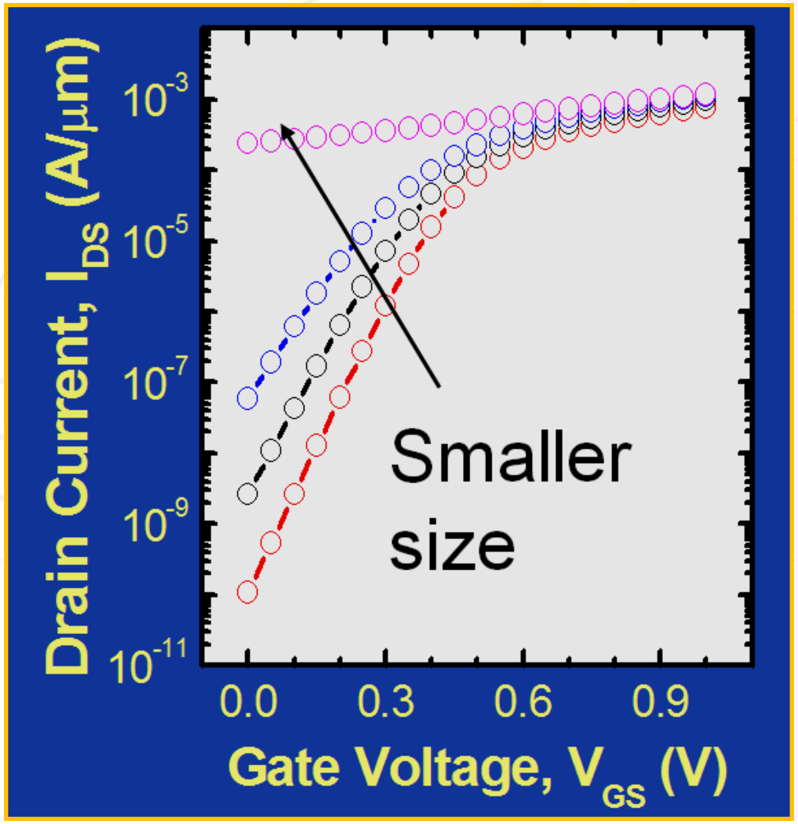
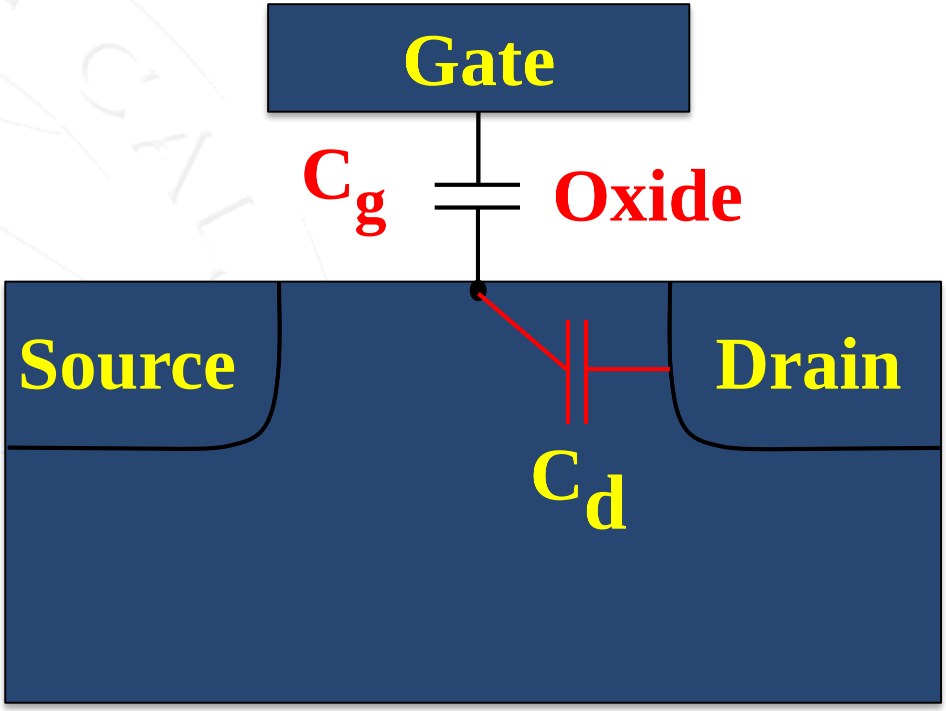
- BSIM-IMG Model

Why next generation transistors?

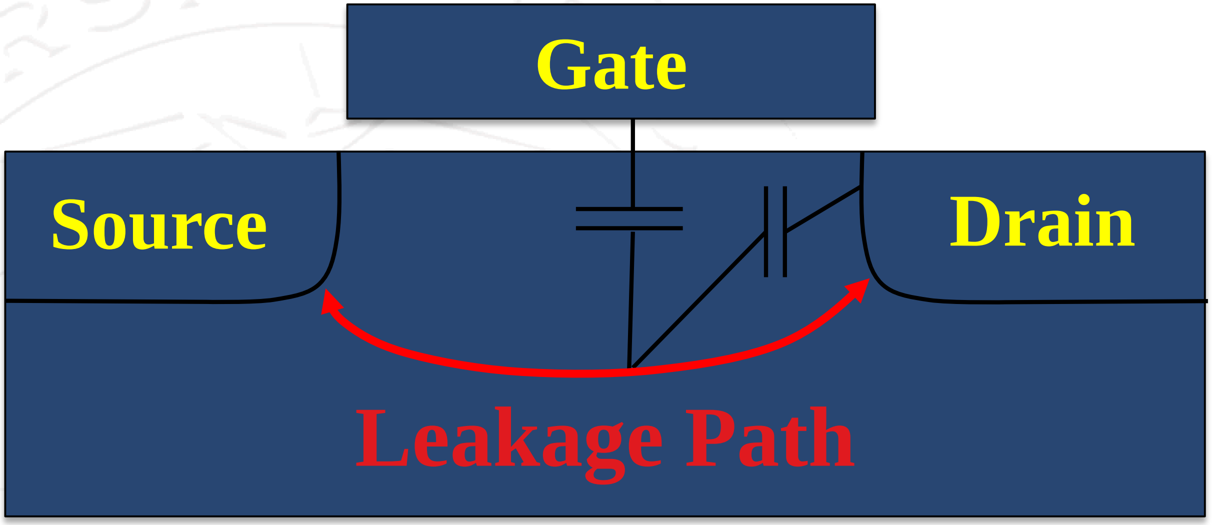




MOSFET becomes “resistor” at small L.

C.Hu, “Modern Semicon. Devices for ICs” 2010, Pearson

Making Oxide Thin is Not Enough



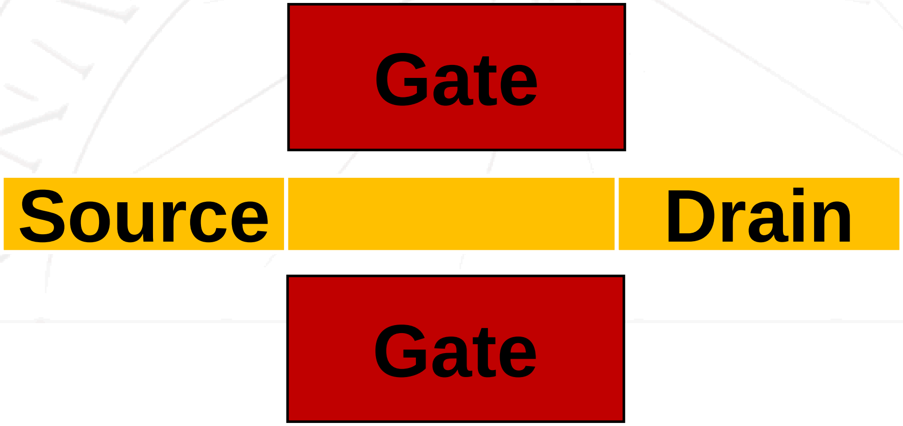
Gate cannot control the leakage current paths that are far from the gate.

C.Hu, “Modern Semicon. Devices for ICs” 2010, Pearson

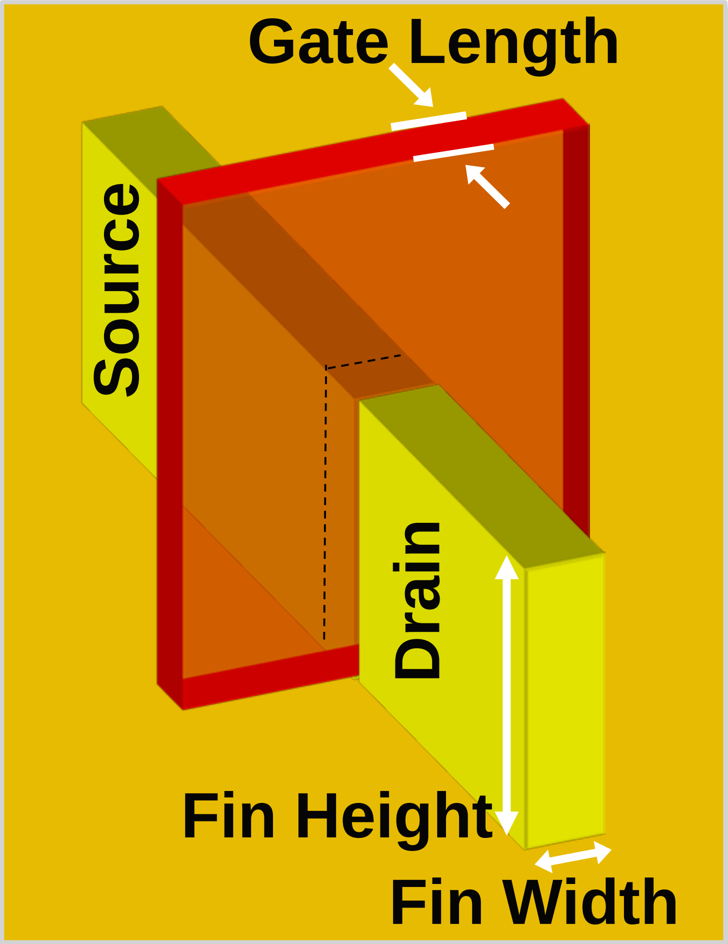
One Way to Eliminate Si Far from Gate

Thin body controlled

By multiple gates.

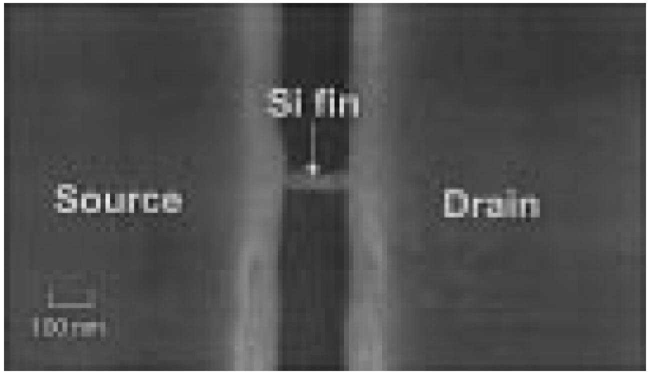


FinFET body is a thin Fin.

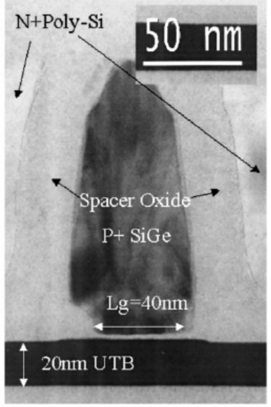


N. Lindert et al., DRC paper II.A.6, 2001

New MOSFET Structures: Demonstratio



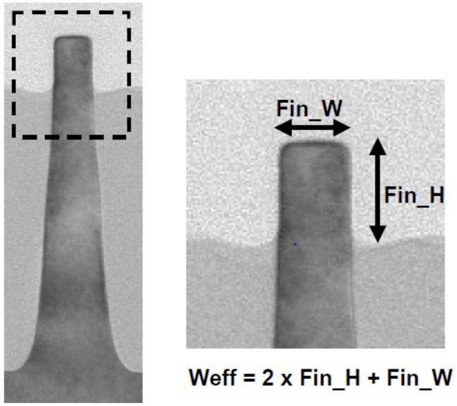
*X. Huang et al. IEDM 1999 (**UC Berkeley**)*



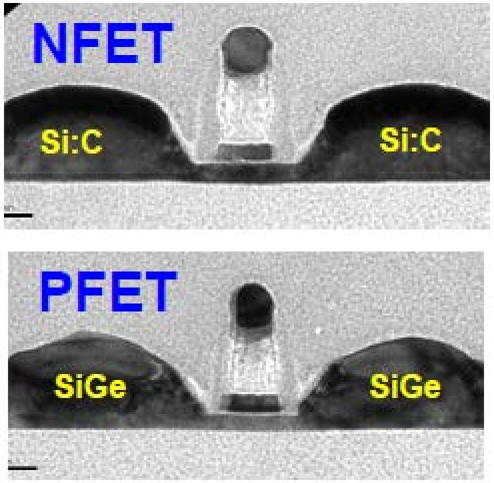
*Y. Choi et al. IEEE EDL 2000- (**UC Berkeley**)*

FinFET

UTBSOI

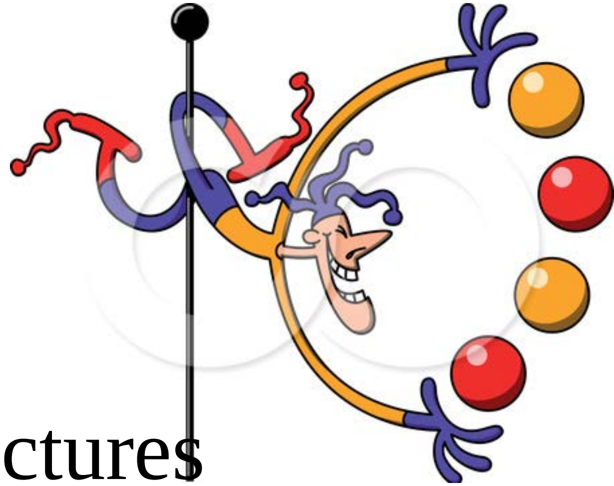


C.C. Wu et al. IEDM 2010 (TSMC)



K. Cheng et al. IEDM 2009 - (IBM / ST)

Challenges in developing a new model



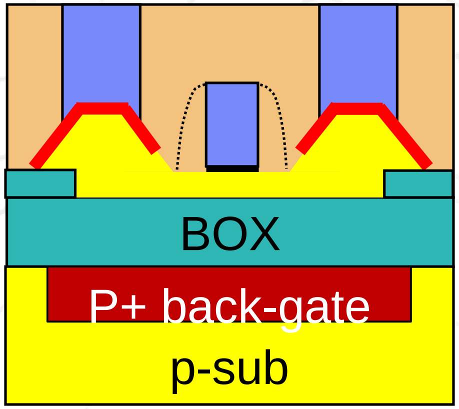
- New Physics
  - Fully depleted channel
  - Quantum confinement etc.
  - When to include them?
- Support Multiple Device architectures
- Inertia with BSIM4 – Large user base
  - Familiarity with the parameters
- Convergence – Model behavior in extreme cases
- Balance Physics and Flexibility
- Balance Speed and Accuracy

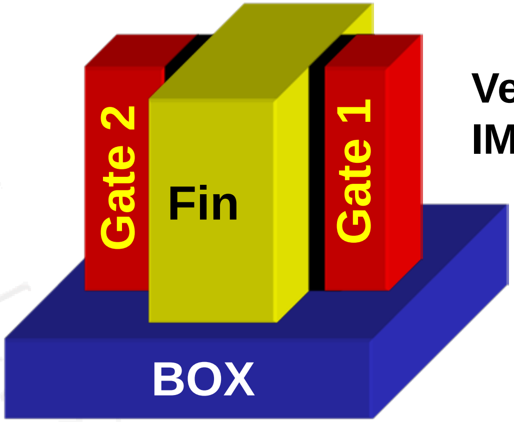
Multi-Gate Compact Model: BSIM-MG

BSIM-IMG

UTBSOI

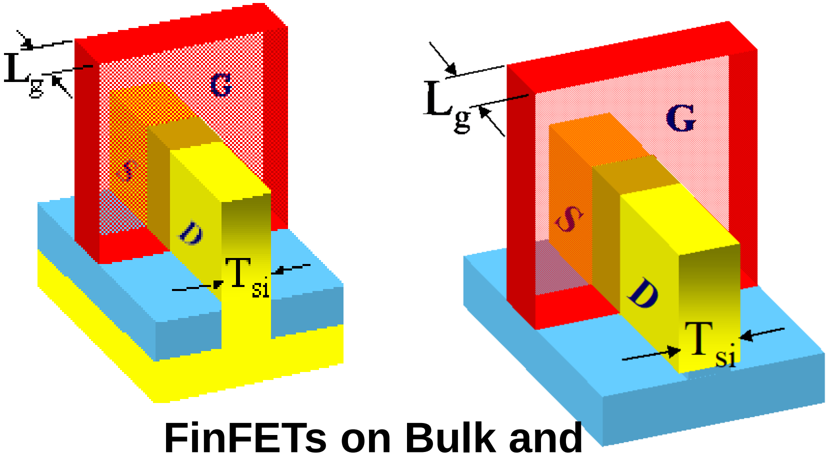
BG-ETSOI



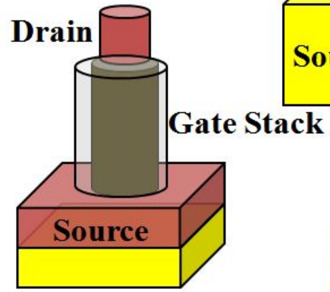


Vertical Fin IMG

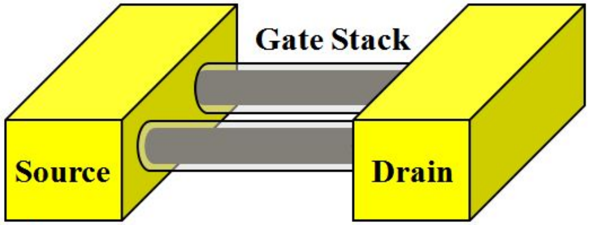
BSIM-CMG



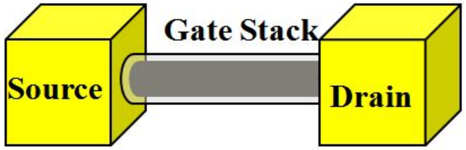
FinFETs on Bulk and SOI Substrates



Vertical CG FET



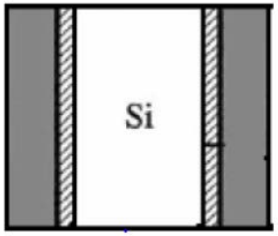
Twin Silicon Nanowire FET



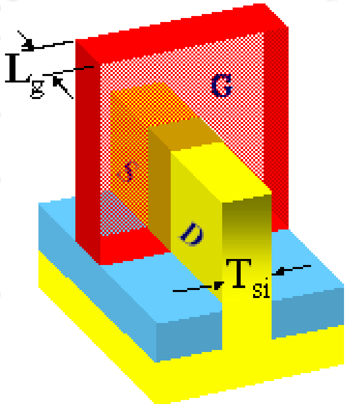
Horizontal Nanowire FET

BSIM-CMG Core Models

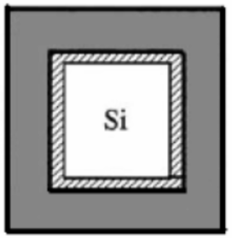
- Four device architectures



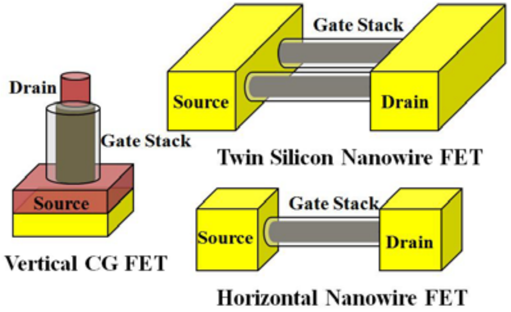
Double Gate



Double Gate / Trigate / FinFET



Quadruple Gate



Cylindrical Gate / Nanowire FET

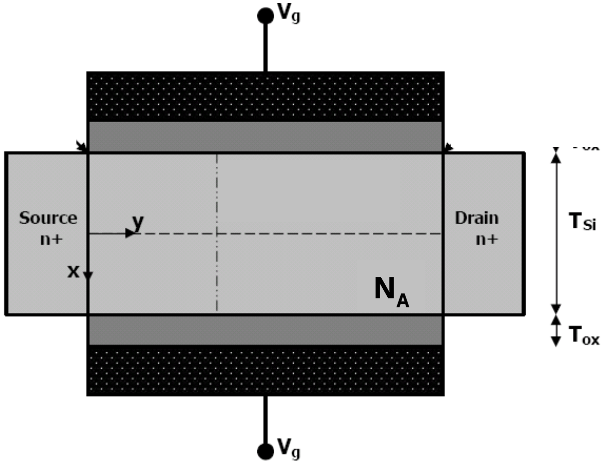
- Three core models
  - Intrinsic Double Gate Core (Y. Taur et al., IEEE EDL, 2004)
  - Perturbation based DG Core for high-doping
  - Cylindrical Gate Core
- Bulk and SOI Substrate

Surface Potential Core – Double Gate

- Solution of Poisson’s equation and Gauss’s Law.
- Poisson’s equation inside the body can be written as (V_{ch} is channel potential)

$$\frac{d^2\psi}{dx^2} = \frac{q n_i}{\epsilon_{Si}} \cdot \left(\underbrace{e^{\frac{q\psi}{kT}} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{-\frac{qV_{ch}}{kT}}}_{\text{Inversion Carriers}} + \underbrace{e^{\frac{q\phi_B}{kT}}}_{\text{Body Doping}} \right)$$

where $\phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$



- Body doping complicates the solution of the Poisson’s equation.
- Perturbation approach is used to solve this problem.

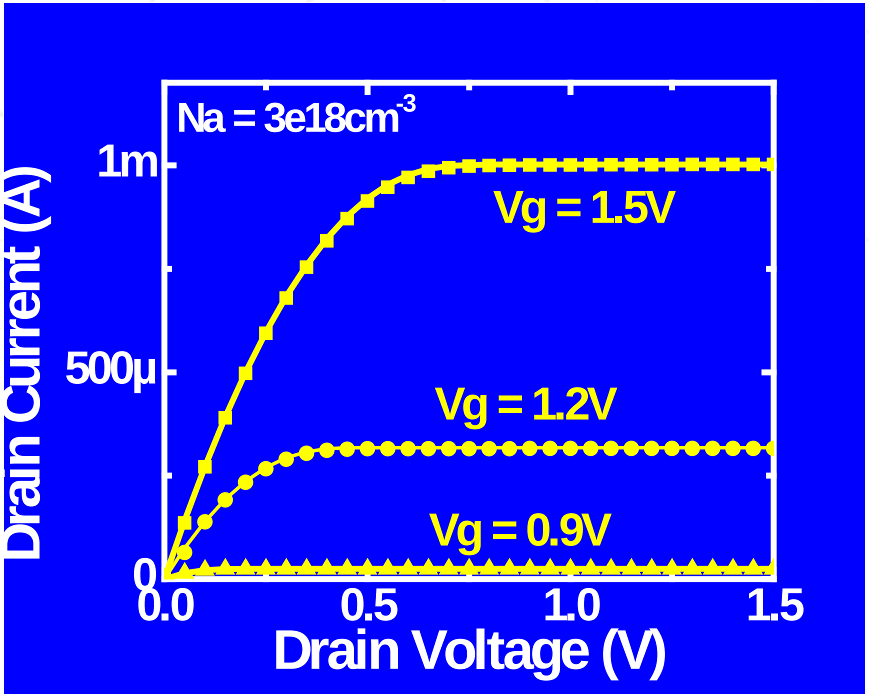
M. Dunga et al., IEEE TED, Vol. 53, No. 9, 2006

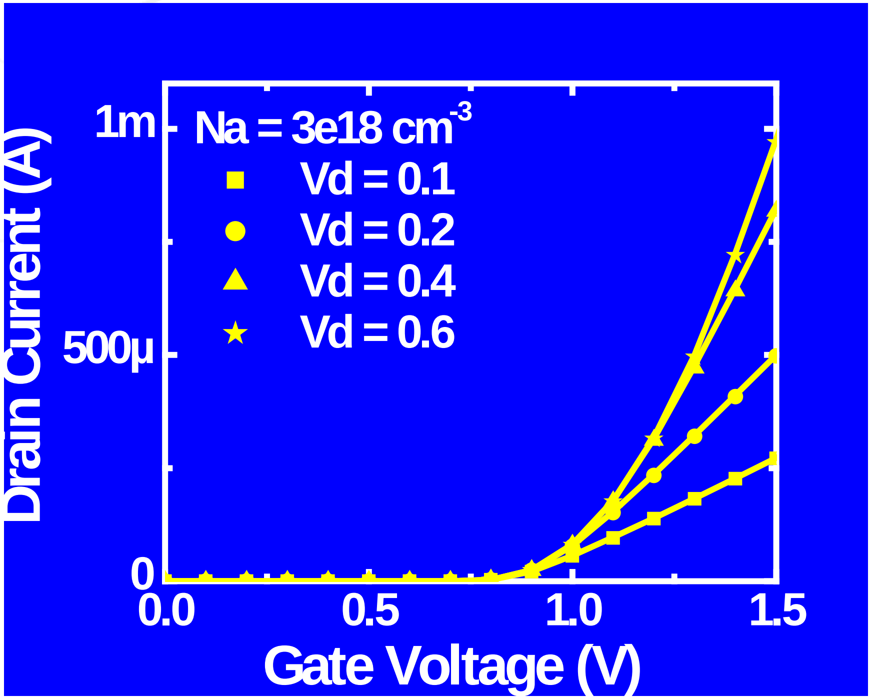
M. Dunga et al., VLSI 2007

Core Drain Current Model

- No charge sheet approximation

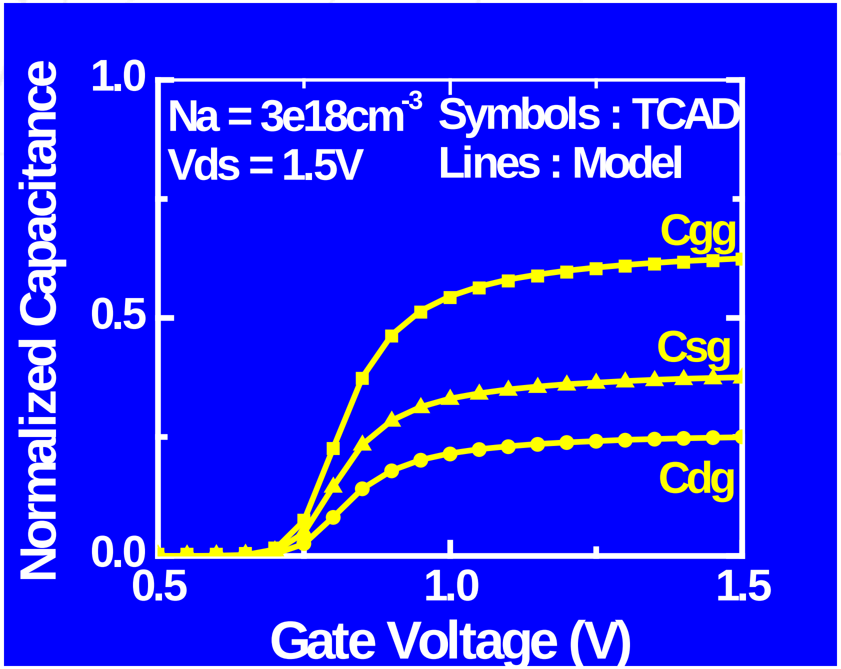
$$\mathrm{Id} = \mu \frac{W_{eff}}{L} \left[\frac{Q_i^2}{2C_{ox}} + 2\,\mathrm{V_t}\,\mathrm{Q_i} - \mathrm{V_t} \cdot \left(5\mathrm{C_{Si}}\mathrm{V_t} + \mathrm{Q_B}\right) \ln\left(5\mathrm{V_t}\mathrm{C_{Si}} + \mathrm{Q_B} + \mathrm{Q_i}\right) \right]_{\mathrm{d}}^{\mathrm{s}}$$

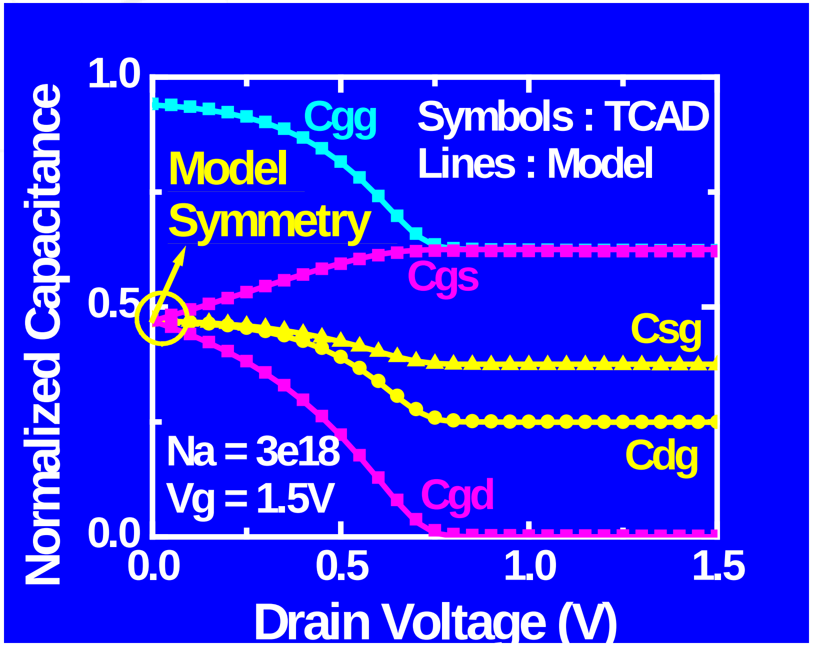




Core Capacitance Model

- Model inherently exhibits symmetry
  - $C_{ij} = C_{ji}$ @ $V_{ds} = 0$ V
- Model matches TCAD data (No parameter used)
- Accurate short channel behavior





Symbols: TCAD Results; Lines: Model

Short Channel (2D) Effects

- Quasi-2D analysis

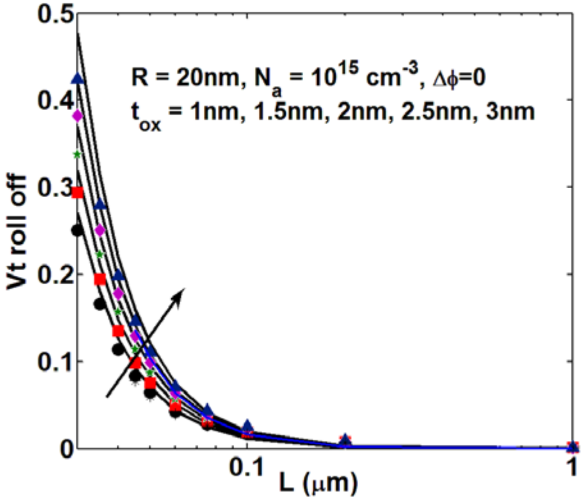
Characteristic Length

$$H_{eff} = \sqrt{\frac{HFIN}{8} \cdot (HFIN + 2 \cdot \epsilon_{ratio} \cdot EOT)}$$

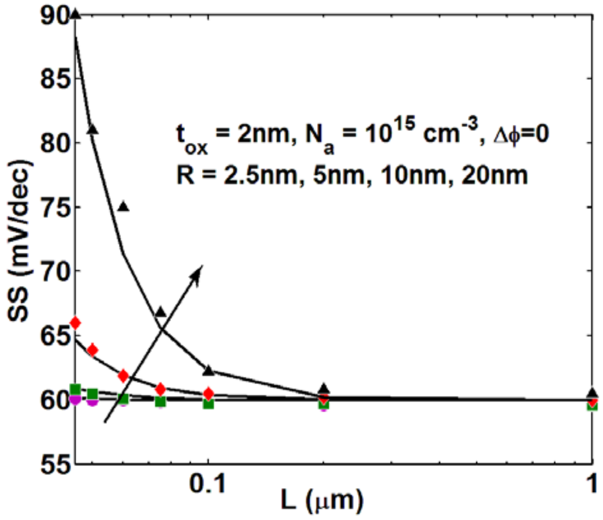
$$\lambda = \begin{cases} \sqrt{\frac{\epsilon_{ratio}}{2}\left(1 + \frac{TFIN}{4\epsilon_{ratio}EOT}\right) TFIN \cdot EOT} & \text{if } GEOMOD = 0 \\ \dfrac{1}{\sqrt{\frac{1}{\frac{\epsilon_{ratio}}{2}\left(1+\frac{TFIN}{4\epsilon_{ratio}EOT}\right)TFIN \cdot EOT} + \frac{1}{4H_{eff}^2}}} & \text{if } GEOMOD = 1 \\ \dfrac{0.5}{\sqrt{\frac{1}{\frac{\epsilon_{ratio}}{2}\left(1+\frac{TFIN}{4\epsilon_{ratio}EOT}\right)TFIN \cdot EOT} + \frac{1}{4H_{eff}^2}}} & \text{if } GEOMOD = 2 \\ \sqrt{\frac{\epsilon_{ratio}}{2}\left(1 + \frac{R}{2\epsilon_{ratio}EOT}\right) R \cdot EOT} & \text{if } GEOMOD = 3 \end{cases}$$

- Analytical expressions model

Auth and Plummer, IEEE EDL, 2007

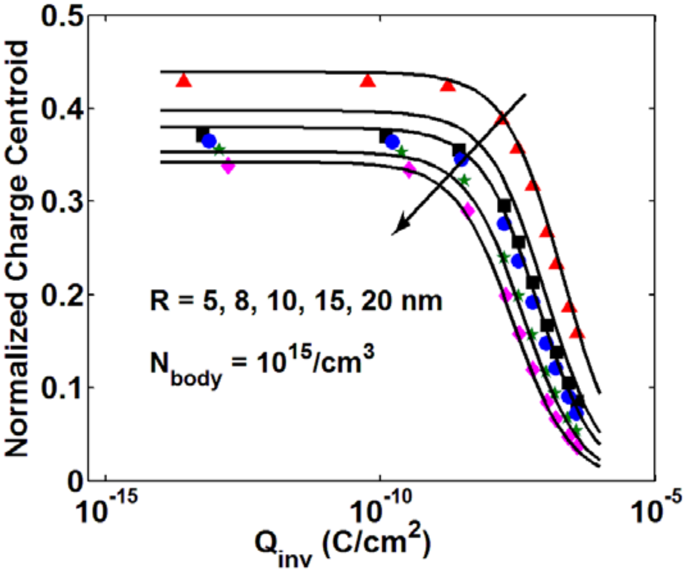


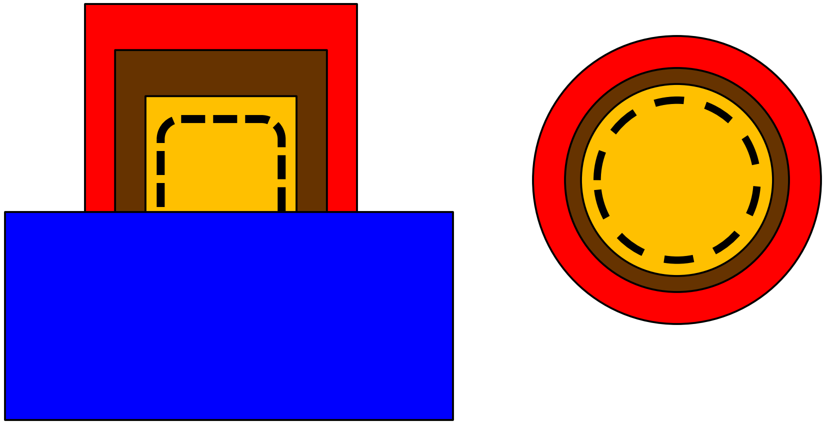
Symbols: TCAD Results; Lines: Model



Quantum Mechanical Effects

- Predictive model for confinement induced Vth shift due to band splitting present in the model
- Effective Width model that accounts for reduction in width for a triple/ quadruple/ surround gate structure

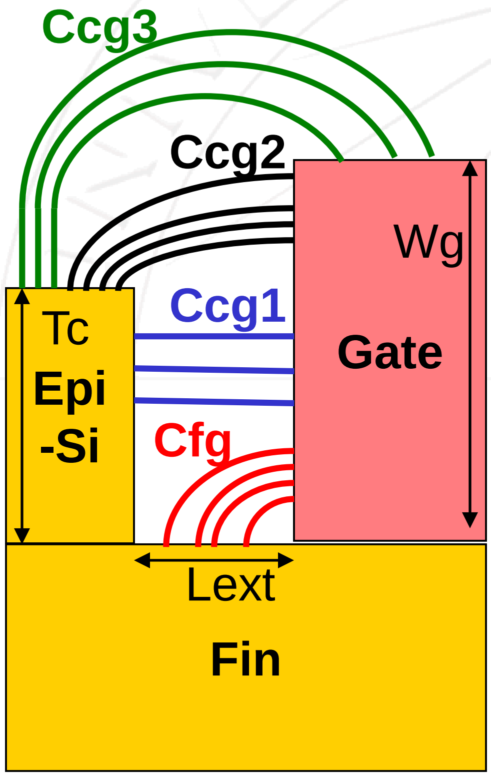


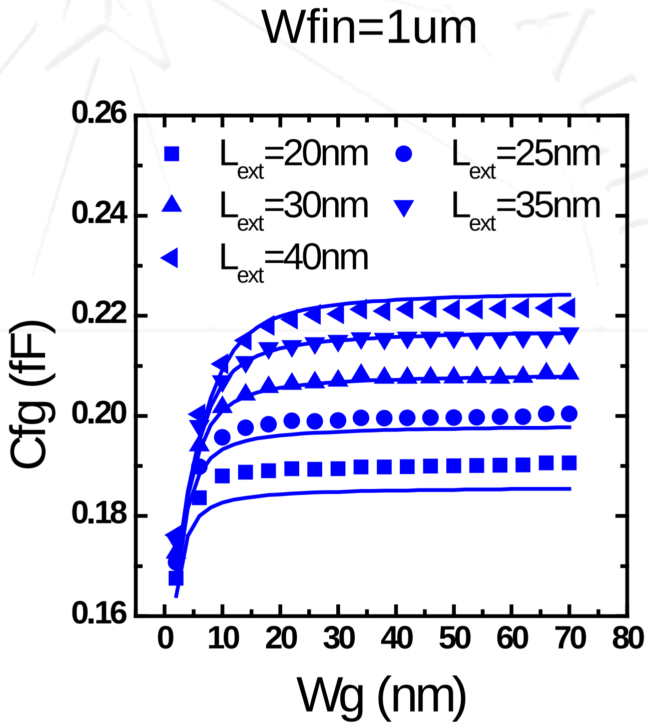


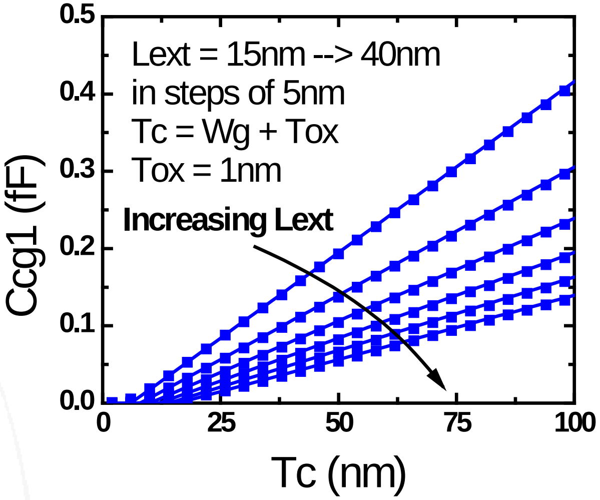
Width reduction due to structural confinement of inversion charge. (Dotted lines represent the effective width perimeter)

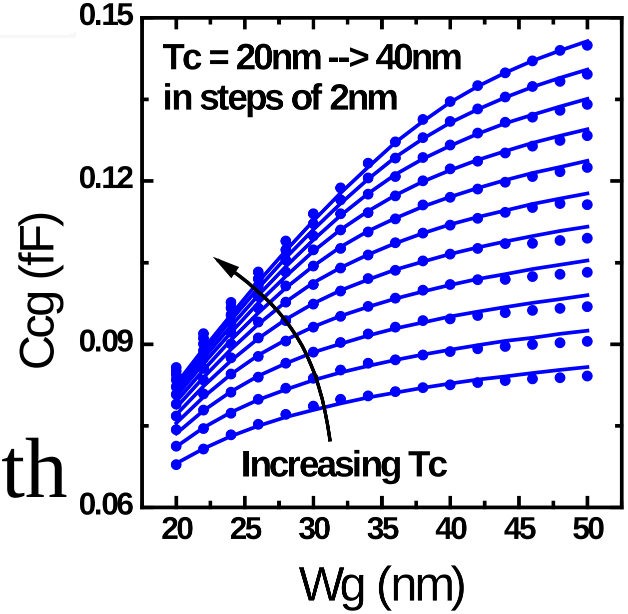
FinFET C_{fr} Modeling – TCAD Verificatio

- C_{fg}: fin ➔ gate
- $C_{cg}=C_{cg1}+C_{cg2}+C_{cg3}$: contact ➔ gate



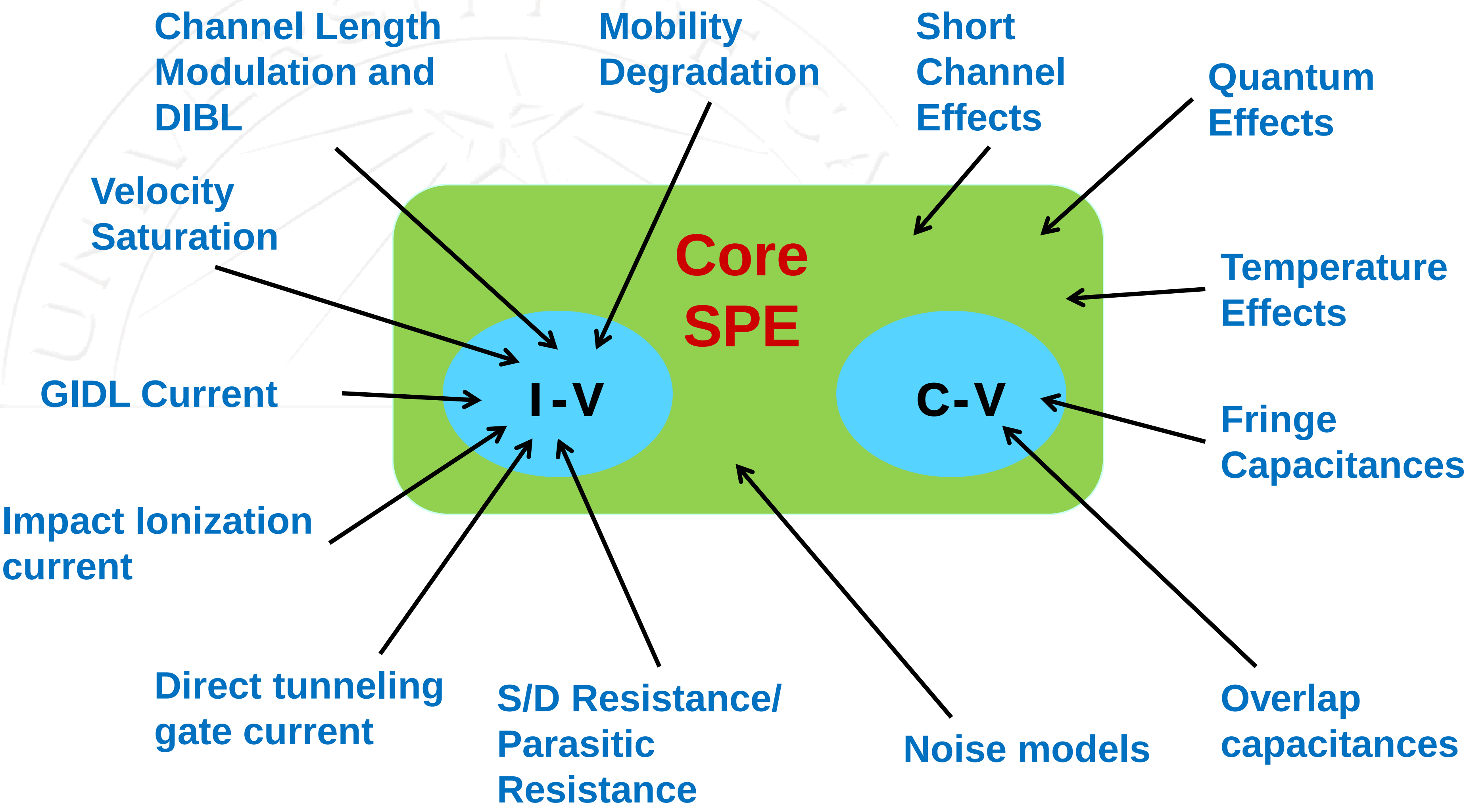






- Both C_{fg} and C_{cg} agree well with 2D numerical simulations

Real Device Effects



Channel Length Modulation and DIBL

Mobility Degradation

Short Channel Effects

Quantum Effects

Velocity Saturation

Core SPE

Temperature Effects

GIDL Current

I-V

C-V

Fringe Capacitances

Impact Ionization current

Direct tunneling gate current

S/D Resistance/ Parasitic Resistance

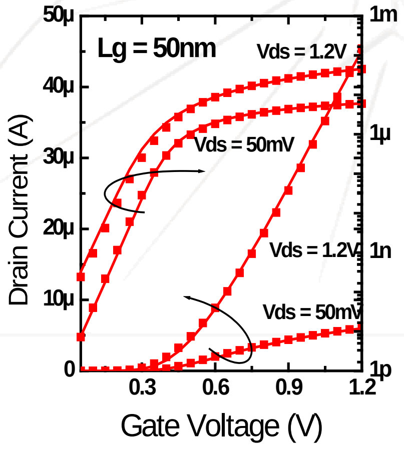
Noise models

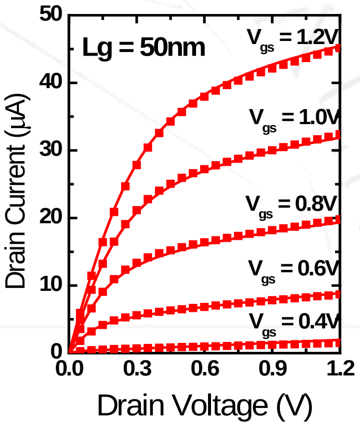
Overlap capacitances

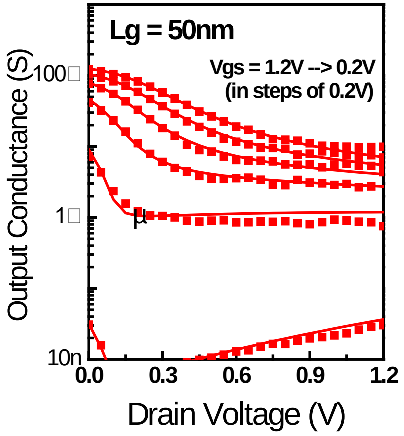
Bulk FinFET Fitting

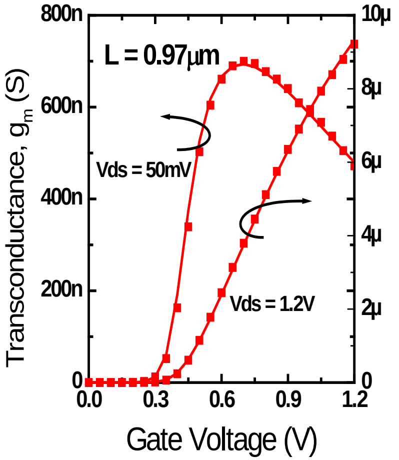
- Bulk FinFETs are fabricated by TSMC
- T_{FIN}=25nm, H_{FIN}=27.5nm, EOT=2.42nm

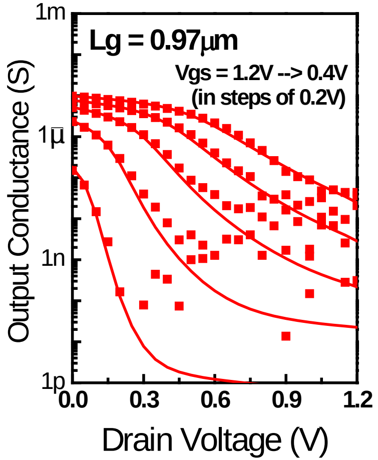
Symbols: Data
Lines: Model

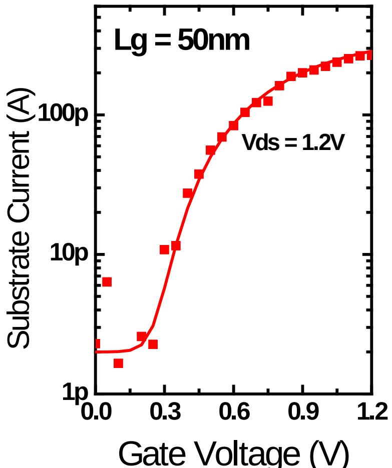

Drain Current vs. V_{gs} (Lg = 50nm)


Drain Current vs. V_{ds} (Lg = 50 nm)


Output Conductance (Lg = 50nm)


Transconductance (Lg = 0.97μm)


Output Conductance (Lg = 0.97 μm)

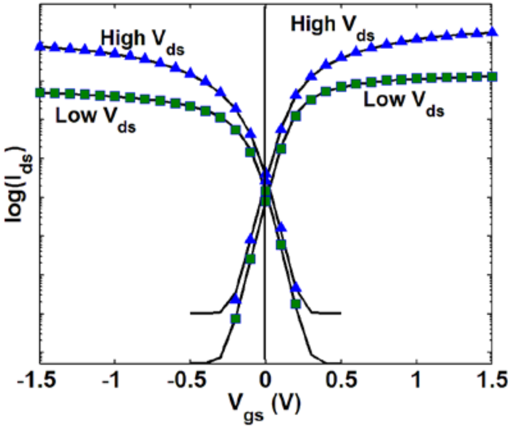

Substrate Current (Lg = 50nm)

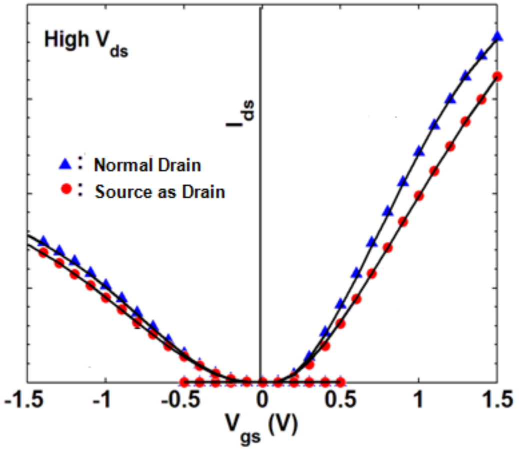
Asymmetric Vertical Nanowire fittiing

- Lg=120nm, D=80nm, Tox=3nm

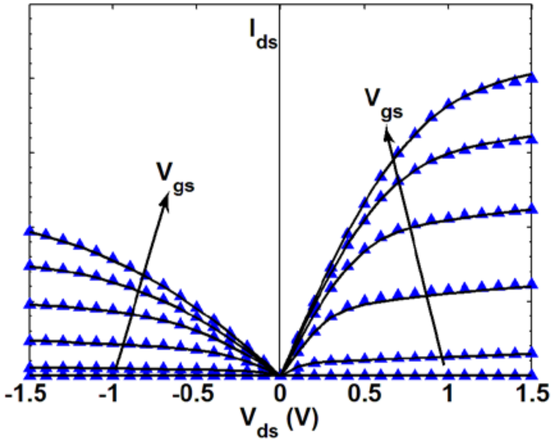
Symbols: Data
Lines: Model

Drain Current vs. V_{gs}

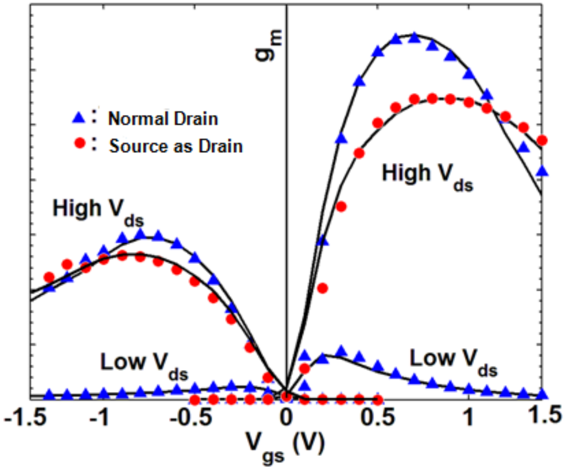




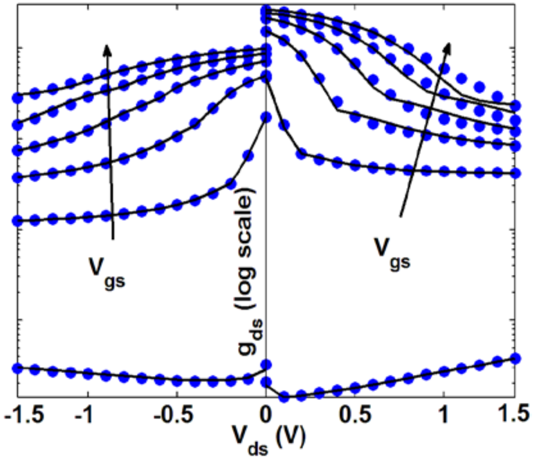
Drain Current vs. V_{ds}



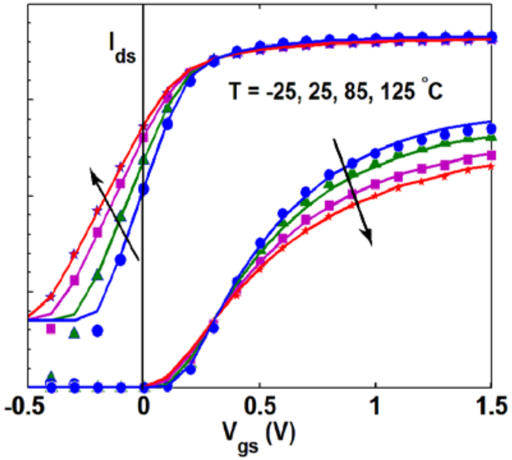
Transconductance



Output Conductance

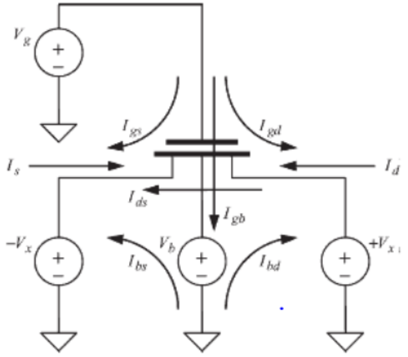


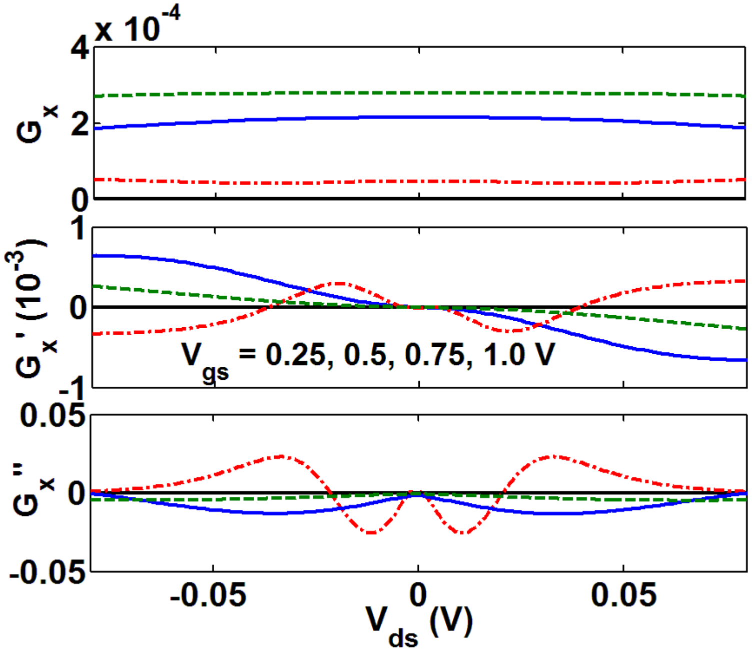
Temperature Dependence



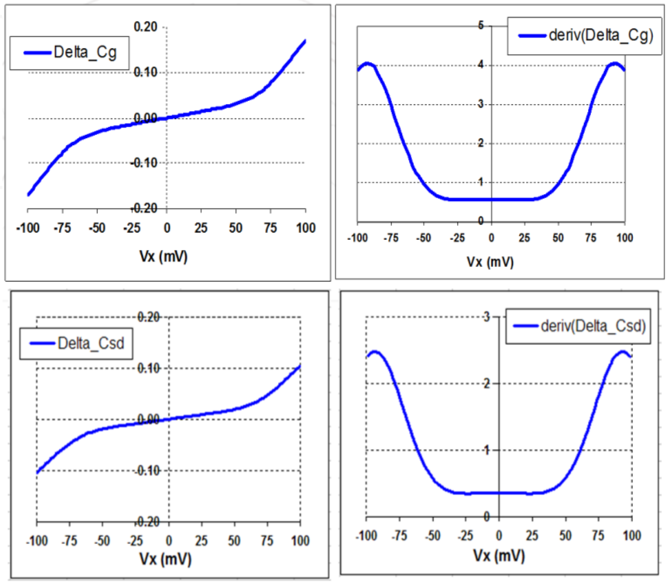
Symmetry / Continuity Tests

- Model passes both DC and AC Symmetry Tests





Drain Current



Capacitances (C_{gg} and C_{sd})

C.C.McAndrew, IEEE TED, Vol. 53, No. 9, 2006

BSIM-CMG Summary

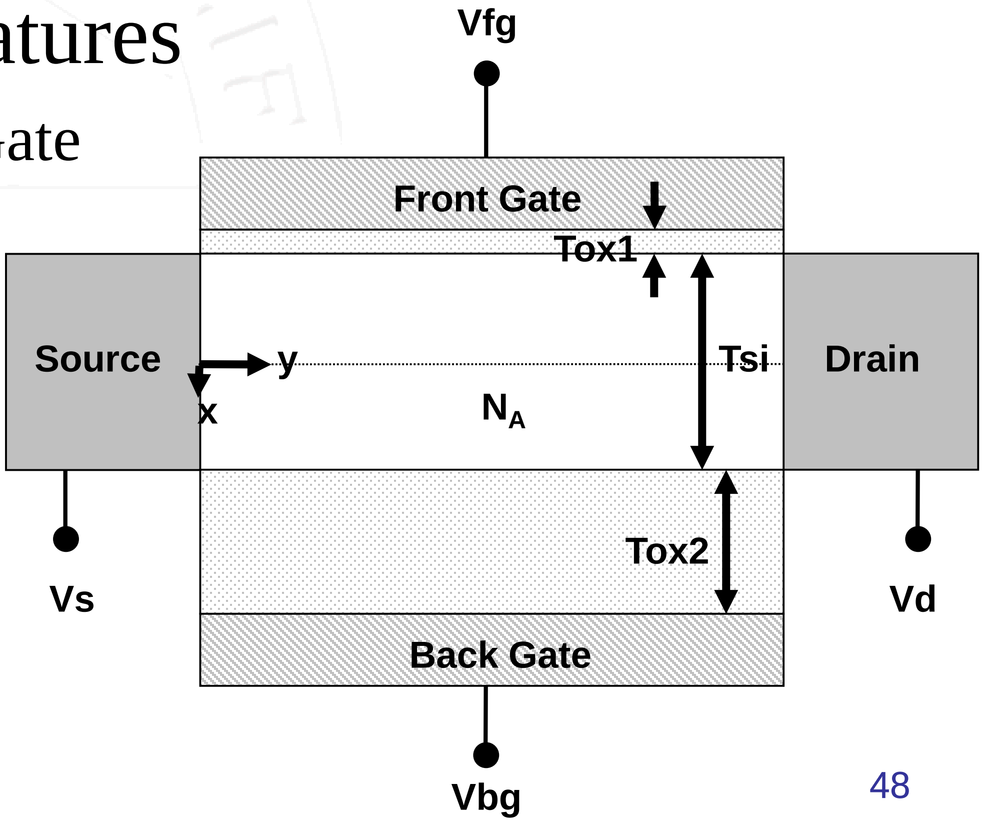
- BSIM-CMG 106.0.0 is industry standard production level model – standardized in March 2012
  - Available in major EDA tools
- Released **BSIM-CMG 106.1.0 in Sept. 2012**
- Physical, Scalable Core Models for multiple device architectures
  - Supports both SOI and Bulk Substrates
  - Many Real Device Effects captured
- Validated on Hardware Data from different technologies

Outline

- History of BSIM Models
- BSIM6 Model
- BSIM-CMG Model
- BSIM-IMG Model

Device Structure & BSIM-IMG

- Asymmetric structure
  - Different Gate Work-functions
  - Allows dissimilar Gate Potentials
  - Different Oxide thickness and Material !
- Captures important features
  - V_{th} tuning through Back-Gate
  - Multi-V_{th} technology

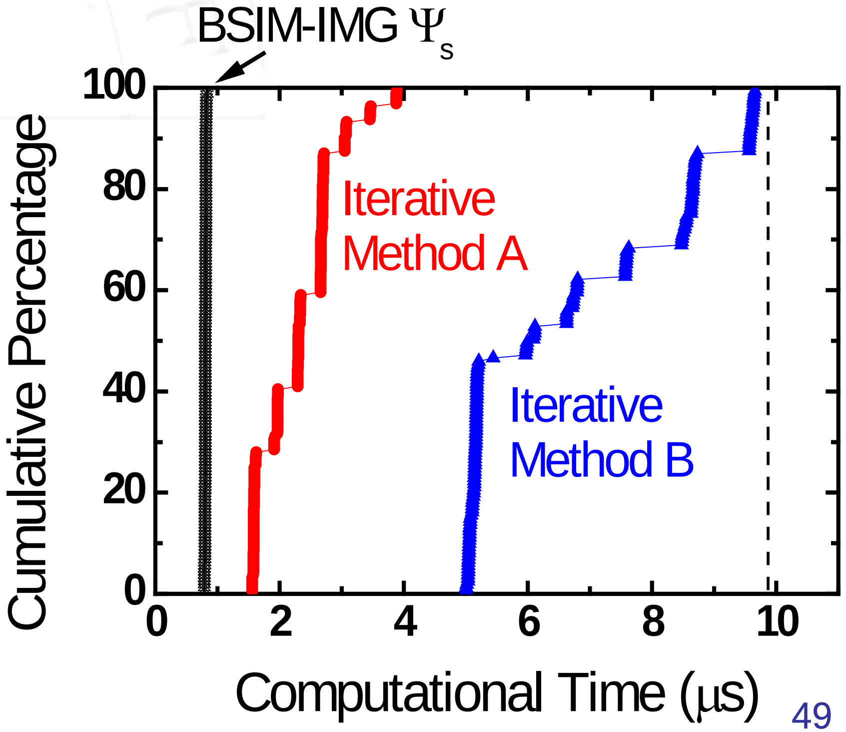


Computationally Efficient Core

- Efficient Non-iterative Surface Potential calculation
- Surface potential needs to solved at least twice - Source and Drain side
  - Obtain ψ_s / Q_{is} and ψ_d / Q_{id}

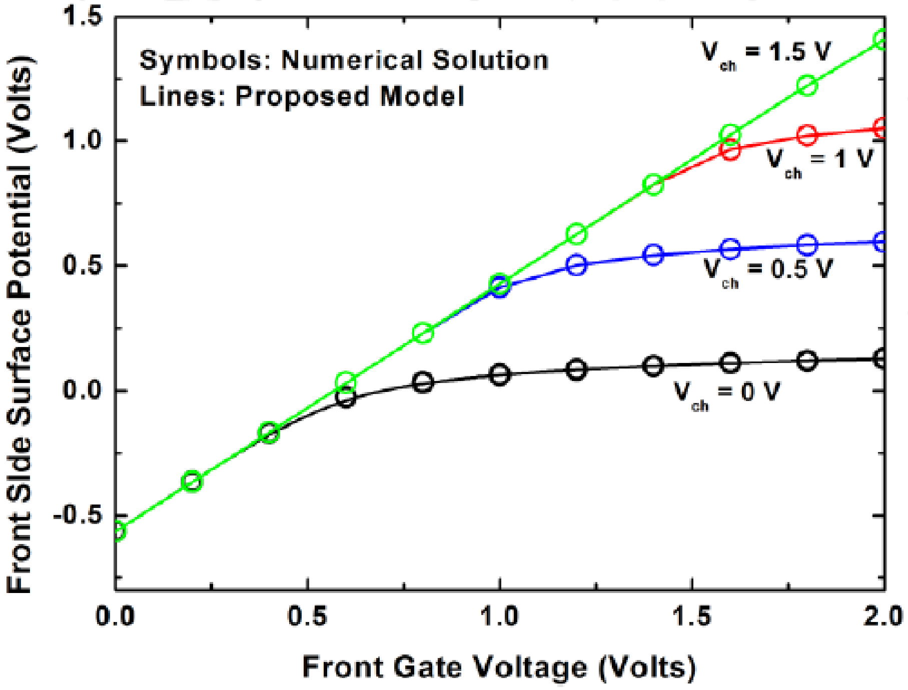
FAST

S. Khandelwal et al., "BSIM-IMG: A Compact Model for Ultra-Thin Body SOI MOSFETs with Back-Gate Control", IEEE TED, Aug. 2012.

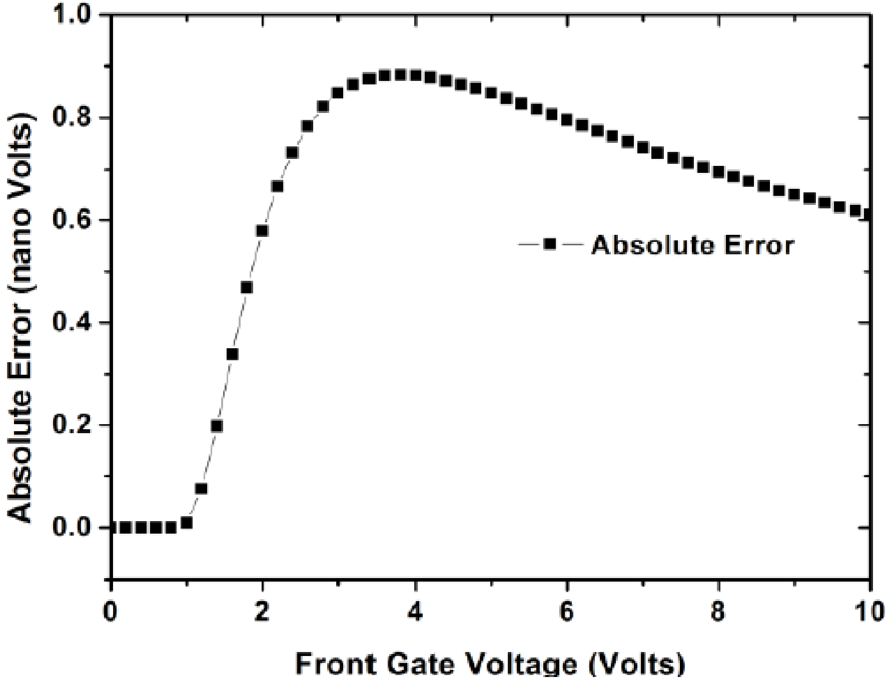


Results: Surface-Potential

Comparison with Numerical Solution



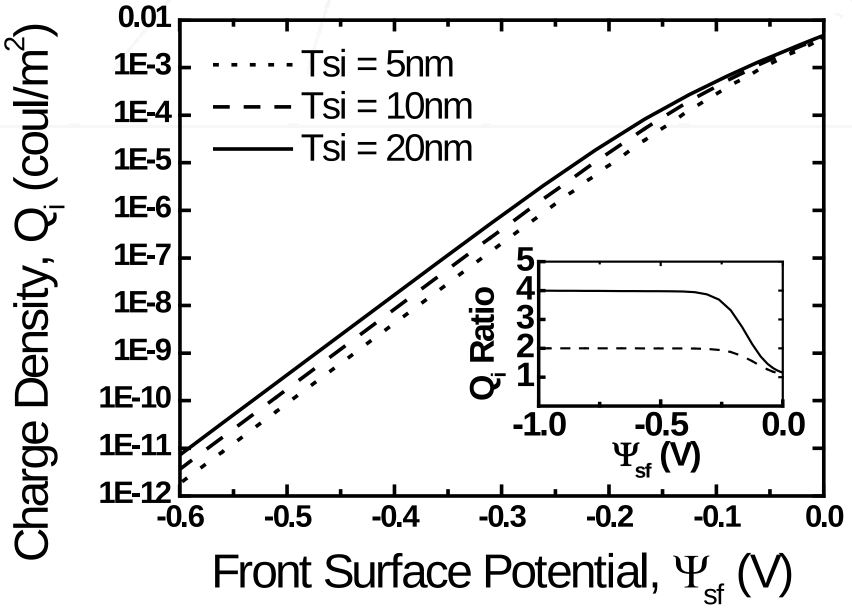
Absolute Error (<nV)

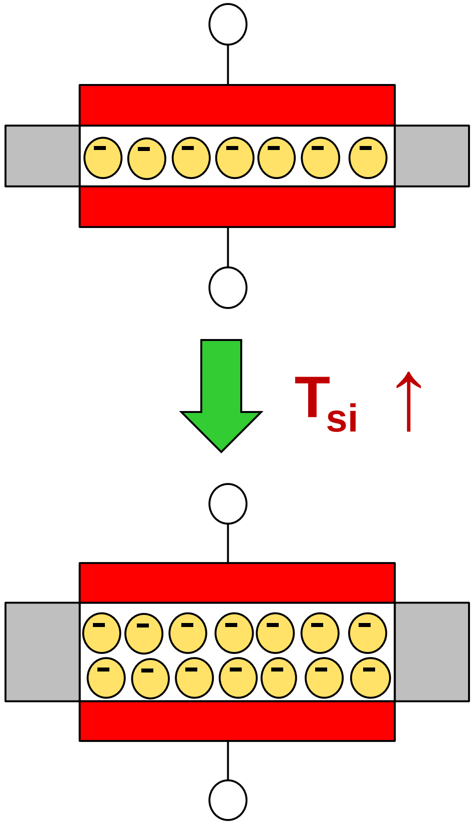


Volume Inversion

- Preserves Important Property like Volume Inversion
  - In sub-threshold (Low field), the charge density Qi is proportional to the body thickness Tsi

T_{oxb} = 10μm





Drain Current Model

$$I_{ds} = \mu \cdot \frac{W}{L} \cdot \left[\frac{Q_{inv,s} + Q_{inv,d}}{2} \left(\psi_{s1,d} - \psi_{s1,s} \right) + \eta \cdot \frac{kT}{q} \left(Q_{inv,s} - Q_{inv,d} \right) \right]$$

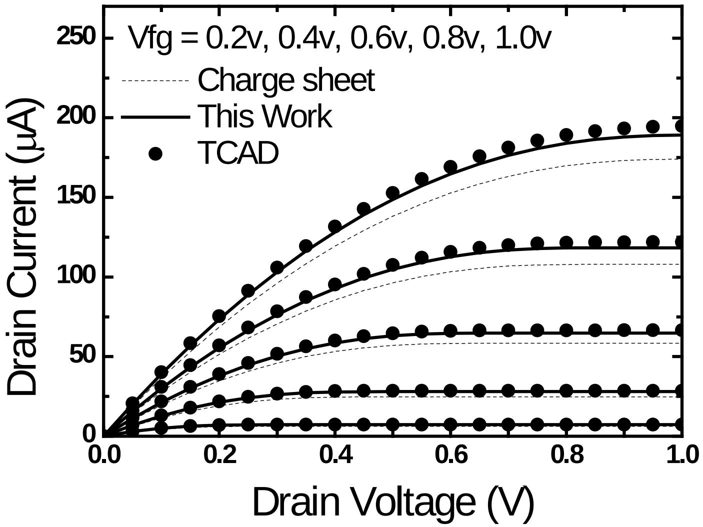
Drift **Diffusion**

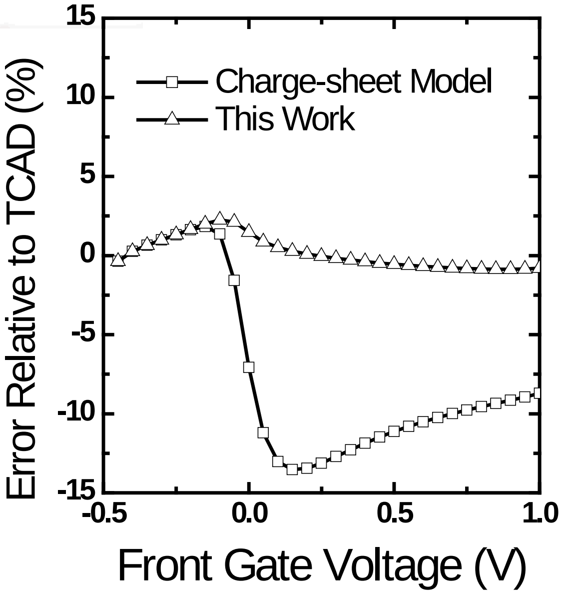
$$\eta = 2 - \frac{2\varepsilon_{si} \overline{E}_{s2}}{\overline{Q}_{inv} + 2\varepsilon_{si} \overline{E}_{s2}}$$

Q_{inv}: inversion carrier density
E_{s2}: back-side electric field
ψ_{s1}: front-side surface potential

No Charge-sheet Approximation

Very high accuracy

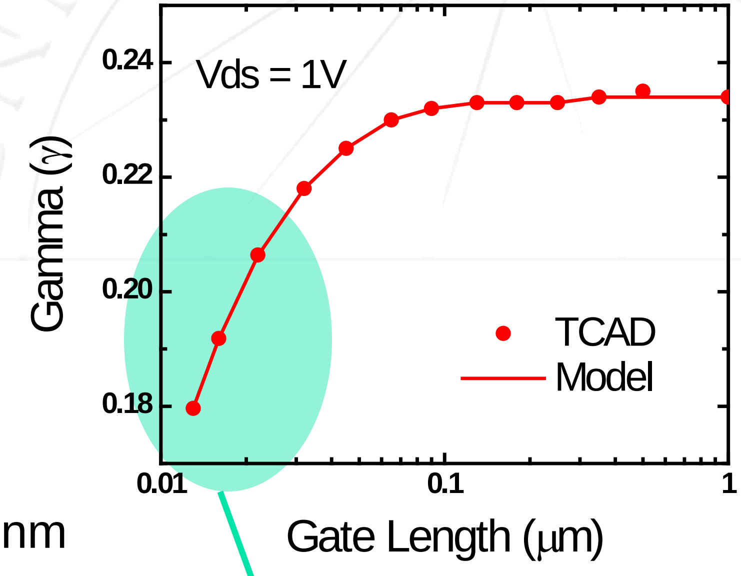




Length Dependent γ Model

- Capacitive coupling ratio

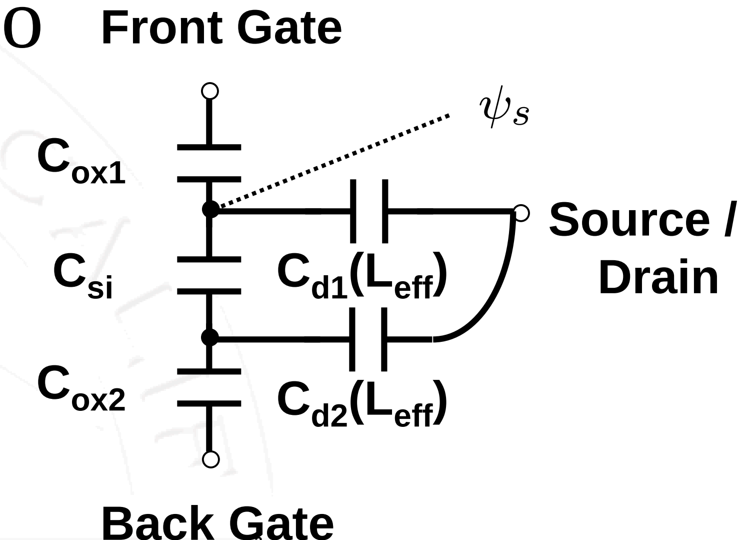
$$\gamma = -\frac{dV_{TH}}{dV_{bg}}$$

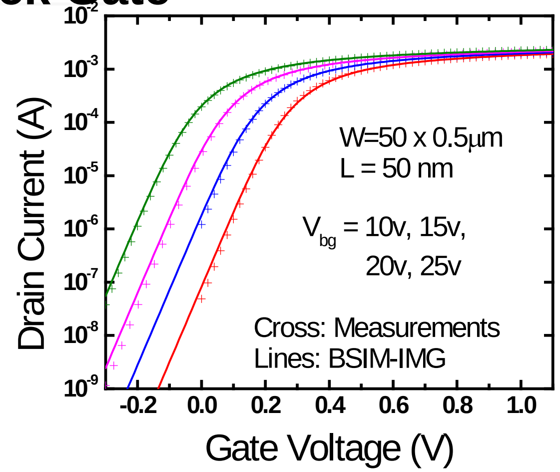


Tsi=8nm

Tbox=4nm

γ degraded at short channel



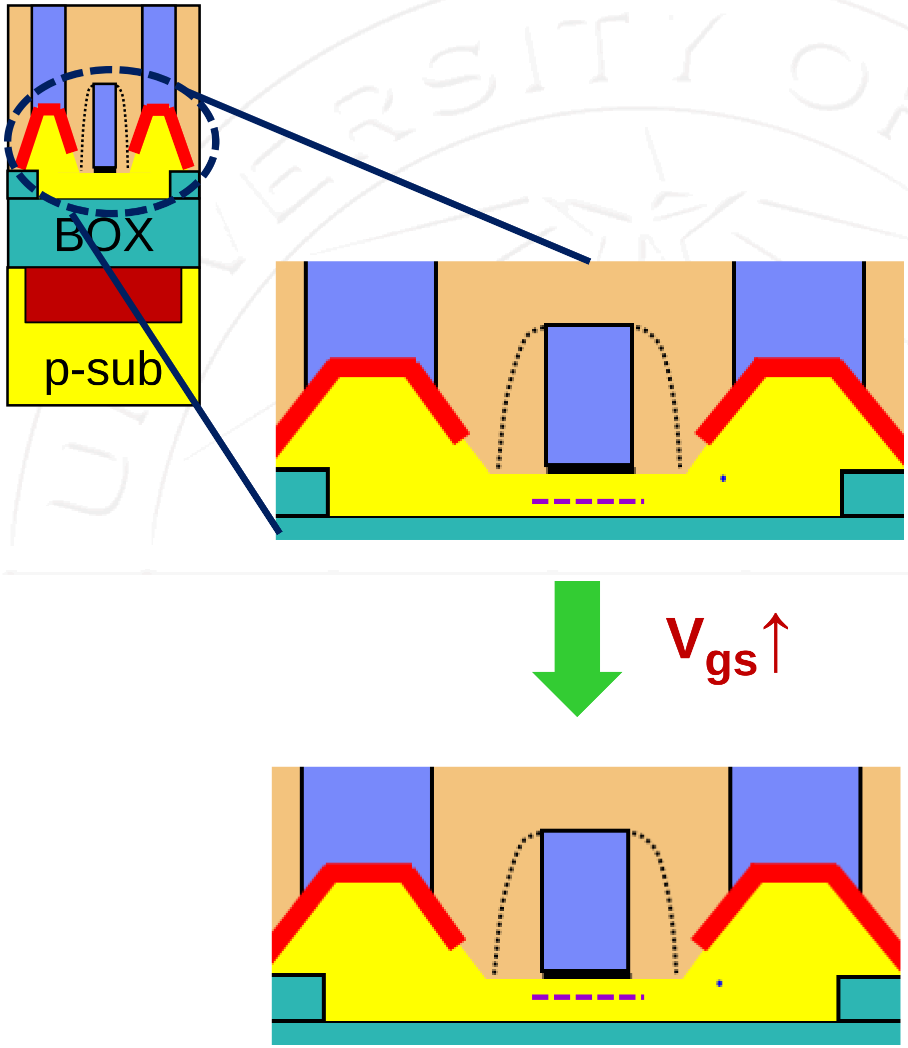


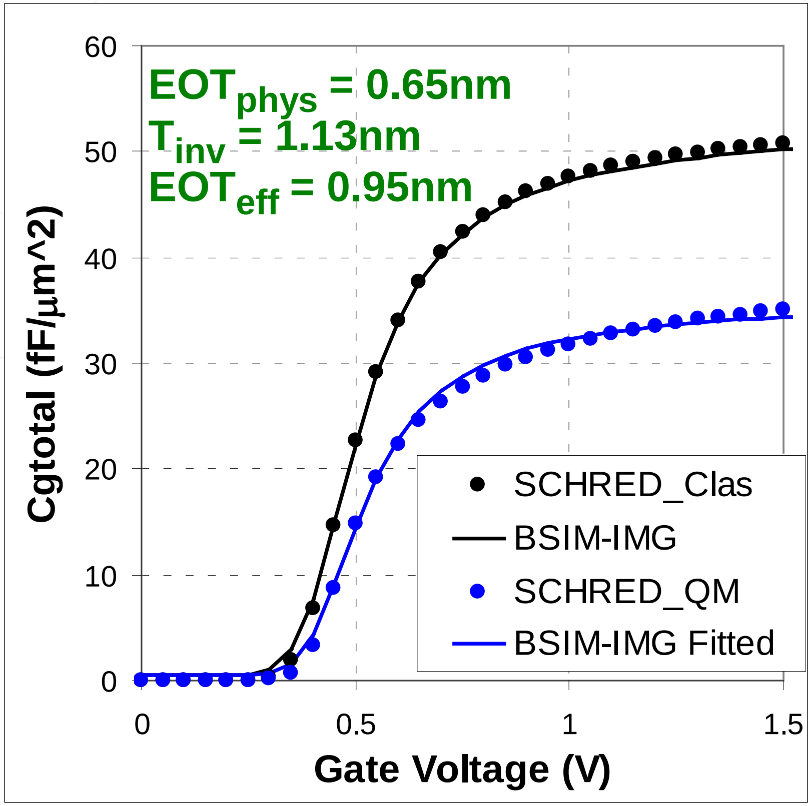
Captures V_{bg} effect in I-V

QM Effect: Inv. Charge Centroid Model

V_{dd} = 0.9 V ; V_{fb} = 28 mV

T_{BOX} = 140nm; T_{si} = 6nm; N_{sub} = 1e16 cm^{-3}





EOT_{phys} = 0.65nm

T_{inv} = 1.13nm

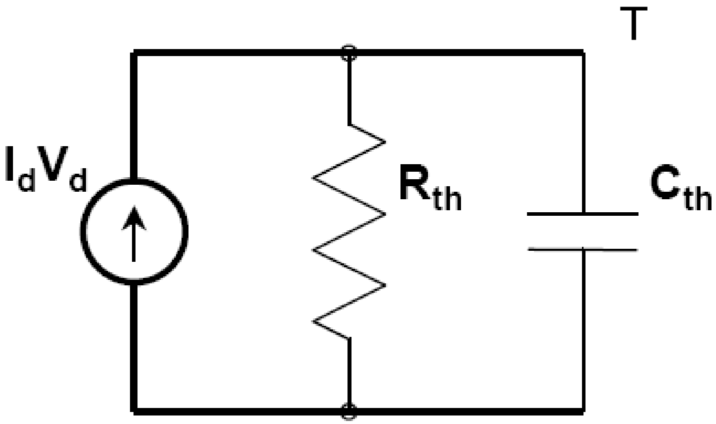
EOT_{eff} = 0.95nm

Self Heating Model

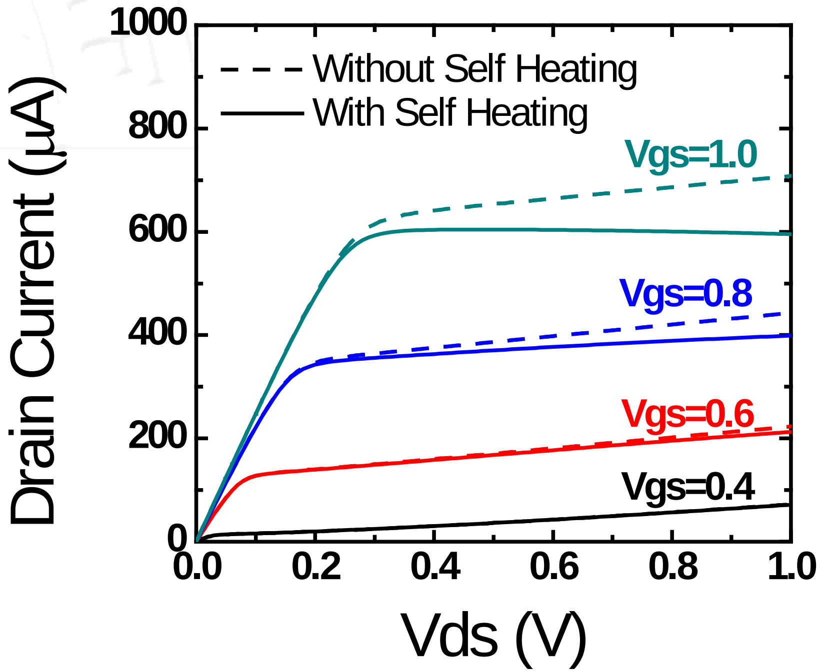
- Thermal Node: Rth/Cth methodology

$$R_{th} = \frac{RTH0}{WTH0 + W_{eff}}$$

$$C_{th} = CTH0 \cdot (WTH0 + W_{eff})$$



- Relies on Accurate physical modeling of Temperature Effects in the model

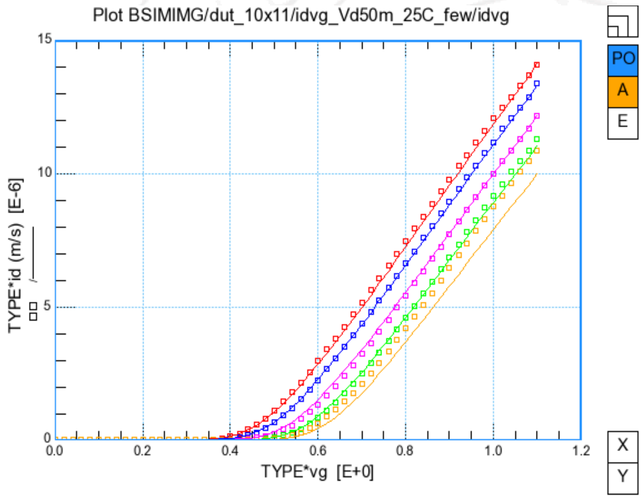


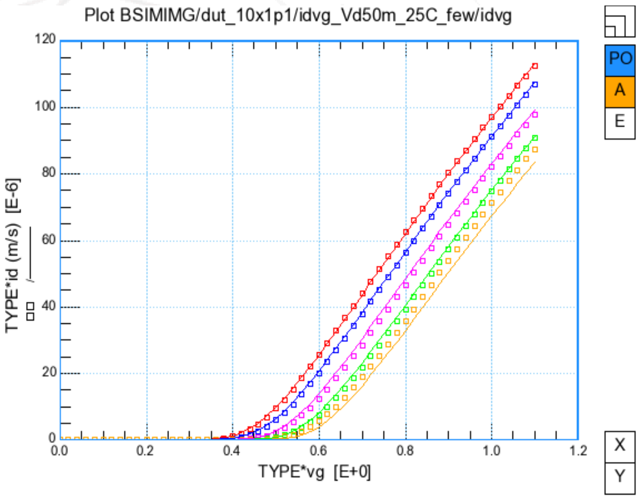
M. A. Karim et al., "Extraction of Isothermal Condition and Thermal Network in UTBB SOI MOSFETs", to appear in IEEE Electron Device Letters, 2012.

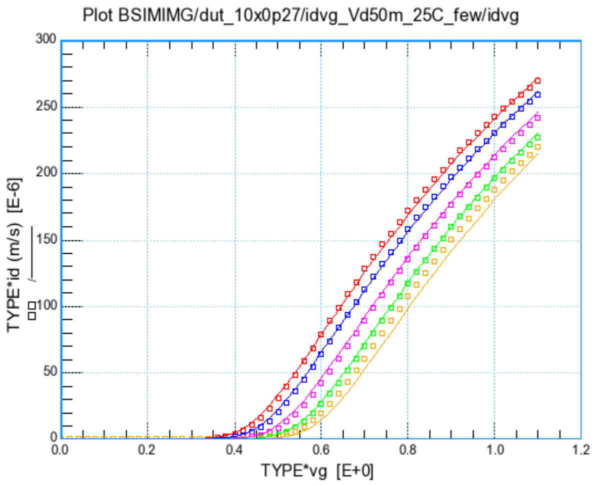
Global Extraction : I_d-V_{gs} at different V_{bg}

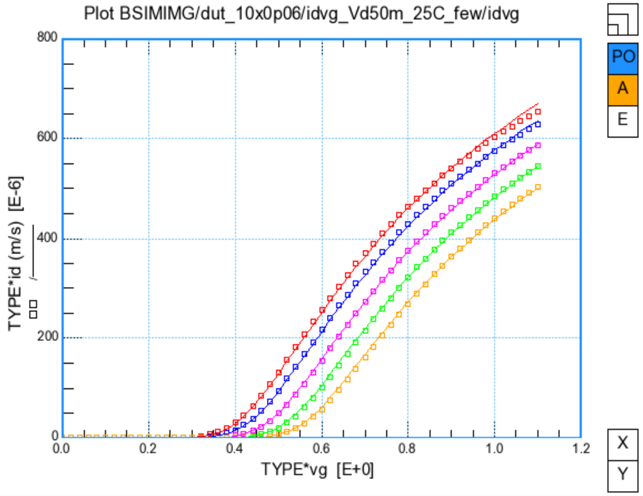
TBOX=10nm

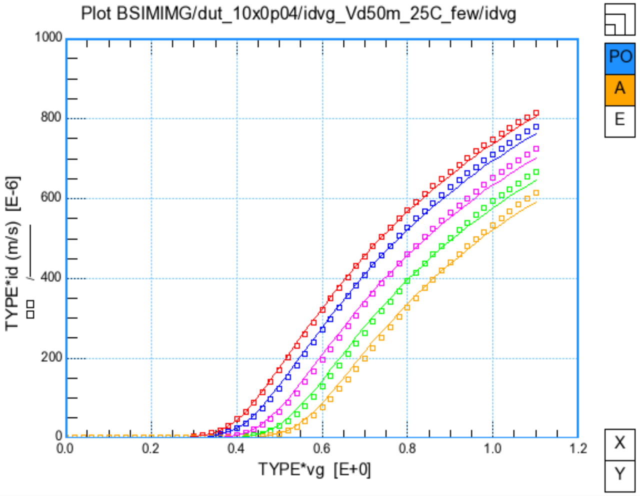
- Vbg=0, -0.2, -0.5, -0.8, -1.1 V; Vds=50mV
- L= 11 um, 1.1 um, 270nm, 60 nm, 40 nm, 30 nm

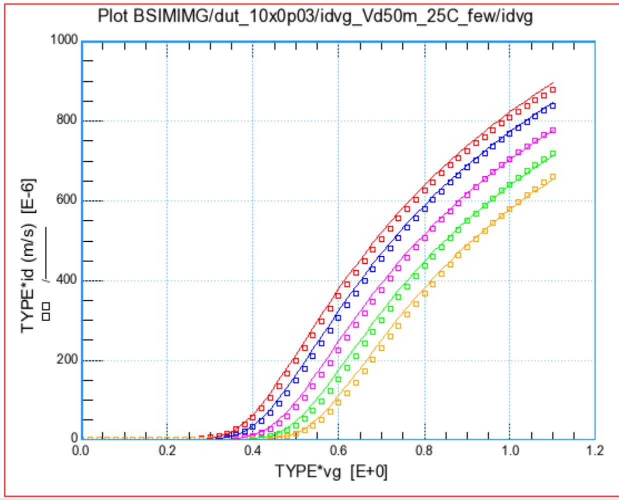

Plot BSIMIMG/dut_10x11/idvg_Vd50m_25C_few/idvg


Plot BSIMIMG/dut_10x1p1/idvg_Vd50m_25C_few/idvg


Plot BSIMIMG/dut_10x0p27/idvg_Vd50m_25C_few/idvg

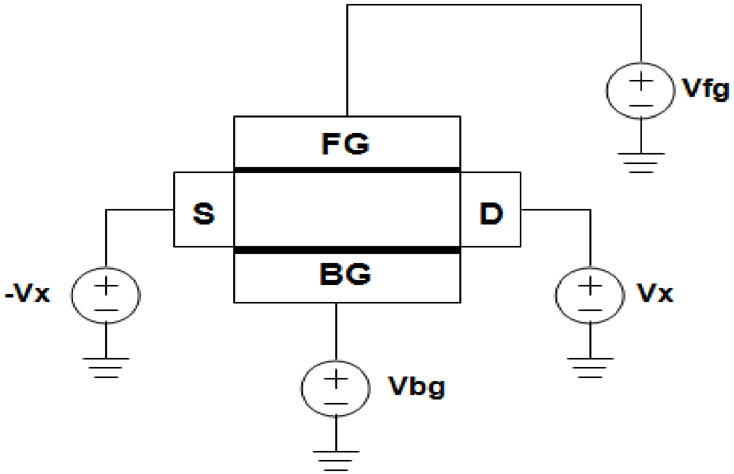

Plot BSIMIMG/dut_10x0p06/idvg_Vd50m_25C_few/idvg

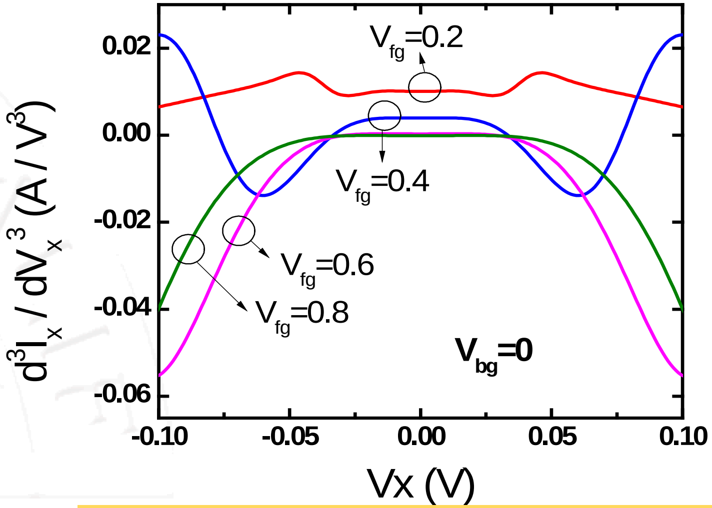

Plot BSIMIMG/dut_10x0p04/idvg_Vd50m_25C_few/idvg


Plot BSIMIMG/dut_10x0p03/idvg_Vd50m_25C_few/idvg

Gummel Symmetry Test

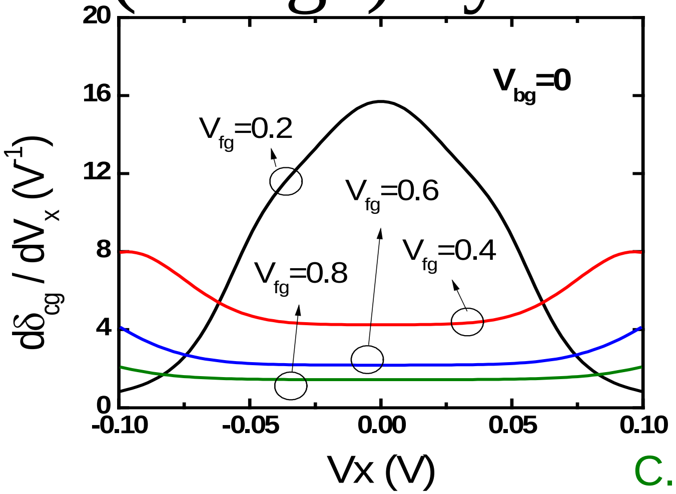
- Drain Current Symmetry

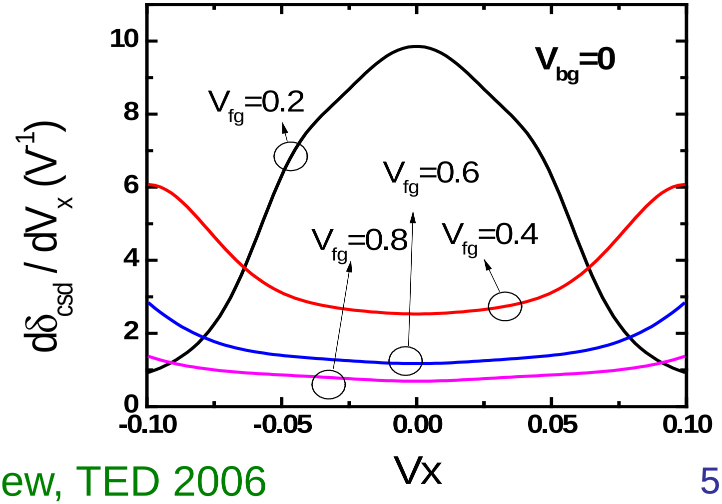




Analog /RF Ready

- AC (charge) Symmetry





C. C. McAndrew, TED 2006

BSIM-IMG: Current Status & Future

- Production level UTBSOI Model
  - Physical and Scalable for FDSOI devices
  - Plethora of Real Device Effects model
- Release of BSIM-IMG 101 (April 2011)
  - Available in different EDA tools
  - Already being used by SOI Consortium
- Under standardization at Compact Model Council
- Verilog-A code and Well-documented Manual
- Next BSIM-IMG Release – Oct. 2012

Acknowledgement

- Models users
- EDA Vendors
  - Agilent, Cadence
  - Synopsys, Proplus
  - Mentor Graphics
- SRC/GRC
- EPFL
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- IIT Kanpur
  - Pragya Kushwaha
  - Chadan Yadav
  - Shantanu Agnihotri
- SOITEC
- LETI
- ST Microelectronics
- Analog Devices
- Texas Instruments
- IBM
- TSMC
- Global Foundries
- All other CMC Members

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Thank You