# The HV-EKV MOSFET Model

***Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland***

EPFL Team –

Yogesh Singh Chauhan, Costin Anghel, Francois Krummenacher, Adrian Mihai Ionescu and Michel Declercq

CONFIDENTIAL

# Industrial and Academic Collaboration for Model Implementation & Validation

R. Gillon, B. Desoete, S. Frere,
***AMI Semiconductor, Belgium***
C. Maier
***Robert Bosch, Germany***
A. Baguenier
***Cadence Design Systems, France***
B. Bakeroot
***University of Gent, Belgium***

European Comission Funding – ROBUSPIC

CONFIDENTIAL

# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

# Motivation

- Robust HV Model for circuit simulators
- Physical Compact Model
- Accuracy in DC & AC
- Small number of parameters: EKV!
- Scaling against physical & electrical parameters
- Convergence and Speed
- Open Source

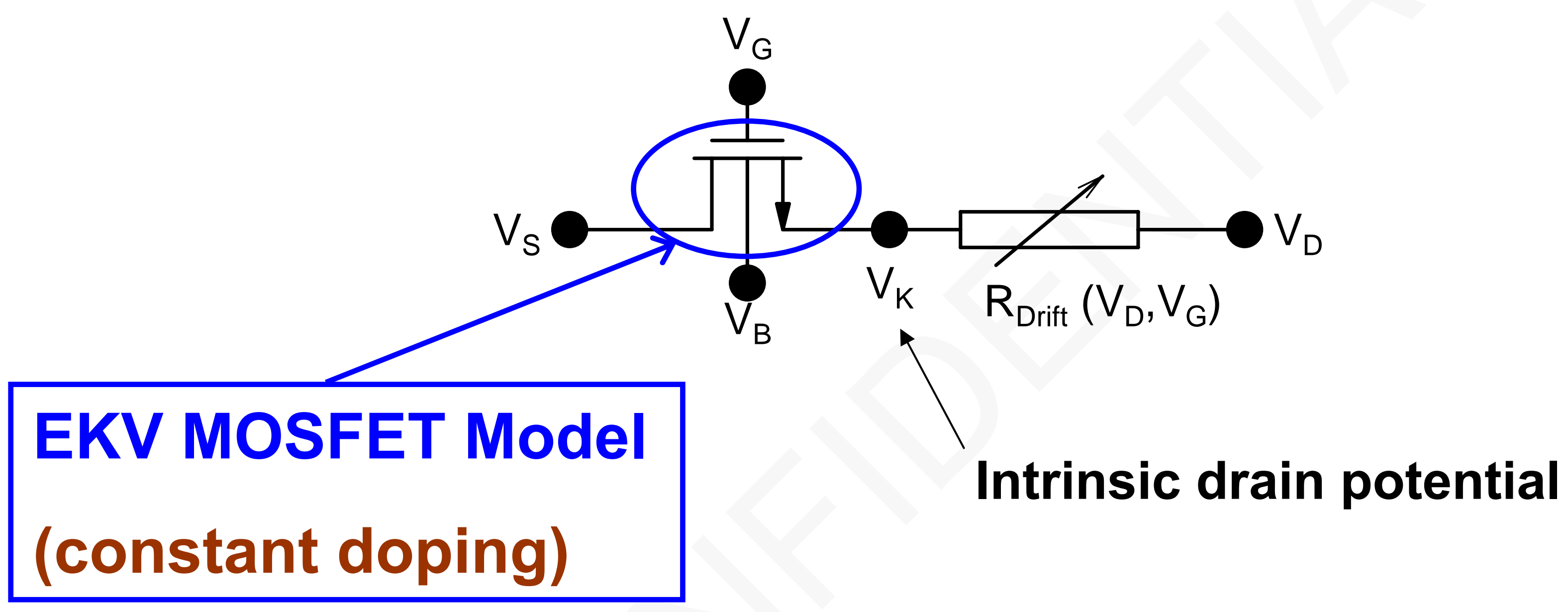
CONFIDENTIAL

# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

# General HV MOSFET Modeling Strategy



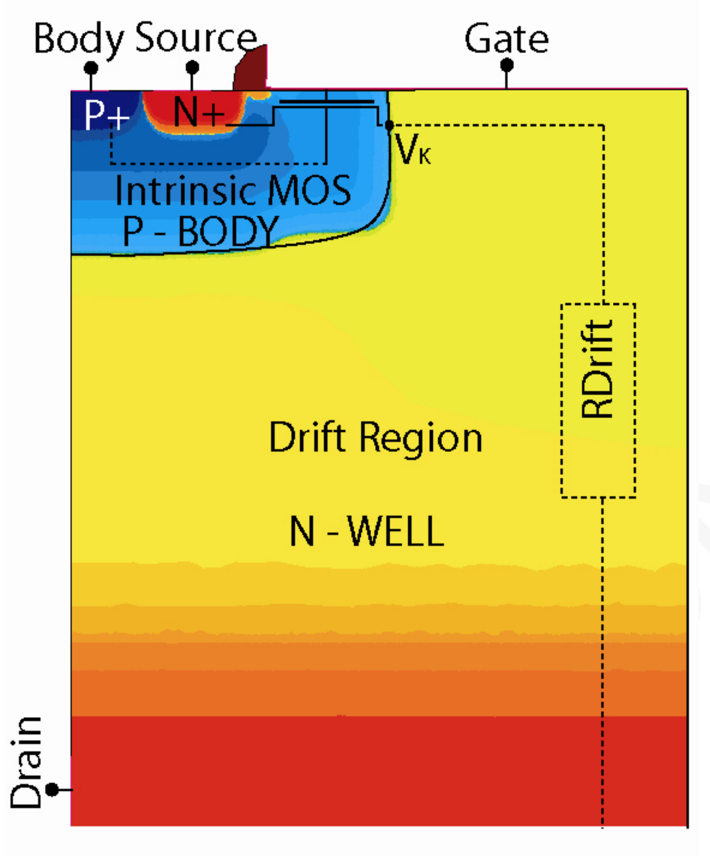

- **EKV Model**
  - **Physically based parameters**
  - **Less parameters than BSIM**

CONFIDENTIAL

# Device Architectures

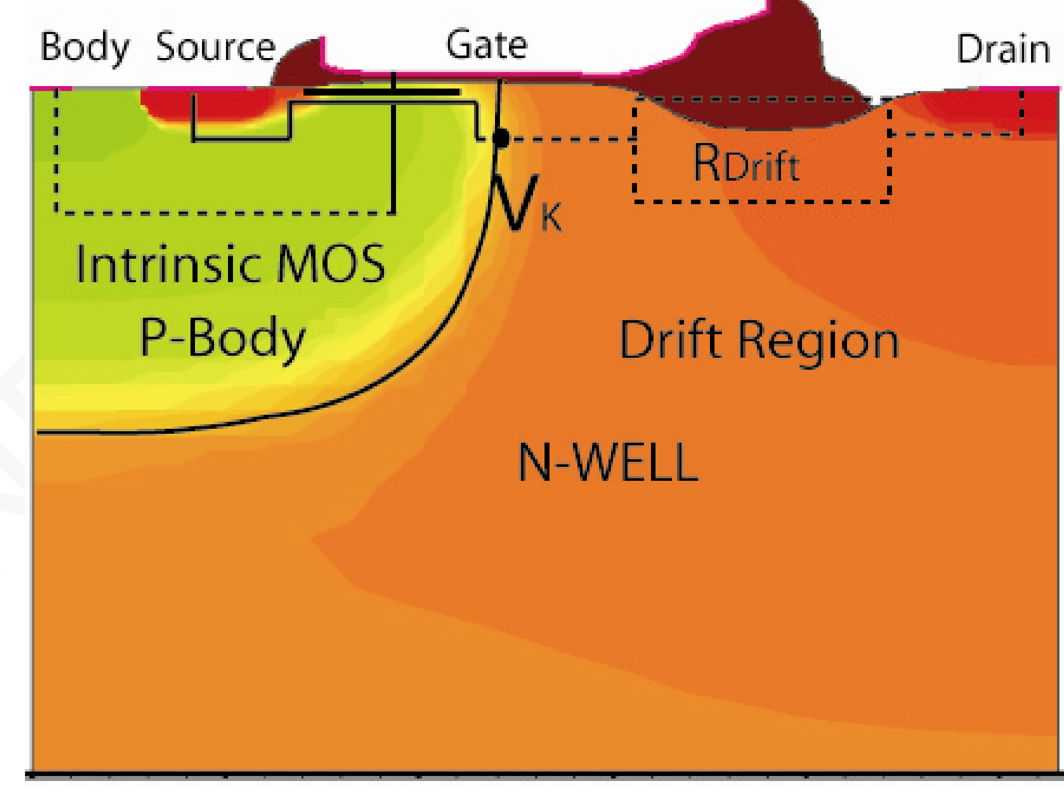
- **VDMOS :**

**$V_{Dmax}$=50V, $V_{Gmax}$=3.3V**




- **LDMOS :**

**$V_{Dmax}$=40-100V, $V_{Gmax}$=13V**

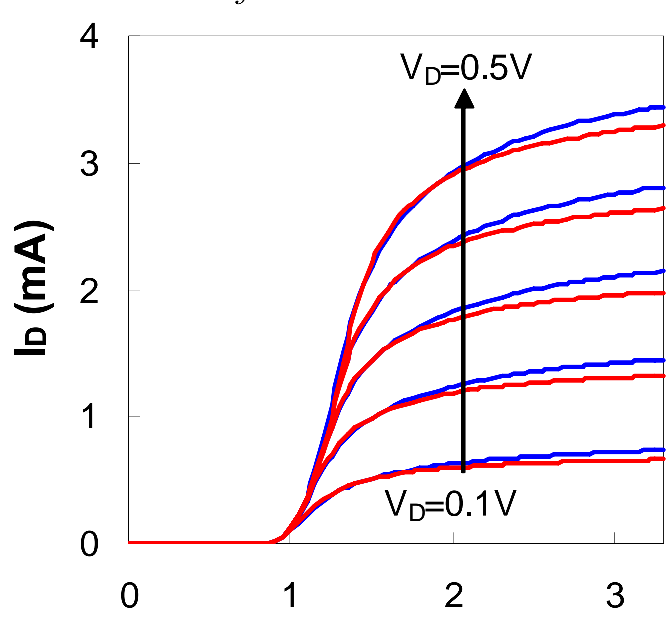


# Modeling Strategy

- Drift Resistance expression

**Why not?**

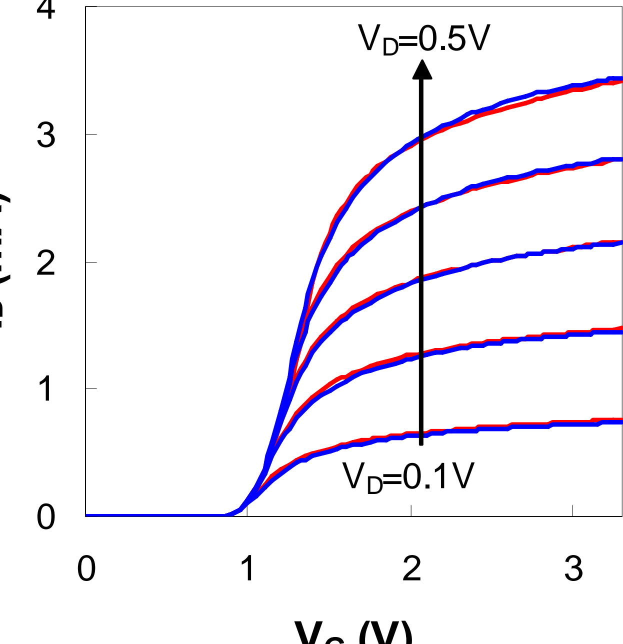
$$R_{Drift} = R = \text{constant}$$




**Low $V_D$**

Accumulation in Drift

$$R_{Drift} = \frac{R_{Drift0}}{(1+\theta_{Acc}.V_G)}$$




(red - model & blue - measurement)

# Modeling Strategy

- Drift part mainly affects the linear region of the output characteristics.
- Delayed transition between linear and saturation regime at high $V_G$ - velocity saturation in the drift

**High $V_D$ but linear region**

$$R_{Drift} = \frac{R_{Drift0}}{(1+\theta_{Acc}.V_G)}$$

$$R_{Drift} = R_{Drift0}\frac{\left[1+\left(\frac{V_D - V_K}{VSAT}\right)^{\alpha_{vsat}}\right]}{1+\theta_{Acc}.V_G}$$

$I_D$ (mA) vs $V_D$ (V): $V_G$ = 2.8V … $V_G$ = 1.2V (left and right plots; axes 0–20 mA, 0–10 V)

(red - model & blue - measurement)

# Scalable Drift Resistance

+ : Drain in-sides

- : Drain all-around

Effect of Temperature

$$R_{Drift} = R_{Drift0} \frac{\left[1+\left(\frac{V_D - V_K}{VSAT}\right)^{\alpha_{vsat}}\right]}{(1+\theta_{Acc} V_G)} \left(1 \pm (k_{rd} - 1)\frac{N_F - 1}{N_F + N_{CRIT}}\right)(1+\alpha_T . \Delta T)$$

$$R_{Drift0} = \rho_{Drift0} \left(\frac{L_{DR}}{N_F (W + \Delta W)}\right)$$

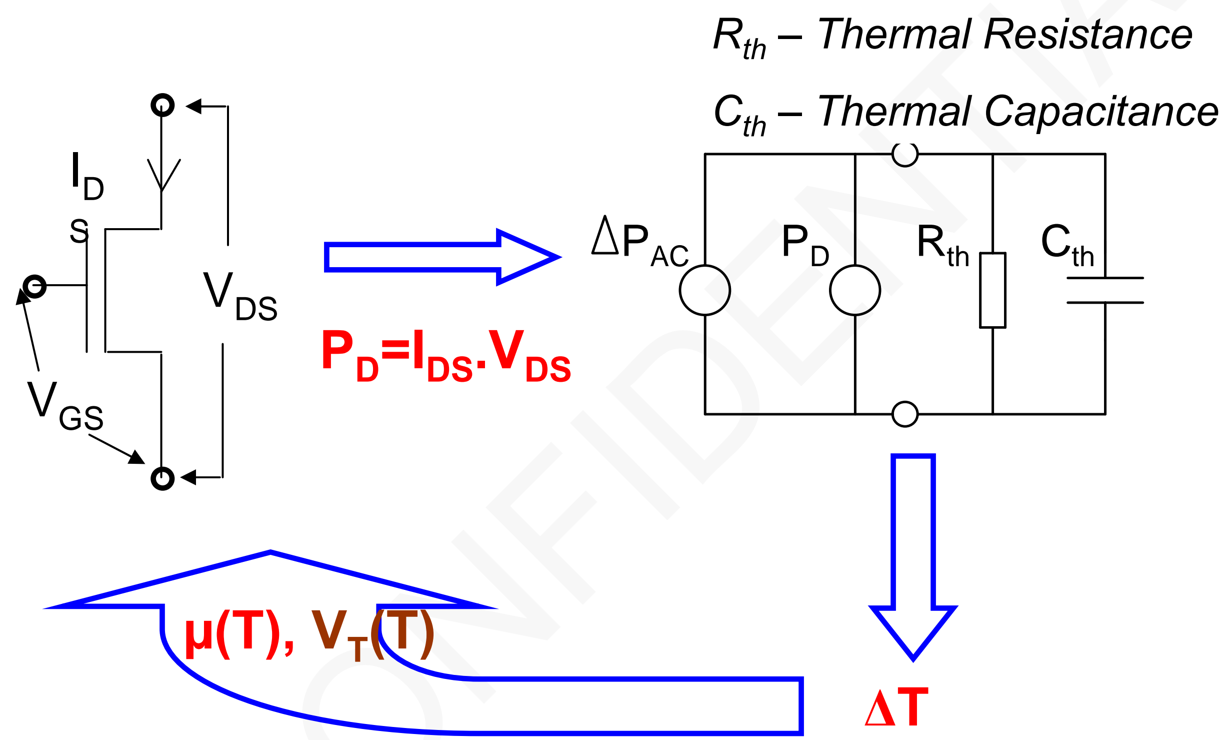
Drift Length

Number of Fingers

Width and Width Offset

CONFIDENTIAL

# Modeling of Self Heating Effect




- External Temperature Node

Ref: C. Anghel et al., "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs", IEEE Electron Device Lett., 141 - 143, 2004



CONFIDENTIAL

# Modeling of impact Ionization Current

- Impact ionization in MOSFET – EKV
- Impact ionization in drift –

$$I_{avl} = (M-1).I_{DS}$$

$$M-1 \cong 1-\frac{1}{M} = 2.8X10^{-73}.N_{eff}^{3}.V_{DS}^{4}$$

or

$$M-1 \cong NEFF^{3}.V_{DS}^{4}$$

CONFIDENTIAL

Ref.: P. Rossel et al., "Avalanche Characteristics of MOS Transistors," presented at 21st International Conference on Microelectronics, Yugoslavia, 1997.

# AC Modeling

- $V_K$ behavior and Charges

Current in EKV Model $I_{DS}=I_S\ (i_f - i_r)$, $I_S$=Specific Current

Normalized forward Current

$$i_f = [\ln(1+e^{\frac{v_p - v_s}{2}})]^2$$

Normalized reverse Current

$$i_r = [\ln(1+e^{\frac{v_p - v_k}{2}})]^2$$

Normalized Charge related to $V_S$ (EKV) $\quad q_s = \sqrt{i_f + 0.25} - 0.5$

Normalized Charge related to $V_K$ (EKV) $\quad q_k = \sqrt{i_r + 0.25} - 0.5$

Normalized $v_k$ (EKV)

$$v_k = \frac{V_K}{U_T} = v_p - (2.q_k + \ln(q_k))$$

CONFIDENTIAL

Ref: J.-M. Sallese et al., “Inversion charge lineariazation in MOSFET modeling and rigorous derivation of the EKV compact model”, Solid-State Electronics,pp. 677-683, 2003

# $V_K$ vs. $V_G$ and $V_D$ for VDMOS

- $V_K$ – Important parameter for design of HV-MOS

$V_D$ = 5V
$V_D$ = 1V
$V_K$(V)
$V_G$ (V)

$V_G$ = 3V
$V_G$ = 0.5V
$V_K$ (V)
$V_D$ (V)

- Matches with literature

Ref: C.H. Kreuzer et al., “Physically based description of quasi-saturation region of vertical DMOS power transistors”, IEDM,pp. 489 - 492, 1996

# AC Modeling

- Charges in MOSFET and Drift region

$$Q_G = Q_K + Q_S + Q_B + Q_{Drift}$$

$$Q_S = -W.L.C_{ox}.U_T.q_s = -W.L.C_{ox}.U_T.\left(\sqrt{i_f + 0.25} - 0.5\right)$$

$$Q_K = -W.L.C_{ox}.U_T.q_k = -W.L.C_{ox}.U_T.\left(\sqrt{i_r + 0.25} - 0.5\right)$$

$$Q_{Drift} = (V_G - V_{FB} - \psi_s).W.L_{DR}.C_{ox}$$

Assumptions

- $\Psi_S$ varies linearly across accumulation charge sheet

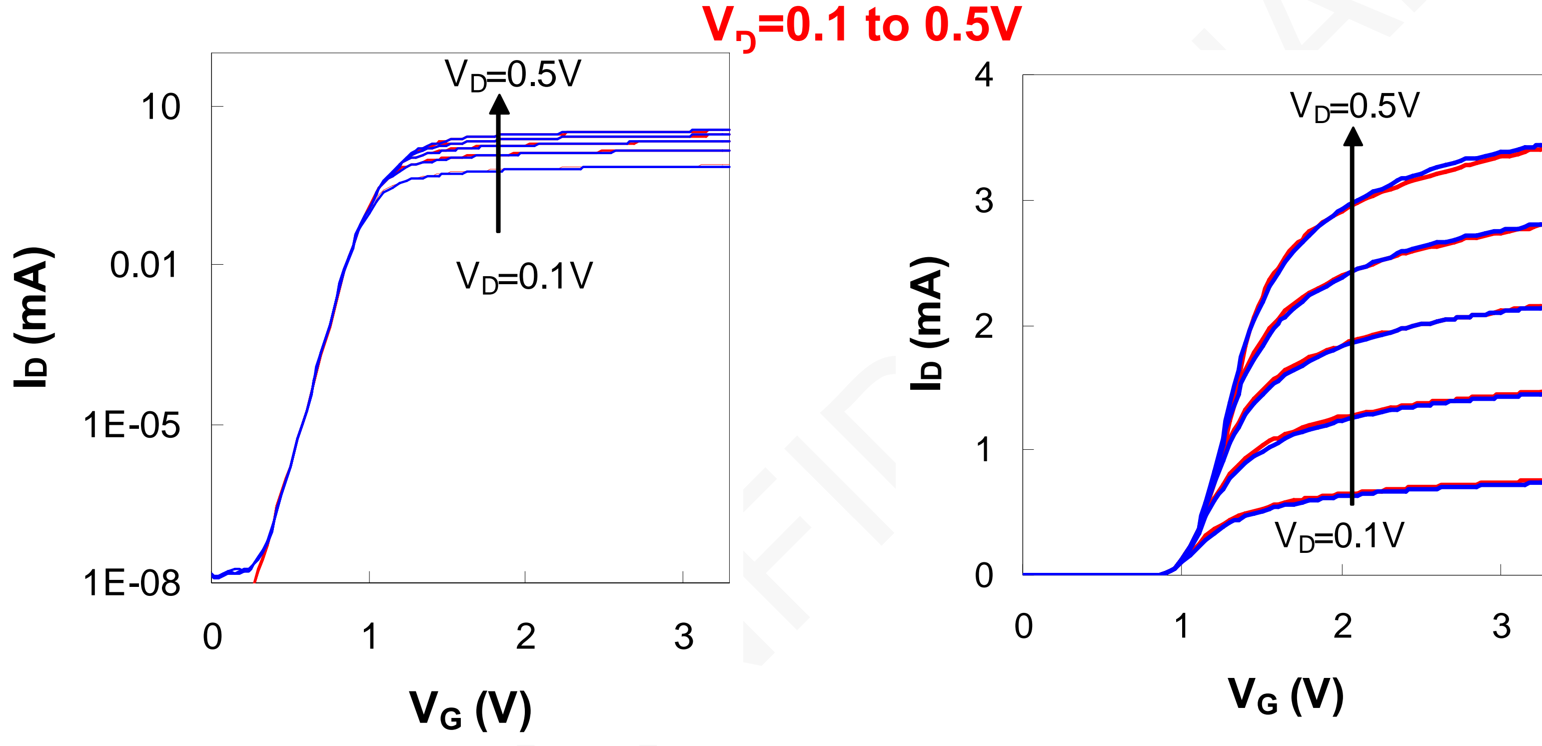
CONFIDENTIAL

# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

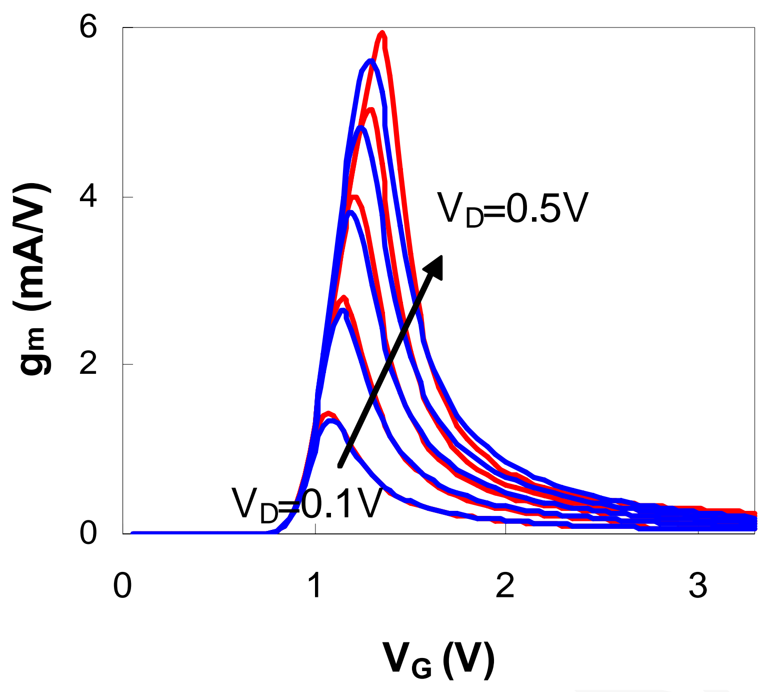
# Model Validation on 50V VDMOS

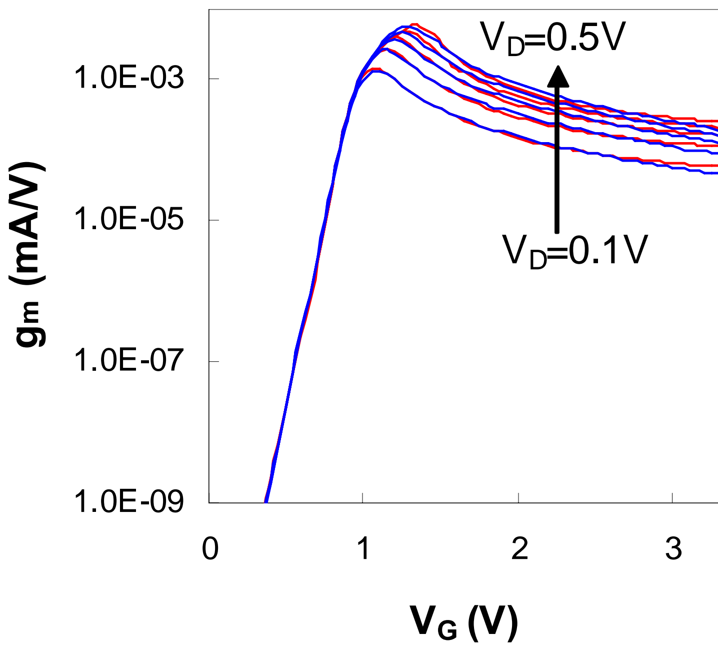



- Weak inversion to Strong inversion transition
- Subthreshold slope correctly matched
- Good accuracy

(red - model & blue - measurement)

# Transconductance for $V_D$=0.1-0.5V




- Subthreshold slope correctly matched
- descending slope – drift resistance

(red - model & blue - measurement)

# Output Characteristics

$V_G$=3.3V

$V_G$=1.2V

$I_D$ (mA)

$V_D$ (V)

$V_G$=2.1V

$V_G$=1.8V

$V_G$=0.9V

$|g_{ds}|$ (mA/V)

$V_D$ (V)

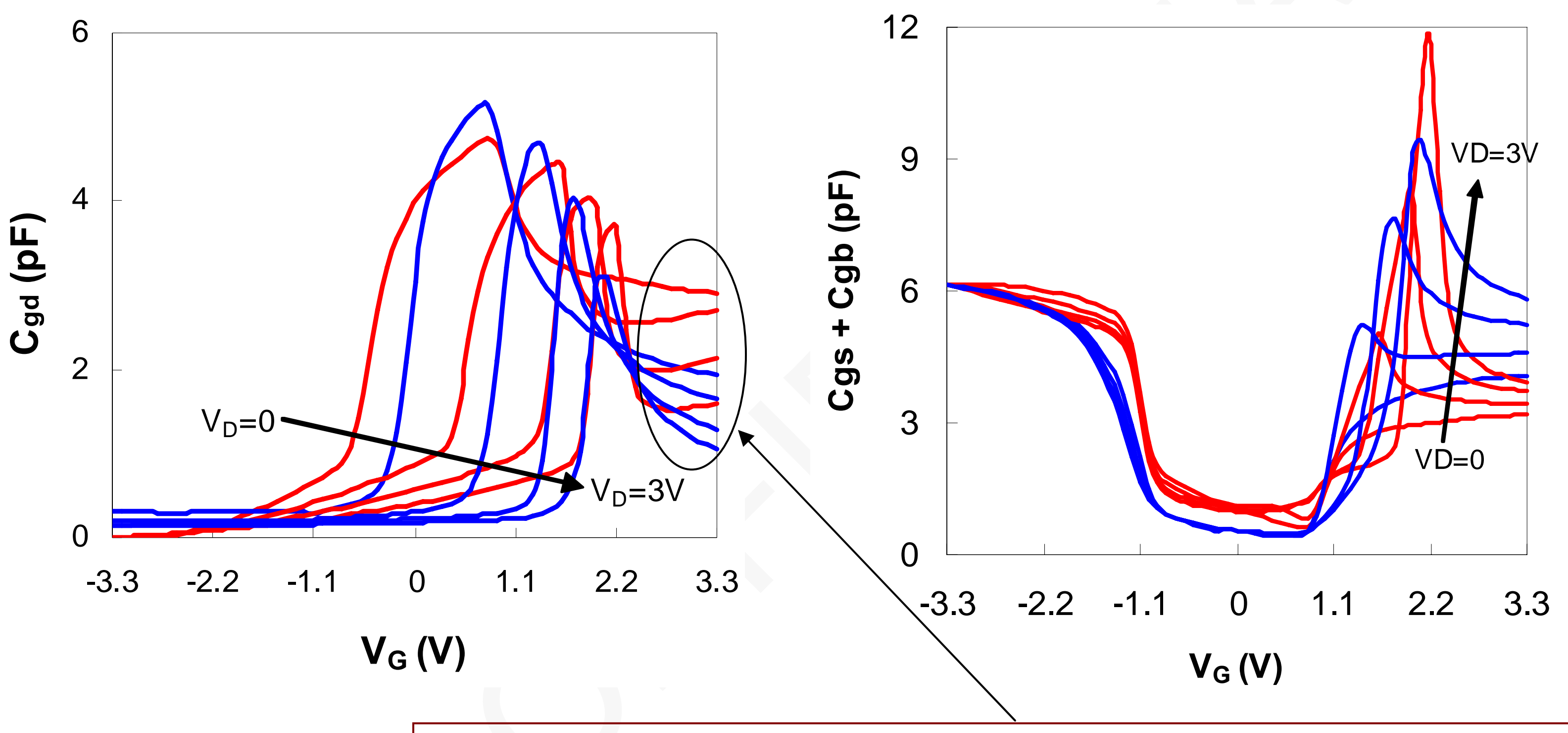
Self-Heating

Impact-Ionization

- Linear region correctly modeled by drift resistance.
- Self Heating Effect
- Peaks on $g_{ds}$

(red - model & blue - measurement)

# $C_{GD}$ and $C_{GS}+C_{GB}$ vs $V_G$
# $V_D$=0-3V




Interpolation function used in drift – to be improved

(red - model & blue - measurement)

# $C_{GD}$ and $C_{GS}$+$C_{GB}$ vs $V_D$

**$V_G$=0-2V**

$C_{gd}$ (pF)

4
2
0

0 5 10 15

$V_D$ (V)

**$V_G$=1.5 & 2V**

Cgs + Cgb (pF)

10
8
6
4
2
0

0 5 10 15 20

$V_D$ (V)

(red - model & blue - measurement)

# Temperature Scaling

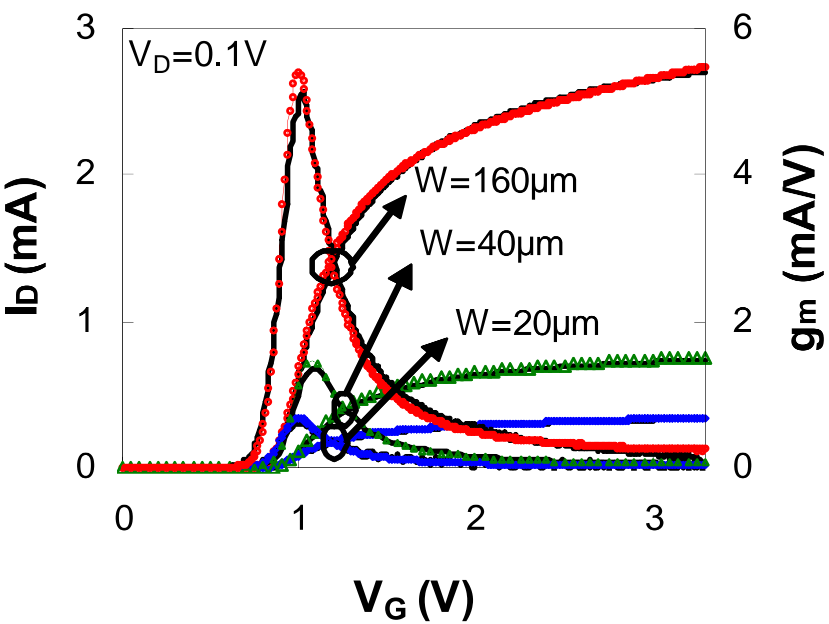
(color - model & black - measurement)

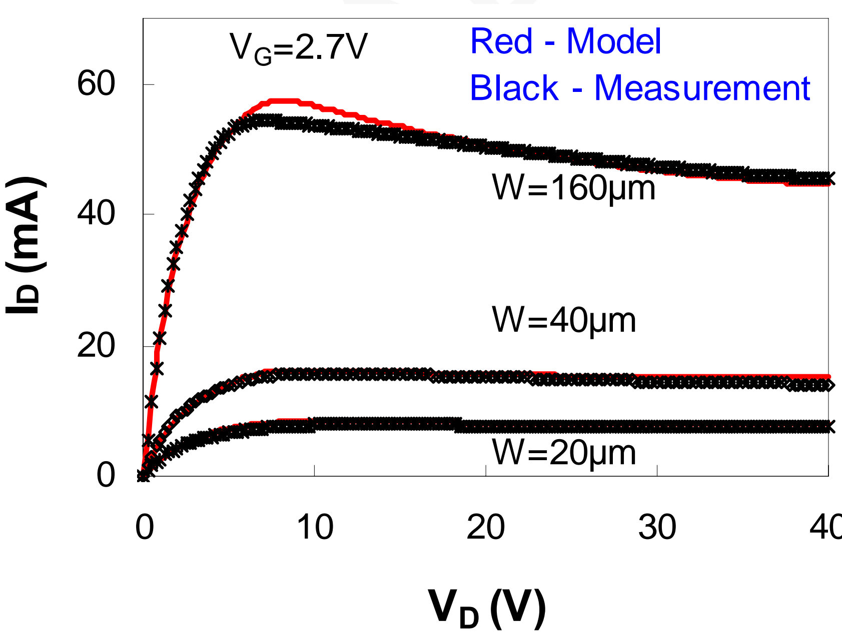
0.8
0.6
0.4
0.2
0
$I_D$ (mA)
T=30°C
T=85°C
T=130°C
$V_D$=0.1V
1.2
0.8
0.4
0
$g_m$ (mA/V)
0
1
2
3
$V_G$ (V)

18
12
6
0
$I_D$ (mA)
T=30°C
T=130°C
$V_G$=2.7V
0
10
20
30
40
$V_D$ (V)

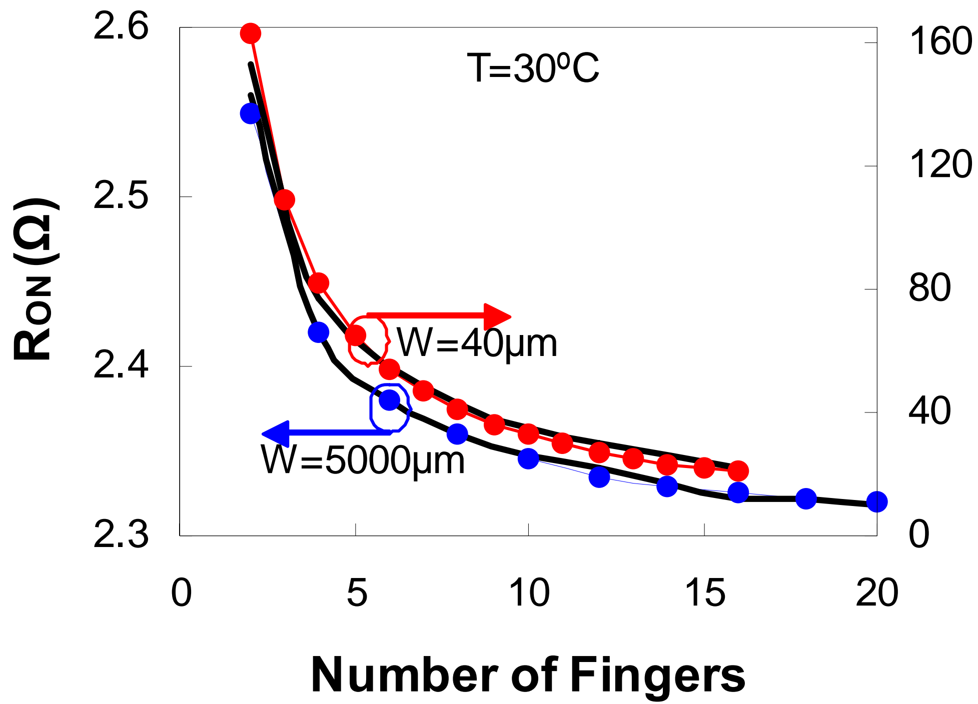
0.4
0.3
0.2
0.1
0
$I_D$ (mA)
ZTC point
0.9
1
1.1
1.2
$V_G$ (V)

# Width Scaling



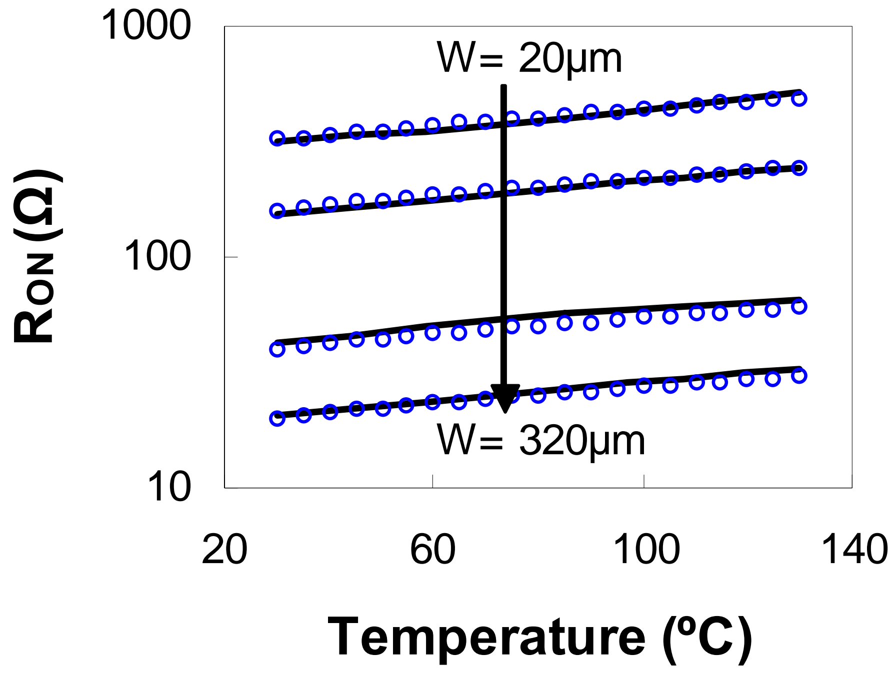



# $R_{ON}$ Scaling with number of fingers



# $R_{ON}$ Scaling with Temperature

W=20µm, 40µm, 160µm, 320µm



# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

# Model Validation on 40V LDMOS

## Transfer Characteristics

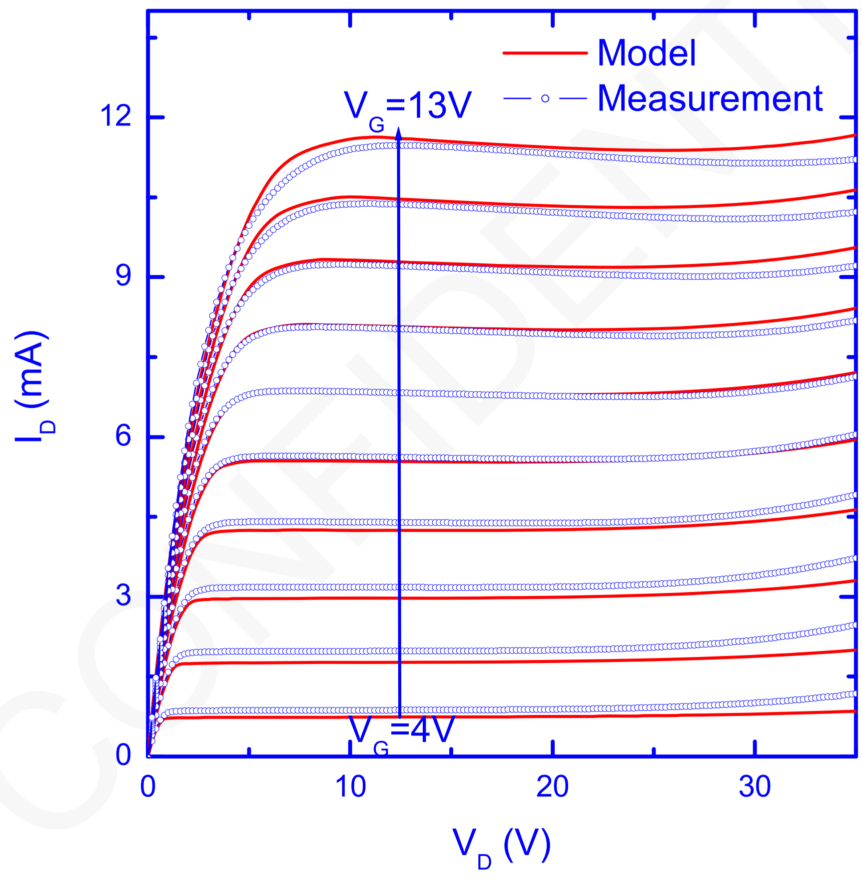
$I_D$ (mA)
10
1
0.1
0.01
1E-3
1E-4
1E-5
1E-6
1E-7
$V_D$=0.5V
$V_D$=0.1V
Model
Measurement
$V_D$=0.5V
$V_D$=0.1V
2.5
2.0
1.5
1.0
0.5
0.0
$I_D$ (mA)
0 2 4 6 8 10 12
$V_G$ (V)

$g_m$ (mA/V)
1
0.1
0.01
1E-3
1E-4
1E-5
1E-6
$V_D$=0.5V
$V_D$=0.1V
Model
Measurement
$V_D$=0.5V
$V_D$=0.1V
0.8
0.6
0.4
0.2
0.0
$g_m$ (mA/V)
0 2 4 6 8 10 12
$V_G$ (V)

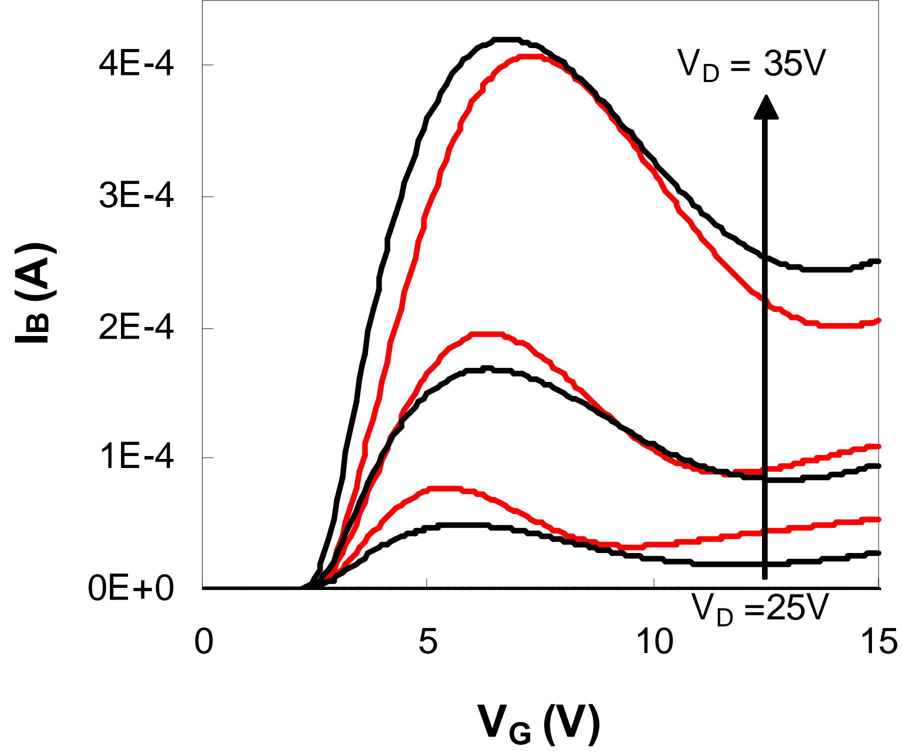
CONFIDENTIAL

# Model Validation on 40V LDMOS

## Output Characteristics



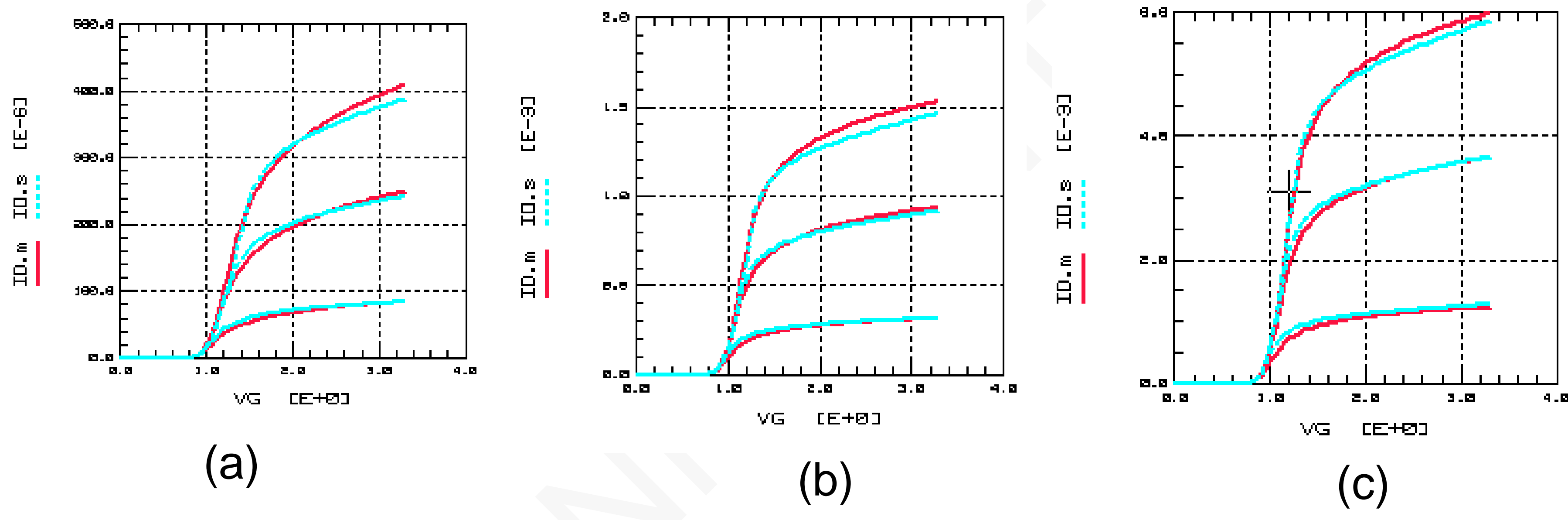
# Body Current vs. Gate bias




(red - model & black - measurement)

# Width Scaling : LDMOS device

## Transfer Characteristics

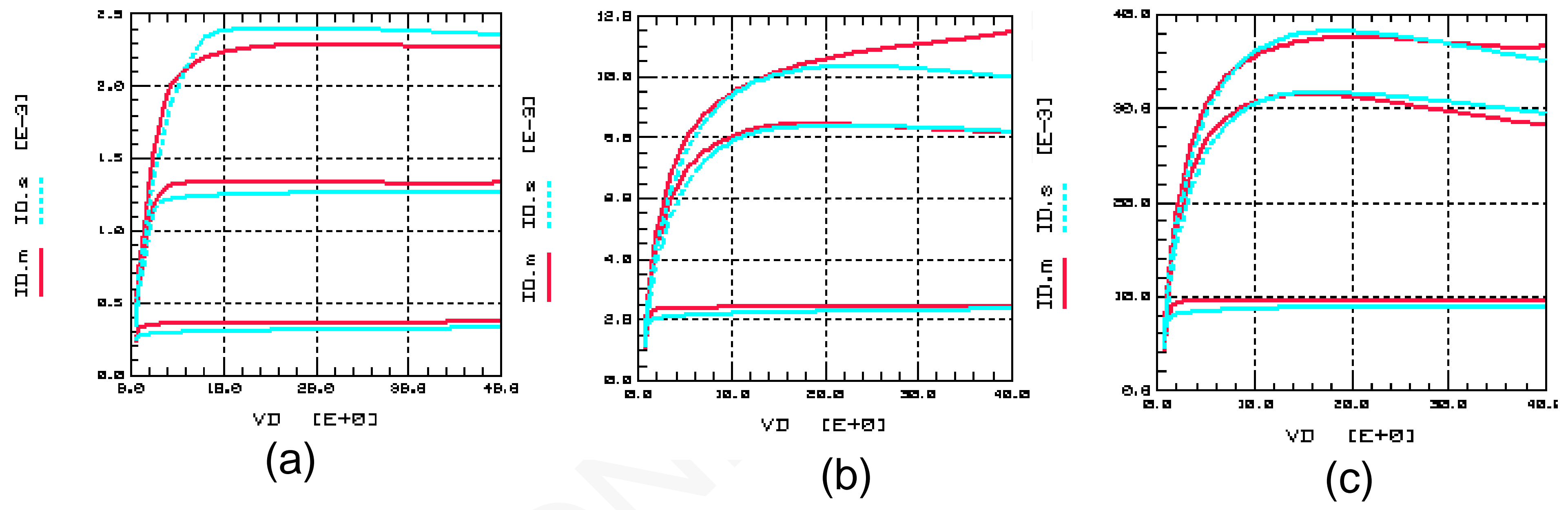



model (blue) & measurement (red):

$I_D$ vs. $V_G$ - a) minimum width, (b) medium width and (c) maximum width.

# Width Scaling : LDMOS device

## Output Characteristics




model (blue) & measurement (red):

$I_D$ vs. $V_D$ for a) minimum width, (b) medium width and (c) maximum width.

# Drift Length Scaling : 100V LDMOS

$I_D$ (mA)

0.15
0.12
0.09
0.06
0.03
0.00

Model
Measurement

$g_m$ (mA/V)

0.12
0.09
0.06
0.03
0.00

0 2 4 6 8 10 12

$V_G$ (V)

$I_D$ (mA)

10
8
6
4
2
0

Measurement
model

$V_G$=12V

$V_G$=4V

0 20 40 60 80 100

$V_D$ (V)

CONFIDENTIAL

# Demonstration of Quasi-Saturation Modeling

# Parameter Extraction and Model Calibration @ T=27°C

- Required characteristics:
  - $I_D V_{G1}$ ($I_D$ *vs* $V_G$ for $V_D$ =0.1V-0.5V)
  - $I_D V_{G2}$ ($I_D$ *vs* $V_G$ for $V_D$ =1V-5V)
  - $I_D V_D$ ($I_D$ *vs* $V_D$ for entire $V_G$)
  - $C_{GD} V_G$ @$V_D$=0V
  - $C_{GG} V_G$ @$V_D$=0V

| **EKV Parameters** | **DC – 10** |
|---|---|
| **Drift Parameters** | **DC – 8** |
| **Fitting Parameters** | **AC – 3** |
| **SHE** | **3** |

CONFIDENTIAL

# Parameter Extraction and Model Calibration

- **DC Model Calibration procedure:**
- Extract *VT0* and *U0* at low VD voltage (100mV)
- $I_D V_{G1}$ – calibrate *VT0*, *PHI* and *GAMMA* for sub-threshold slope
- $I_D V_D$ – calibrate *PHI*, *GAMMA*, *KP*(= *U0.COX*), *E0*, *UCRIT* and *LAMBDA* for saturation current
- $I_D V_{G1}$ and $I_D V_{G2}$– calibrate Drift parameters: $R_{Drift0}$, $\theta_{Acc}$ for medium-high $V_G$
- $I_D V_D$ – calibrate Drift parameters: *VSAT*, $\alpha_{vsat}$ for linear to saturation regime transition.
- The rest of the EKV parameters – default values

- **AC Model Calibration procedure:**
- 3 fitting parameters - transition from inversion to accumulation on $C_{GD}$ vs $V_G$

CONFIDENTIAL

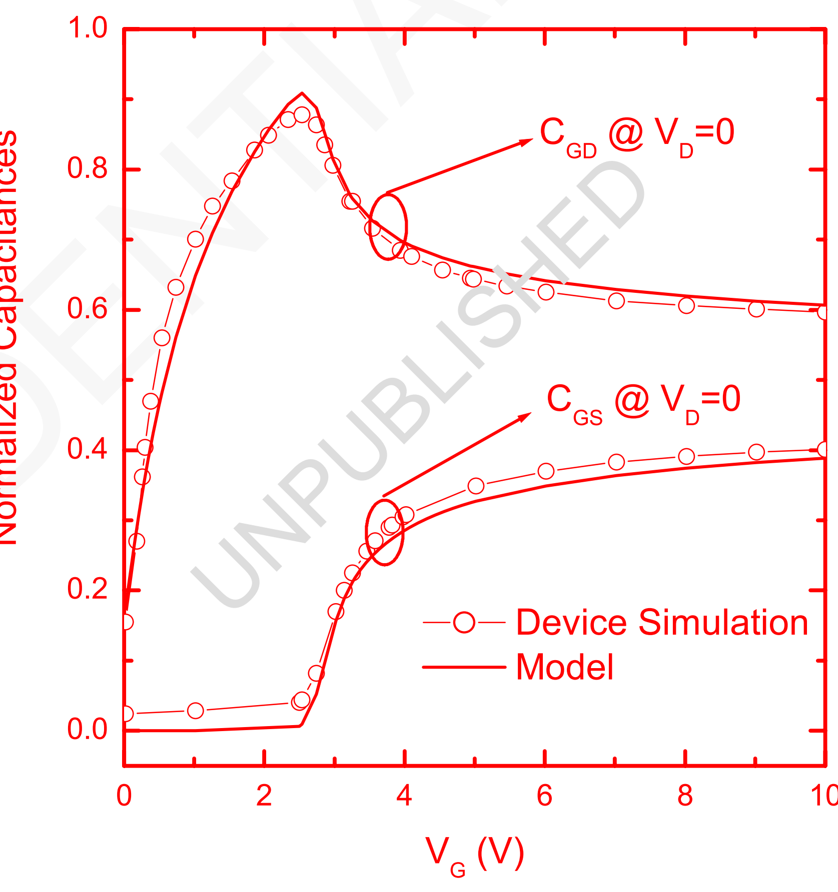
# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Recent and Ongoing R&D
- Conclusion

CONFIDENTIAL

# Modeling of Lateral Non-uniform Doping in Intrinsic MOSFET

- A charge based analytical EKV compact model developed
- Excellent results for DC and AC especially *peaks* on Capacitances




CONFIDENTIAL
UNPUBLISHED

# Model Status vs. CMC Criteria

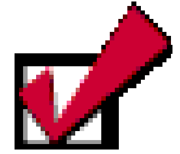
## (Must-have model features)

1. Capable for analog and RF IC simulations, which requires-

a. Accurate modeling of DC/AC behavior as well as the derivatives of terminal currents and node charges with respect to node voltages for all working modes (off, linear, saturation regions and reverse modes).

Charge model has to be charge conservative, and intrinsic charge model has to take into account the effects of voltage drop across the source and drain resistances.

b. Accurate modeling of drain extension (drift region) region resistance including velocity saturation.



c. Accurate modeling of gate/drain overlap region bias dependent capacitance and resistance.

d. Accurate modeling of parasitic effects (gate, source and drain, and substrate resistances, and source/drain-body junction diodes)

e. Accurate modeling of the 1/f, thermal, and gate induced noise.

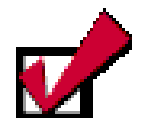
CONFIDENTIAL

# Model Status vs. CMC Criteria

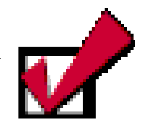
## (Must-have model features)

CONFIDENTIAL

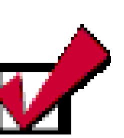
2. Capable of modeling accurately with power supplies up to 200 volts and temperature ranges from -50°C to 200°C.



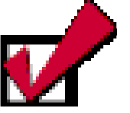
3. Capable of modeling self-heating effects accurately and efficiently, which requires scalable temperature-dependence modeling.



4. Capable of modeling accurately quasi-saturation effects and Gm fall-off in the saturation region, namely, the channel current compressions at higher Vgs when Vds is greater than Vdsat.

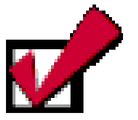


5. Capable of modeling accurately Cgd drop at higher external Vgs biases.



6. Capable of accurate modeling of the true asymmetry of the source and drain resistances and the source and drain junctions in IV and CV.

7. Capable of modeling substrate current behavior correctly including the impact ionization taking place in the drain drift extension regions.



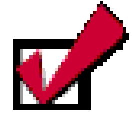
# Model Status vs. CMC Criteria

## (Must-have model features)

8. Capable of handling scalability over a wide range of geometries, biases, and temperatures with one set of global model parameter set to cover the entire device matrix provided for model extraction. Provides drain drift region length as an instance parameter.

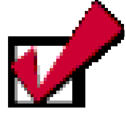
9. Capable of covering reverse working mode for both symmetric and asymmetric structure ( i.e. when Vds < 0 )

10. Capable of handing of p-type devices as well as n-type devices. **(Tested by Bosch)**



11. Capable of prediction correctly breakdown behavior.

12. Good convergence in reasonable scale circuit simulation.



CONFIDENTIAL

# Model Status vs. CMC Criteria

## (Nice-to-have model features)

1. Capable of modeling accurately a wide array of HV-MOSFET process technologies and device structures, which would include LDMOS and EDMOS (Extended Drain), both symmetrical and asymmetrical, and other drain drift extension structures including, but not limited to, those of various RESURF flavors.

2. Capable of modeling accurately the long-channel DIBL and Rout degradation for drain extended devices.

3. Capable of modeling layout dependent characteristics including multi-finger device structures that have separate, merged, and shared source and drain connections, and point and wide source/drain contacts.

4. Capable of modeling body bias dependency of DC and AC characteristics, as well as Vds-dependence of the body bias effects.

CONFIDENTIAL

# Model Status vs. CMC Criteria

**(Nice-to-have model features)**

CONFIDENTIAL

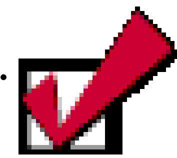
5. Capable of modeling multiple junctions for complicated LDMOS drain structures.

6. Capable of providing optional temperature node for thermal electrical coupling simulation.

7. Capable of accurately modeling the non-quasi-static effects up to 20GHz.

8. Capable of creating accurate statistical models.

9. Capable of modeling diode breakdown.

10. Capable of modeling parasitic BJT effects. 

11. Capable of modeling gate current due to hot carrier in channel and tunneling.

12. Capable of handling body diode model reverse recovery and high-level current injection effect.

13. Capable of handling second breakdown characteristics.

14. Capable of identification of SOA violations.

15. Capable of handling thermal run away.

CONFIDENTIAL

# Conclusion

- **An EKV HV MOSFET model proposed**
- **Good performance in DC and AC operations**
  - **Error ($I_{DS}$) ~ 10%**
  - **Error ($g_m$) ~ 10%**
  - **Error (*Capacitance*) ~ 25%**
- **Tested for transient operations**
- **Model validated on industrial devices**
- **Excellent convergence and scalability**
- **Self-Heating effect included – No ill convergence**
- **Implemented in *Verilog-A* – Platform independent**
- **Tested on *ELDO*, *SABER*, Spectre, *UltraSim* simulators**
- **Non-uniform doping in intrinsic MOS will be included**

CONFIDENTIAL

# Contact Person-

Prof. Adrian Mihai Ionescu

Institute of Microelectronics and Microsystems,
Electronics Laboratory (LEG-2)
Room: ELB 335
CH-1015 Lausanne, Switzerland
Phone: +41 21 693 3978 / +41 21 693 3975
Fax: +41 21 693 3640

E-mail: Adrian.Ionescu@epfl.ch

CONFIDENTIAL