# A Highly Scalable High Voltage MOSFET Model

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# Outline

- Motivation – why new HV MOSFET Model
- Device Architecture and Modeling Strategy
  - Core – Low Voltage EKV MOSFET Model
  - Analytical bias dependent drift resistance
  - Strategy for charge evaluation based on $V_K$
- Validation and Results
  - Most of the results on VDMOS
  - Some results on LDMOS
- Conclusion

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# Motivation

- Robust HV Model for circuit simulators
- Analytical & Physical Compact Model
- Accuracy in DC & AC
- Small number of parameters: EKV!
- Scaling with physical & electrical parameters
- Convergence and Speed
- Open Source

- ***General*** **HV-MOS Model?**

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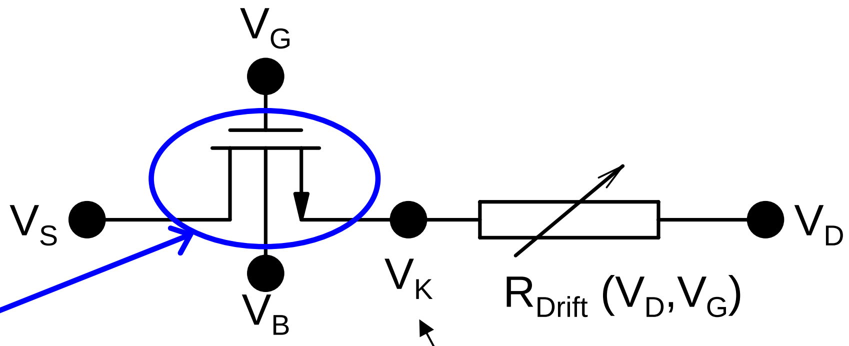
# *General* HV MOSFET Modeling Strategy



**EKV MOSFET Model**

**(constant doping)**

**Intrinsic drain potential**

- **EKV Model**
  - **Physically based parameters**
  - **Less parameters than BSIM**

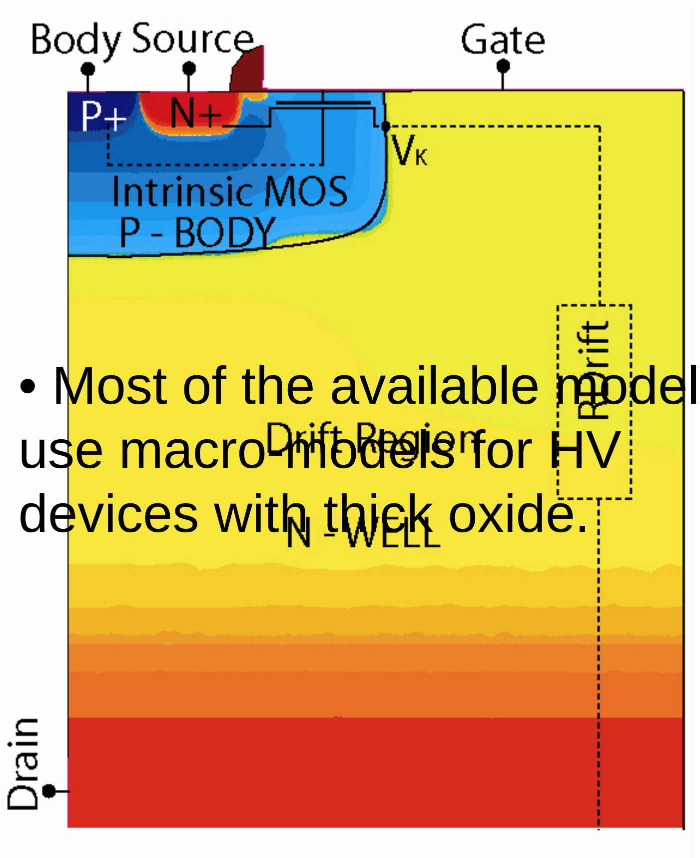
# Device Architectures

- **VDMOS :**

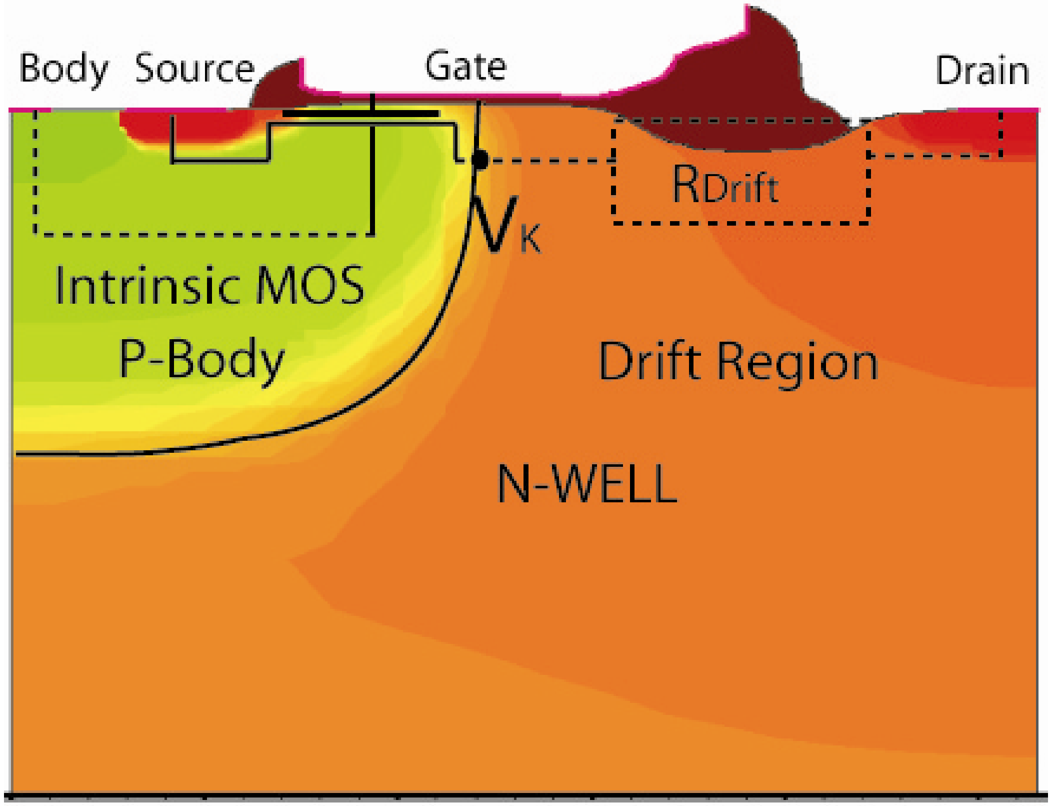
**$V_{Dmax}$=50V, $V_{Gmax}$=3.3V**

- **LDMOS :**

**$V_{Dmax}$=40-100V, $V_{Gmax}$=13V**



- Most of the available models use macro-models for HV devices with thick oxide.



# Main EKV Parameters

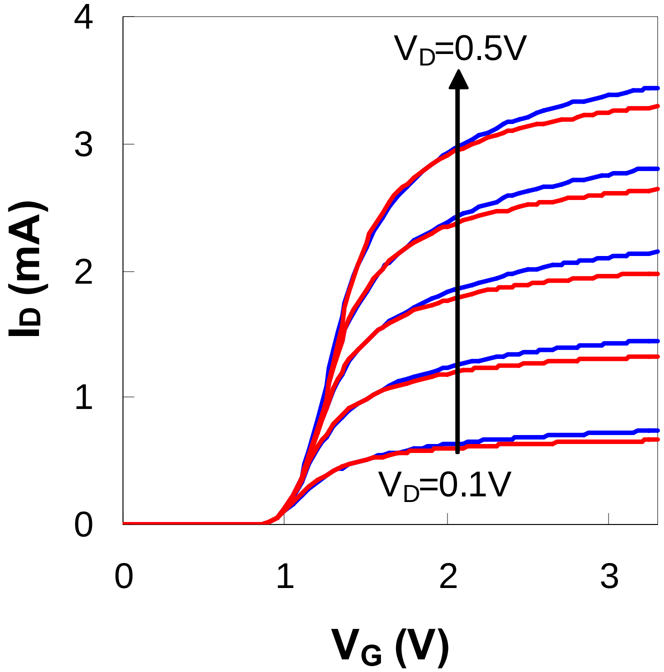
| Name | Description | Units |
|---|---|---|
| W | Channel Width | m |
| L | Channel Length | m |
| COX | Oxide Cap. per unit area | $F/m^2$ |
| VT0 | Long-channel Threshold Voltage | V |
| U0 | Low Field mobility | $cm^2/Vs$ |
| GAMMA | Body Effect Parameter | $V^{1/2}$ |
| PHI | Bulk Fermi Potential | V |
| E0 | Mobility Reduction Coefficient | V/m |
| UCRIT | Longitudinal Critical Field | V/m |
| LAMBDA | Channel Length Modulation | - |

# Modeling Strategy

- Drift Resistance expression

**Why not?**

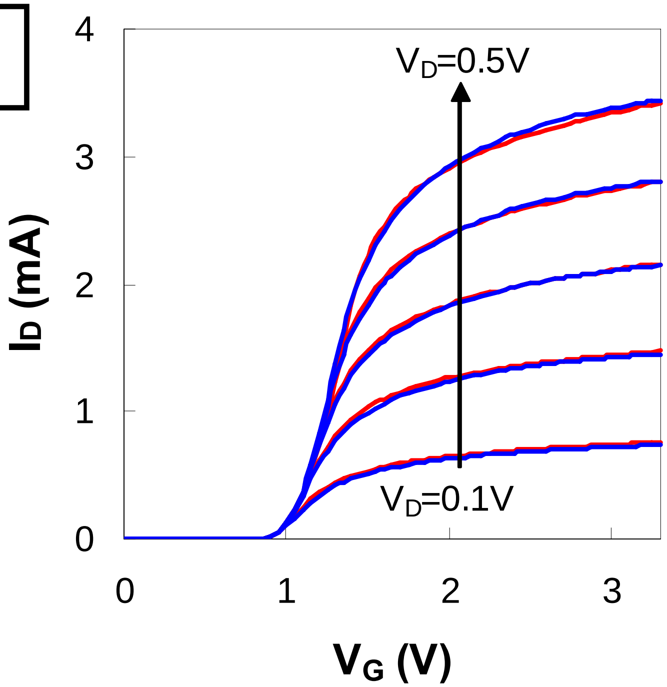
$$R_{Drift} = R = \text{constant}$$



**Low $V_D$**

**Accumulation in Drift**

$$R_{Drift} = \frac{R_{Drift0}}{(1+\theta_{Acc}.V_G)}$$



(red - model & blue - measurement)

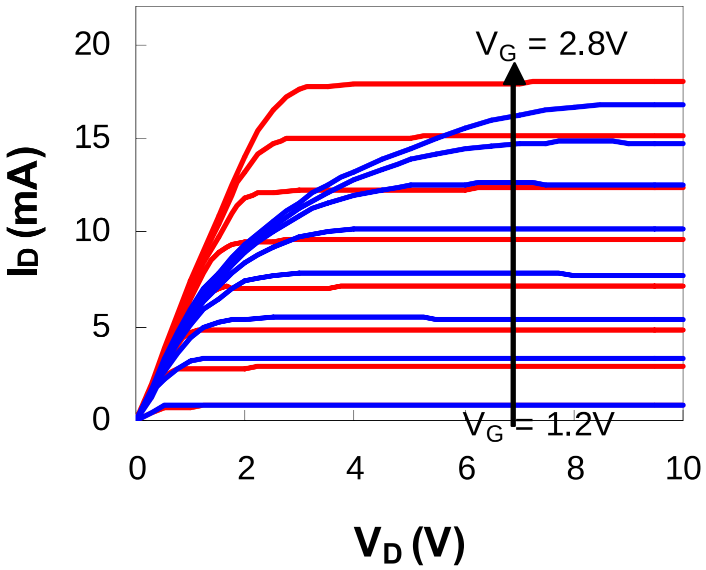
# Modeling Strategy

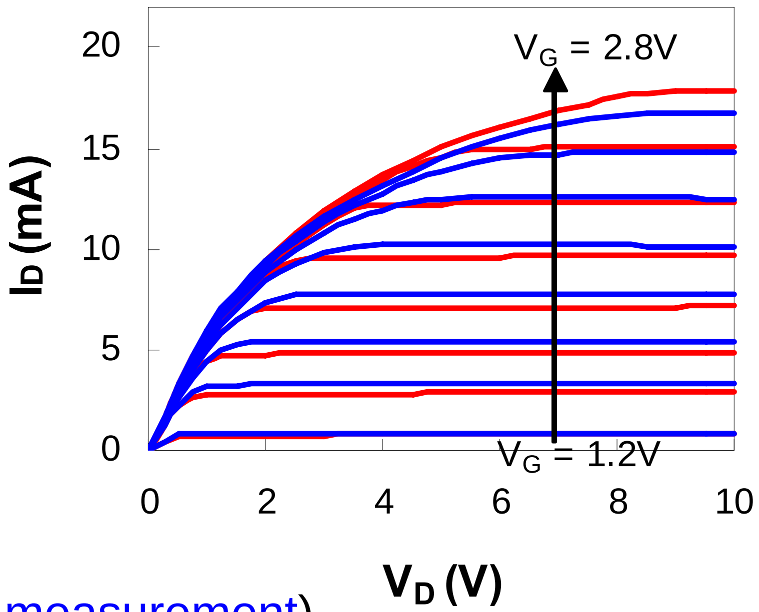
- Drift part mainly affects the linear region of the output characteristics.
- Delayed transition between linear and saturation regime at high $V_G$ - velocity saturation in the drift

**High $V_D$ but linear region**

$$R_{Drift} = \frac{R_{Drift0}}{(1+\theta_{Acc}.V_G)}$$

$$R_{Drift} = R_{Drift0}\frac{\left[1+\left(\frac{V_D - V_K}{VSAT}\right)^{\alpha_{vsat}}\right]}{1+\theta_{Acc}.V_G}$$





(red - model & blue - measurement)

# Scalable Drift Resistance

+ : Drain-on-sides

- : Drain all-around

Effect of Temperature

$$R_{Drift} = R_{Drift0}\frac{\left[1+\left(\frac{V_D - V_K}{VSAT}\right)^{\alpha_{vsat}}\right]}{(1+\theta_{Acc}V_G)}\left(1\pm(k_{rd}-1)\frac{N_F-1}{N_F+N_{CRIT}}\right)\overbrace{\left(1+\alpha_T.\Delta T\right)}$$

$$R_{Drift0} = \rho_{Drift0}\left(\frac{L_{DR}}{N_F\underbrace{(W+\Delta W)}}\right)$$

Drift Length

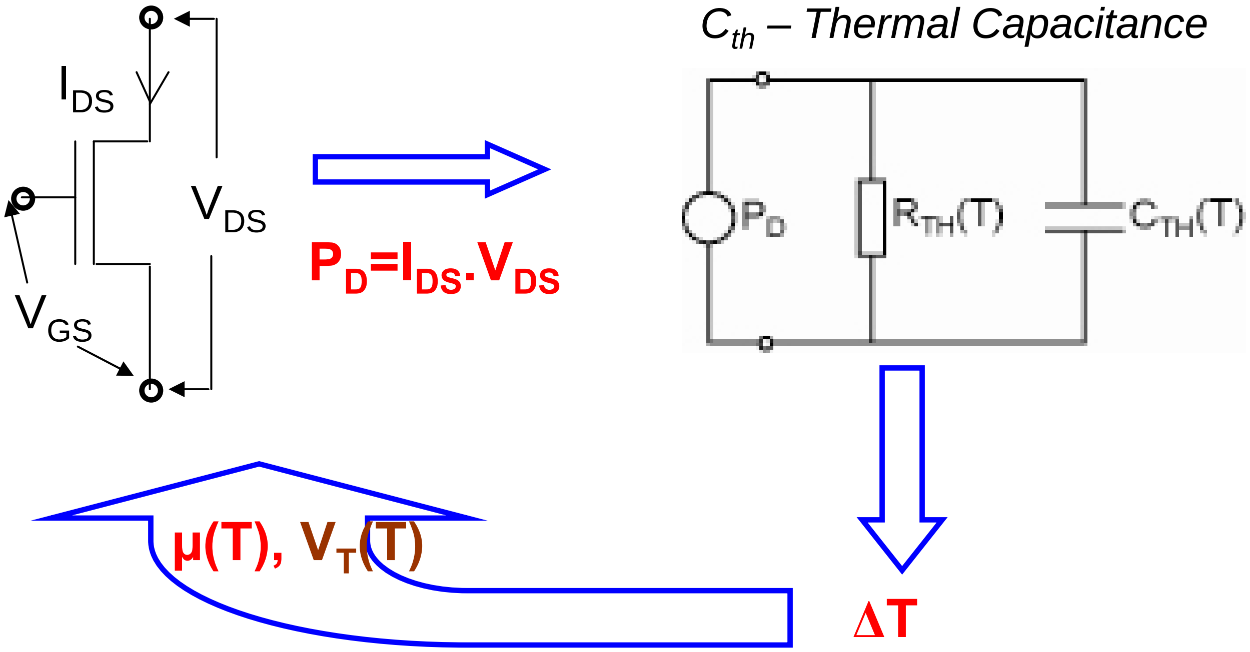
Number of Fingers

Width and Width Offset

# Modeling of Self Heating Effect

*$R_{th}$ – Thermal Resistance*

*$C_{th}$ – Thermal Capacitance*



$P_D = I_{DS} . V_{DS}$

$\mu(T)$, $V_T(T)$

$\Delta T$

- External Temperature Node

Ref: C. Anghel et al., “Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs”, IEEE Electron Device Lett., 141 - 143, 2004

# AC Modeling

- Charges in MOSFET and Drift region

$$Q_G = Q_{EKV} + Q_{Drift} = Q_S + Q_K + Q_B + Q_{Drift}$$

$$Q_{Drift} = (V_G - V_{FB} - \psi_s).W.L_{DR}.C_{ox}$$

Assumptions

- $\Psi_S$ varies linearly across accumulation charge sheet

# AC Modeling

## $V_K$ behavior

- As mentioned earlier, Drift does not affect the transistor characteristics in saturation.
- $V_K$ obtained from Spice is valid for linear region. Many models use interpolation function for smooth $V_K$ from linear to saturation.

Normalized reverse Current

$$i_r = [\ln(1+e^{\frac{v_p - v_k}{2}})]^2$$

Normalized charge density at $V_K$ (EKV)

$$q_k = \sqrt{i_r + 0.25} - 0.5$$

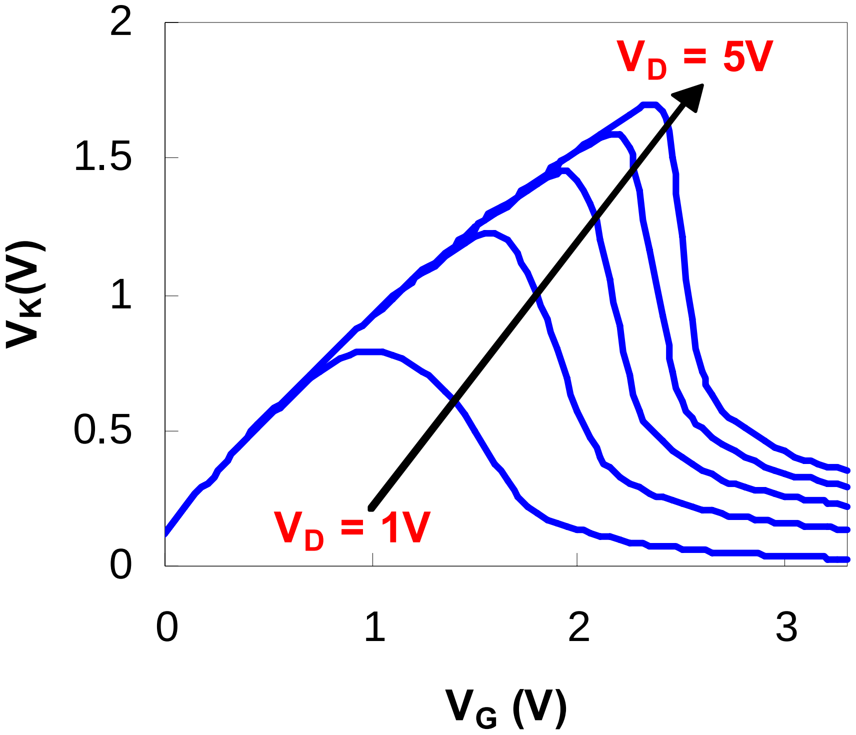
Normalized $v_k$ (EKV)

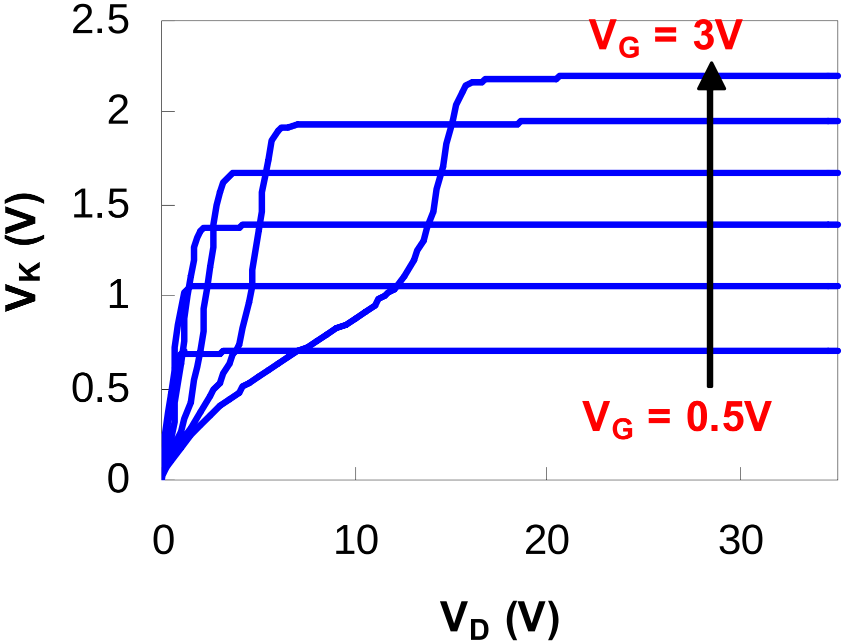
$$v_k = \frac{V_K}{U_T} = v_p - (2.q_k + \ln(q_k))$$

Ref: J.-M. Sallese et al., “Inversion charge lineariazation in MOSFET modeling and rigorous derivation of the EKV compact model”, Solid-State Electronics,pp. 677-683, 2003

# $V_K$ vs. $V_G$ and $V_D$ for VDMOS

- $V_K$ – Important parameter for design of HV-MOS





- Trend matches with device simulation and also reported with literature

Ref: C.H. Kreuzer et al., "Physically based description of quasi-saturation region of vertical DMOS power transistors", IEDM,pp. 489 - 492, 1996

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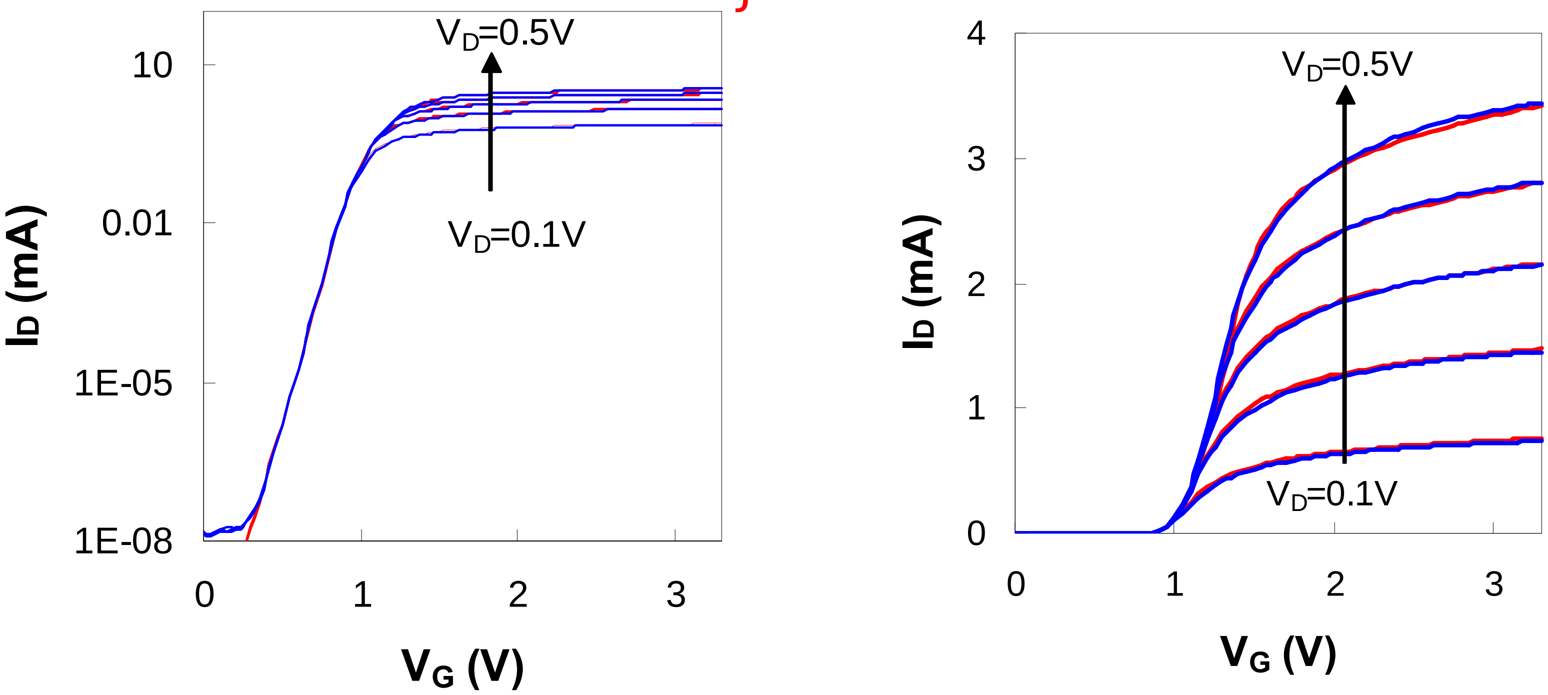
# Model Validation on 50V VDMOS

## Transfer Characteristics ($I_D$-$V_G$)

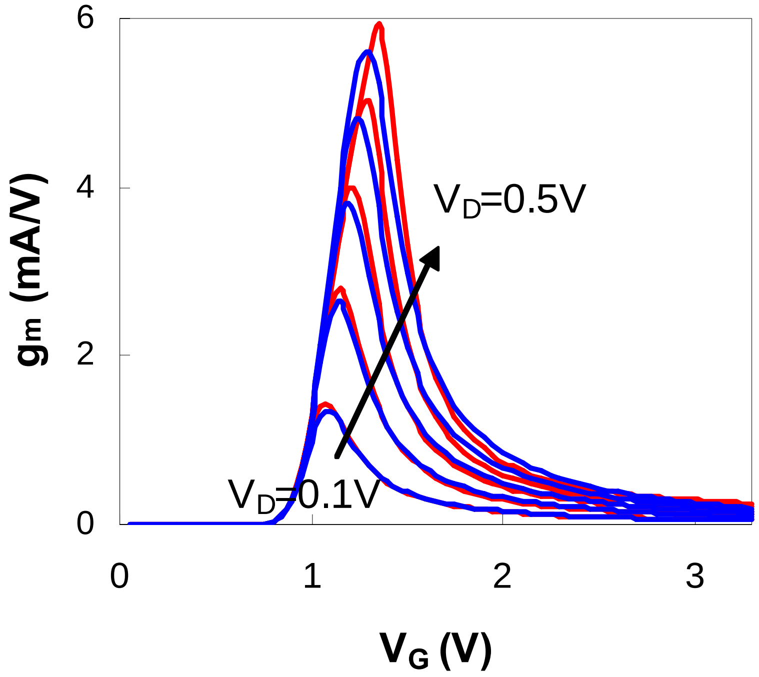
$V_D$=0.1 to 0.5V

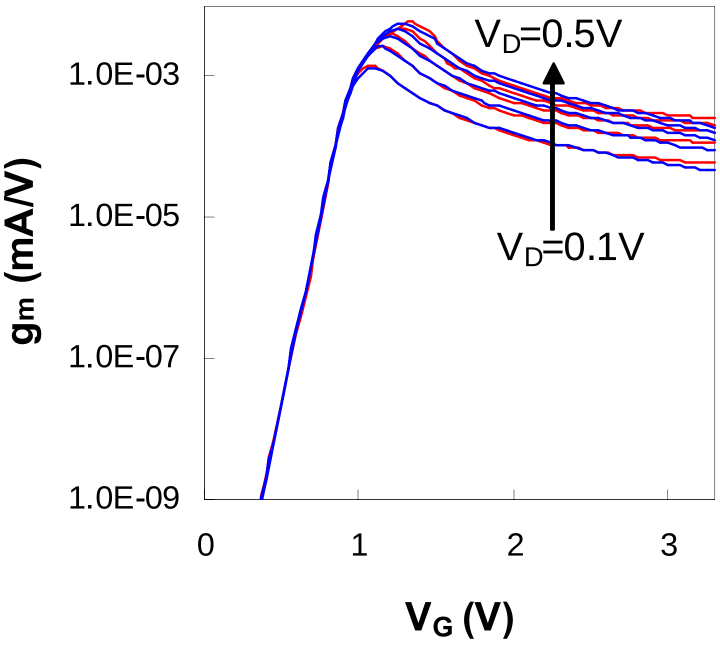


- Weak inversion to Strong inversion transition
- Subthreshold slope correctly matched
- Good accuracy

(red - model & blue - measurement)

# Transconductance for $V_D$=0.1-0.5V

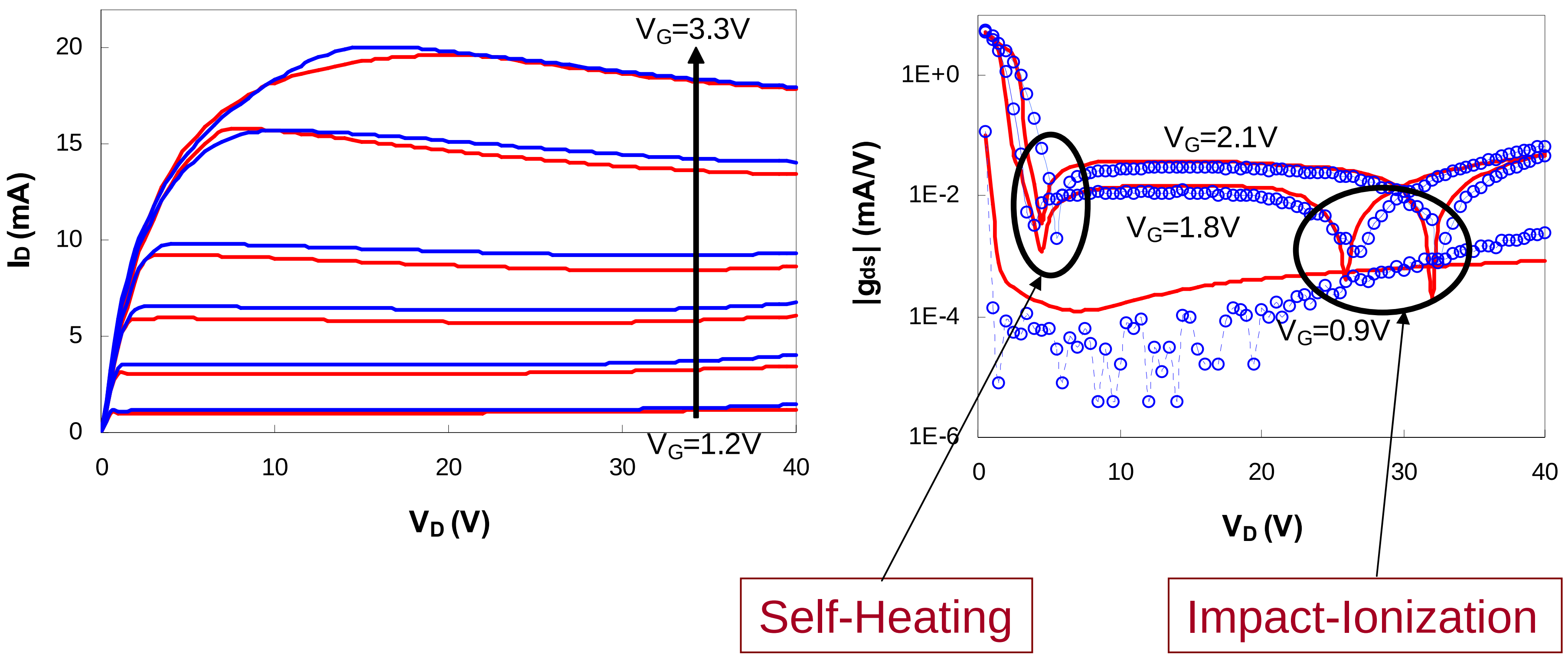




- Subthreshold slope correctly matched
- descending slope – drift resistance

(red - model & blue - measurement)

# Output Characteristics



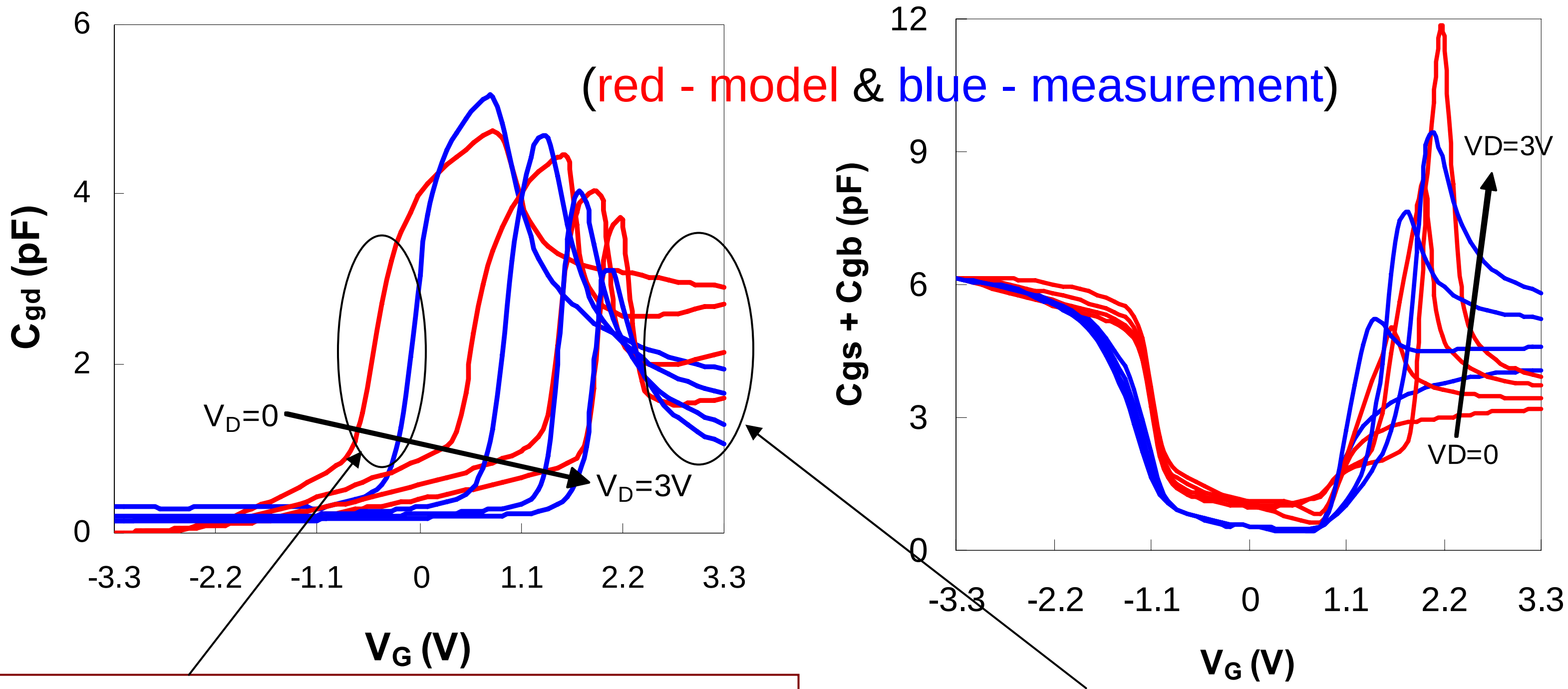
Self-Heating

Impact-Ionization

- Linear region correctly modeled by drift resistance.
- Self Heating Effect
- Peaks on $g_{ds}$

(red - model & blue - measurement)

# $C_{GD}$ and $C_{GS}$+$C_{GB}$ vs $V_G$
# $V_D$=0-3V



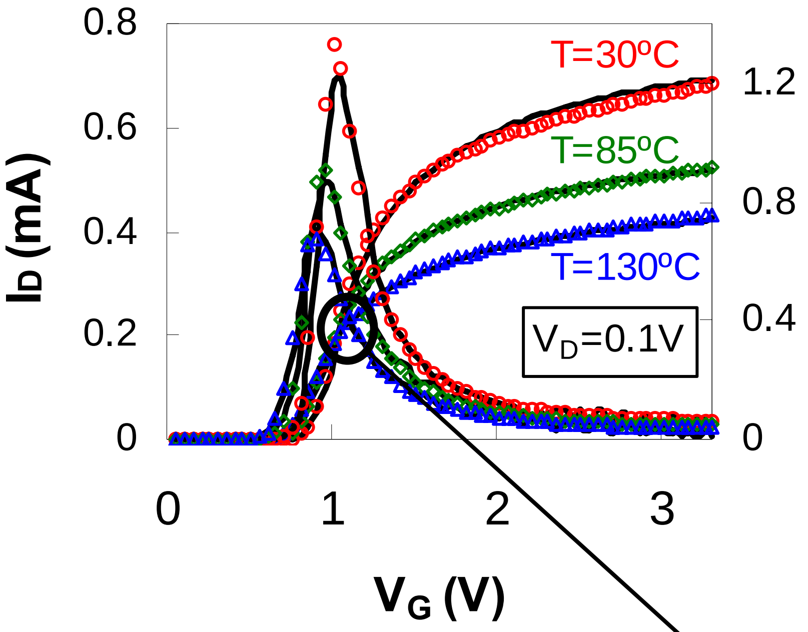
Lateral Doping in the channel

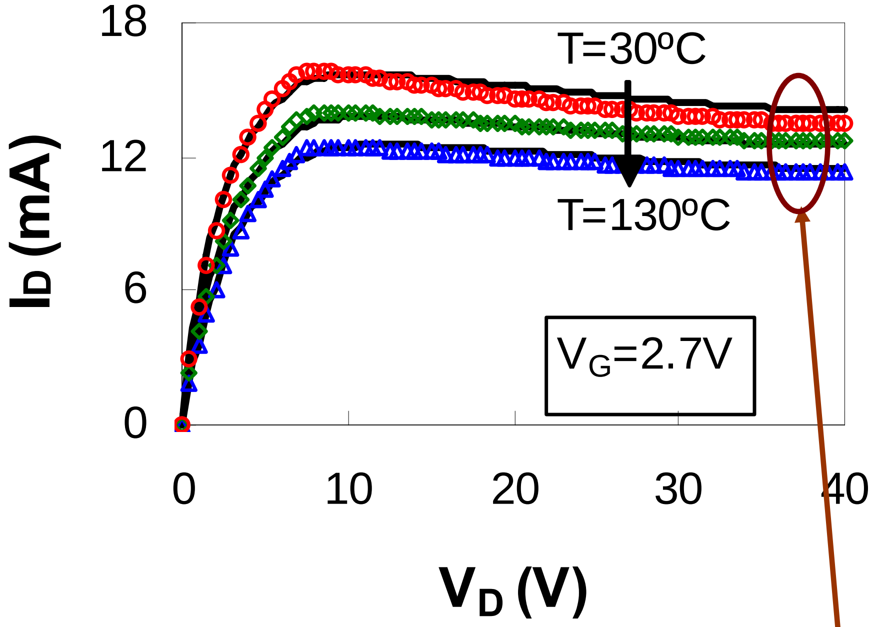
Interpolation function used in drift (to be improved)

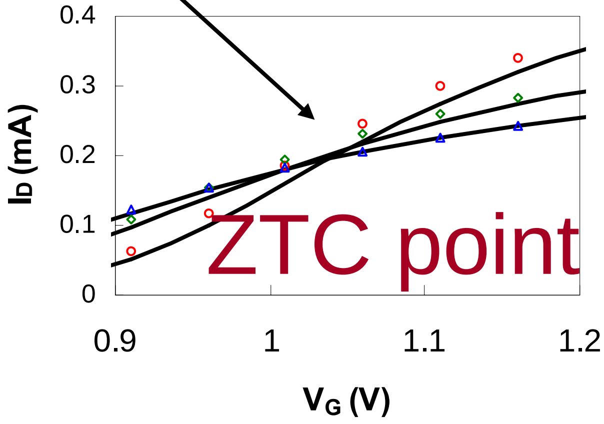
- Modeling of Non-uniform doping in intrinsic MOS (Chauhan et al. in *IEDM 2006*)

# Temperature Scaling in VDMOS

(color - model & black - measurement)

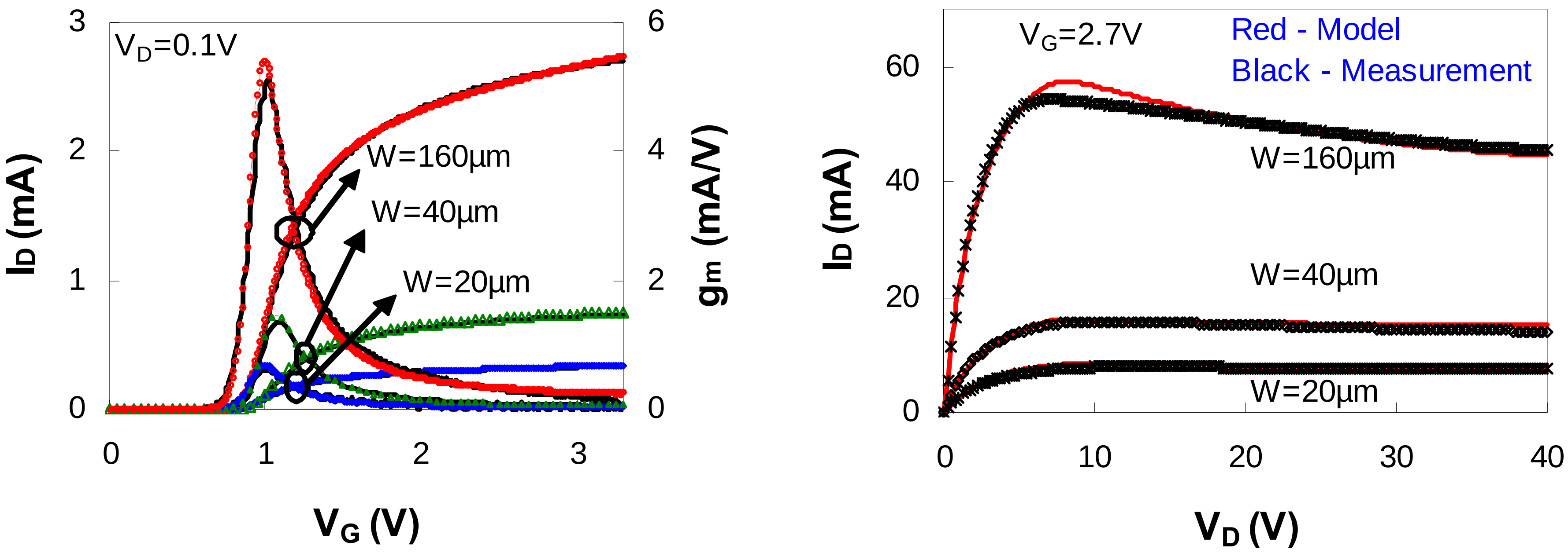






Self-Heating scales well with temperature

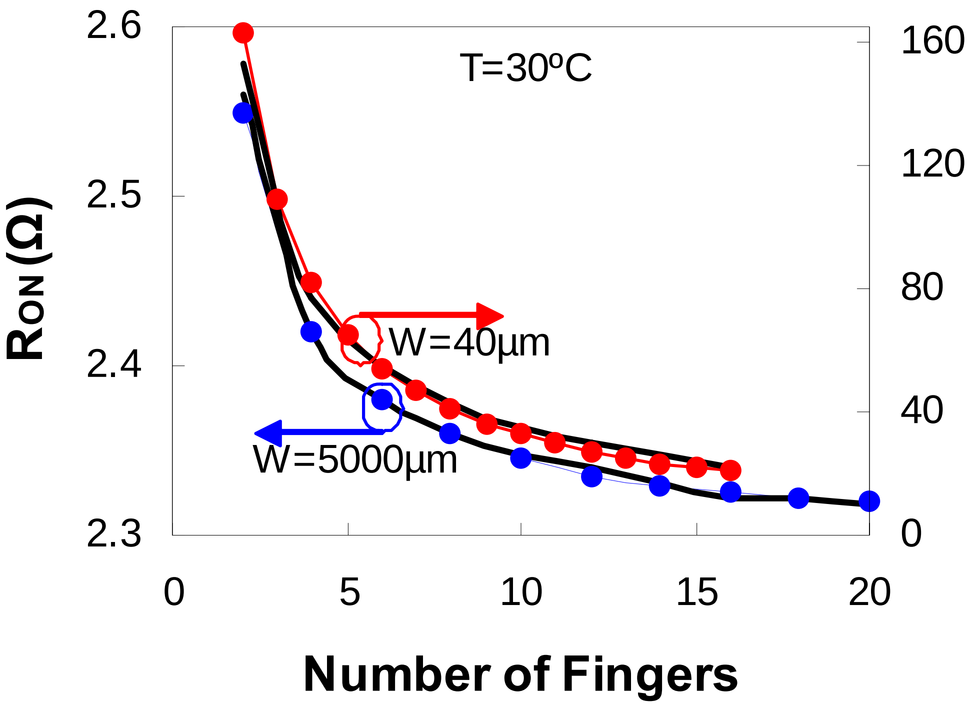
# Width Scaling in VDMOS



- Increase in Current and transconductance with Width

(red - model & black - measurement)

# $R_{ON}$ Scaling with number of fingers in VDMOS



- $R_{ON}$ ⬇ - $N_F$ ⬆ for drain all-around-device due to current spreading at finger edges

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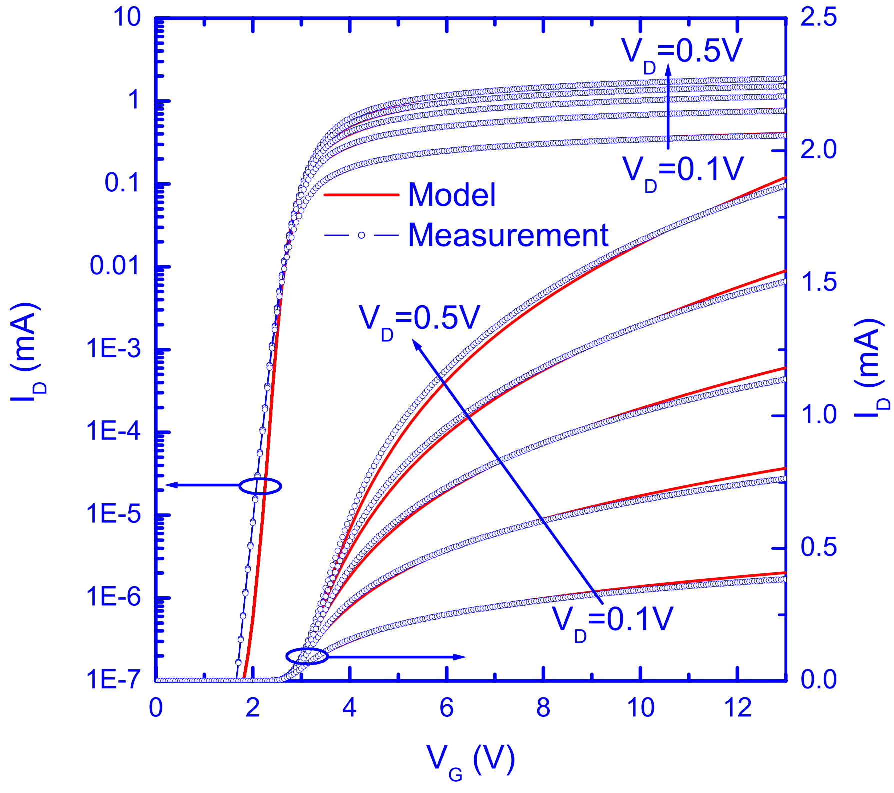
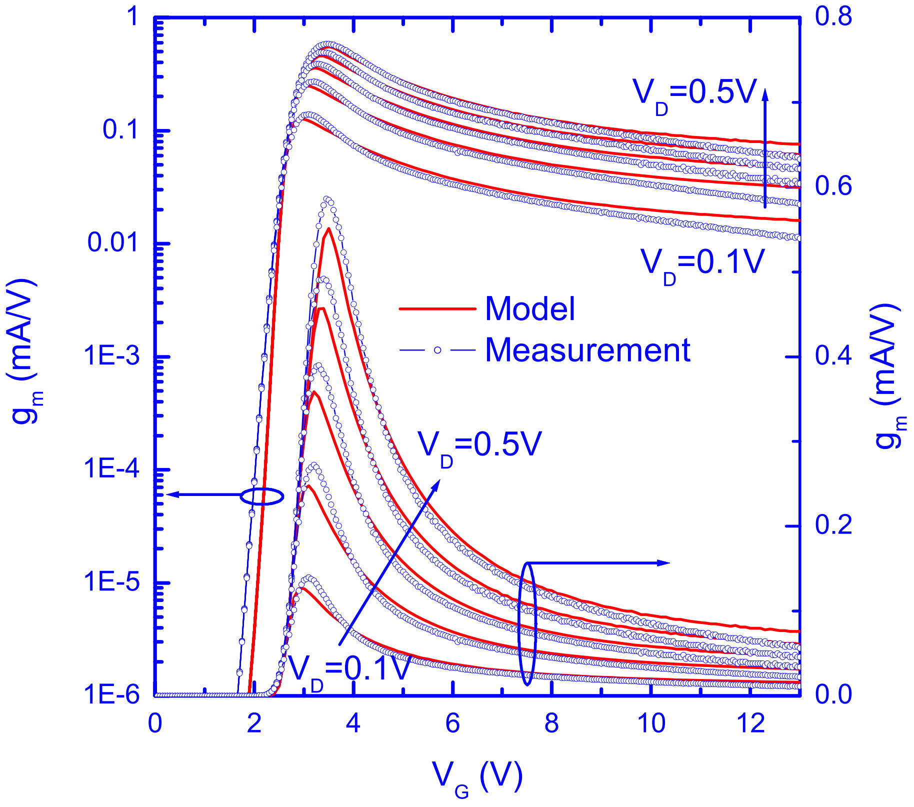
# Model Validation on 40V LDMOS

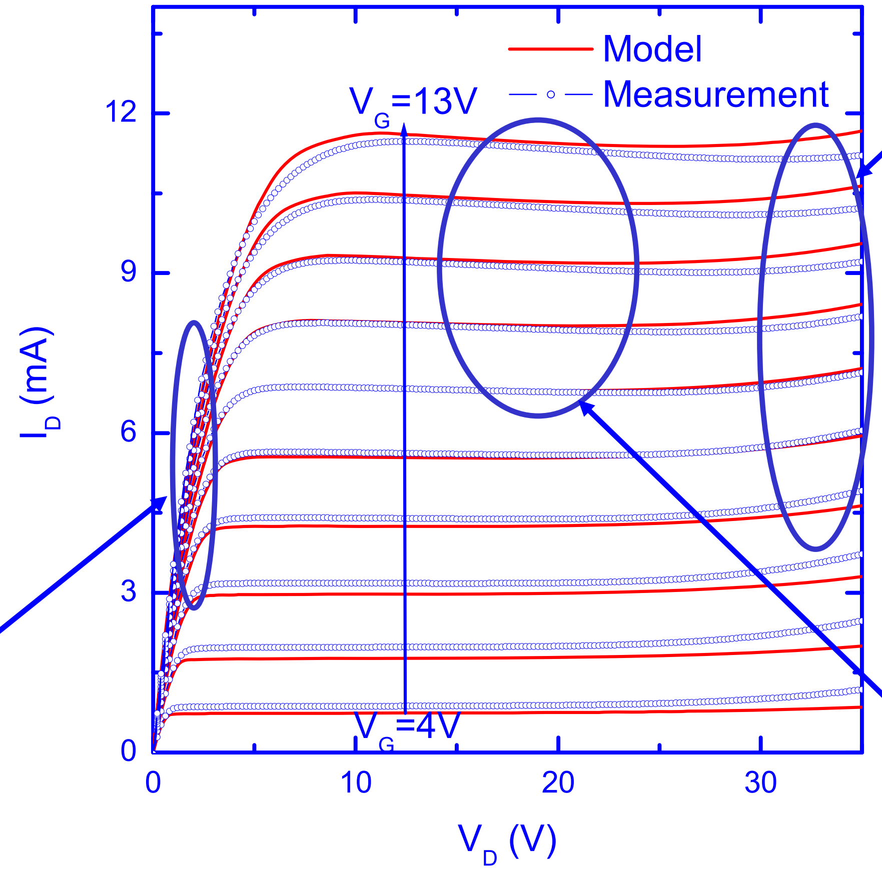
## Transfer Characteristics





# Model Validation on 40V LDMOS

## Output Characteristics

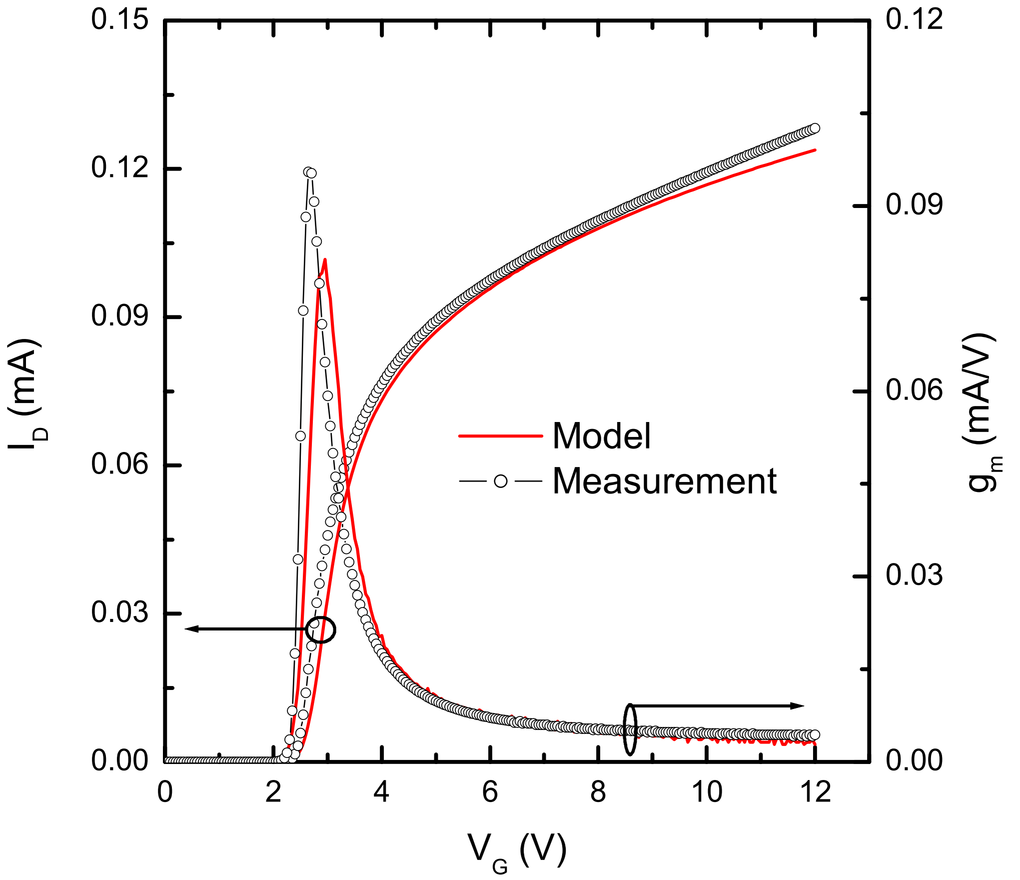


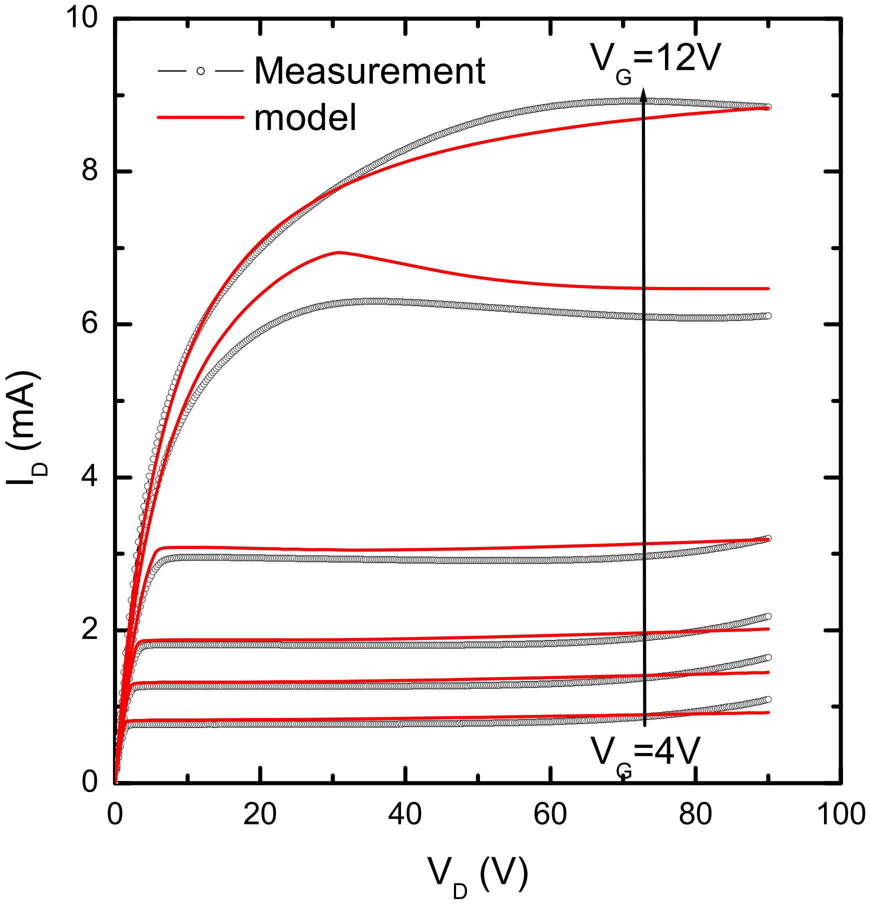
Impact-Ionization Effect

Effect of drift resistance

Self-Heating Effect

# Drift Length Scaling : 100V LDMOS





# Conclusion

- An HV-EKV MOSFET model proposed
- Main number of parameters - 24
- Good performance in DC and AC operations
  - Error ($I_{DS}$) ~ 10%
  - Error ($g_m$) ~ 10%
  - Error (*Capacitance*) ~ 25%
- Tested for transient operations
- Model validated on industrial devices
- Excellent convergence and scalability
- Self-Heating effect included – No ill convergence
- Implemented in *Verilog-A* – Platform independent
- Tested on *ELDO*, *SABER*, Spectre, *UltraSim* simulators
- Model has been accepted for evaluation as a candidate for LDMOS standardization by *CMC*

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