Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs

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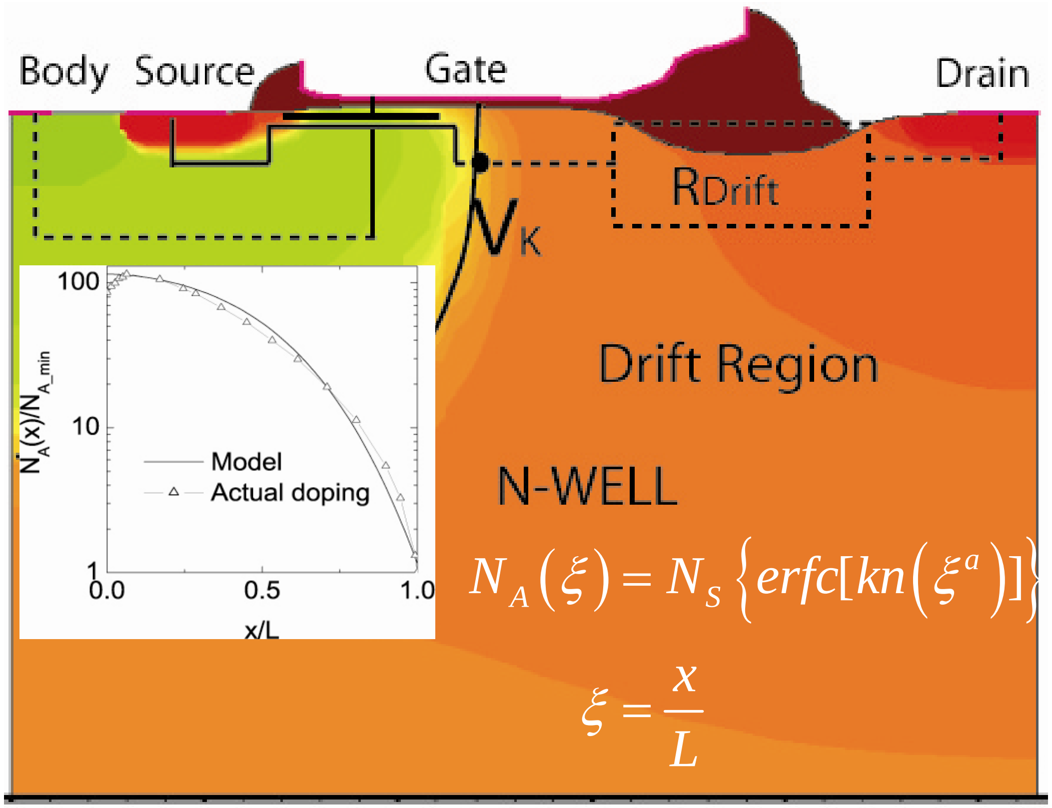
Outline

- High Voltage device architectures
- Impact of Lateral non-uniform doping on device characteristics
- Model description
- Model validation
  - VDMOS – shown in this presentation
  - LDMOS – shown in the paper
- Conclusion

Device Architectures

- **LDMOS :**

V_{Dmax}=40-100V, V_{Gmax}=13V

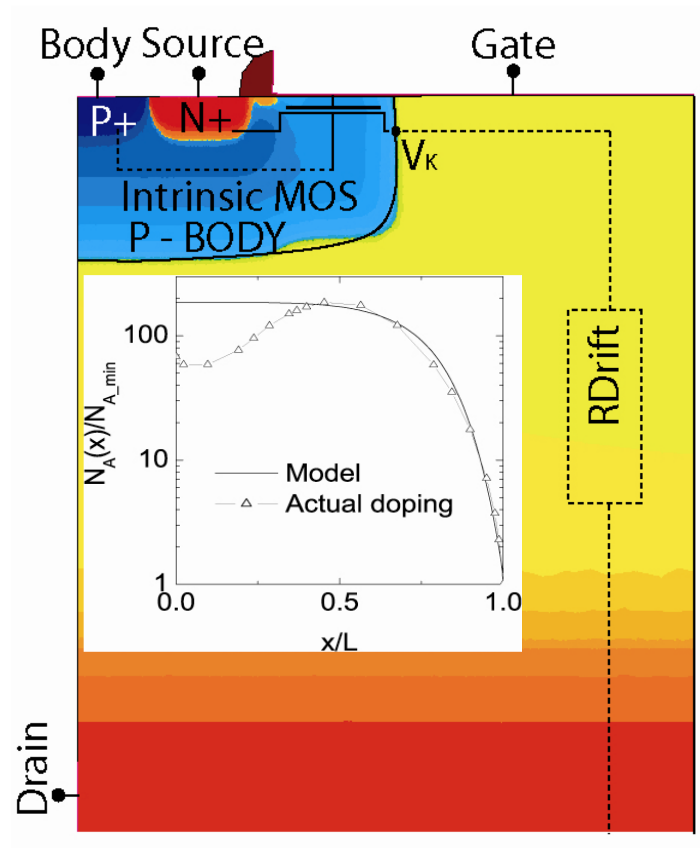


$$N_A(\xi) = N_S\left\{erfc[kn(\xi^a)]\right\}$$

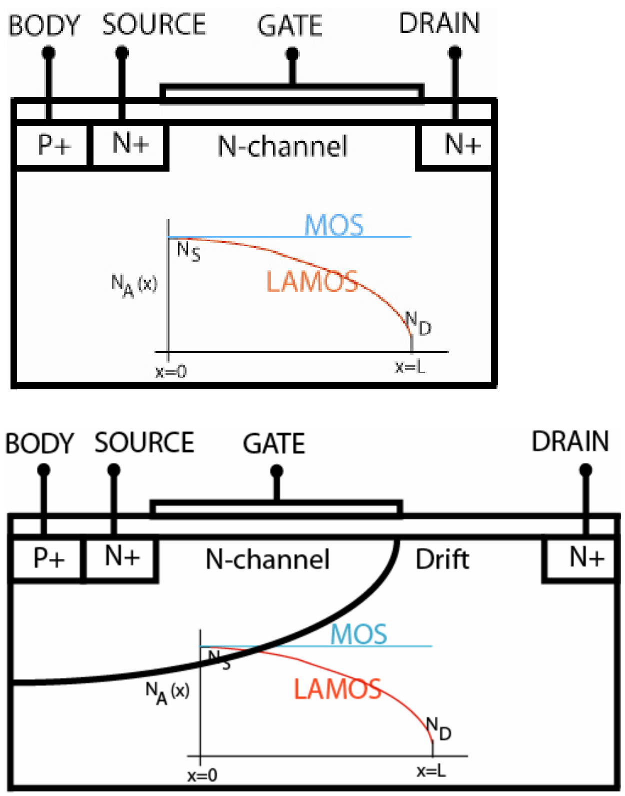
$$\xi = \frac{x}{L}$$

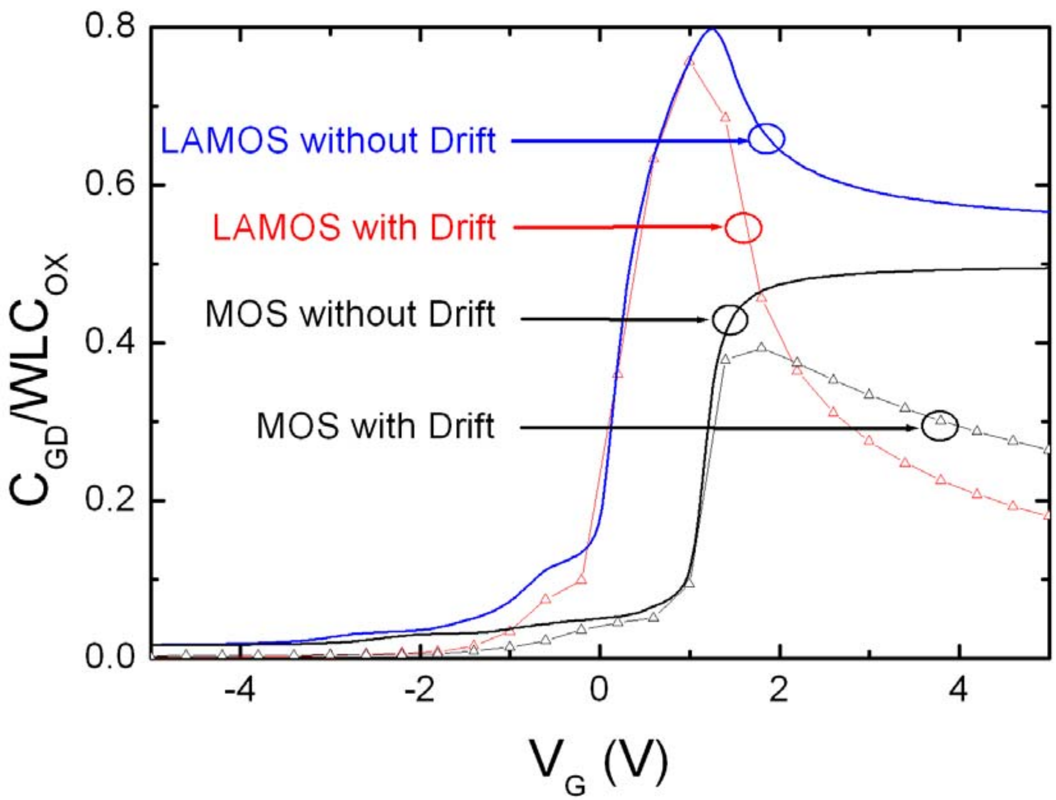
- **VDMOS :**

V_{Dmax}=50V, V_{Gmax}=3.3V



Difference between Conventional MOS and Lateral Asymmetric MOS (LAMOS)



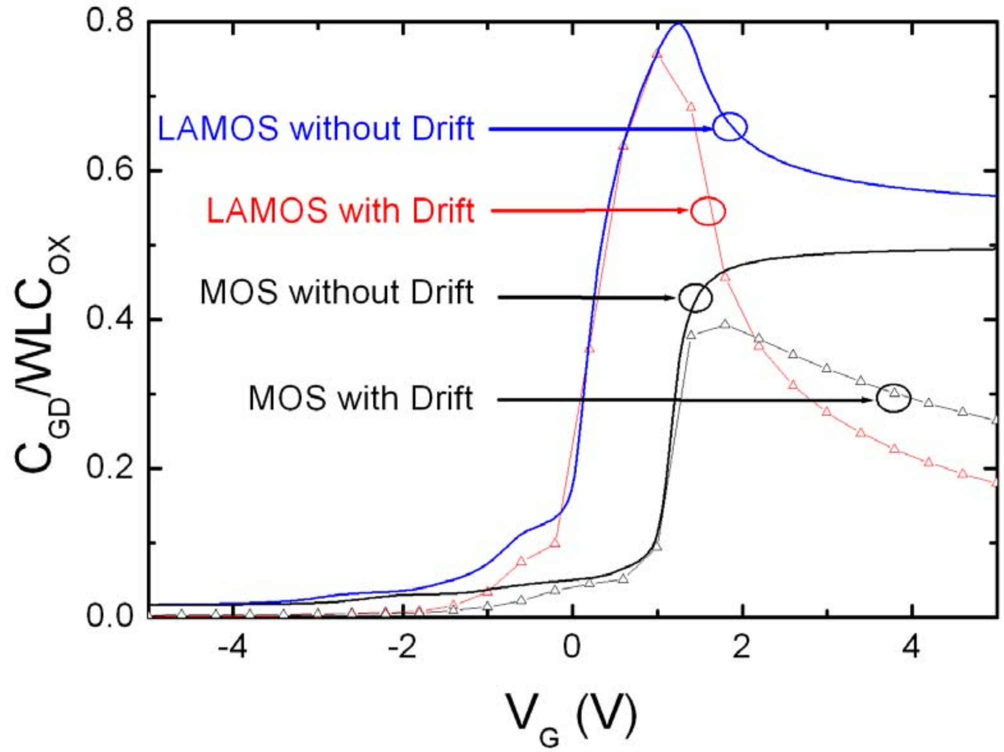


- LAMOS –higher C_{GD}
- Drift region in high voltage MOS decreases C_{GD}
- The peak in C_{GD} of LAMOS – effect of lateral doping

Difference between Conventional MOS and Lateral Asymmetric MOS (LAMOS)

$$C_{GD} = \frac{dQ_G(V_G, V_K, V_S)}{dV_D}$$

$$= C_{GD\_LAMOS} \frac{dV_K}{dV_D}$$



- LAMOS –higher C_{GD}
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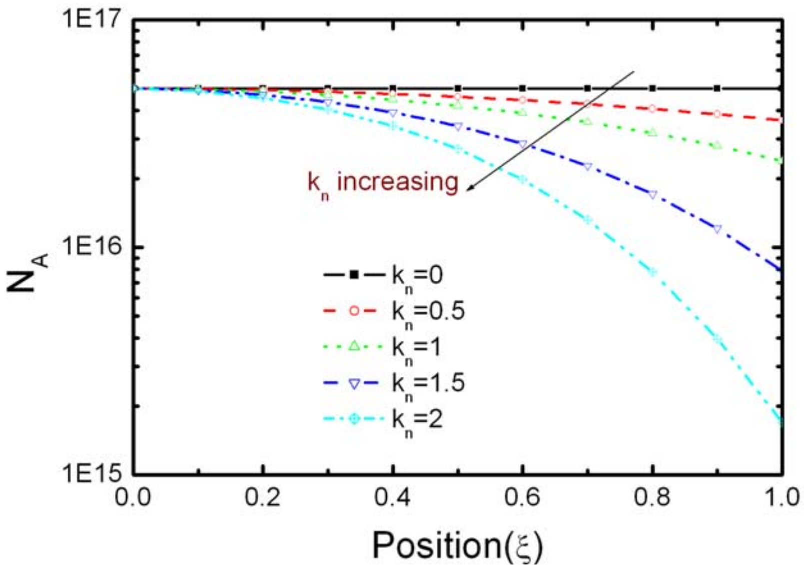
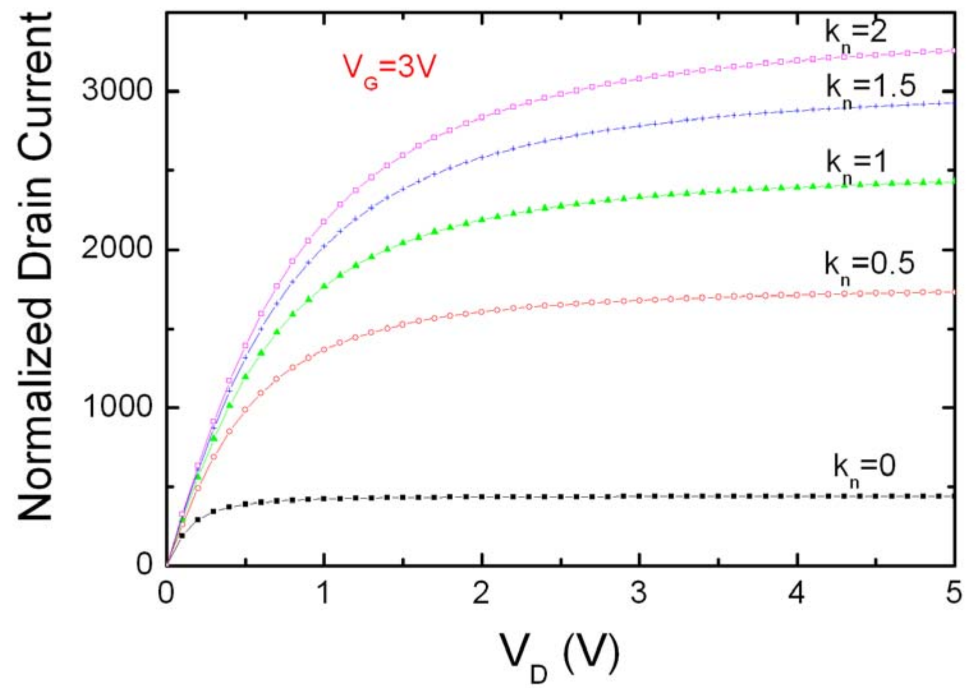
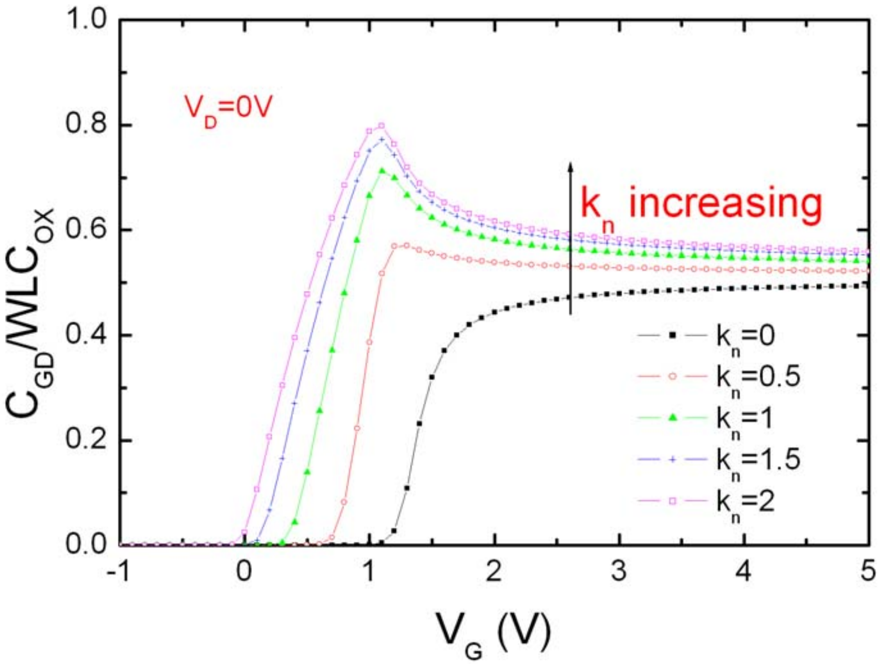
Impact of different Doping gradients on device characteristics

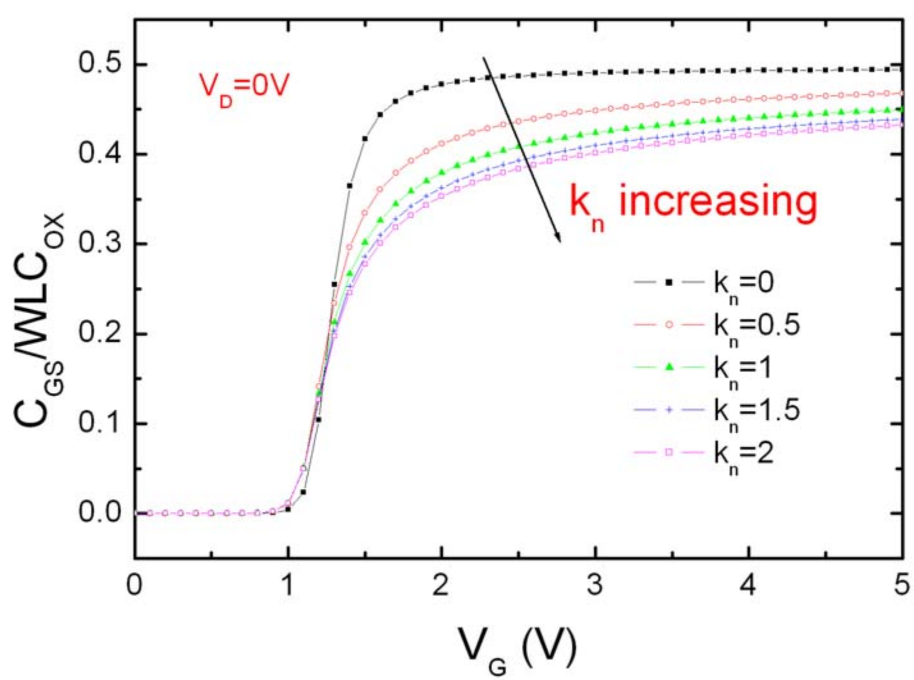




- Higher gradient – higher current
- Higher gradient – higher saturation voltage

Contd.- Impact of different Doping gradients on device characteristics





- Higher doping gradient
  - Higher C_{GD} and lower C_{GS} in strong inversion
  - Rising slope decreases
  - Peak on C_{GD} increases

Modeling of LAMOS

$$I_D = I_{Drift} + I_{Diff} = \mu W \left(-Q_i \frac{d\Psi_S}{dx} + U_T \frac{dQ_i}{dx} \right)$$

Q_i: explicit fun. of x

Ψ_p: explicit fun. of x

Nonlinear Ordinary Diff. Eq. ⇨

$$\frac{dq}{d\xi} = -\frac{i_{ds} + \rho_v \left(i_{ds} \frac{\delta_{sat}}{2} - q \right) \frac{d\psi_p}{d\xi}}{\rho_v \left(1 + 2q - \delta_{sat} i_{ds}\right)}$$

Assume

$$\frac{d\psi_p}{d\xi} = \Delta\psi_p = \text{constant}$$

Drain Current

$$\Delta\psi_p = 2(q_d - q_s) + \left(1 + \frac{2i_{ds}}{\rho_v \Delta\psi_p}\right) \ln \left[\frac{q_d - i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)}{q_s - i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)} \right]$$

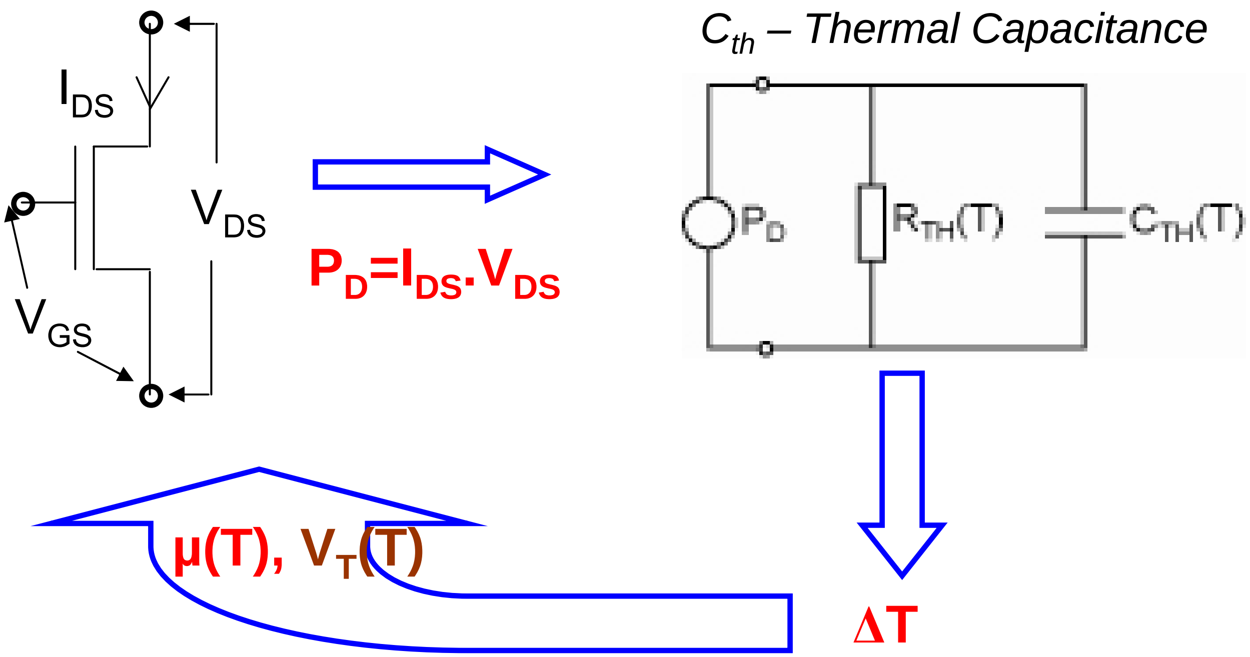
Total Inversion Charge Density

$$q_c = \frac{q_d^2 - q_s^2}{\Delta\psi_p} + \frac{q_d - q_s}{\Delta\psi_p}\left(1 - \delta_{sat} i_{ds}\right) + i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)$$

Modeling of Self Heating Effect

R_{th} – Thermal Resistance

C_{th} – Thermal Capacitance

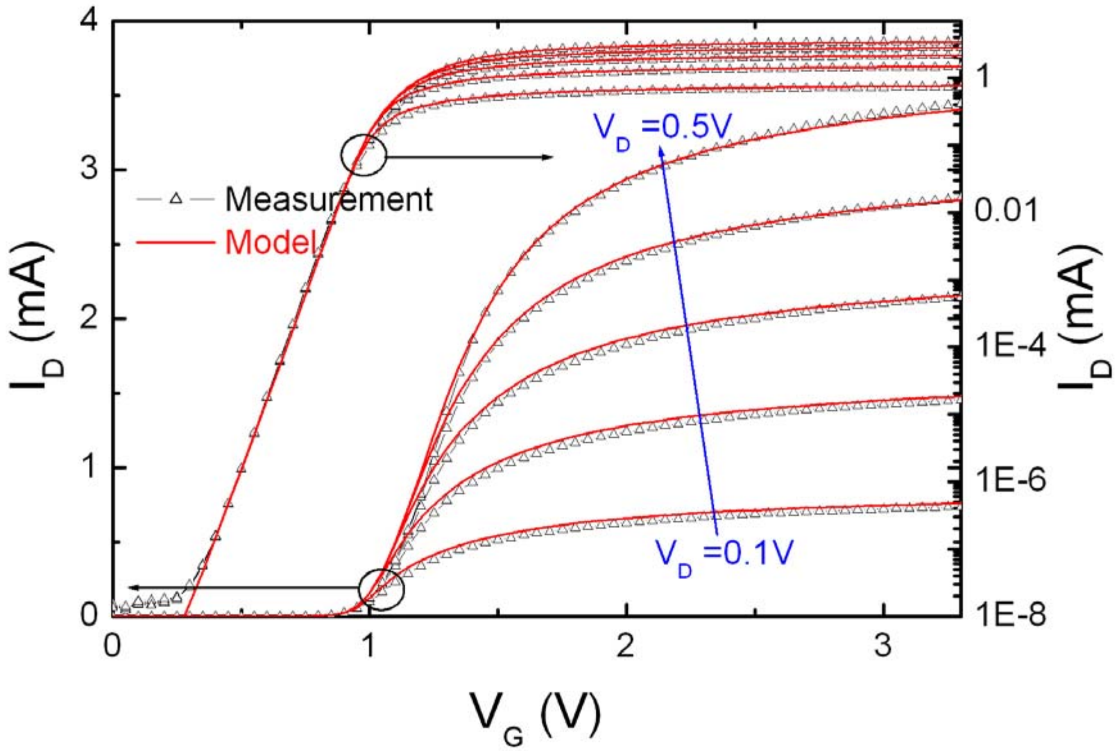


- External Temperature Node

Ref: C. Anghel et al., “Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs”, IEEE Electron Device Lett., 141 - 143, 2004

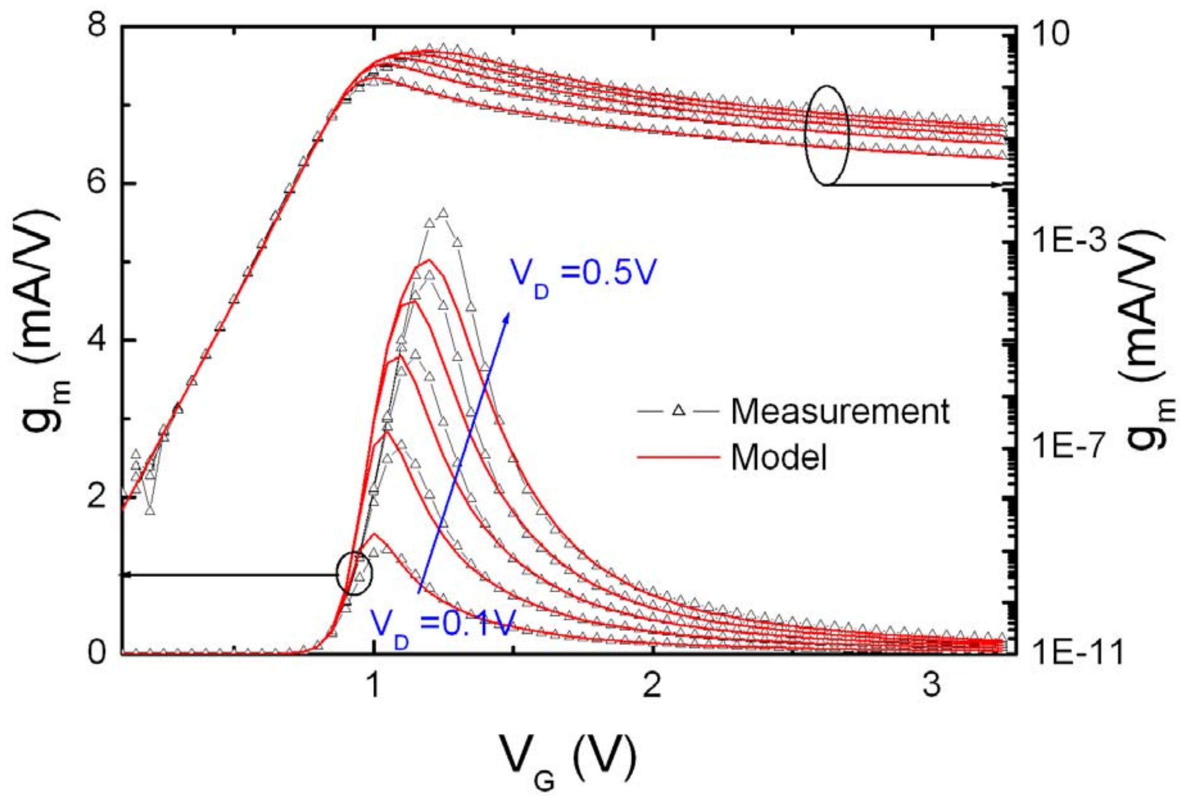
Model Validation on 50V VDMOS

Transfer Characteristics (I_D-V_G)



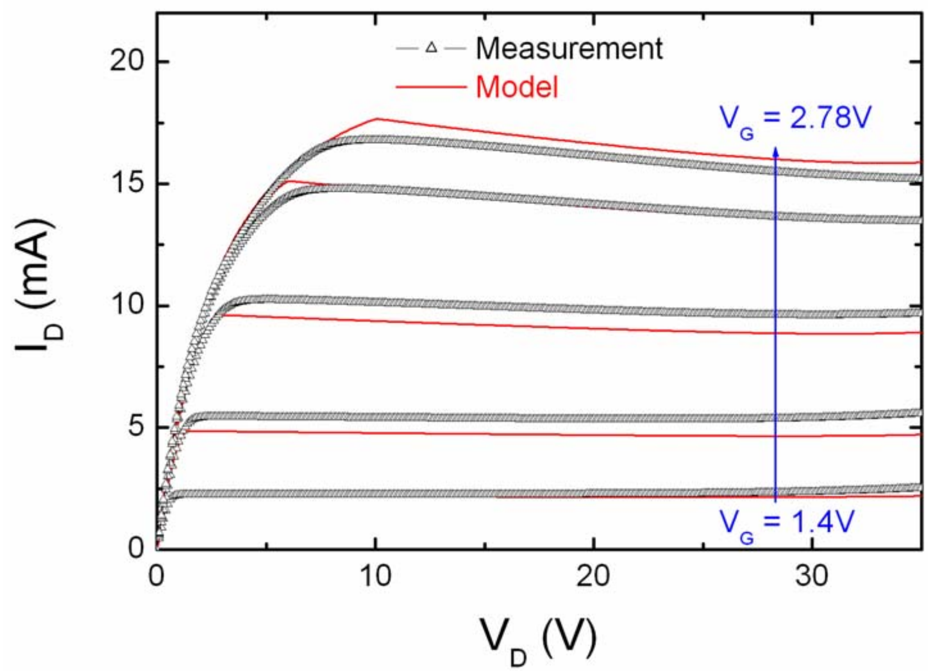
- Weak inversion to Strong inversion transition
- Subthreshold slope correctly matched
- Good accuracy

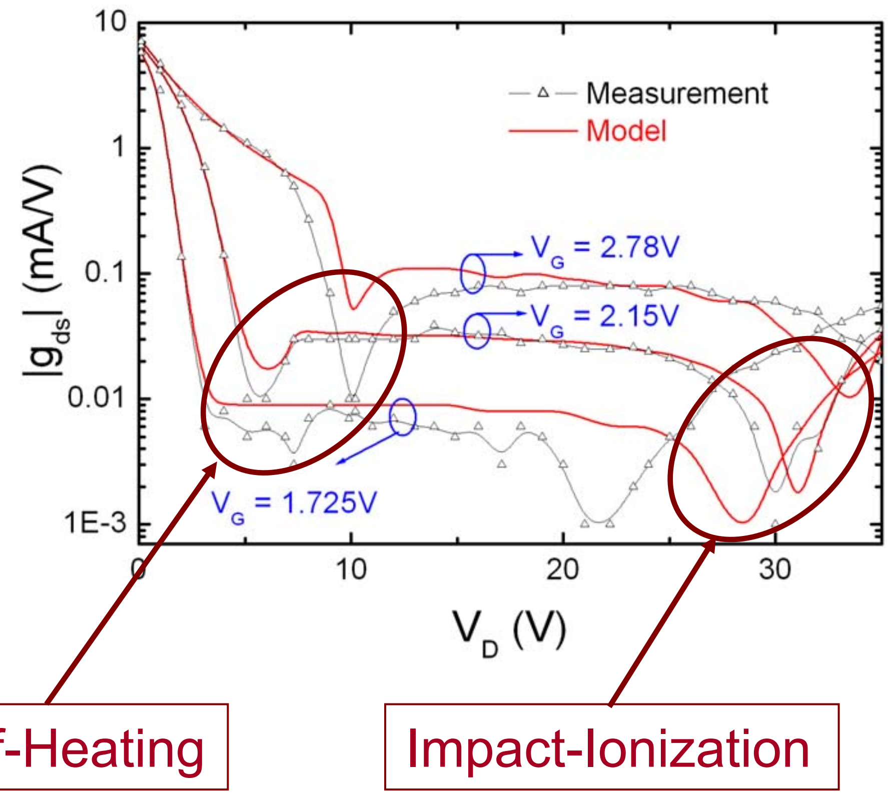
Transconductance for V_D=0.1-0.5V



- Subthreshold slope correctly matched
- Descending slope – drift resistance
- g_{max} – Mobility and drift resistance

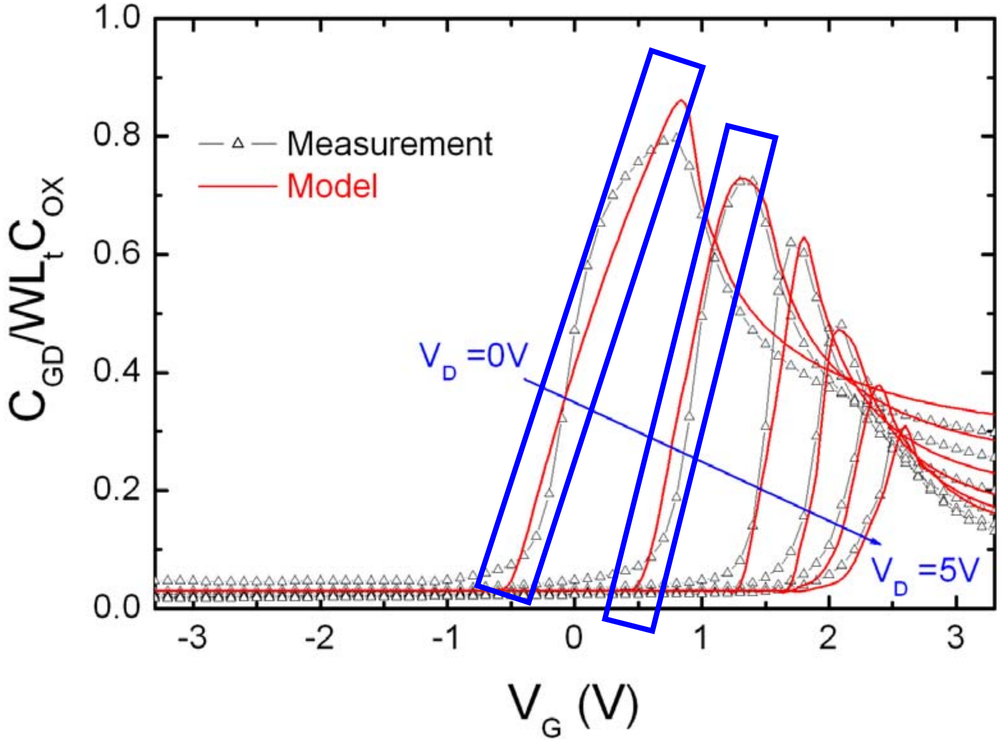
Output Characteristics

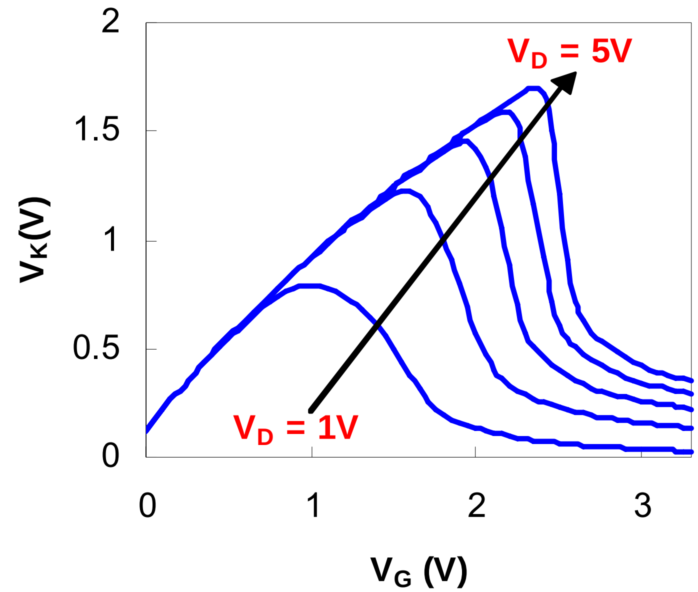




- Linear region correctly modeled by drift resistance
- Self Heating Effect
- Valleys on g_{ds} : Physical effects SHE, Impact Ionization

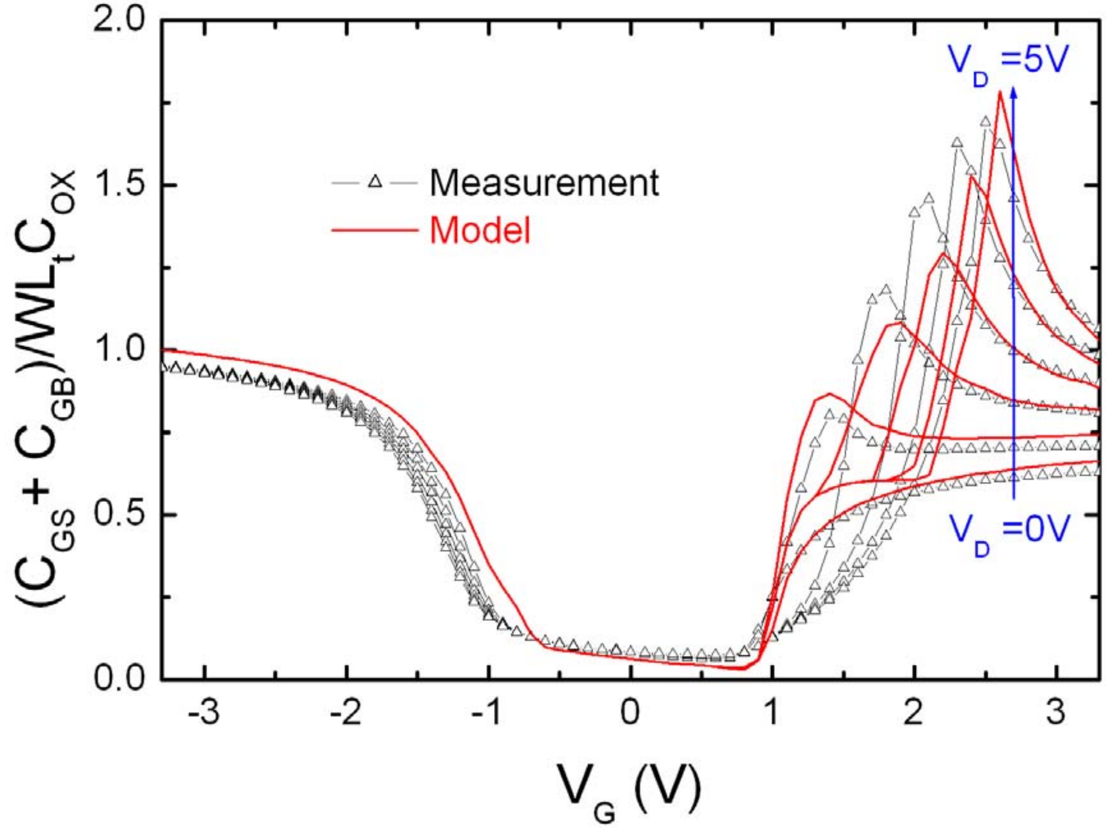
Gate-to-Drain Capacitance
C_{GD} vs V_G





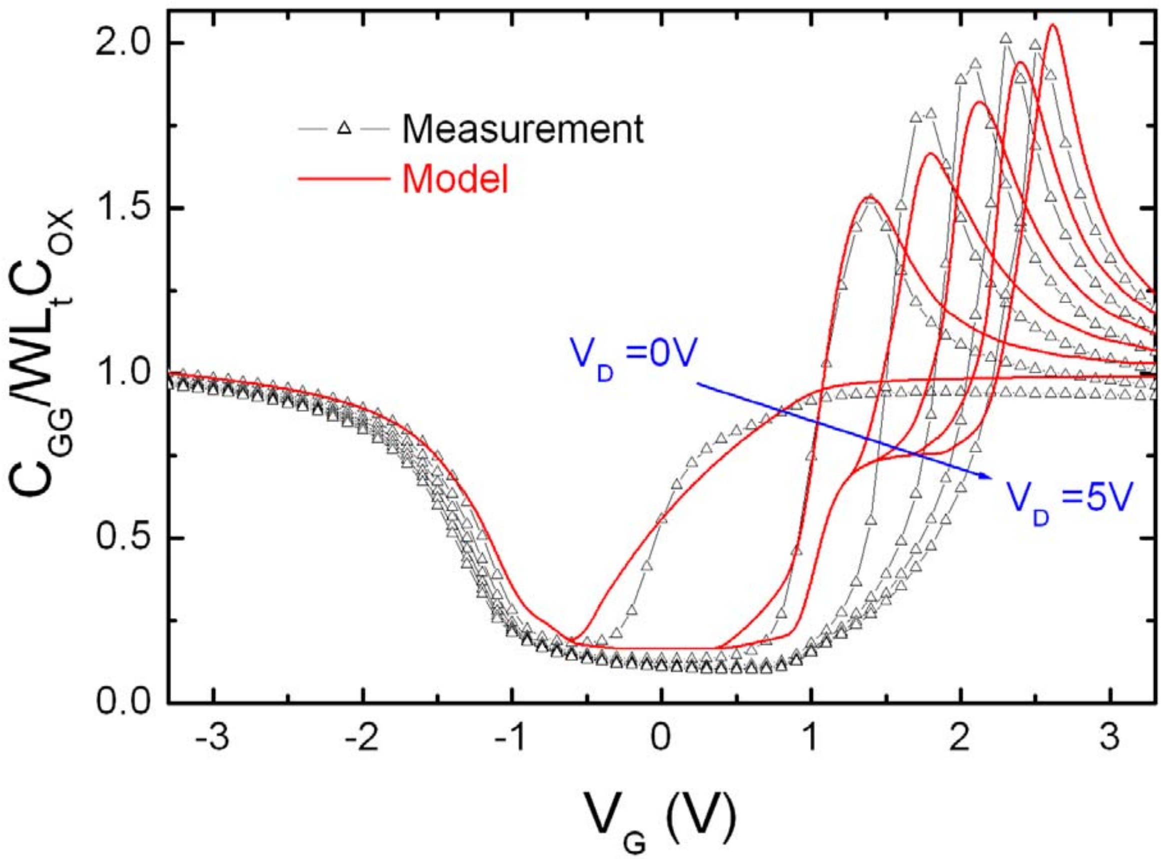
- Rising Slope & Peaks – effect of lateral non-uniform doping
- Sharp decrease – effect of drift region (good modeling of drift region or V_K must)

Gate-to-Source and Gate-to-Body Capacitances $C_{GS}+C_{GB}$ vs V_G



- Peaks – effect of lateral non-uniform doping
- Sharp decrease and shift of peaks – effect of drift region

Gate-to-Gate Capacitance
C_{GG} vs V_G



• Peaks and shift of peaks – little contribution from lateral non-uniform doping and greater contribution from drift region

Partioning Scheme in LAMOS

- Drain & Source charge: do NOT exist! (Philips IEDM'04)

- Solve continuity & transport eq. (Philips IEDM'04)
- New Partioning scheme for LAMOS (ESSDERC'06)

} C_{DG} & C_{SG}

- Capacitance implementation in simulators: Charge conservation problem!
- Use proposed partioning scheme or even WD to get Q_D & Q_S: Theoretically incorrect but still solves the problem at the moment for industry
- Some novel solution?

Conclusion

- **Modeling of lateral non-uniform doping in HV-MOSFET**
- Complex capacitance behavior of HV-MOS explained using numerical simulations : lateral doping and drift effects
- Peaks and shift of peaks in capacitances with bias correctly modeled : Major improvement over state of the art HV-MOS models
- Self-Heating and Impact-Ionization effect included
- Very good performance in DC and transient operations
- Model validated on advanced HV devices – 50 VDMOS and 40V LDMOS

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