# GaN HEMT Characterization and Modeling using ASM-HEMT

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- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
- Modeling Power Devices using ASM-HEMT
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

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# Nanolab:
# Characterization and Modeling Capabilities

- *About Nanolab*
- *Hardware Capabilities*
- *EDA Capabilities*

# About Nanolab: Some Stats

Funding

- Government Agencies
- Industry Partners
- Compact Model Coalition (CMC)

Publications

| | 2020 | 2019 | 2018 | 2017 | 2016 | 2015 |
|---|---|---|---|---|---|---|
| Books | | 1 | | | | 1 |
| Journal | 16 | 14 | 20 | 19 | 18 | 9 |
| Conference | 9 | 15 | 19 | 11 | 30 | 30 |

Current Members

- Postdoc – 5
- Ph.D. – 27
- Ten PhDs graduated

# About Nanolab: Collaborations

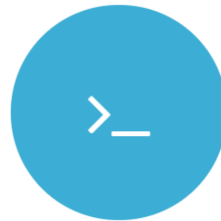
# About Nanolab: Areas of Research

### Atomistic Simulation

Strong compute and storage infrastructure for atomistic simulations - paving the way for first principle studies of materials. Research topics include materials like VO2, V2O5, black phosphoros, TMDs like MoS2, phosphorene, borophene among many others.

### DC and RF Device Characterization

State-of-the-art equipment for DC and RF characterization of packaged and on-wafer devices. High power measurement capabilities coupled with pulsed IV/RF and load pull systems allow for characterizations of higher level circuits like power amplifiers.



### SPICE/Compact Modeling

Strong collaboration with the industry in terms of model development. Working closely with UC Berkeley to maintain and develop the BSIM standard models. Out ASM-HEMT model for GaN-HEMTs was recently recognized as an industry standard by the Compact Model Coalition (CMC)

### RF Circuit Design

Hardware and software capabilities to design and implement prototypes for RF circuits. Power Amplifier and Low Noise Amplifier design using advanced device technologies.

# Hardware Capabilities I

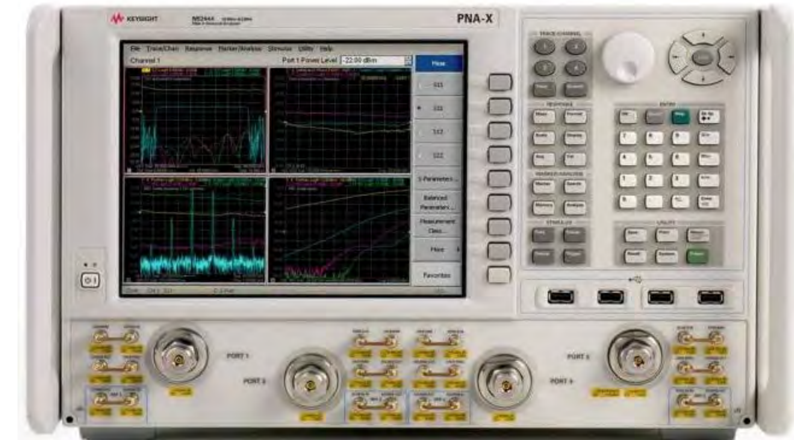
## Keysight Semiconductor Device Analyzer (B1500A) Measurement capabilities:

- IV, CV, pulse/dynamic IV range of 0.1 fA - 1 A / 0.5 µV - 200 V
- Evaluation of devices, materials, semiconductors, active/passive components
- AC capacitance measurement in multi frequency from 1 kHz to 5 MHz
- Pulsed IV measurement min 10 ns gate pulse width with 2 ns rise and fall times with 1 µs current measurement resolution

## Maury Microwaves/ AMCAD AM3221

- Bipolar ±25V/1A (gate) and high-voltage 250V/30A (drain) models
- Pulse widths down to 200ns
- Synchronized pulsed S-parameter measurements
- Connect systems in series for synchronizing 3+pulsed channels
- Long pulses into the tens and hundreds of seconds for trapping and thermal characterization

# Hardware Capabilities II




### Keysight ENA (E5071C) 100KHz to 8.5 GHz

- 9 kHz to 4.5/ 6.5/ 8.5/ 14/ 20 GHz
- 2- or 4-port, 50-ohm, S-parameter test set
- Improve accuracy, yield and margins with wide dynamic range 130 dB, fast measurement speed 8ms and excellent temperature stability 0.005 dB/ °C

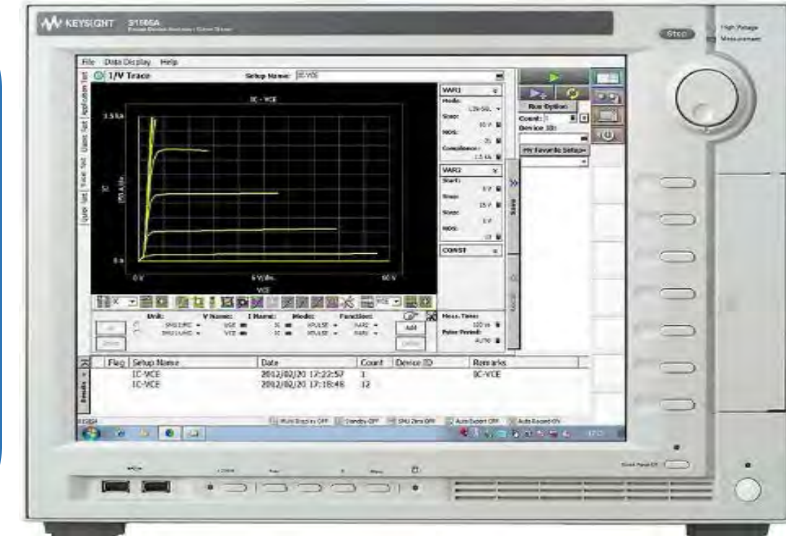
### Keysight PNA-X (N5244A) 10 MHz to 43.5 GHz

- High Frequency Device Characterization (Microwave Network Analyzer)
- 100Khz to 8.5 GHz and 10 MHz to 43.5 GHz
- 2-port and 4-ports with two built-in sources
- High output power (+16 dBm)
- Best dynamic accuracy: 0.1 dB compression with +15 dBm input power at the receiver
- Low noise floor of -111 dBm at 10 Hz IF bandwidth

# Hardware Capabilities III

## Keysight Power Device Characterization System: B1505

- Power device characterization up to 1500 A & 10 kV
- Medium current measurement with high voltage bias (e.g. 500 mA at 1200 V)
- μΩ on-resistance measurement capability
- Accurate, sub-picoamp level, current measurement at high voltage bias
- Fully automated Capacitance measurement at up to 3000 V of DC bias
- High power pulsed measurements down to 10 μs
- High voltage/ high current fast switch option to characterize GaN current collapse effect
- Fully automated thermal testing from -50 ℃ to +250 ℃



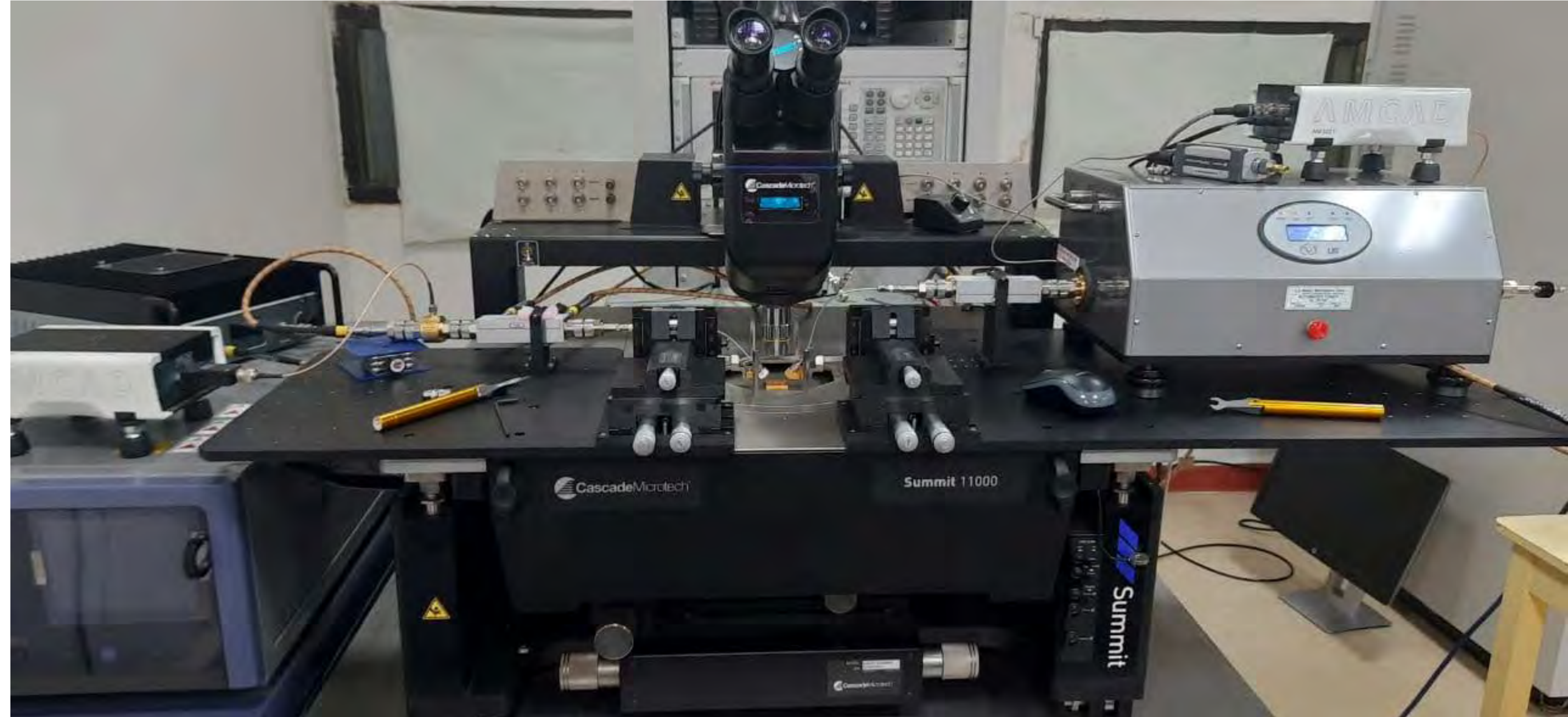
## Keysight N8975B Noise Figure Analyzer

- Frequency range 10 MHz to 26.5 GHz in a one-box solution
- Includes Spectrum Analyzer and IQ Analyzer (Basic) modes
- SNS series noise source N4002A
- U7227C 100 MHz to 26.5 GHz External USB Preamplifier included

# Load Pull Characterization

Maury Load Pull Characterization system

- A fundamental passive load pull system capable of performing load pull characterization up to 15W.
- XT982GL01 – 0.6 to 18 GHz Load tuner
- Plan to expand to a 3 harmonic hybrid load pull system soon.



# EDA Capabilities

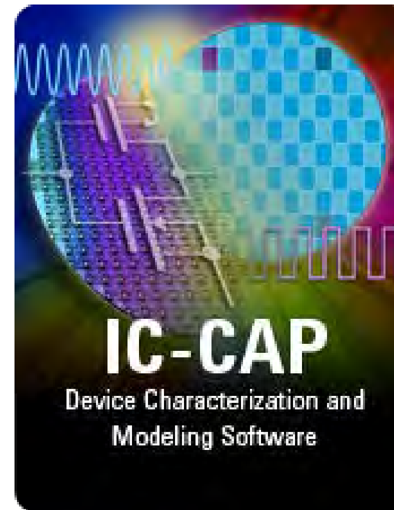
SPICE SIMULATORS

Advanced Design System

Advanced Design System

RF

TCAD




Atomistic Simulations

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# An introduction to ASM-HEMT

- *About ASM-HEMT and its core*
- *Extraction flow*
- *Other models incorporated into the core*
- *Geometric Scaling*

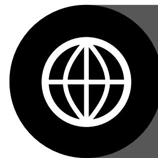
# A brief history of HEMT models

| FET Models | Approx. Number of Parameters | Electrothermal (Rth-Cth) Model | Geometry Scalability Built-In | Original Device Context |
|---|---|---|---|---|
| Curtice3 [12] | 59 | No | No | GaAs MESFET |
| Motorola Electrothermal (MET) [25] | 62 | Yes | Yes | LD MOSFET |
| CMC (Curtice/ Modelithics/Cree) [26] | 55 | Yes | Yes | LD MOSFET |
| BSIMSOI3 [24] | 191 | Yes | Yes | SOI MOSFET |
| CFET [5] | 48 | Yes | Yes | HEMT |
| EEHEMT [13] | 71 | No | Yes | HEMT |
| Angelov [14] | 80 | Yes | No | HEMT/MESFET |
| Angelov GaN [11] | 90 | Yes | No | HEMT |
| Auriga [4] | 100 | Yes | Yes | HEMT |

# Various classes of compact models

Compact Models (GaN HEMT)
- Table Based
- Empirical
- Physics Based
  - Threshold Voltage Based
  - Surface Potential Based (ASM-HEMT)
  - Charge Based (MVSG)

**Advanced SPICE Model for GaN HEMTs (ASM-HEMT)**



www.iitk.ac.in/asm

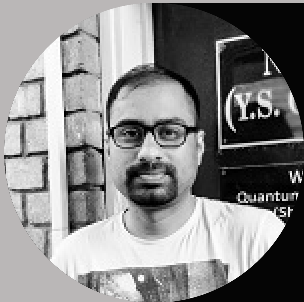
# ASM-HEMT Team

Directors

Prof. Yogesh Singh Chauhan

Prof. Sourabh Khandelwal

Developers




Dr. Sudip Ghosh

Dr. Aamir Ahsan

Dr. Avirup Dasgupta

Ahtisham Pampori

Raghvendra Dangi

# ASM-HEMT: Summary

**Electrostatics**

Analytical Solution of Schrodiger's & Poisson's

2-DEG Charge, Ef, Surface Potential

**Transport**

SP-Based Current & Charge Model

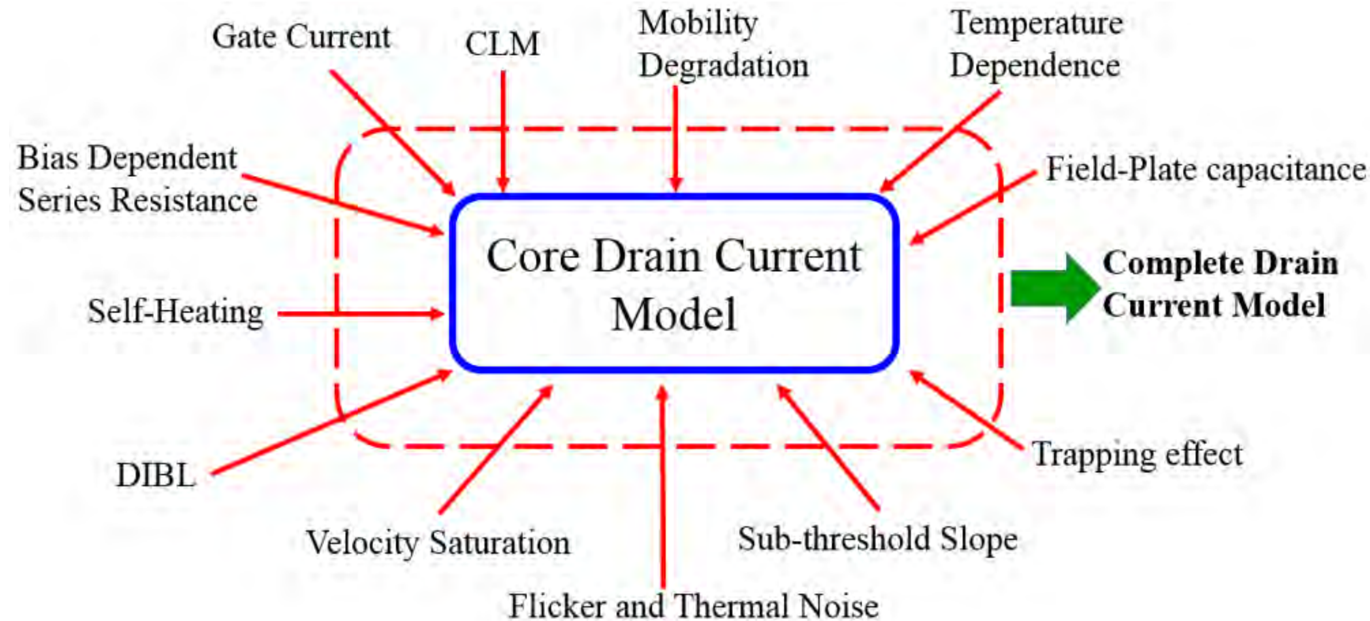
I-V, C-V, DIBL, Rd, Rs, Vel. Sat., ...

**Higher-order Effects**

Noise, Trapping, Self-Heating, Field Plate

DC, AC, Transient Harmonic Sim., Noise, ...

# ASM-HEMT: Core Model




Real Device Effects Incorporated into the Model

## Core Model Parameters

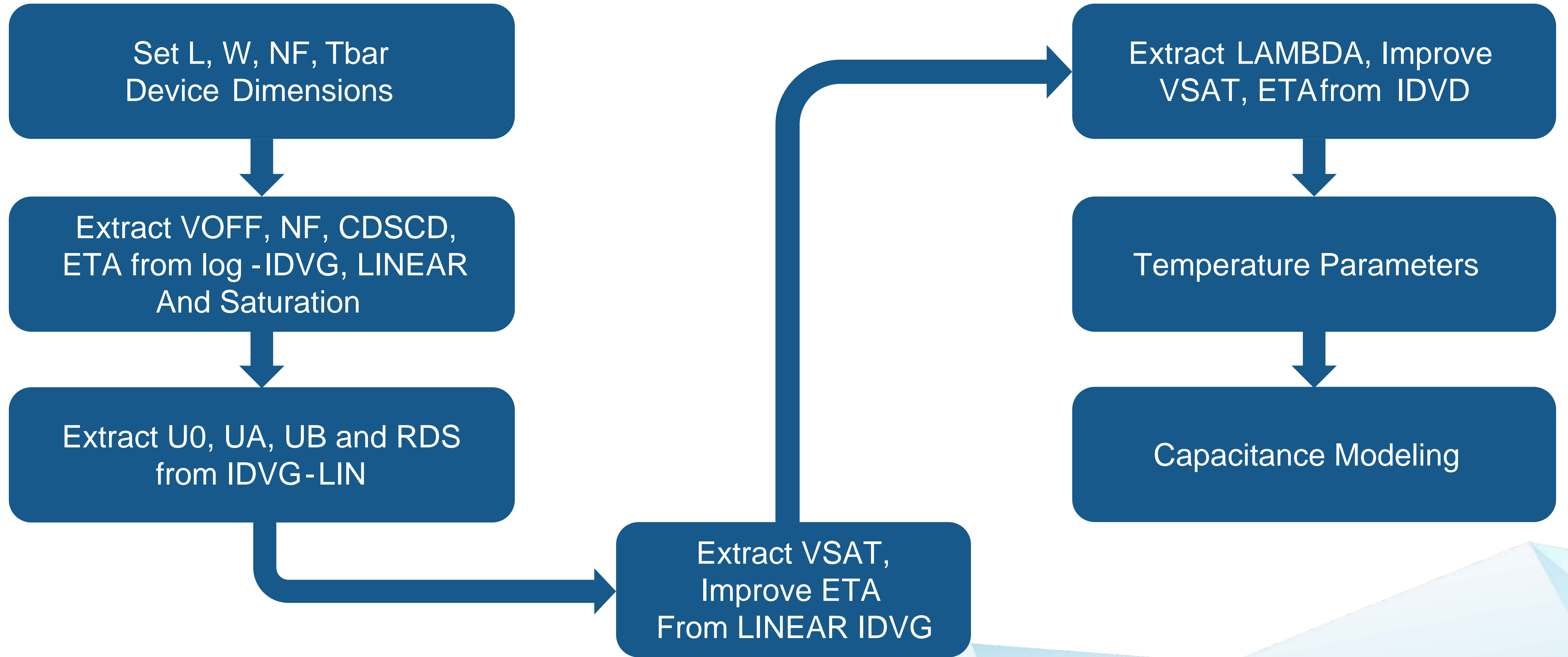
| Parameter | Description | Extracted Value |
| --- | --- | --- |
| $V_{OFF}$ | Cutoff Voltage | $-2.86\ V$ |
| $N_{FACTOR}$ | Subthreshold Slope Factor | 0.202 |
| $C_{DSCD}$ | SS Degradation Factor | $0.325\ V^{-1}$ |
| $\eta_0$ | DIBL Parameter | 0.117 |
| $U_0$ | Low Field Mobility | $33.29\ mm^2/Vs$ |
| $N_{S0ACCS}$ | AR 2DEG Density | $1.9e+17\ /m^2$ |
| $V_{SATACCS}$ | AR saturation velocity | $157.6e+3\ cm/s$ |
| $R_{TH0}$ | Thermal Resistance | $22\ \Omega$ |

## Core drain current expression

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}}\frac{W}{L}C_g N_f\left[V_{go} - \left(\frac{\psi_s+\psi_d}{2}\right) + V_{th}\right] \times \psi_{ds}$$

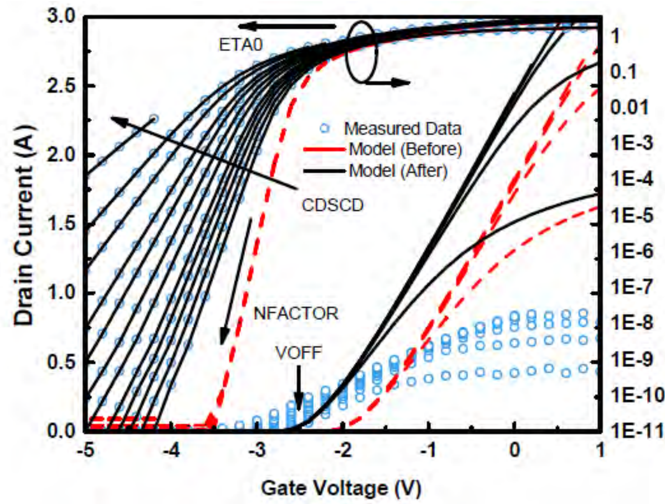
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# Extraction Flow I

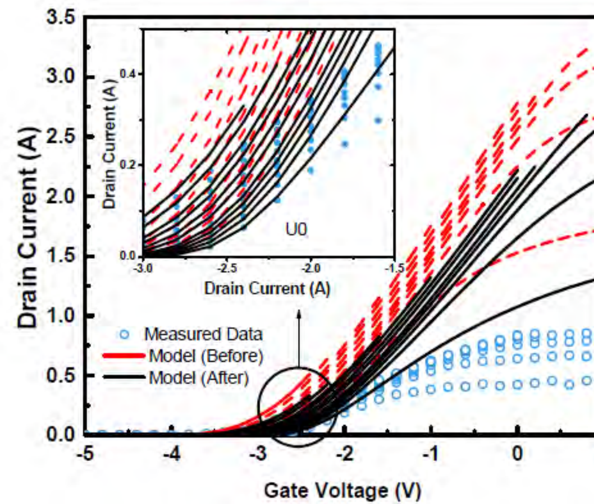



[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

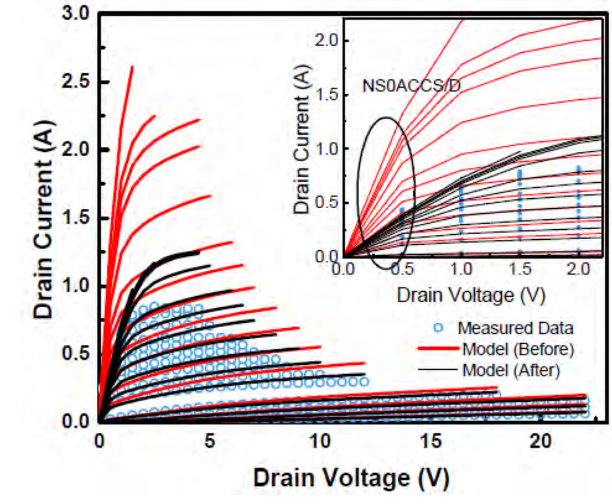
# Extraction Flow II



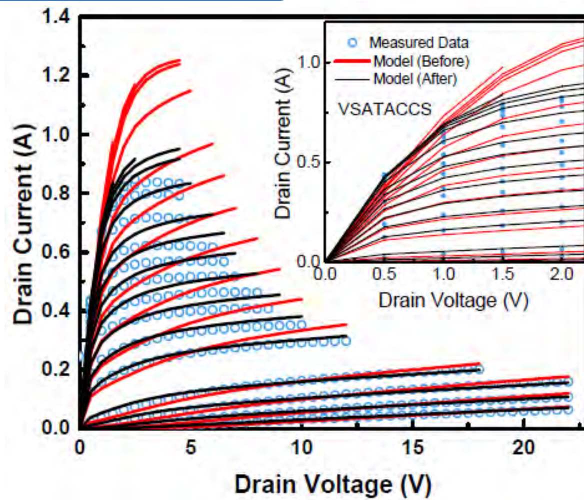

$I_d - V_g$ (Extract $V_{OFF}$, $N_{FACTOR}, C_{DSCD}$)



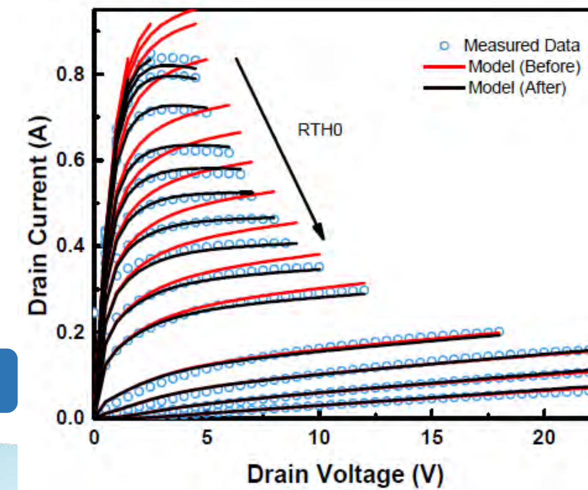

$I_d - V_g$ (Extract $U_0$)




$I_d - V_d$ (Extract $N_{S0ACCS}$)



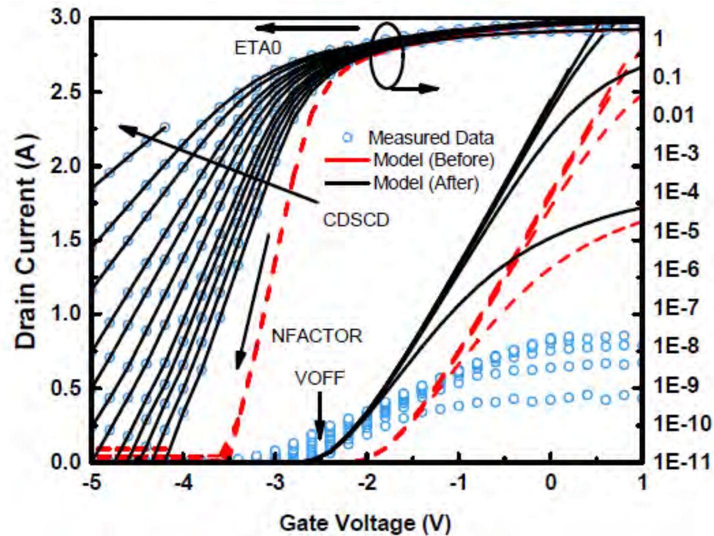

$I_d - V_d$ (Extract $V_{SATACCS}$)

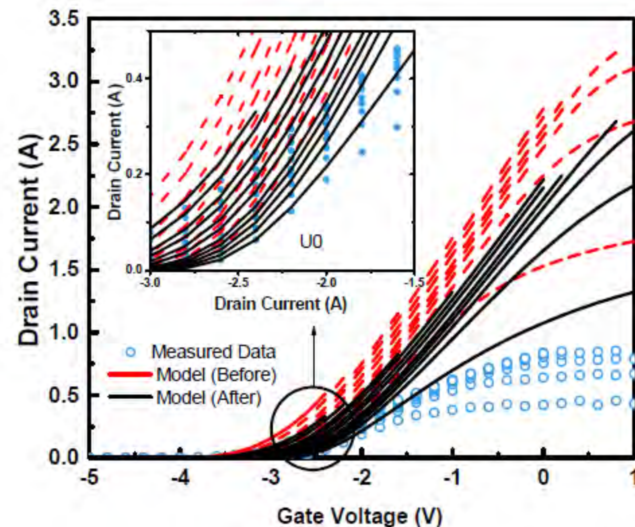



$I_d - V_d$ (Extract $R_{TH0}$)

[1]S. A. Ahsan *et al.*, *MOS-AK Workshop*, Shanghai, [2016]

# Extraction from Id - Vg curves




Start with $I_d - V_g$ characteristics in the log scale

$\boldsymbol{ETA0}$ – DIBL Parameter

$\boldsymbol{NFACTOR}$ – Sub-threshold slope parameter

$\boldsymbol{CDSCD}$ – Captures the drain voltage dependence on the sub-threshold slope.

$\boldsymbol{VOFF}$ – Cut-Off Voltage

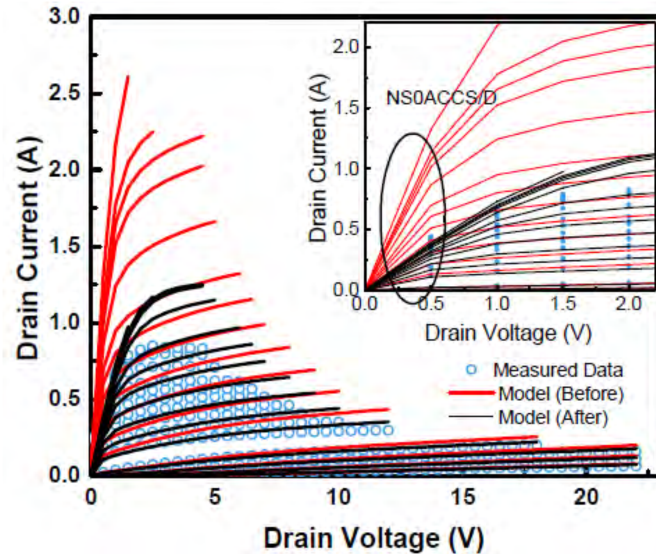
$I_d - V_g$ characteristics in the linear scale

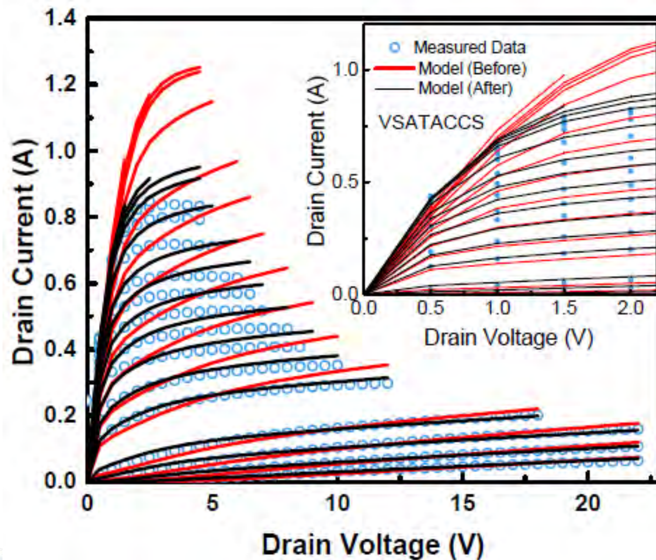
$\boldsymbol{U0}$ – Low field mobility

$\boldsymbol{UA, UB}$ – Mobility degradation parameters


[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# Extraction from Id - Vd curves




## $I_d - V_d$ characteristics

$\boldsymbol{VSAT}$ – Velocity saturation parameter

$\boldsymbol{UA},\ \boldsymbol{UB}$ – Mobility degradation parameters

Access Region Parameters extracted from $I_d - V_d$ characteristics:

$\boldsymbol{NS0ACCS(D)}$ – 2DEG density in the access region.

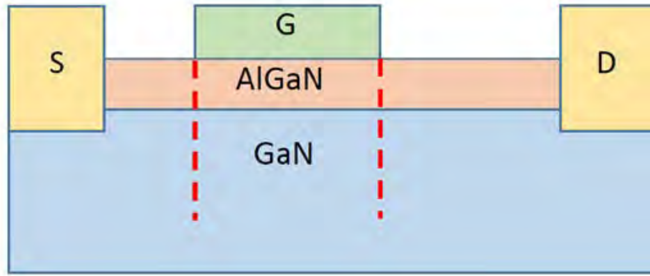
$\boldsymbol{VSATACCS}$ – Saturation velocity in the access region.

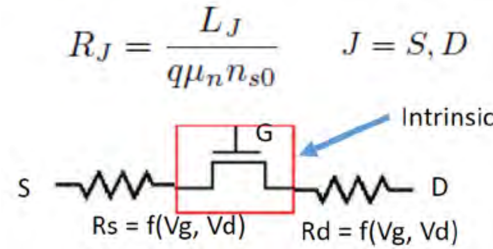
$\boldsymbol{U0ACCS(D)}$ – Low field mobility in the access region.

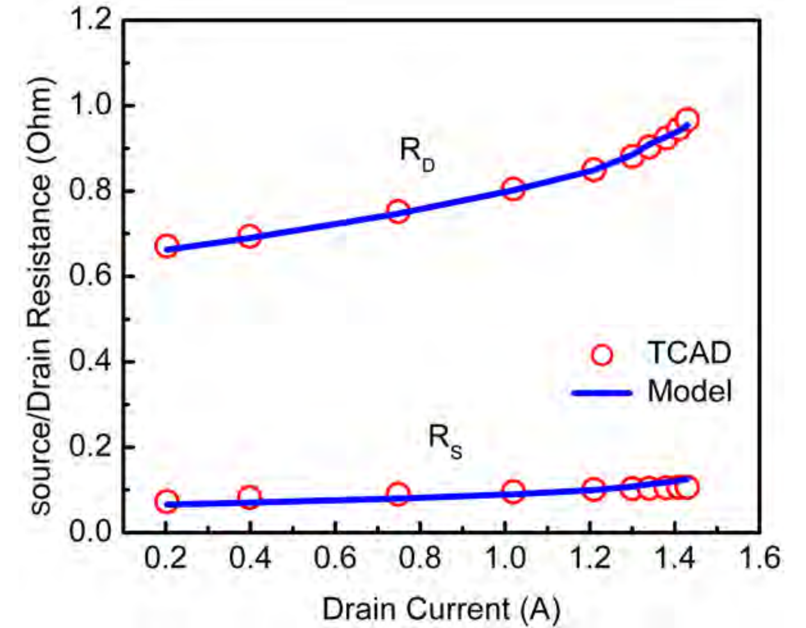
$\boldsymbol{U0ACCS(D)}$ independently tunes the access region resistance around Vds = 0 and helps extract $g_{ds}$ at that point.


[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# Bias-dependent access region resistance model: Overview




$$I_{acc} = Q_{acc} \cdot v_s = Q_{acc} \cdot v_{sat} \cdot \frac{V_R/V_{Rsat}}{\left[1 + \left(\frac{V_R}{V_{Rsat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

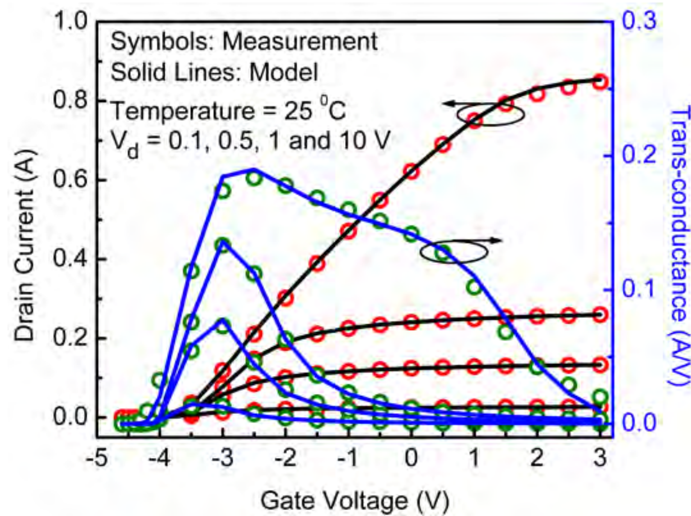
$$R_{d/s} = \frac{V_R}{I_{acc}} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_d}{I_{acc,sat}}\right)^{\gamma}\right]^{\frac{1}{\gamma}}}$$

$$\mathrm{I_{ds,acc}} = \frac{\mathrm{R_c}}{\mathrm{W{\cdot}N_f}} + \frac{\mathrm{L_{acc}}}{\mathrm{W{\cdot}N_f{\cdot}q{\cdot}N_{S0ACCS}{\cdot}U_{0ACCS}}} \times \left(1 - \left(\frac{\mathrm{I_{ds}}}{\mathrm{W{\cdot}N_f{\cdot}N_{S0ACCS}{\cdot}V_{SATACCS}}}\right)^2\right)^{-1/2}$$

Nonlinear variation of source/ drain access resistances with Ids extracted from TCAD simulation and comparison with model.

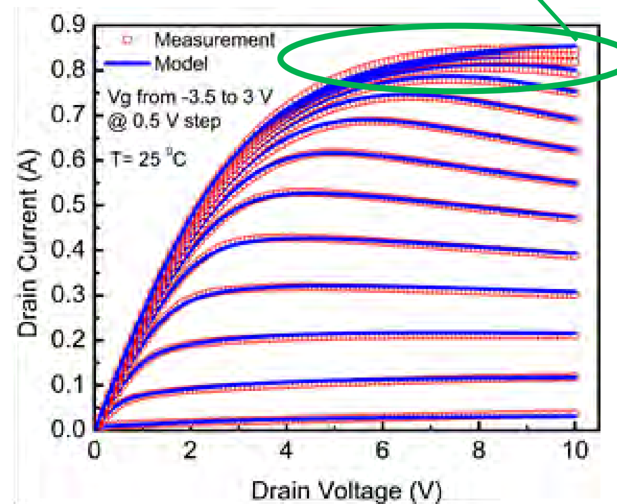

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

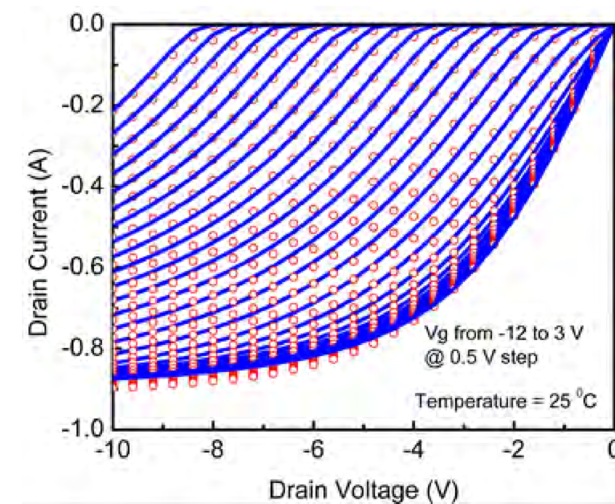
# Bias-dependent access region resistance model: Results




Id - Vg and trans-conductance for the Toshiba power HEMT. Different slopes above Voff in gm-Vg: self-heating governs the first slope while velocity saturation in access region affects second slope.

Effect of high access region resistance at high $V_g$




Ids-Vds and reverse Ids-Vds fitting with experimental data. The non-linear Rs/d model shows correct behavior for the higher Vg curves in the Id-Vd plot; the S-P based model can accurately capture the reverse output characteristics.

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

# Bias-dependent access region resistance model: Temperature scaling

The temperature dependence of $R_{d/s}$ model is extremely important as it increases significantly with increasing temperature

Temperature dependence of 2-DEG charge density in the drain or source side access region:

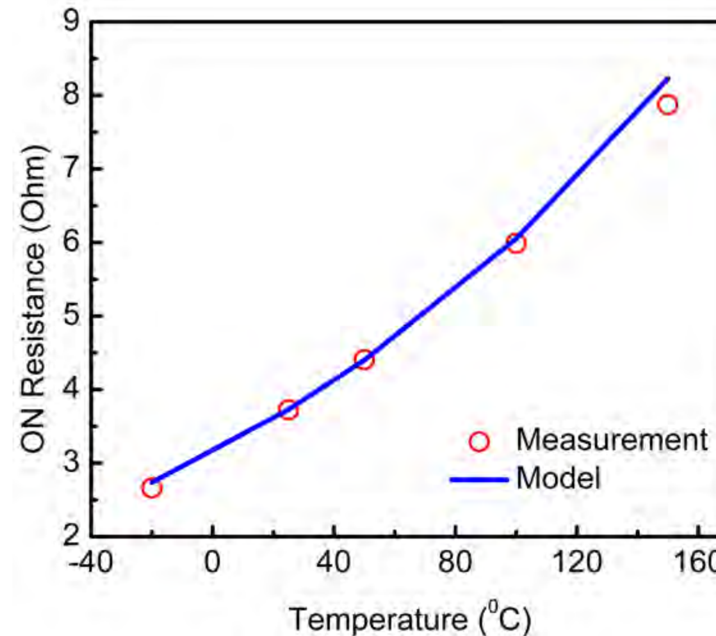
$$n_{s0}(T) = NS0ACC \cdot \left(1 - KNS0 \cdot \left(\frac{T}{TNOM} - 1\right)\right)$$

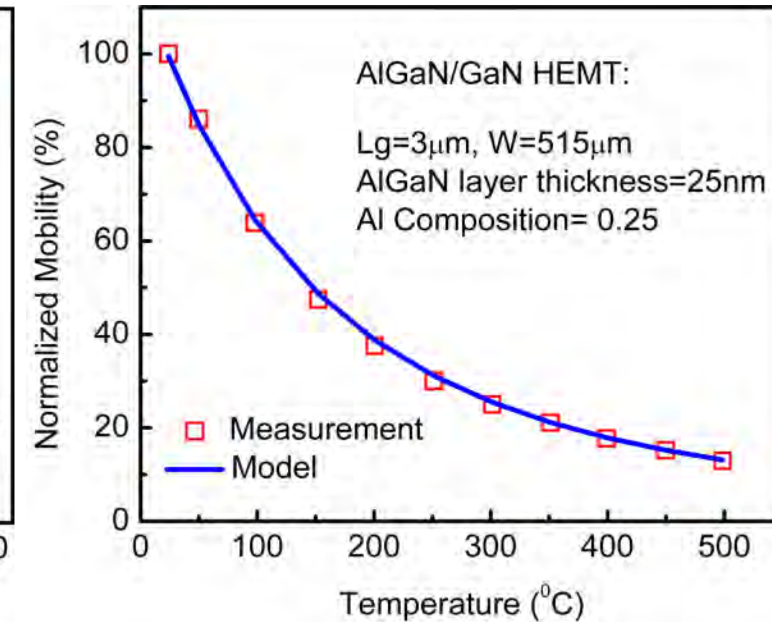
Temperature dependence of Saturation Velocity:

$$V_{sat}(T) = VSATACCS \cdot [1 + ATS(T - TNOM)]$$

Temperature dependence of electron Mobility:

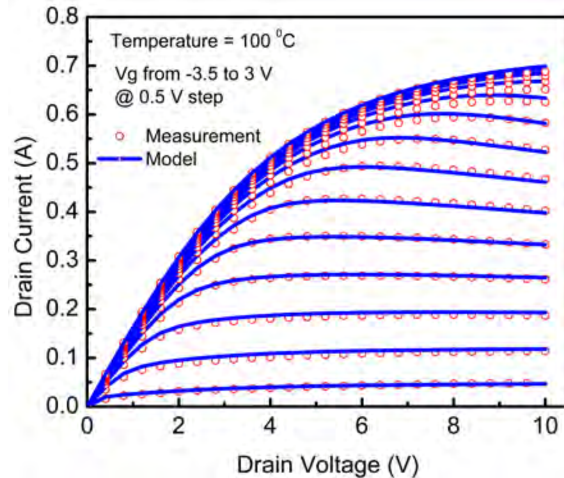
$$\mu_{acc}(T) = U0ACC \cdot \left(\frac{T}{TNOM}\right)^{UTEACC}$$



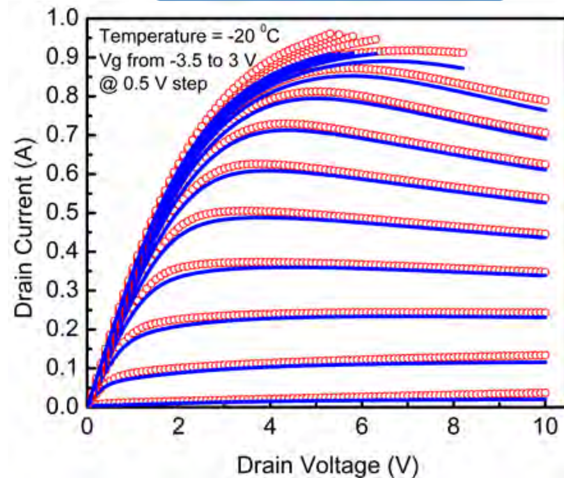




[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

# ASM-HEMT: Temperature scaling results




Id - Vd at 100℃



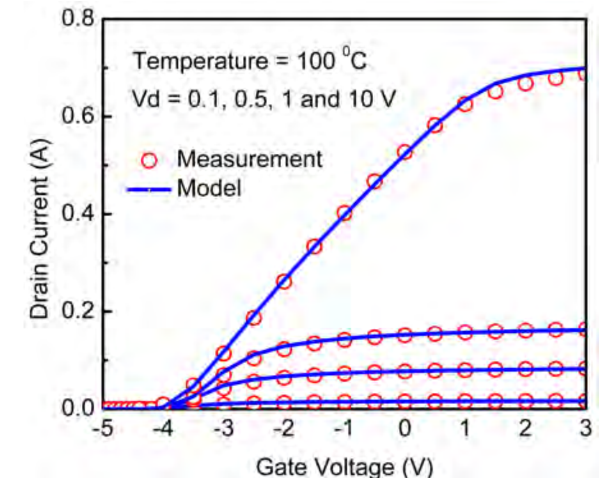

Id - Vd at -20℃

ASM-HEMT features a robust temperature scaling model which has been validated across a broad range of device temperatures.

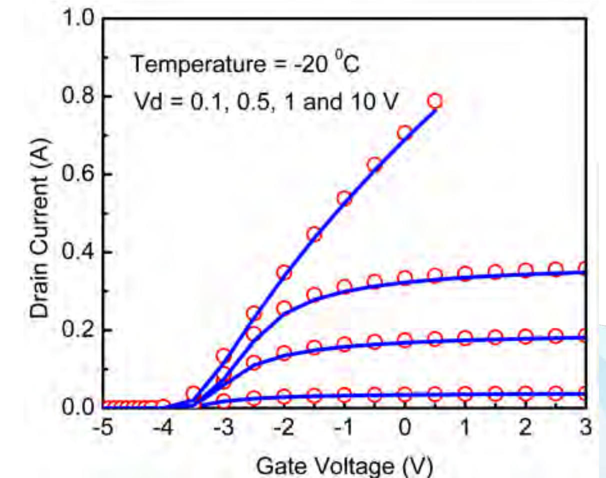
$$V_{off,DIBL}(T) = V_{off,DIBL} - \left(\frac{T_{dev}}{T_{NOM}} - 1\right) \cdot \boldsymbol{KT1} + TRAPVOFF \cdot vcap + voff_{trap}$$

$$U0(T) = U0 \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{UTE}}$$

$$VSAT(T) = VSAT \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{\boldsymbol{AT}}$$




Id - Vg at 100℃




Id - Vg at -20℃

[1] S. Ghosh et al., IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), [2016]

# Geometric Scaling I

## Charge Scaling

$$Q_g = \frac{C_g LW}{V_{g0} - \psi_m + V_{tv}}[V_{g0}^2 + \frac{1}{3}(\psi_d^2 + \psi_s^2 + \psi_d\psi_s) - V_{g0}(\psi_d + \psi_s - V_{tv}) - V_{tv}\psi_m]$$

$$\begin{aligned} Q_d = -\frac{C_g LW}{120(V_{g0} - \psi_m + V_{tv})^2}&[12\psi_d^3 + 8\psi_s^3 + \psi_s^2(16\psi_d - 5(V_{tv} + 8V_{g0})) \\ &+2\psi_s(12\psi_d^2 - 5\psi_d(5V_{tv} + 8V_{g0}) + 10(V_{tv} + V_{g0})(V_{tv} + 4V_{g0})) \\ &+15\psi_d^2(3V_{tv} + 4V_{g0}) - 60V_{g0}(V_{tv} + V_{g0})^2 \\ &+20\psi_d(V_{tv} + V_{g0})(2V_{tv} + 5V_{g0})] \end{aligned}$$

## Current Scaling

$$I_d = \frac{W}{L}\mu C_g(V_g0 - \psi_m + V_{th})\psi_{ds}$$

Where $\psi_m = (\psi_d + \psi_s)/2,\ \psi_d s = (\psi_d - \psi_s)$

## Access Region Resistance Scaling

$$\begin{aligned} R_{source} = &\frac{RSC(T)}{W \cdot NF} + TRAPRS \cdot vcap \\ &+ \frac{LSG}{W \cdot NF \cdot q \cdot NS0ACCS(T) \cdot U0ACCS(T)} \\ &\cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCS}\right)^{\frac{-1}{MEXPACCS}} \end{aligned}$$

where

$$I_{sat,source} = W \cdot NF \cdot NS0ACCS(T) \cdot VSATACCS(T)$$

$$\begin{aligned} R_{drain} = &\frac{RDC(T)}{W \cdot NF} + TRAPRD \cdot vcap + R_{trap}(T) + ron_{trap} \\ &+ \frac{LDG}{W \cdot NF \cdot q \cdot NS0ACCD(T) \cdot U0ACCD(T)} \\ &\cdot \left(1 - \left(\frac{I_{ds}}{I_{sat,source}}\right)^{MEXPACCD}\right)^{\frac{-1}{MEXPACCD}} \end{aligned}$$

where $I_{sat,drain} = W \cdot NF \cdot NS0ACCD(T) \cdot VSATACCS(T)$

# Geometric Scaling II

## Thermal Noise and Flicker Noise Scaling

$$S_{if}(f) = \frac{k_B T}{W L^2 f^{EF}} \frac{I_{DS}^2 K_r}{C_g^2} \Big[ NOIAV_{th}C_g \left( \frac{1}{Q_{ch,d}} - \frac{1}{Q_{ch,s}} \right) + (NOIA + NOIBV_{th}C_g) ln \left( \frac{Q_{ch,d}}{Q_{ch,s}} \right) + (NOIB + NOICV_{th}C_g)(-Q_{ch,d} + Q_{ch,s}) + \frac{NOIC}{2}(Q_{ch,d}^2 - Q_{ch,s}^2) \Big]$$

$$S_{it} = \frac{4k_B T_{dev}}{I_D L_{eff}^2} (\mu_{eff,sat} W q C_g)^2 \left( V_{go}^2 \psi_{ds} + \frac{\psi_d^3 - \psi_s^3}{3} - V_{go} \left( \psi_d^2 - \psi_s^2 \right) \right)$$

## Gate Current Scaling

$$I_{gs} = W \cdot L \cdot NF \cdot \left[ IGSDIO + \left( \frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGS \right] \left[ exp \left\{ \frac{V_{gs}}{NJGS \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

$$I_{gd} = W \cdot L \cdot NF \cdot \left[ IGDDIO + \left( \frac{T_{dev}}{TNOM} - 1 \right) \cdot KTGD \right] \left[ exp \left\{ \frac{V_{gd}}{NJGD \cdot K_B \cdot T_{dev}} \right\} - 1 \right]$$

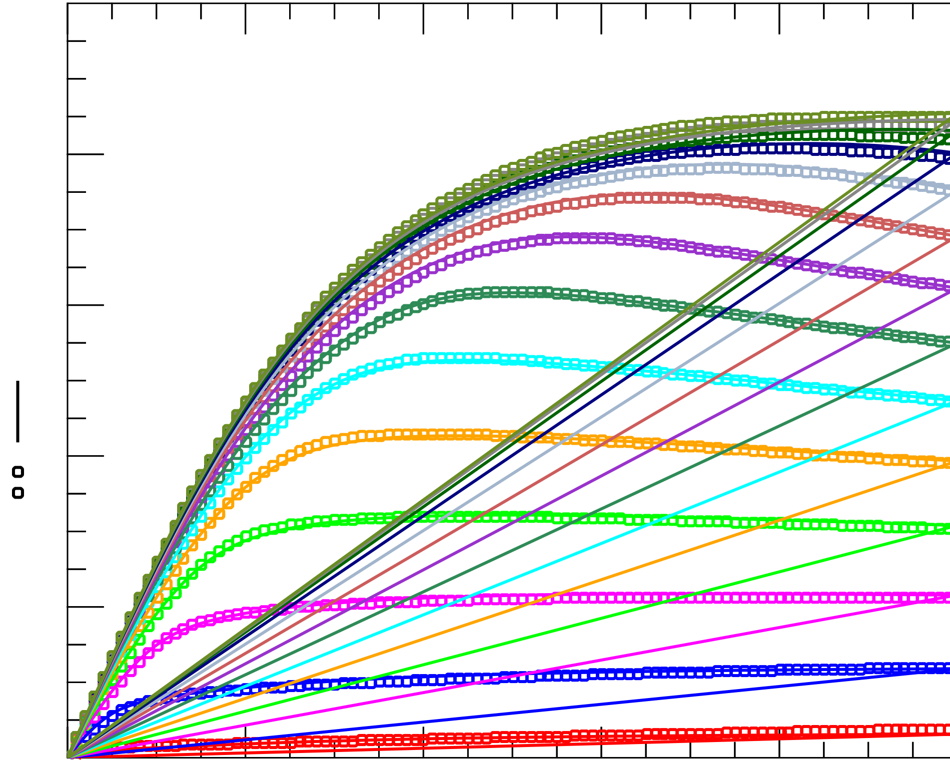
# Contents

- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
- Modeling Power Devices using ASM-HEMT
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

# Modeling Power Devices using ASM - HEMT

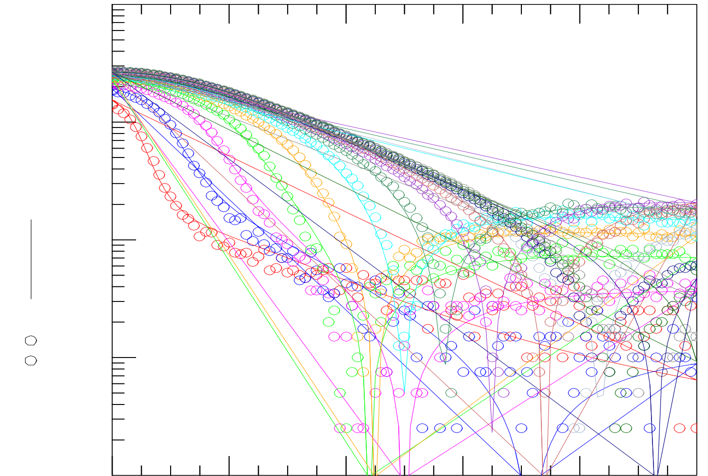
– *Modeling DC*
– *Modeling field plates*
– *Model comparison with a mixed mode device*

# Modeling DC: Room Temperature Output Characteristics



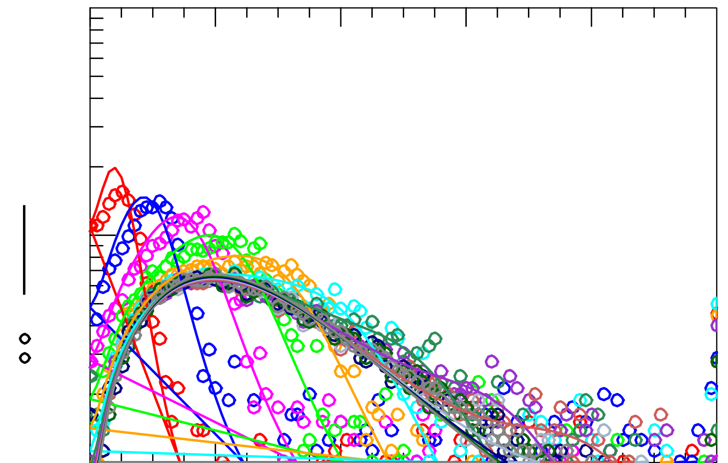
Output Characteristics at T=25 ℃

Output conductance versus Vd

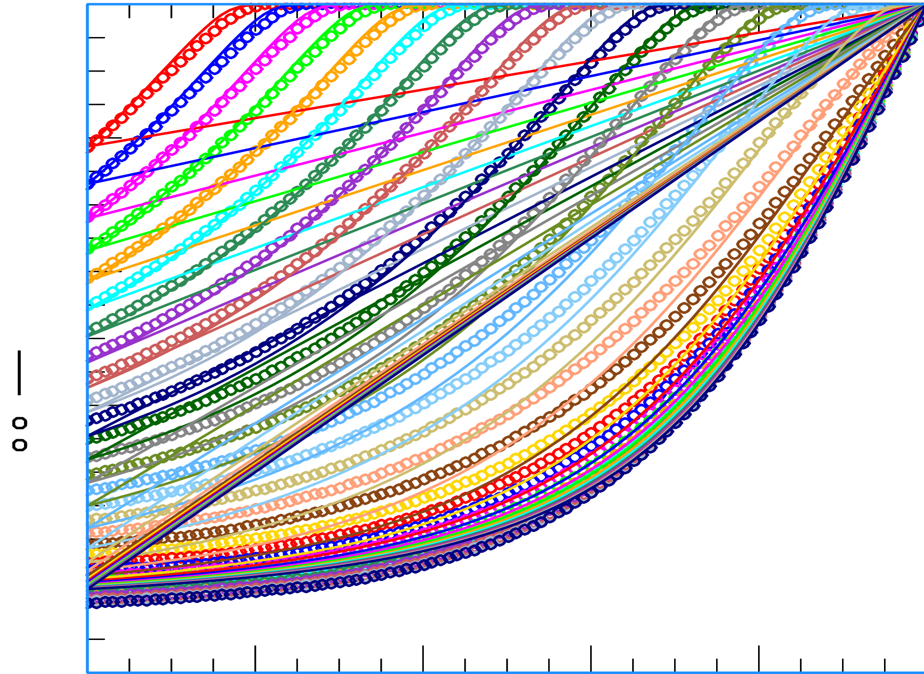


*ASM-HEMT accurately captures the IV characteristics of a power GaN HEMT device.*

Derivative of output conductance versus Vd

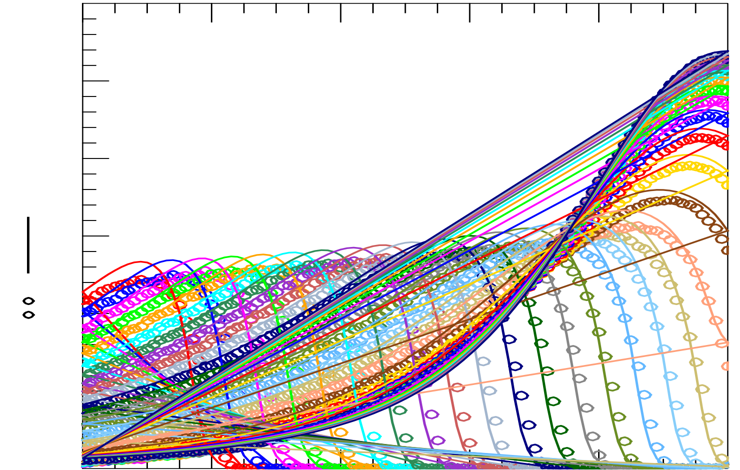


# Modeling DC: Room Temperature Reverse Output Characteristics

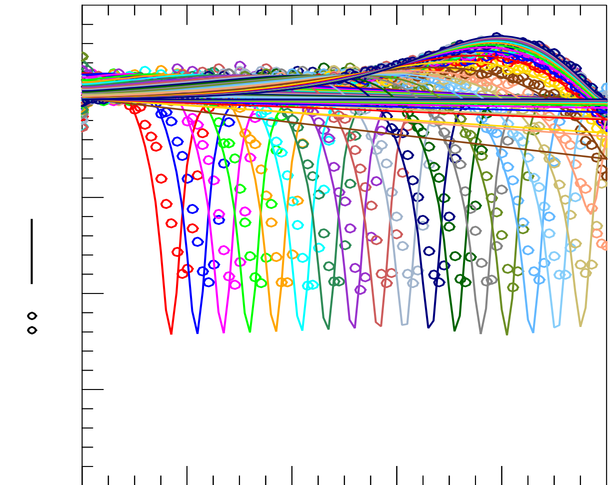


Reverse Output Characteristics at T=25°C

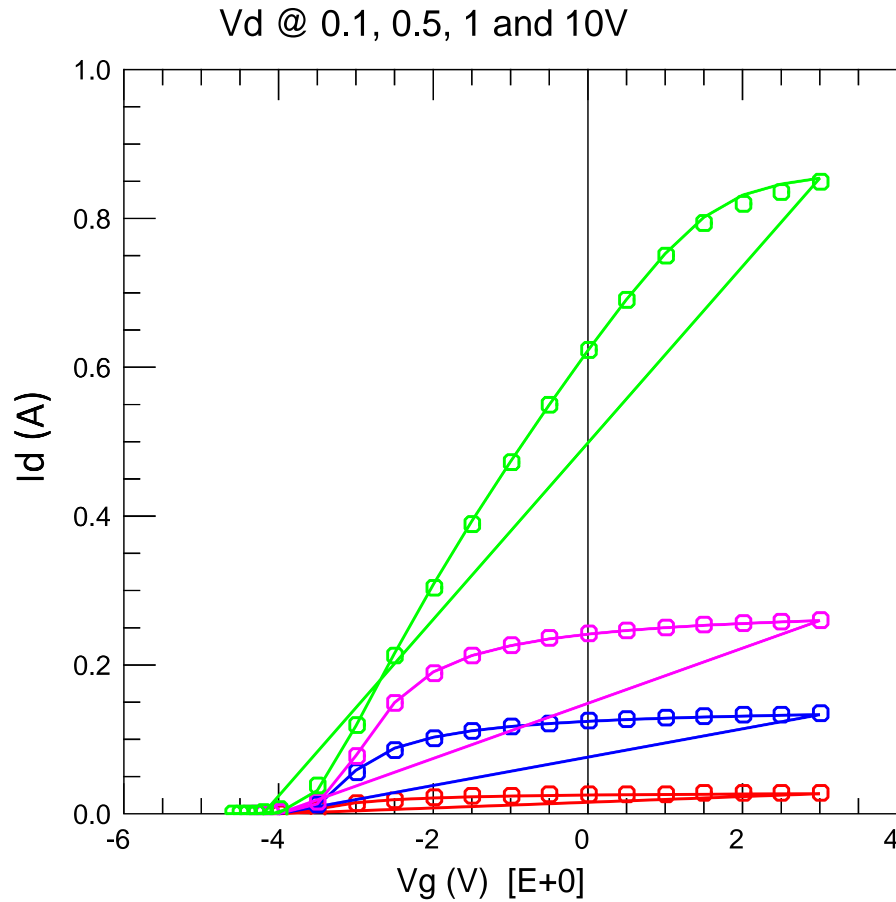
Reverse Output conductance versus Vd



Derivative of reverse output conductance versus Vd

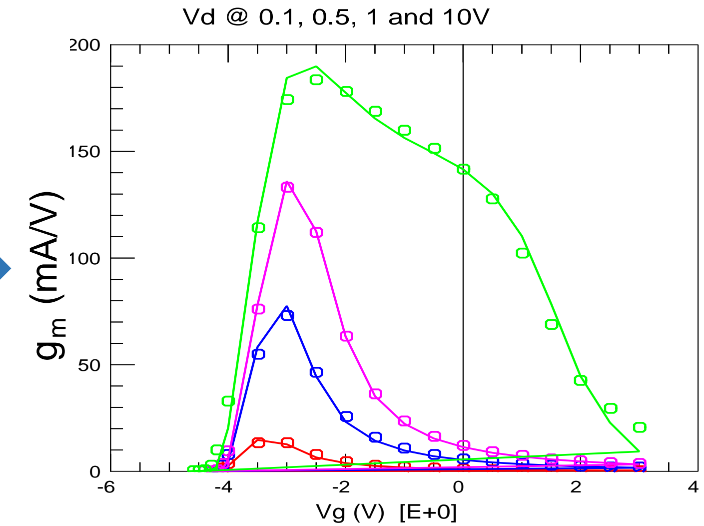


# Modeling DC: Room Temperature Transfer Characteristics

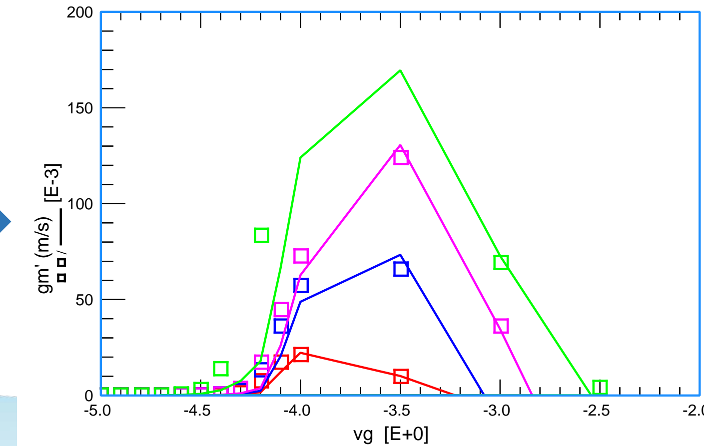



Transfer Characteristics at T=25℃

Transconductance versus Vg

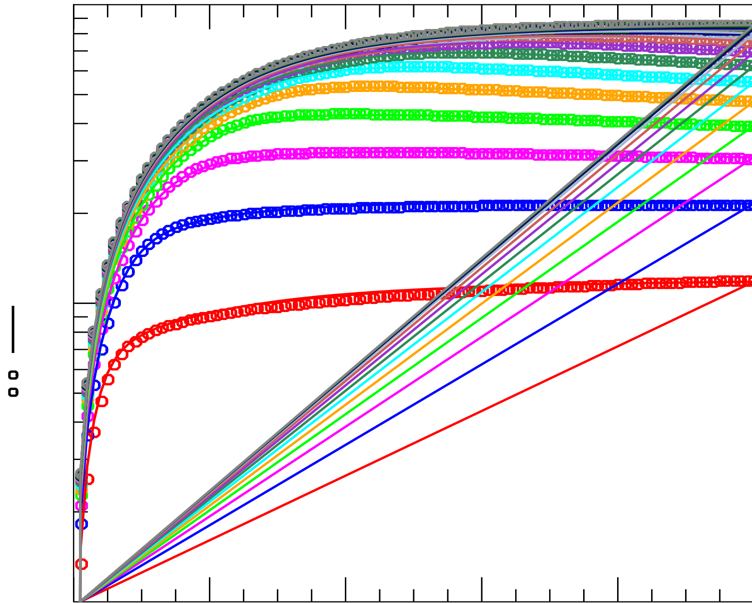



Derivative of transconductance versus Vg

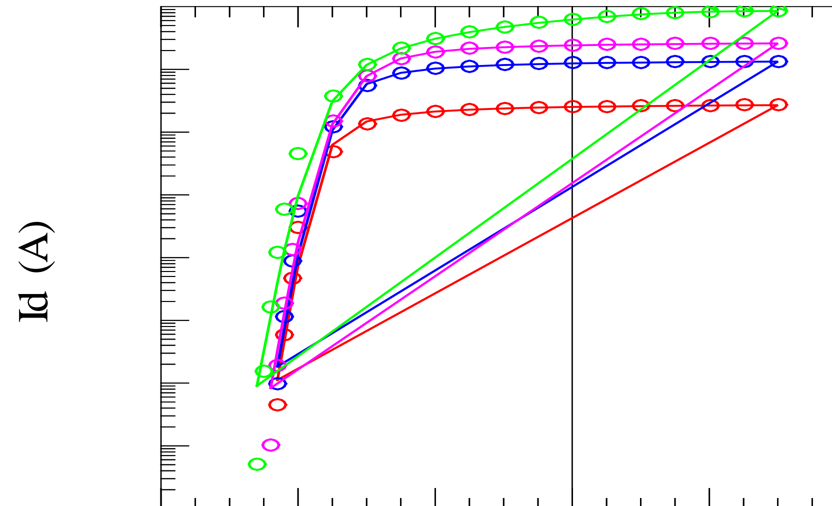


# Modeling DC: Room Temperature IV – Log Scale

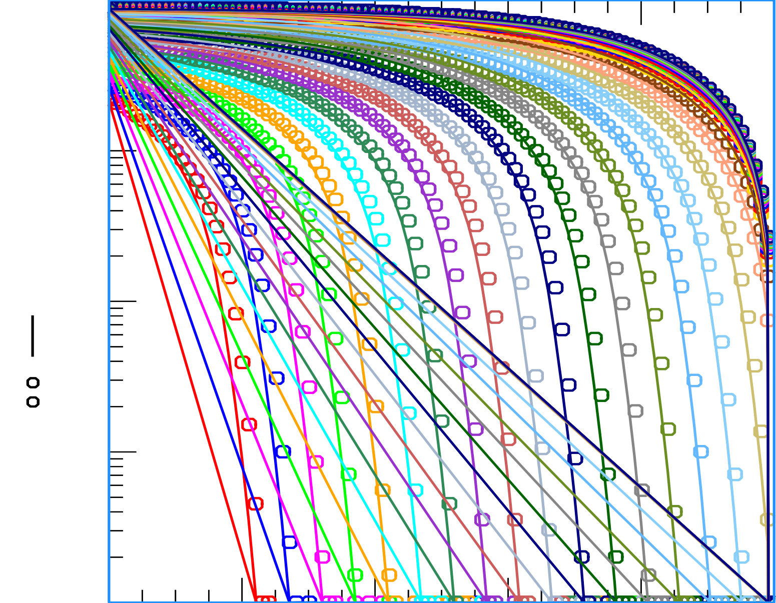
Log (Id) - Vds (Vd>0) T=25°C



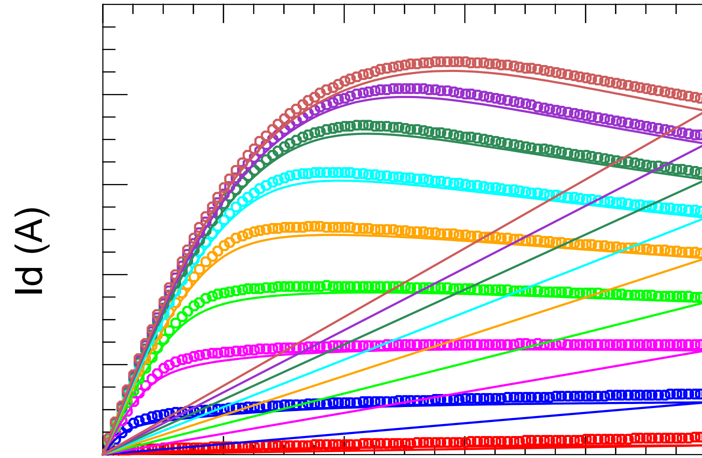
Log (Id) - Vgs T=25°C




Log (Id) - Vds (Vd<0) T=25°C

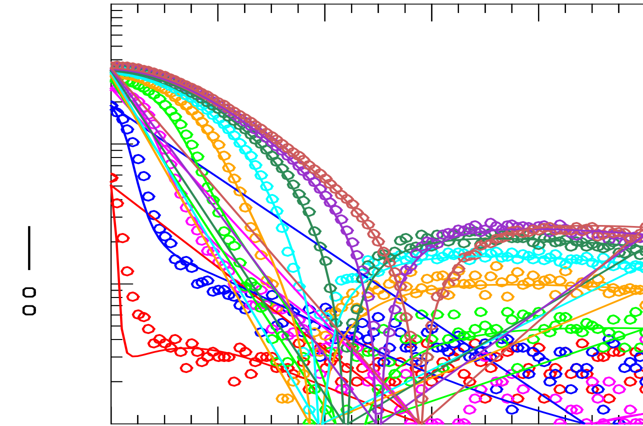


# Modeling DC: Output Characteristics @ T=-20℃

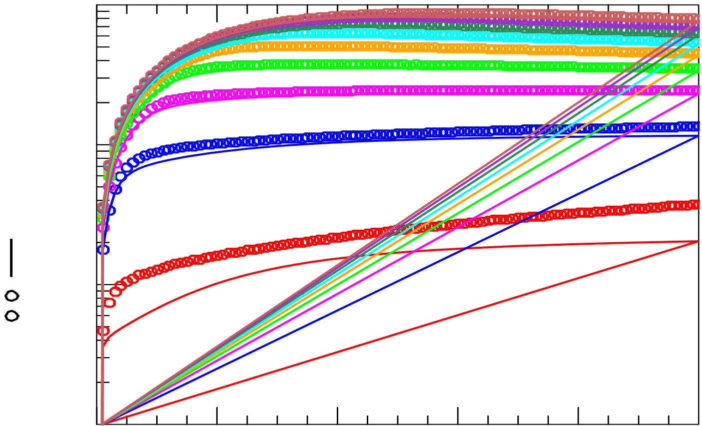



Output Characteristics @ -20℃

Output conductance versus Vd @ -20℃

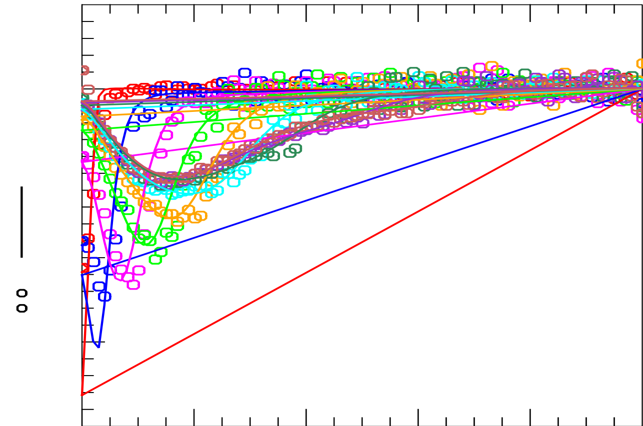


*The model scales accurately to sub-zero temperatures.*

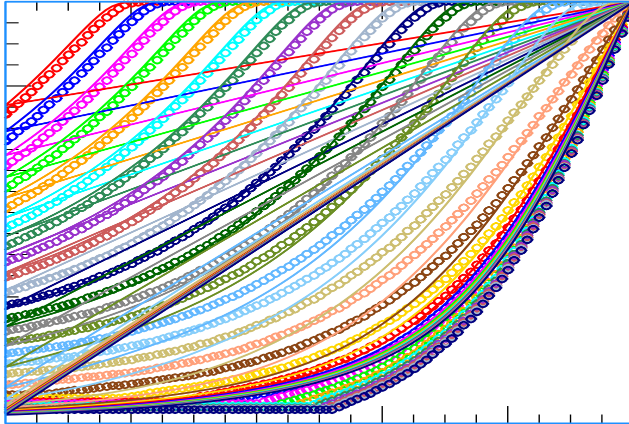


Log Output Characteristics @ -20℃

Derivative of output conductance versus Vd @ -20℃



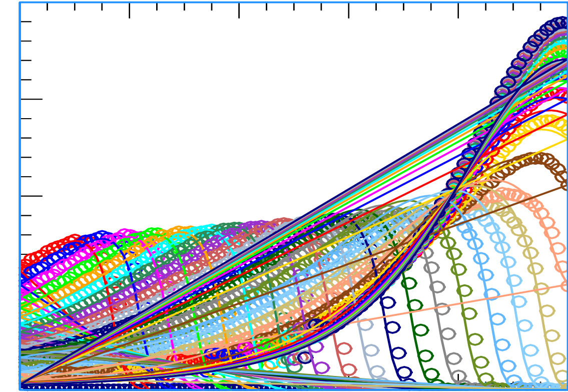
# Modeling DC: Reverse Output Characteristics @ T=-20℃



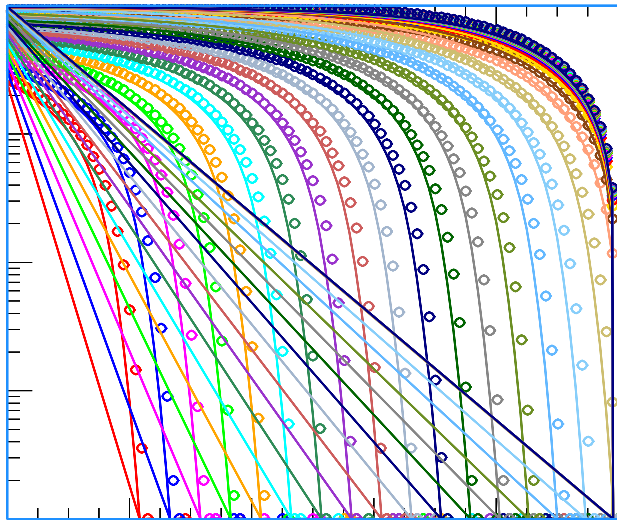
Vg from -12 to 3 V @ 0.5V step

Reverse Output Characteristics @-20℃

Reverse Output conductance versus Vd @-20℃

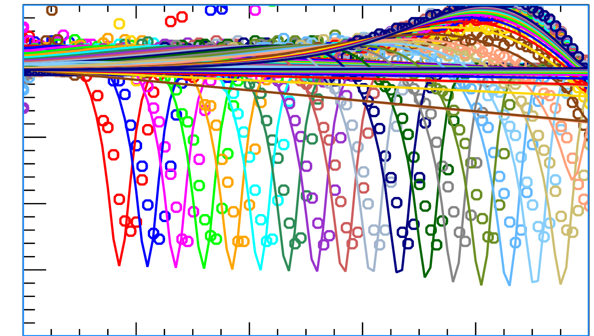


*The model scales accurately to sub-zero temperatures.*



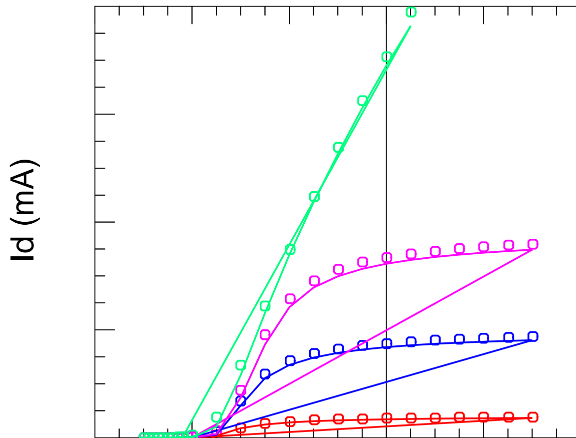
Log Output Characteristics @-20℃

Derivative of reverse output conductance versus Vd @-20℃

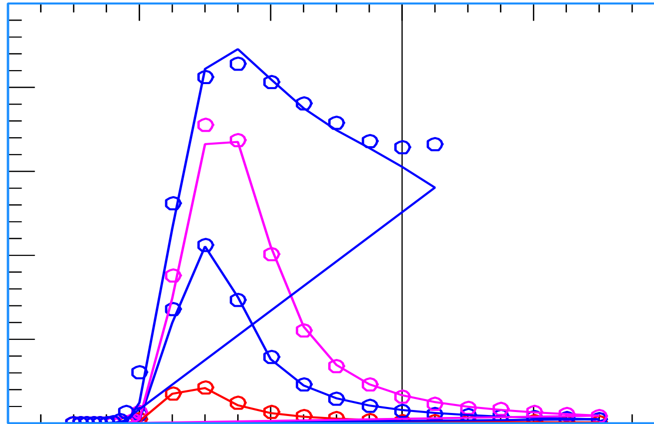


# Modeling DC: Transfer Characteristics @ T=-20℃

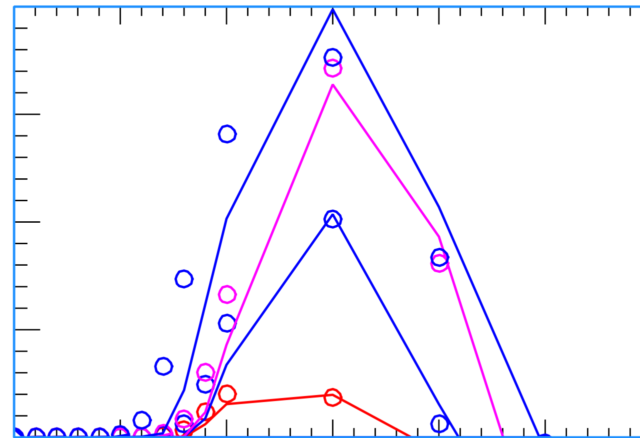
*The model scales accurately to sub-zero temperatures.*



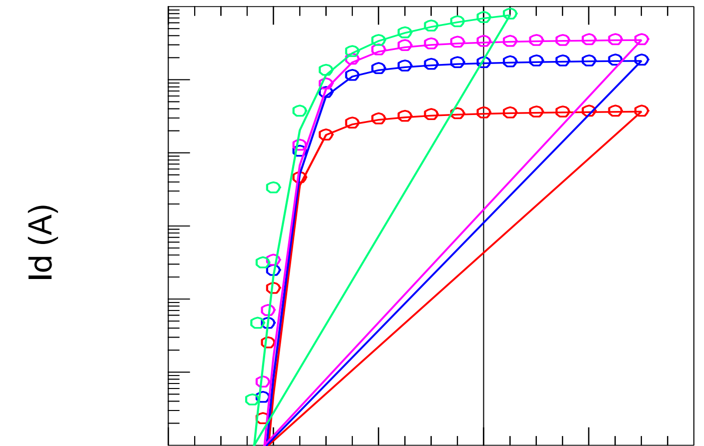

Transfer Characteristics @ T=-20℃



Transconductance @ T=-20℃

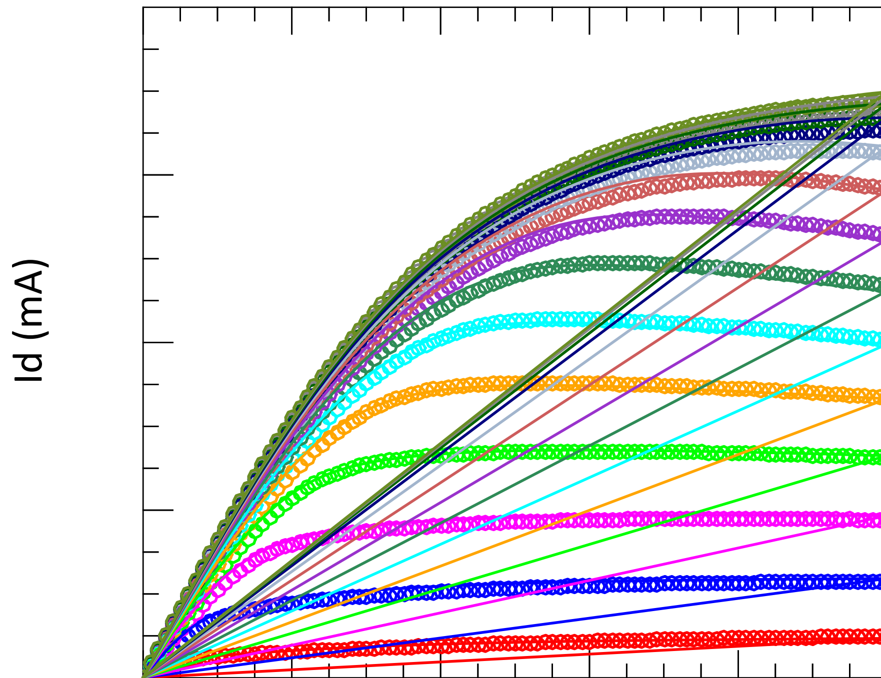


Derivative of Transconductance @ T= -20℃




Transfer Characteristics (Log) @ T=-20℃

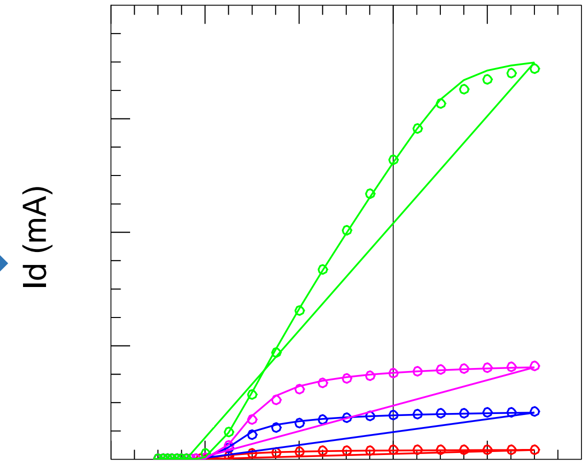
# Modeling DC: IV Characteristics @ T=100℃



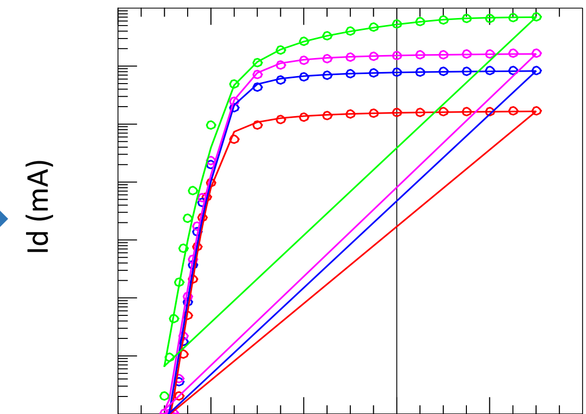

Output Characteristics @ T=100℃

*The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.*

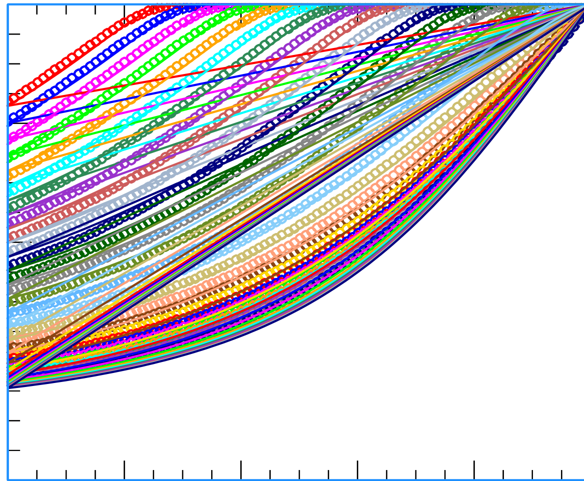
Transfer Characteristics @ T=100℃




Transfer Characteristics (Log) @ T=100℃



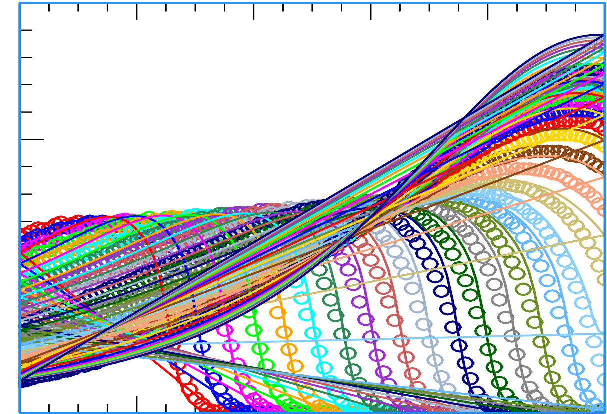
# Modeling DC: Reverse Output Characteristics @ T=150℃



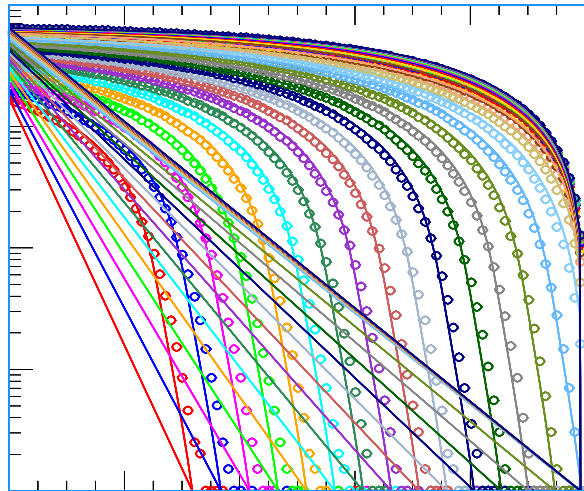
Vg from -12 to 3 V @ 0.5V step

Reverse Output Characteristics @ 150℃

Reverse Output conductance versus Vd @ 150℃

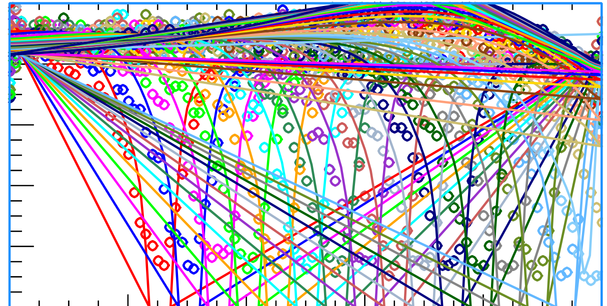


*The model can accurately capture high temperature operation of the device. This is particularly important for power devices which generate a lot of heat.*

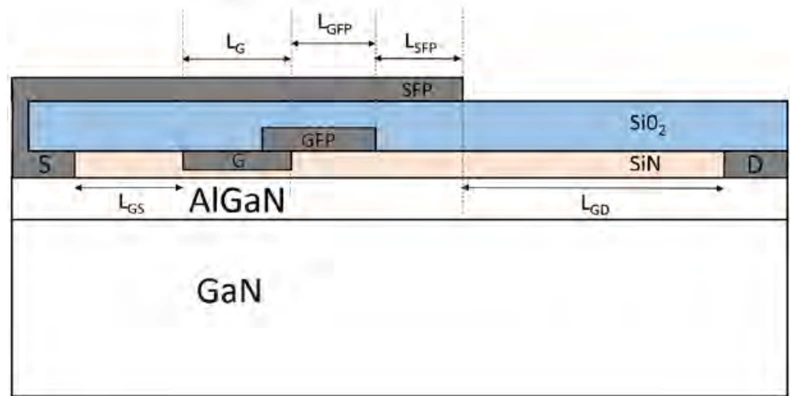


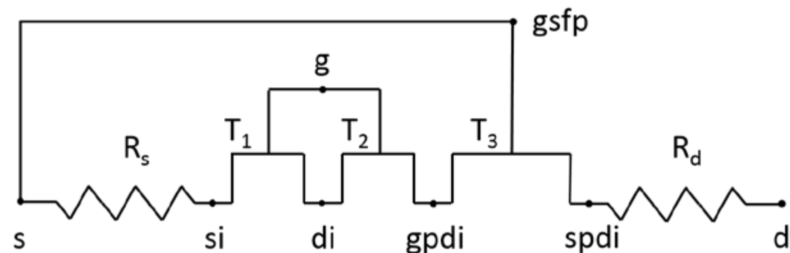
Log Output Characteristics @ 150℃

Derivative of reverse output conductance versus Vd @ 150℃



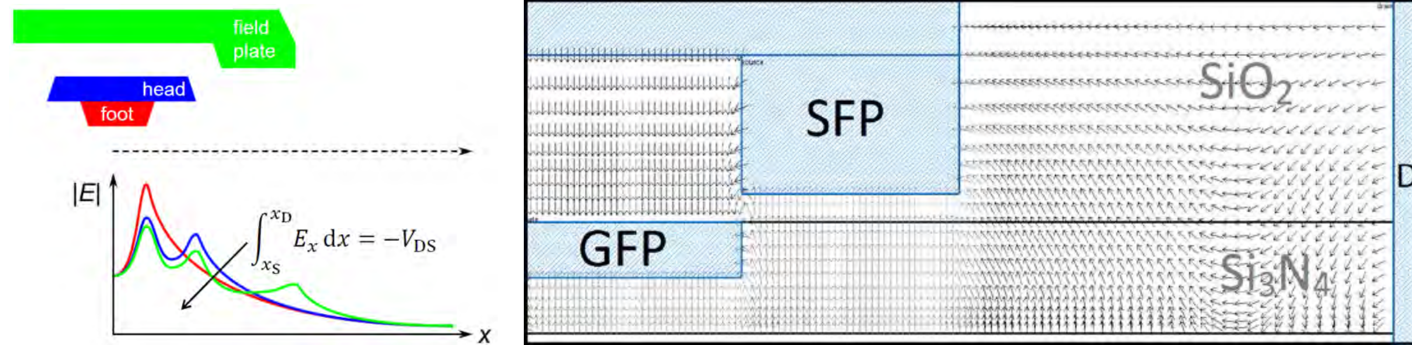
# Modeling field plates: Structure




A Gate Field Plate (GFP) and a Source Field Plate (SFP) structure modeled as transistors in series.

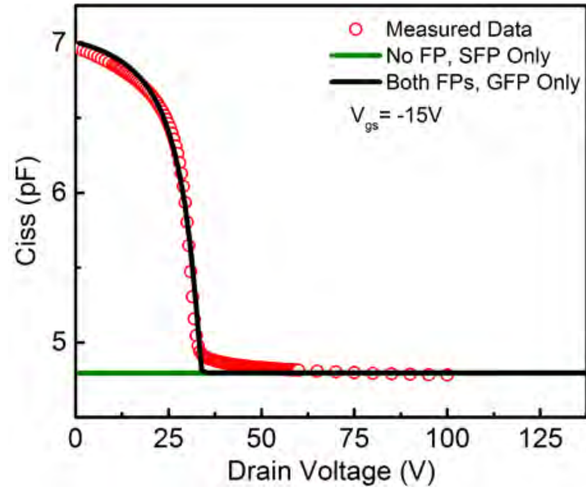
Field plates flatten out the peak in the electric field caused by the sudden drop in potential at the gate edge. TCAD showing field fluctuations leading to a distributed field inside the device.





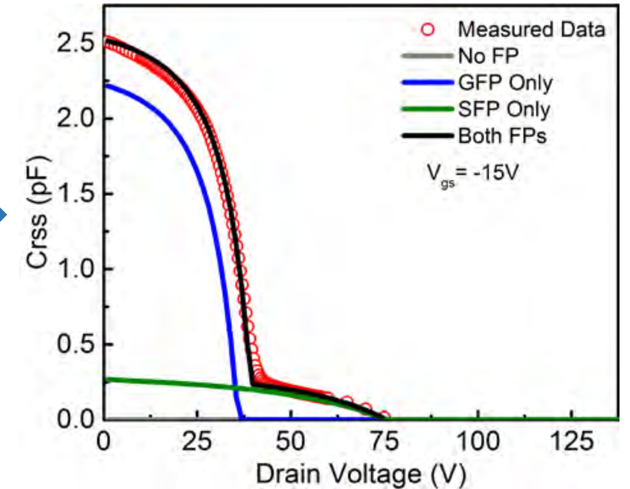
[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

# Modeling field plates: Trends w.r.t Drain Voltage

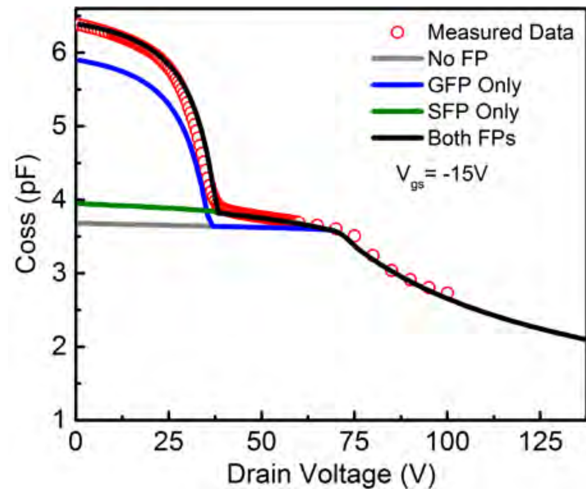



Terminal Capacitance: Input side ( Ciss)

Terminal Capacitance: Reverse (Crss)

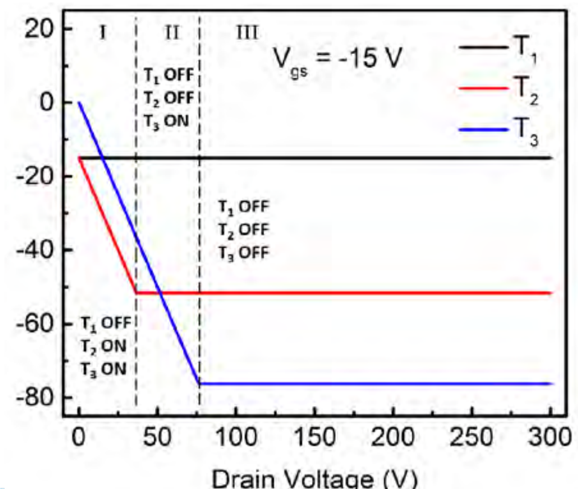



*The plateaus in each capacitance curve denote the **switching -off** of one of the transistors in series as depicted in the previous slide.*



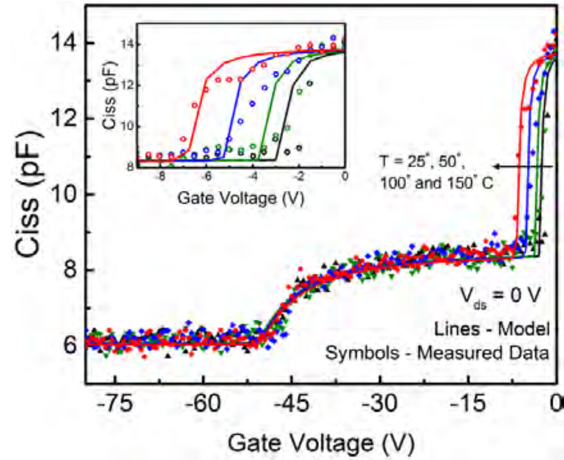

Terminal Capacitance: Output side ( Coss)

Activation of different series transistors with increasing drain voltage at a fixed gate bias



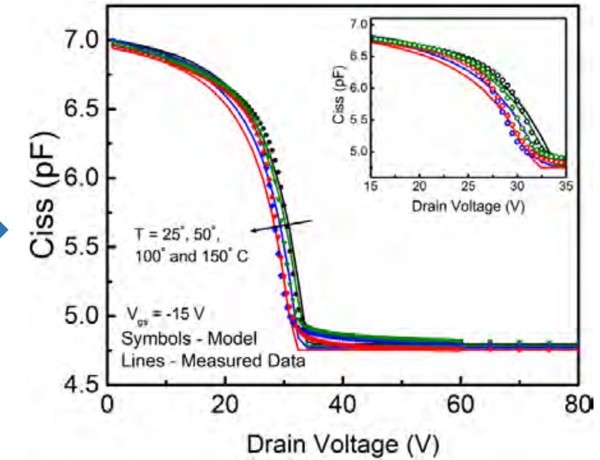

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

# Field Plate Models: Trends w.r.t temperature

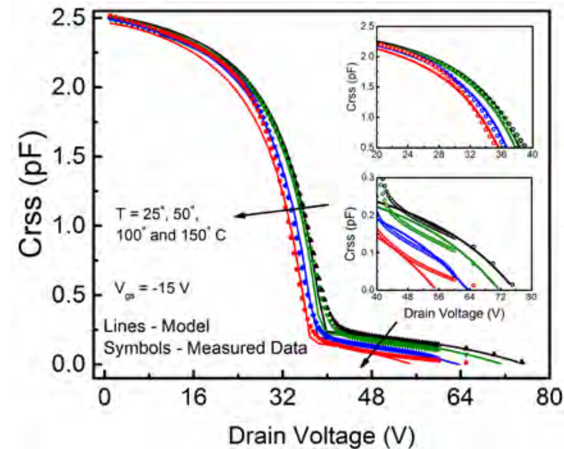



Terminal Capacitance: Input side (Ciss) with gate voltage

Terminal Capacitance: Input side ( Ciss) with drain voltage

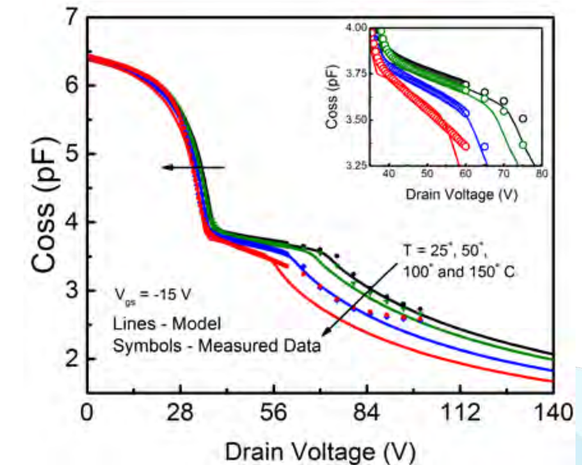



*Increasing temperature shifts the threshold voltage in the negative direction – leading to a corresponding shift in the capacitance curves.*



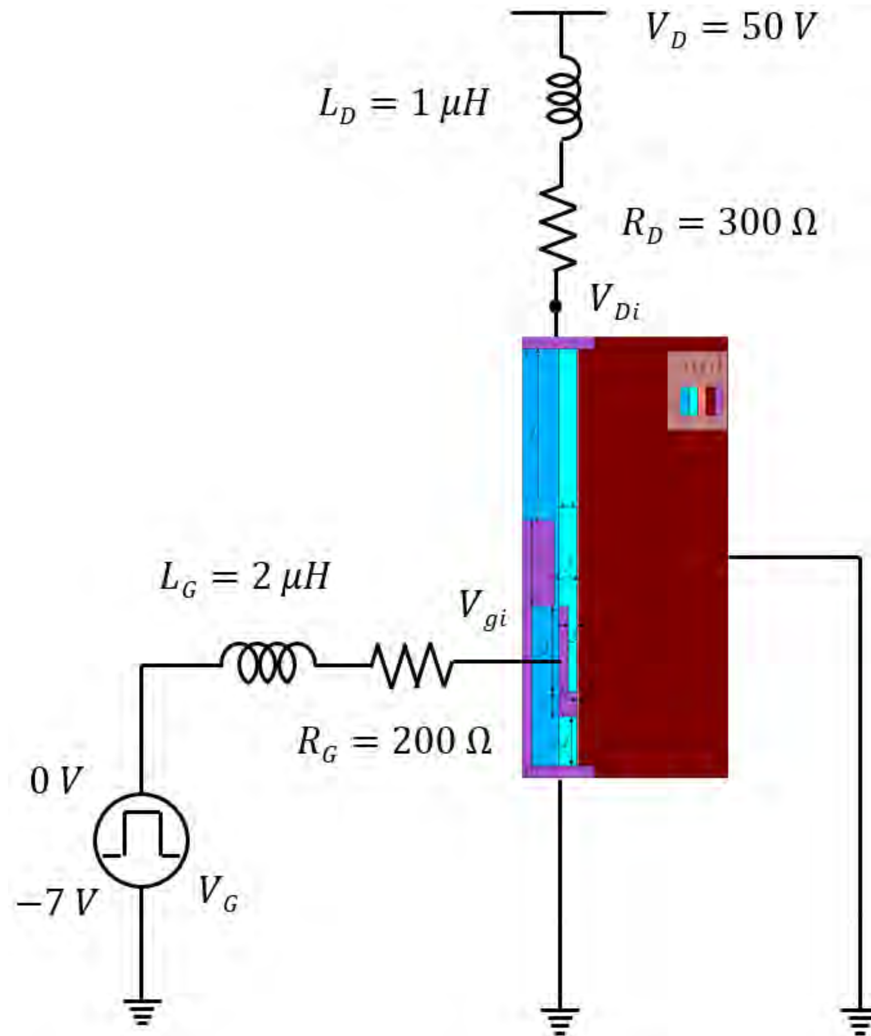

Terminal Capacitance: Reverse (Crss)

Terminal Capacitance: Output side ( Coss)




[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

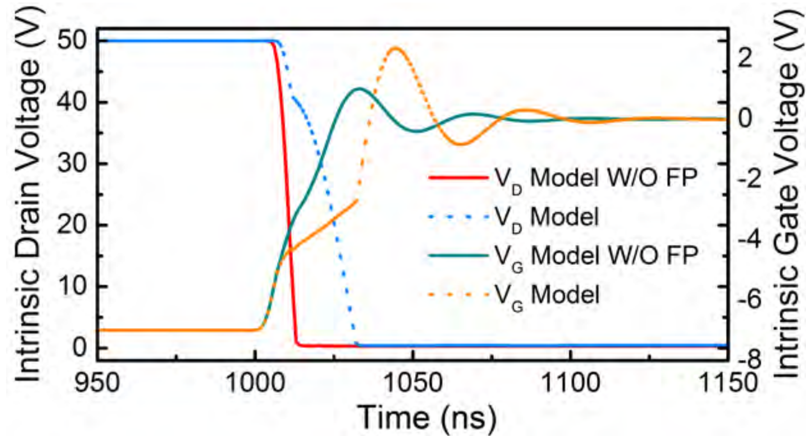
# Mixed mode TCAD circuit using ATLAS



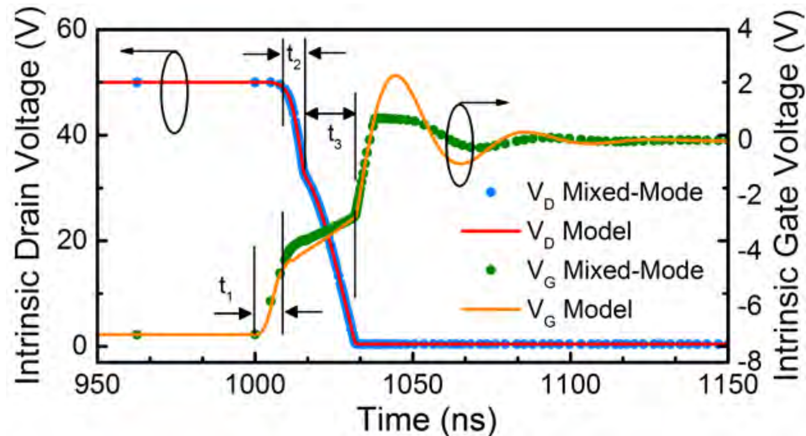

- *Schematic for Mixed-mode simulation using the numerical GaN FP device generated in Atlas.*
- *The FP-HEMT is put as the DUT with7 V and 0 V pulses of 1 MHz at gate.*
- *The pulse has a pulse-width of 480 ns 20 ns rise and fall times.*
- *Supply voltage of 50 V is chosen to capture the maximum effect of cross coupling capacitances on switching transients while an inductive load is put at the drain.*

[1] S. A. Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

# Voltage waveforms

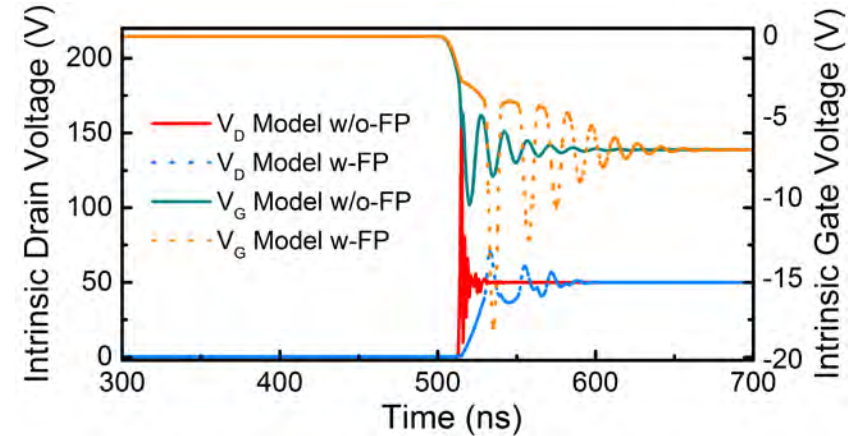



Turn-on by switching applied gate signal from 7 V to 0 V (FP vs no FP)

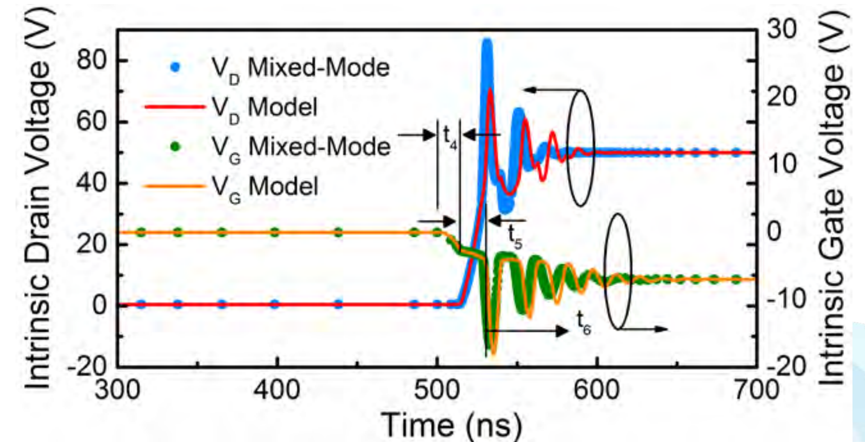



Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)

*The model accurately predicts drain overshoots due to LC ringing, Miller plateaus due to accurate prediction in sharing of the gate drive current to charge Cgs and Cgd and the associated gate-drain charge, and the damping of the oscillations.*



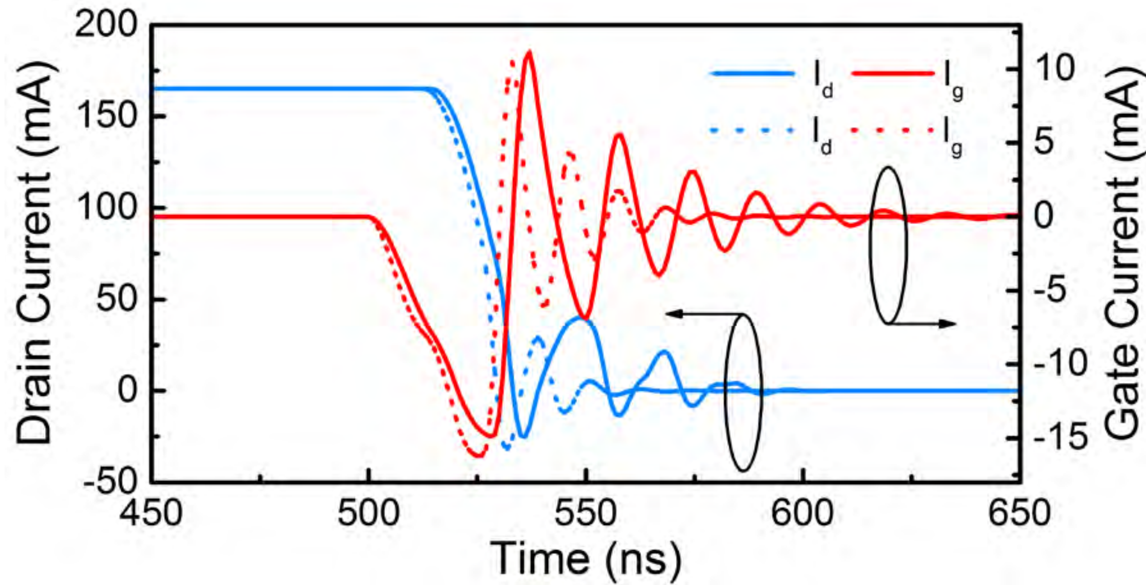

Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (FP vs No FP)




Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed-mode vs Model)

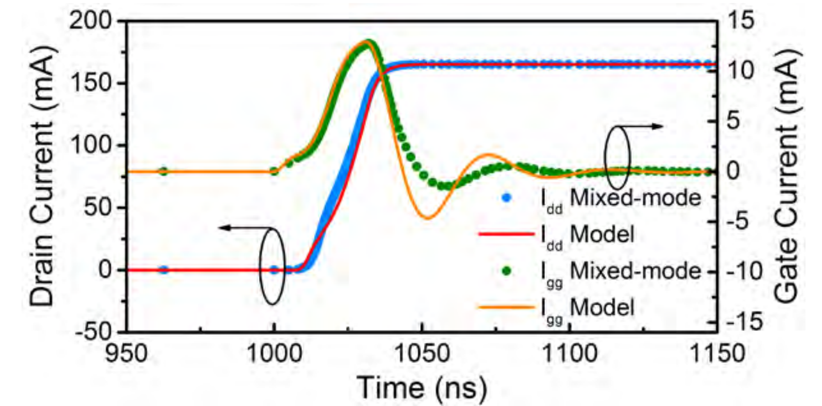
[1]S. A.Ahsan et al., IEEE Transactions on Electron Devices (Special Issue), [2017]

# Current Waveforms

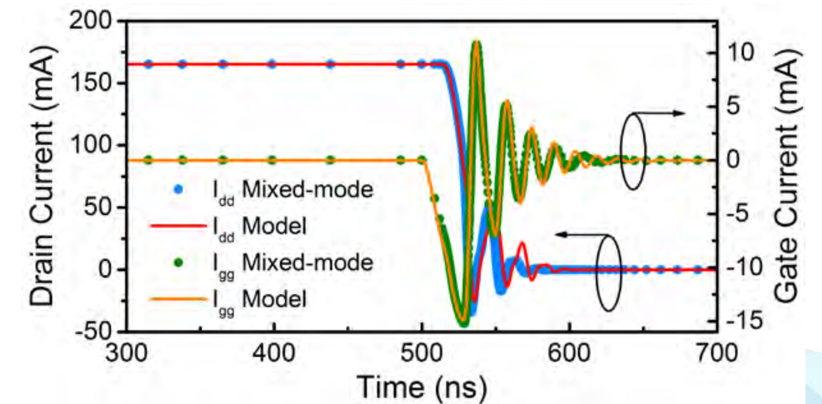



Comparison of modeled time-domain waveforms during turn-off with and without cross-coupling and substrate capacitances.

Solid lines = Cross-Coupling(CC) and substrate model included
Dotted lines = CC and substrate model excluded.




Turn-on by switching applied gate signal from 7 V to 0 V (Mixed-mode vs Model)




Turn-off by switching applied gate signal from 0 V to 7 V, keeping applied drain voltage fixed at 50 V (Mixed-mode vs Model)

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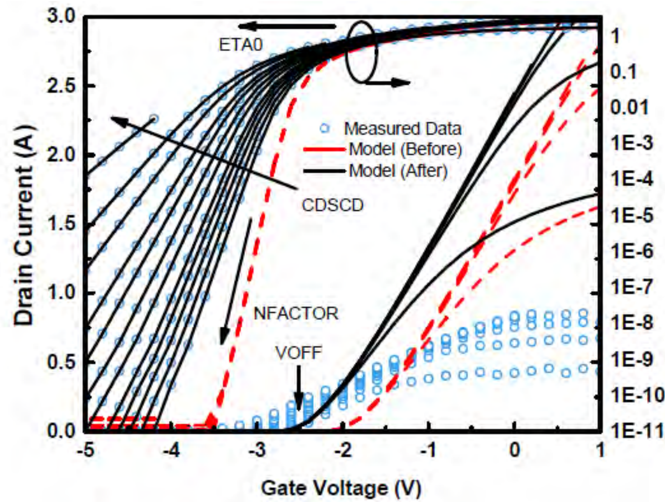
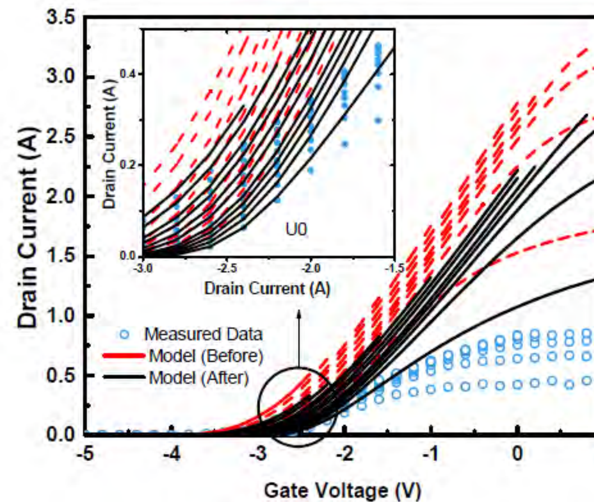
# Modeling RF Devices using ASM - HEMT

- *Extracting DC Parameters*
- *RF Model Extraction*
- *Large signal simulations*
- *Load Pull Simulations*

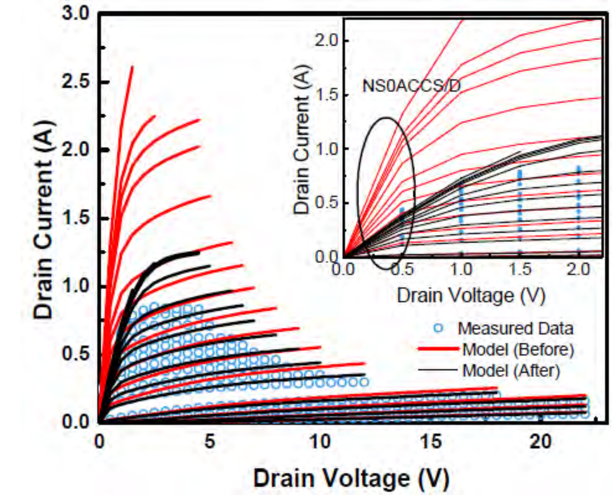
# Extracting DC Parameters



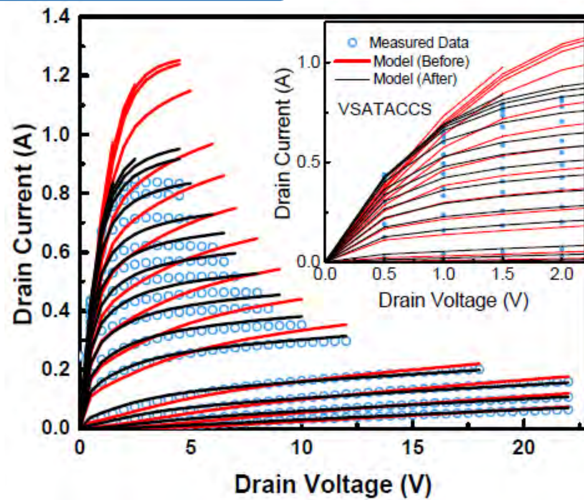

$I_d - V_g$ (Extract $V_{OFF}$, $N_{FACTOR}, C_{DSCD}$)



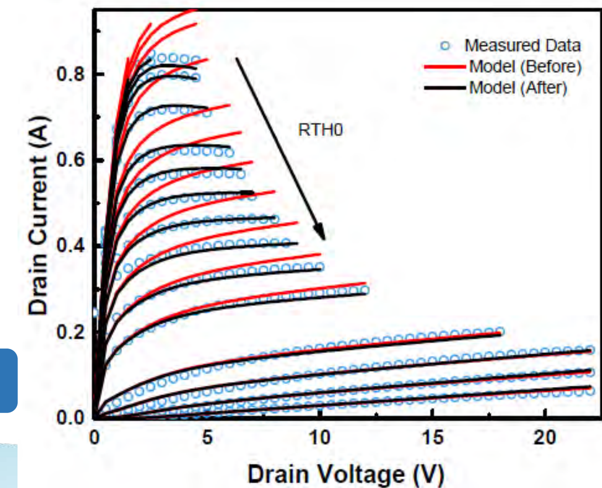

$I_d - V_g$ (Extract $U_0$)




$I_d - V_d$ (Extract $N_{S0ACCS}$)




$I_d - V_d$ (Extract $V_{SATACCS}$)




$I_d - V_d$ (Extract $R_{TH0}$)

[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

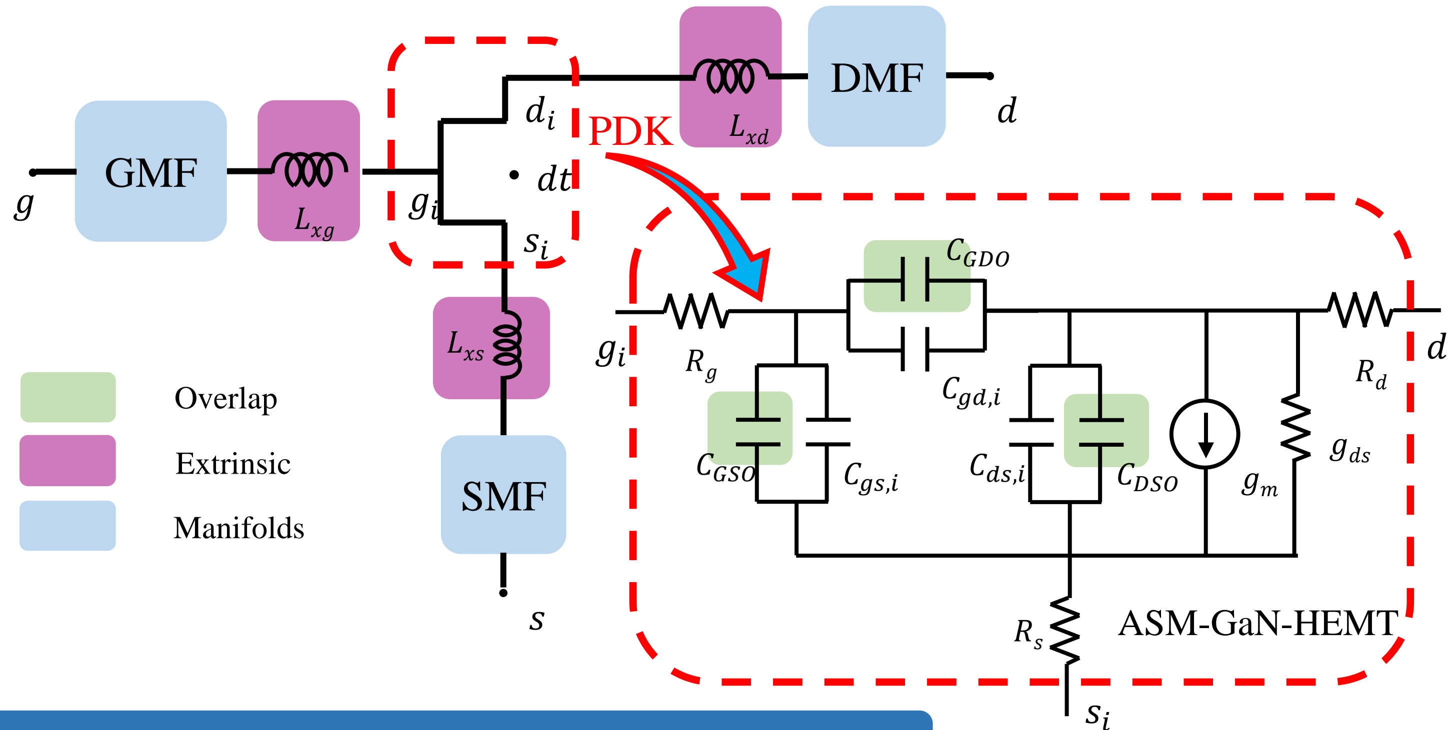
# RF Model & Extraction I

## Three step methodology

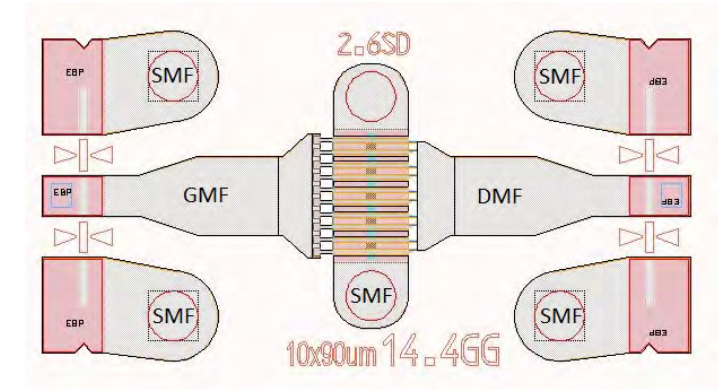
- De-embed manifolds
- Extract the intrinsic core model - Using low frequency Y-parameters
- Extract Inductances - Using high frequency Y-parameters

## Model

- Core surface potential based PDK
- Access region resistances included in core
- Bus-inductances in extrinsics




Pad-level Small Signal Equivalent Circuit Model



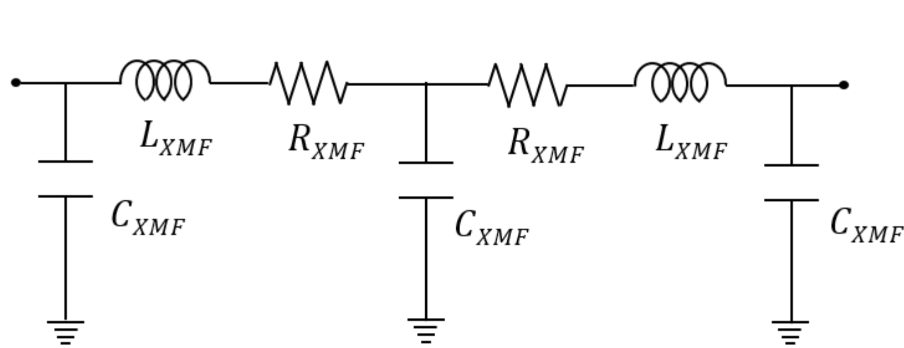

Device Layout

[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

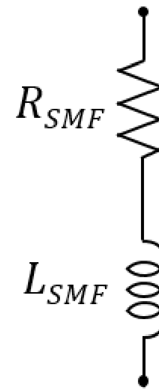
# RF Model & Extraction II: Pad Parasitics

## Manifolds/ Pads

- Used to probe the device
- Feed the signal to gate, drain & source bus-inductances
- Measurements obtained using TRL Calibration
- Transmission line type model
- Reciprocal (may/ may not be symmetric)
- De-embedded using "deembed" s2p components in ADS

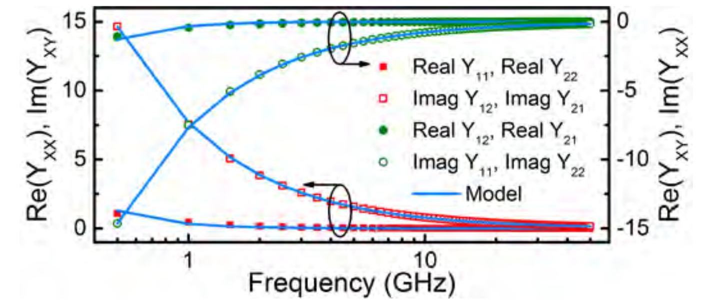



Symmetric network used for GMF/ DMF

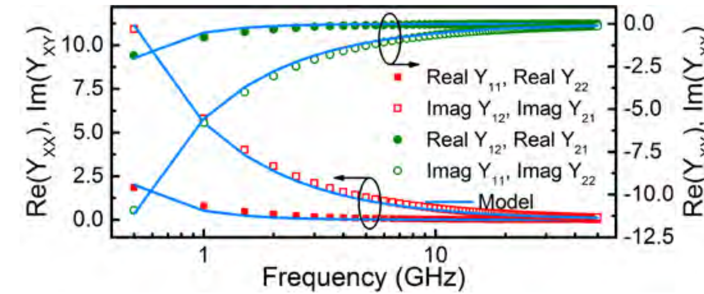



Single port SMF network

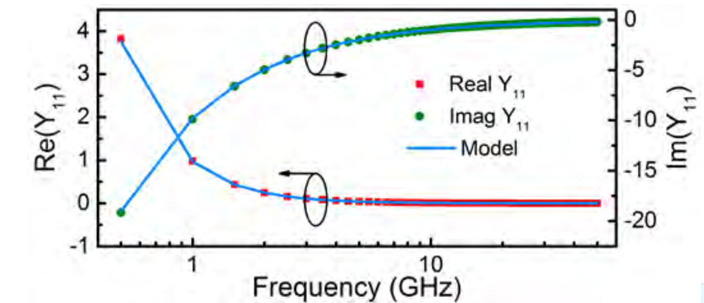
Y-parameters for DMF




Y-parameters for GMF




Y-parameters for SMF




[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# RF Model & Extraction III: Bus Inductances

[1]

$$Y_{11} = \frac{\omega^2 {C_{gg}}^2 R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} + \frac{j\omega C_{gg}}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{12} = -\frac{\omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} - \frac{j\omega C_{gd}}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{21} = \frac{g_m - \omega^2 C_{gd} C_{gg} R_g}{1+\omega^2 {C_{gg}}^2 R_g^2} - \frac{j\omega (C_{gd} + g_m C_{gg} R_g)}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

$$Y_{22} = g_{ds} + \frac{\omega^2 (C_{gs} C_{gd} R_g + R_g C_{gd} C_{gg} (1 + g_m R_g))}{1+\omega^2 {C_{gg}}^2 R_g^2} + j\omega C_{ds} + \frac{j\omega C_{gd} (1 + g_m R_g) + j\omega^3 C_{gs} C_{gd} C_{gg} R_g^2}{1+\omega^2 {C_{gg}}^2 R_g^2}$$

## Key Pointers

- The effect of bus-inductances is ignored at low frequencies (assumption)
- Drain & Source access region resistances ignored from hand analysis (not an assumption, it is [1] an advantage)
- Ignore some terms at low frequency (~ 10 GHz) (assumption)
- Very simple – only need to adjust overlap capacitances & gate finger resistances (advantage)

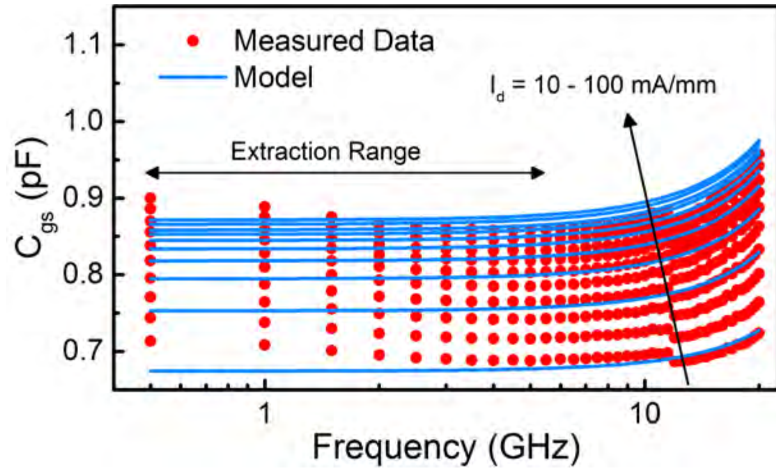
$$[\mathbf{Y}] \approx \begin{bmatrix} \omega^2 {C_{gg}}^2 R_g + j\omega C_{gg} & -\omega^2 C_{gd} C_{gg} R_g - j\omega C_{gd} \\ g_m - j\omega \left(C_{gd} + g_m C_{gg} R_g\right) & g_{ds} + j\omega \left(C_{ds} + C_{gd} (1 + g_m R_g)\right) \end{bmatrix}$$

$$\begin{bmatrix} C_{gs} & C_{gd} & C_{ds} \\ g_m & g_{ds} & R_g \end{bmatrix}$$

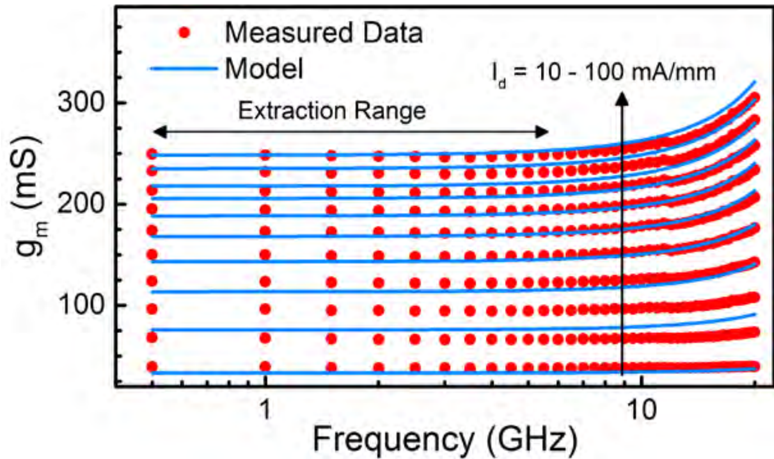
$$\begin{bmatrix} \left(\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}]\right)/\omega & -\mathrm{Im}[Y_{12}]/\omega & \mathrm{Im}[Y_{22}]/\omega - C_{gd}\left(1 + g_m R_g\right) \\ \mathrm{Re}[Y_{21}] & \mathrm{Re}[Y_{22}] & \mathrm{Re}[Y_{11}]/\left(\omega^2 C_{gg}^2\right) \end{bmatrix}$$

[1] I. Kwon et al., IEEE Trans. Microw. Theory Techn., 50 (6), [2002]

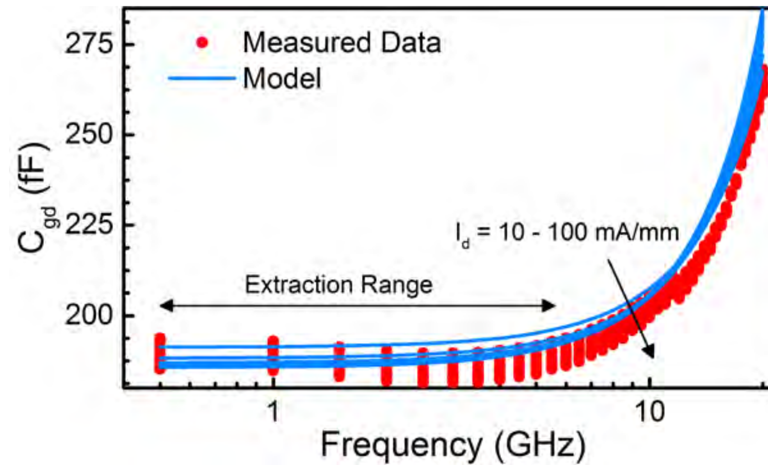
# Fitting core model parameters using ADS



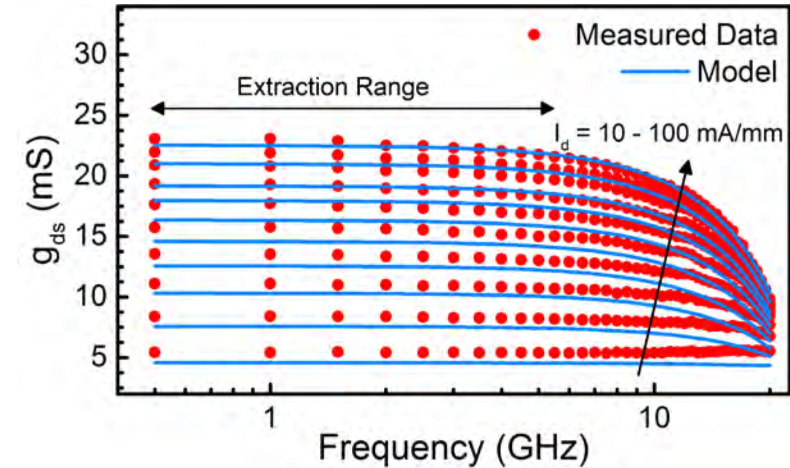

Extract $C_{GSO}$




$g_m$ dispersion handled by trap model



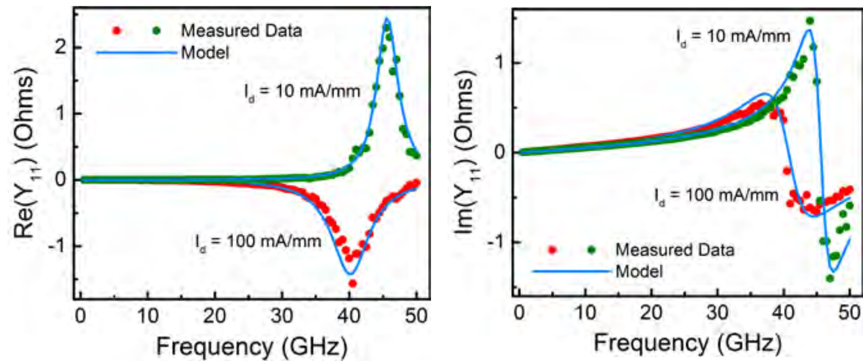

Extract $C_{GDO}$

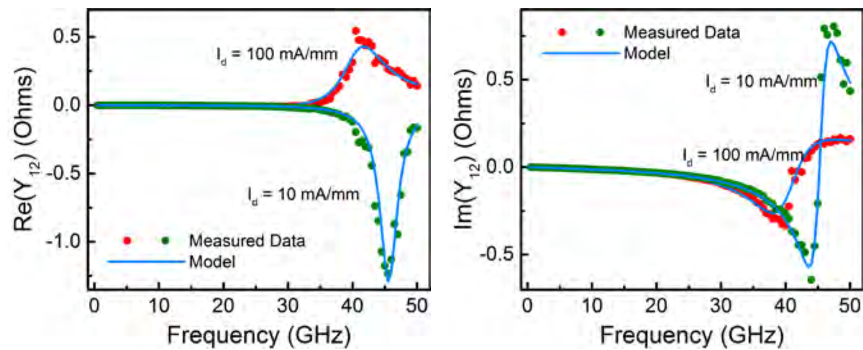



$g_{ds}$ dispersion handled by trap model

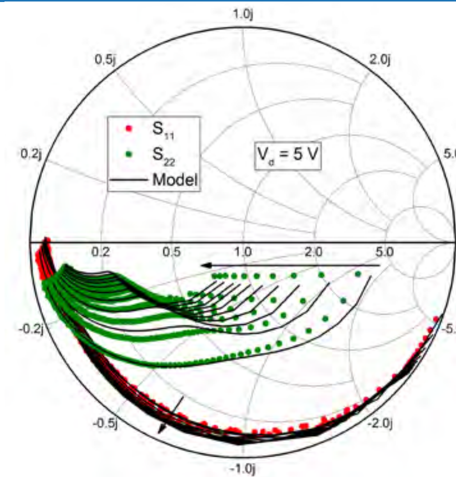
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# Bus Inductance fitting

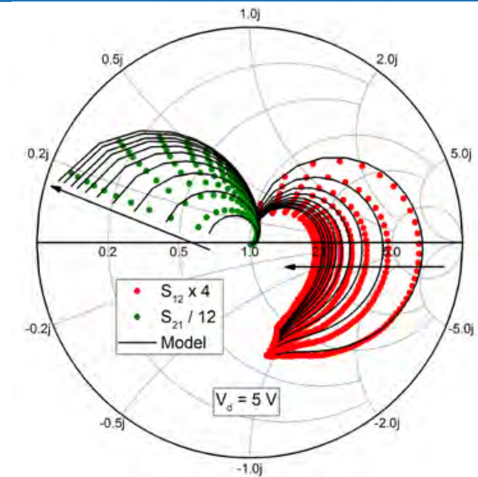


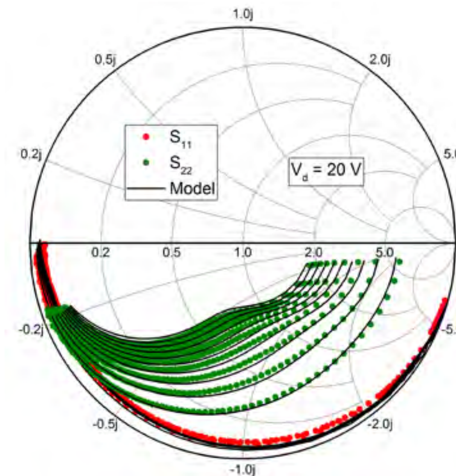

Resonant peaks due to interaction of inductances with intrinsic capacitances



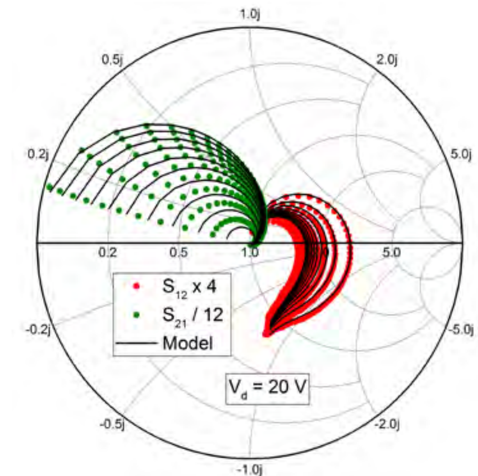

$S_{11}$ & $S_{22}$ (5V)




$S_{12}$ & $S_{21}$ (5V)



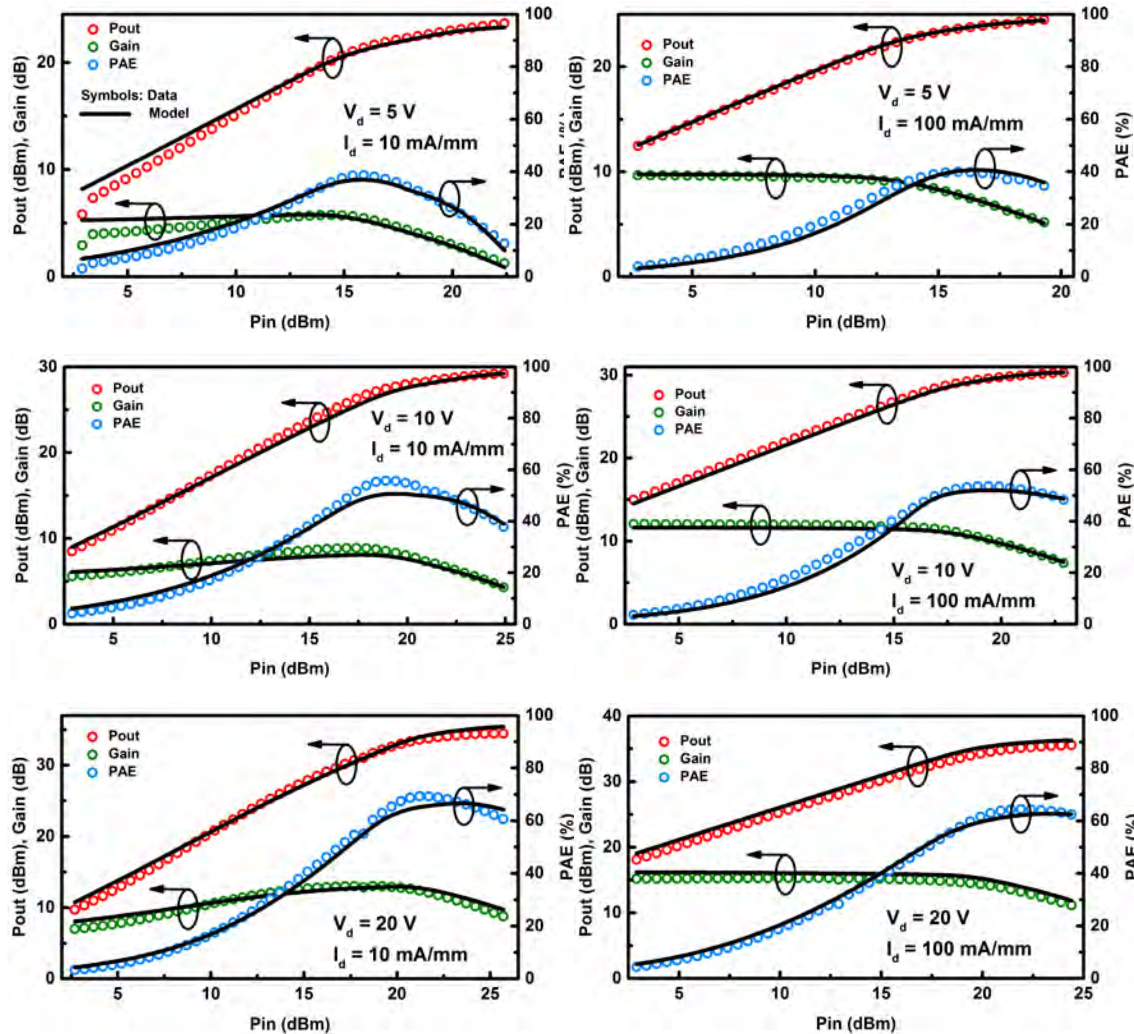

$S_{11}$ & $S_{22}$ (20V)



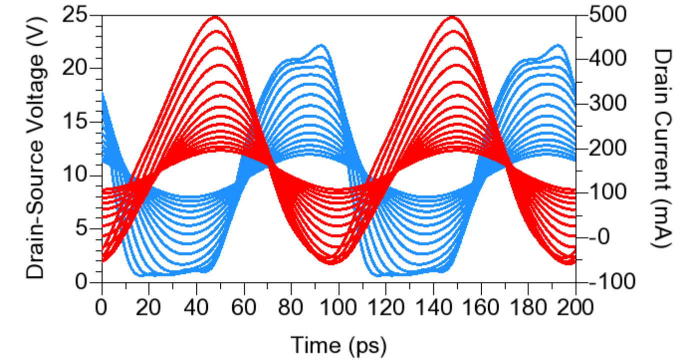

$S_{12}$ & $S_{21}$ (20V)

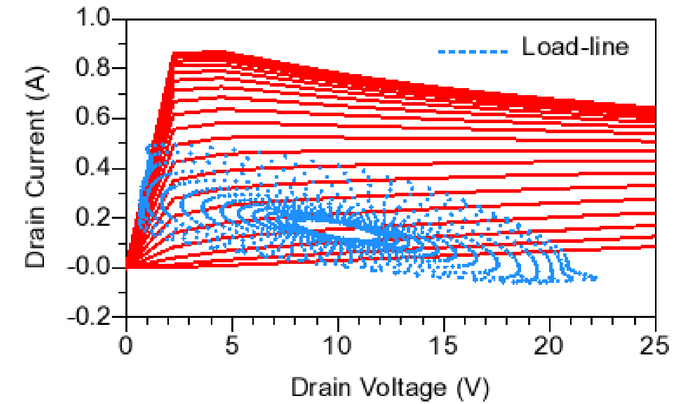
[1] S. A. Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

# Large Signal HB Simulations




Harmonic balance drive -up characteristics showing Pout, PAE & Gain



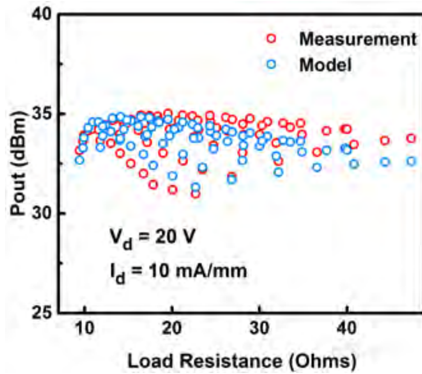



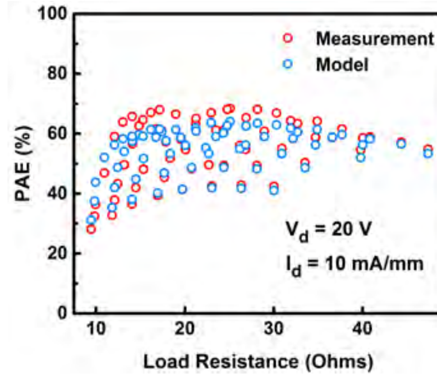

Time domain waveforms of drain voltage & current. Load line contours spanning the IV plane

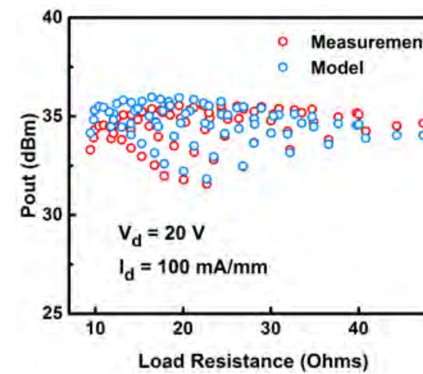
[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

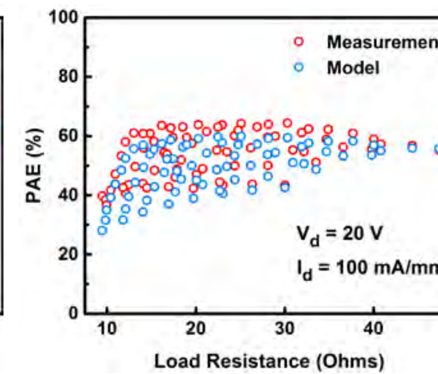
# Validation – Real and Imaginary Loads

Fairly accurate in predicting the maxima for Pout & PAE

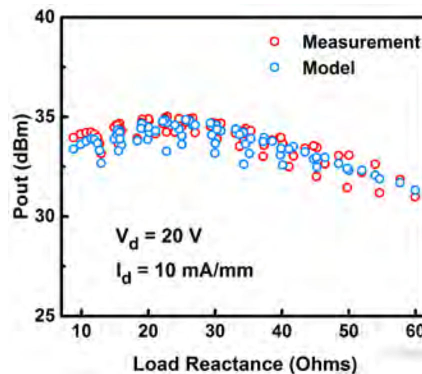


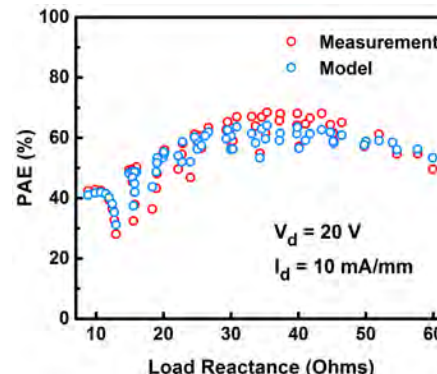



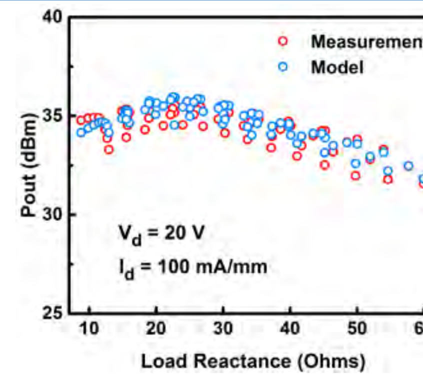



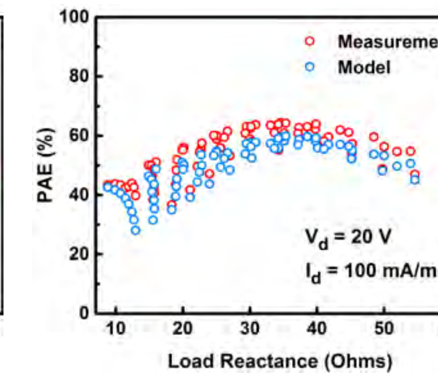




Pout & PAE against load resistance (real load)



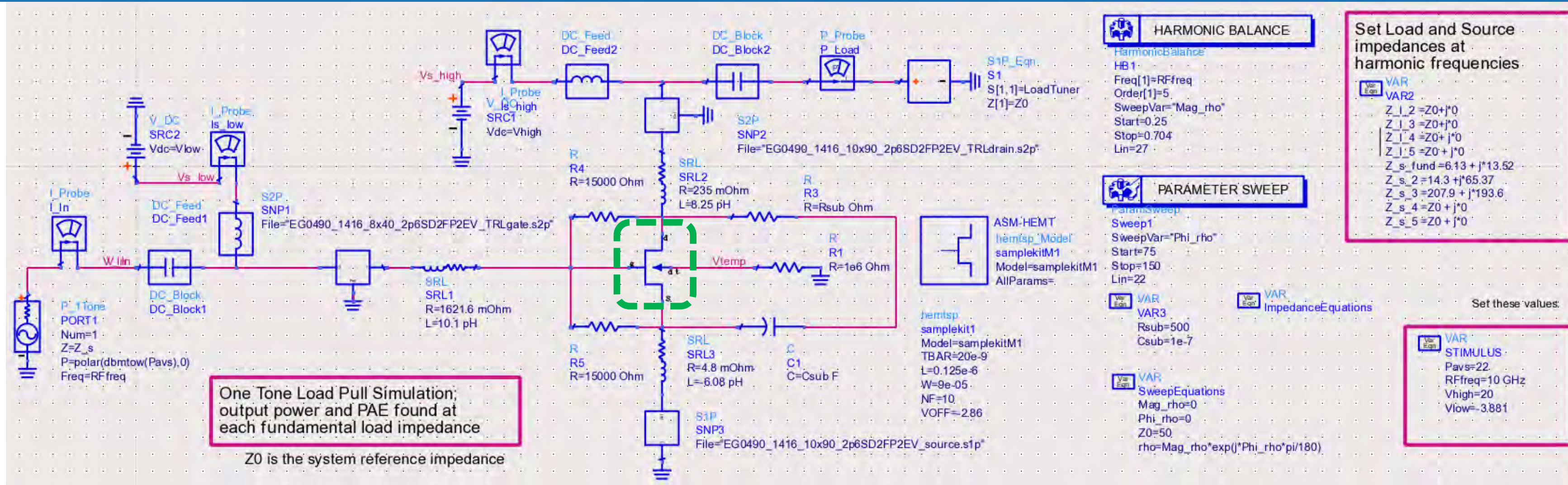




Pout & PAE against load reactance (imaginary load)

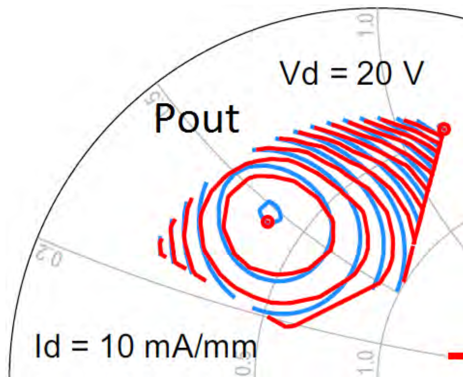
[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

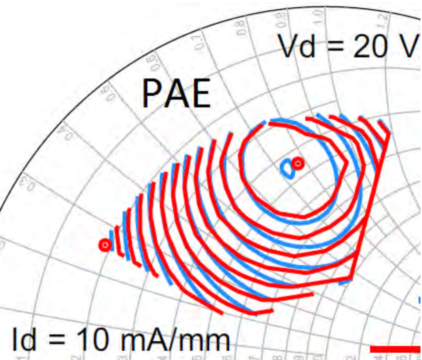
# Load Pull simulations using ASM -HEMT

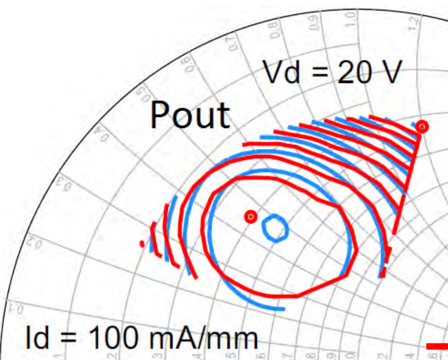


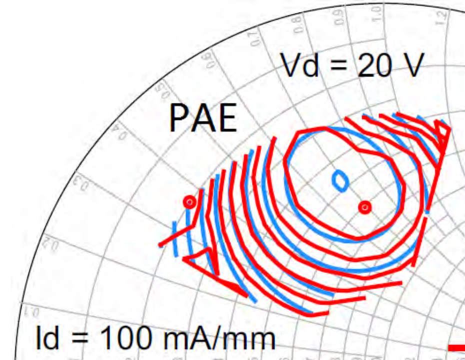
ADS Schematic for simulation of load -pull contours

22 dBm signal @ 10 GHz




Pout & PAE load pull contours for 10 mA/mm

Pout & PAE load pull contours for 100 mA/mm

[1]S. A.Ahsan et al., IEEE J. Electron Devices Society, Sep., [2017]

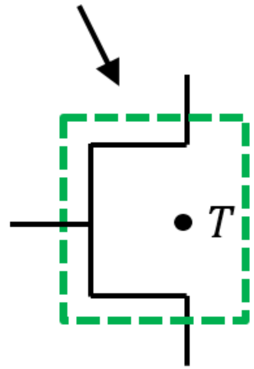
# Contents

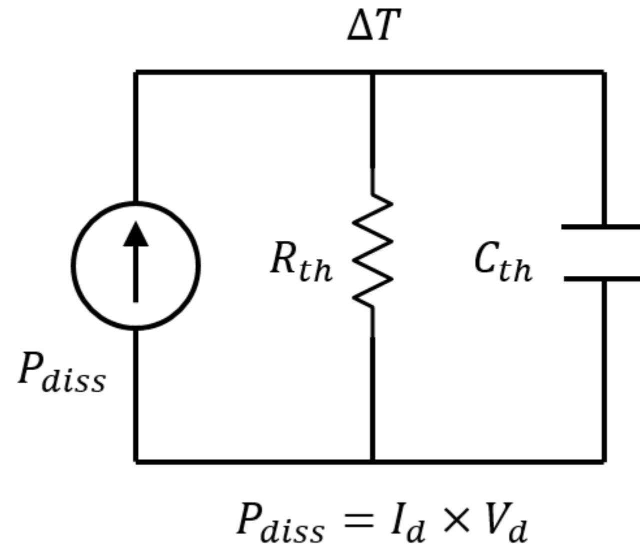

- Nanolab – Characterization and Modeling Capabilities
- An introduction to ASM-HEMT
- Modeling Power Devices using ASM-HEMT
- Modeling RF Devices using ASM-HEMT
- Characterizing Self Heating and its Modeling
- Trapping models in ASM-HEMT

# Characterizing Self Heating and its Modeling

- *Self heating Model*
- *Characterization*

# Self- Heating Model




$$T = T_{NOM} + \Delta T$$

$$P_{diss} = I_d \times V_d$$

Self-Heating Effect

- The self-heating circuit is defined in a thermal discipline.
- For the thermal discipline, power is the equivalent of "current" and temperature is the equivalent of "voltage"

*Under these conditions, applying KCL on the thermal subcircuit, we have*:

$$P(R_{th}) = \frac{Temp(R_{th})}{RTH0}$$

$$P(R_{th}) = \frac{d}{dt}(Temp(R_{th}) \cdot CTH0)$$

# Characterization

$$T_{J1} = T_{NOM,1} + R_{th} \times P_{diss1}$$

$$T_{J2} = T_{NOM,2} + R_{th} \times P_{diss2}$$

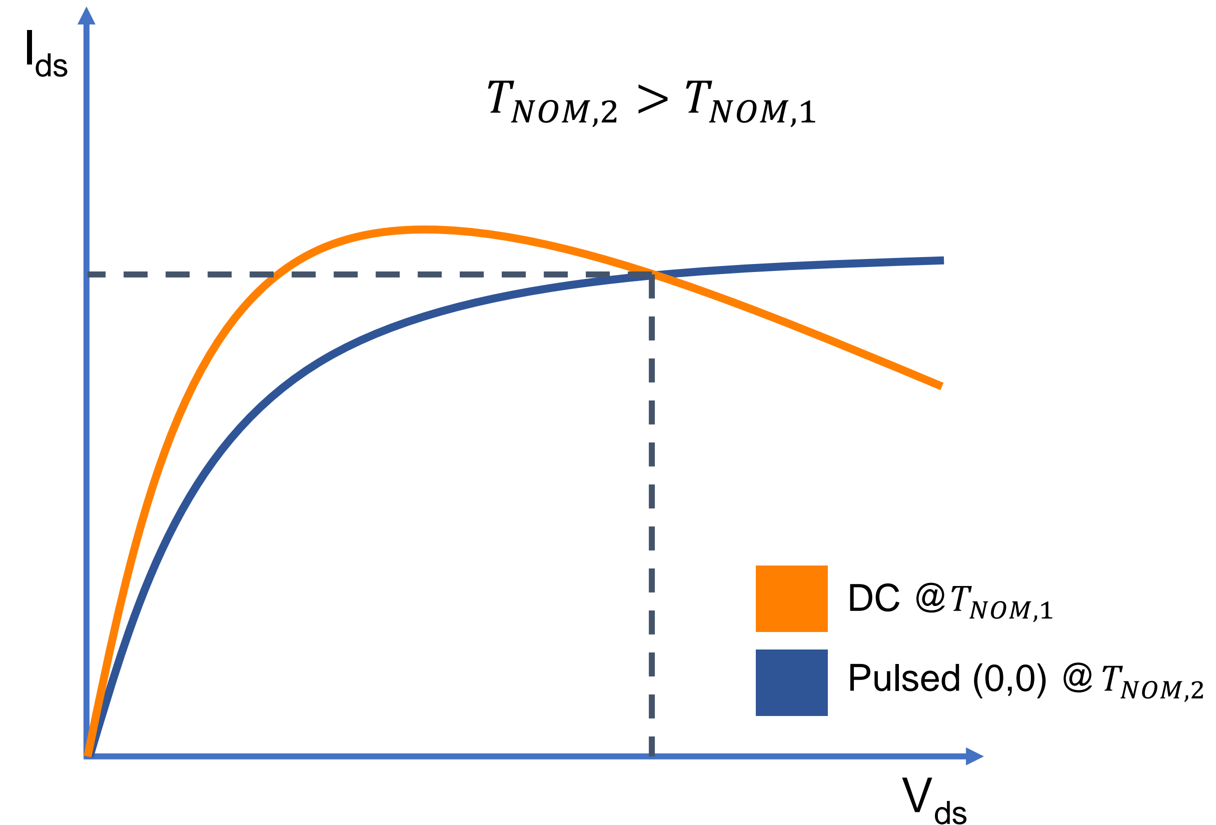
At the intersection point:

$T_{J1} = T_{J2}$

And $P_{diss2} = 0$ (Pulsed at (0,0))

$$\Rightarrow R_{th} = \Delta T_{NOM} / \Delta P_{diss}$$

With the ASM-HEMT model, the parameter **RTH0** is tuned till the simulated intersection point overlaps with the measured intersection point after thermal parameters like **UTE**, **AT** and **KT1** have been extracted.




Extracting Rth. Both curves are measured at the same Vgs. The intersection point denotes a common junction temperature.


[1] T. Peyretaillade et al.,1997 IEEE MTT-S International Microwave Symposium Digest, Denver, CO, USA, 1997. doi: 10.1109/MWSYM.1997.596619.

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- Nanolab – Characterization and Modeling Capabilities
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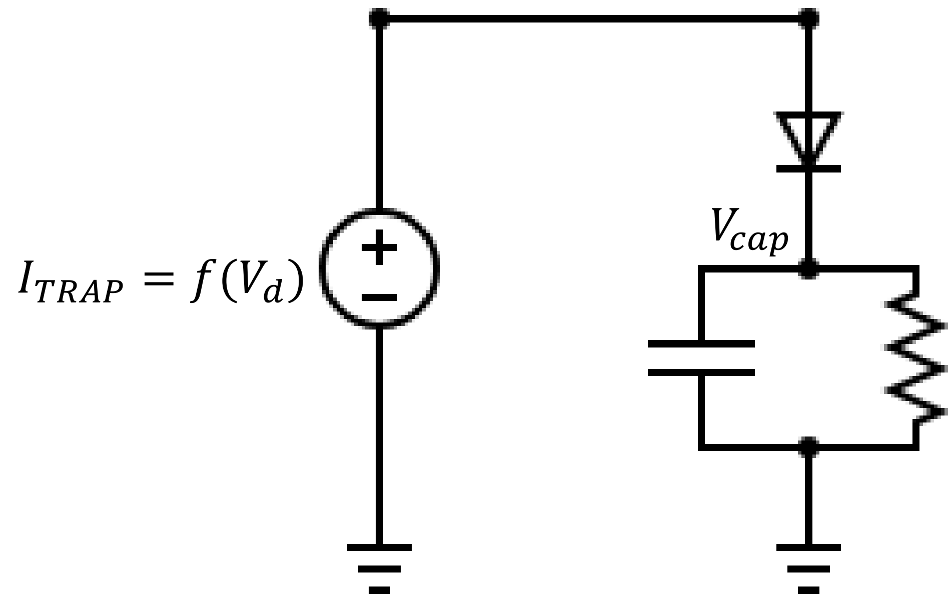
- **Trapping models in ASM-HEMT**

# Trapping models in ASM -HEMT

- *Trapping Models in ASM-HEMT*
- *Extraction using pulsed measurements*

# Trapping Models in ASM -HEMT: TRAPMOD I




### Key highlights

- Dependent on drain voltage only
- Bias-dependent and bias-independent options
- Scales with signal power levels
- Suitable for RF
- Affects threshold voltage, DIBL, AR Resistance.

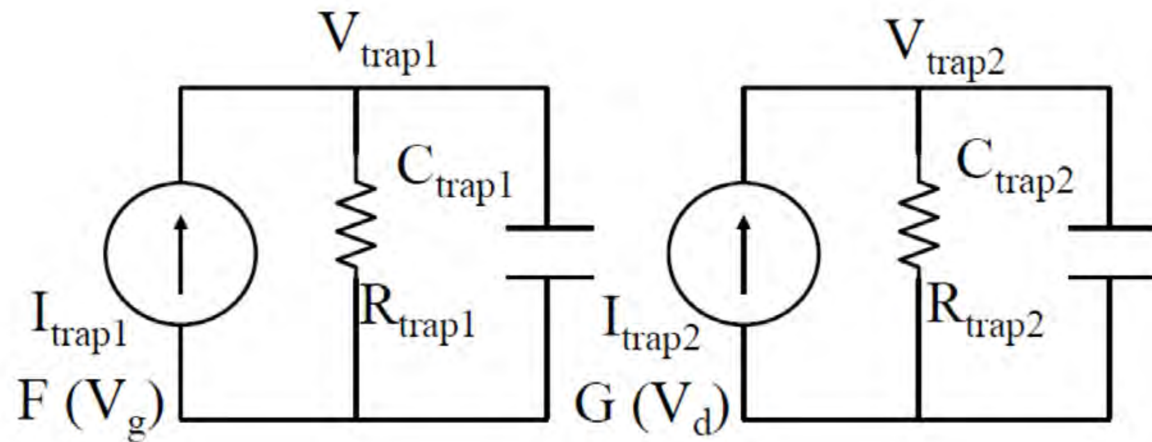
$$V_{OFF}(Trap) = V_{OFF} + (ATRAPVOFF + BTRAPVOFF \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_S(Trap) = R_S + (ATRAPRS + BTRAPRS \cdot e^{-\frac{1}{V_{cap}}})$$

$$R_D(Trap) = R_D + (ATRAPRD + BTRAPRD \cdot e^{-\frac{1}{V_{cap}}})$$

$$\eta_0(Trap) = \eta_0 + (ATRAPETA0 + BTRAPETA0 \cdot e^{-\frac{1}{V_{cap}}})$$

# Trapping Models in ASM -HEMT: TRAPMOD II




### Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance
- Suitable for PIV simulation
- Affects threshold voltage, DIBL, Subthreshold Slope, AR Resistance.

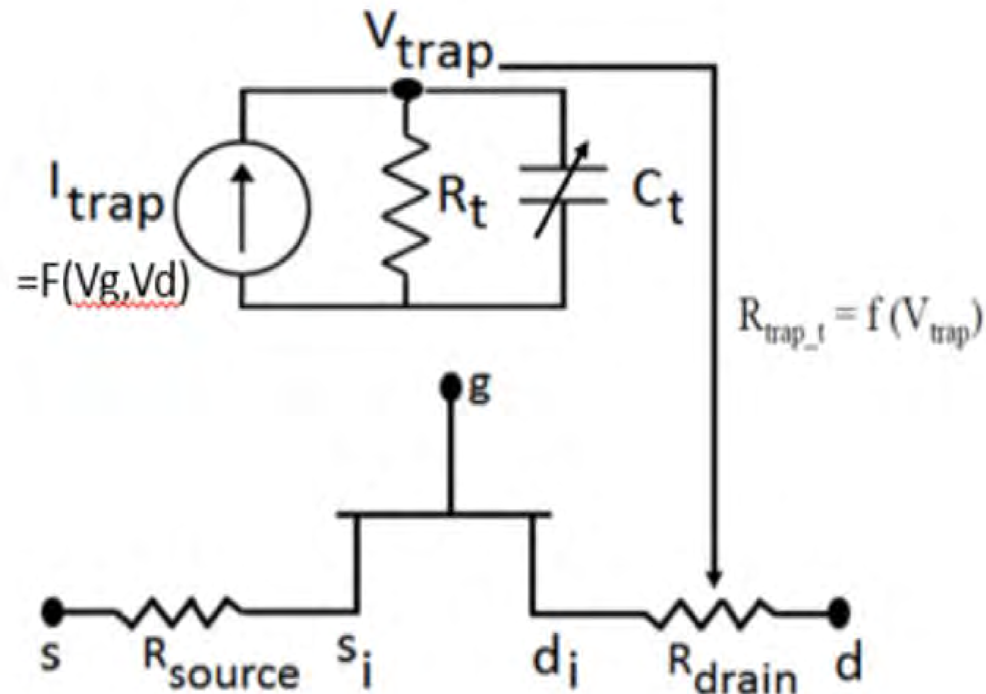
$$V_{OFF}(Trap) = V_{OFF} + (V_{OFFTR} \cdot V_{trap2})$$

$$\eta_0(Trap) = \eta_0 + (\eta_{0TR} \cdot V_{trap2})$$

$$C_{DSCD}(Trap) = C_{DSCD} + (C_{DSCDTR} \cdot V_{trap2})$$

$$R_{ds}(Trap) = R_{ds} - (R_{TR1} \cdot V_{trap1}) + (R_{TR2} \cdot V_{trap2})$$

# Trapping Models in ASM -HEMT: TRAPMOD III

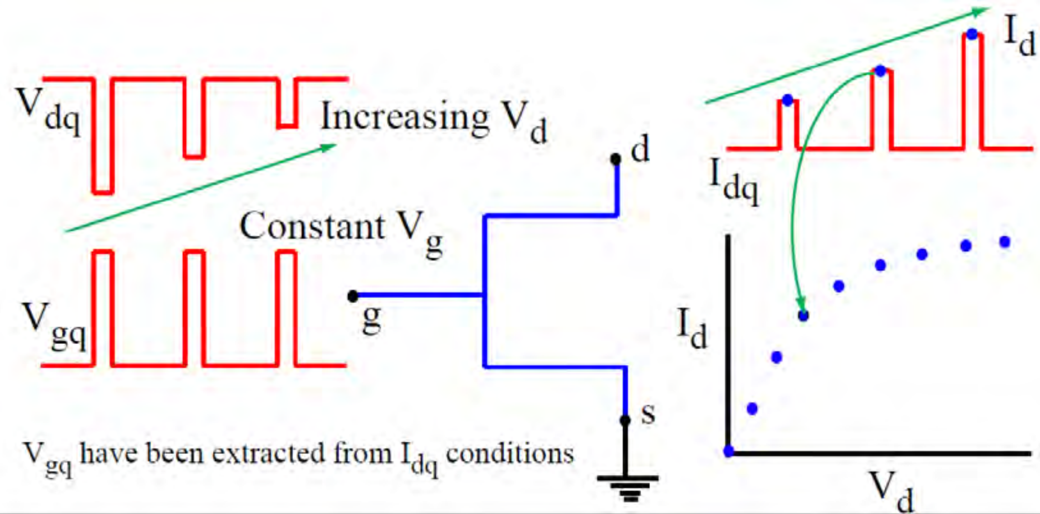



Key highlights

- Dependent on both gate and drain voltages
- Modulates just the drain side access region resistance for dynamic Ron
- Suitable for simulating Power Devices
- Incorporates temperature dependence.

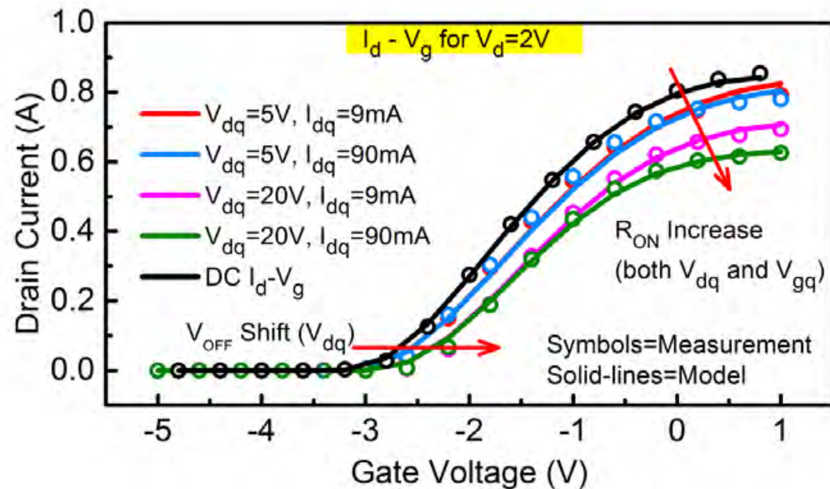
$$R_D(Trap) = R_D + \frac{V(trap1)}{VATRAP} \cdot \left(\frac{T_{dev}}{T_{NOM}}\right)^{TALPHA}$$

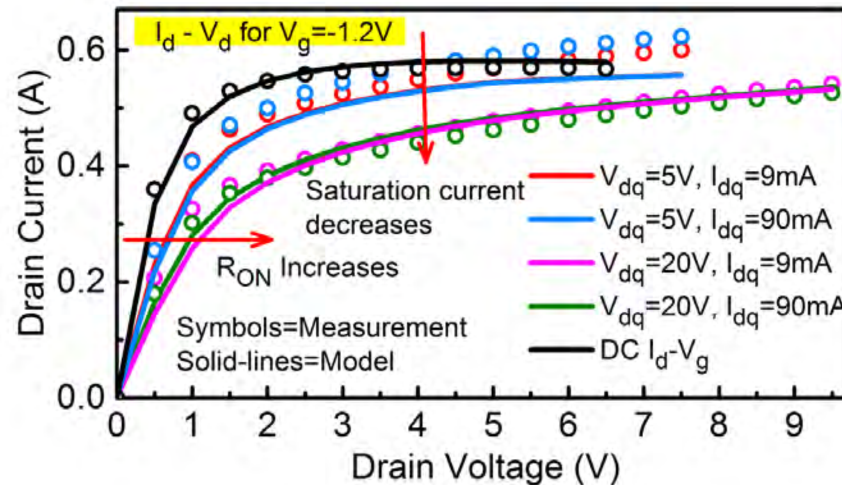
# Extraction using pulsed measurements




Pulsed-IV Scheme used to simulate the P-IV Characteristics

- Pulsed IV characterization in dual-pulse mode at a pulse frequency of 1000 Hz with a duty-cycle of 0.02 % is performed under multiple quiescent drain and gate bias conditions such that both the gate and the drain voltages are pulsed simultaneously from the quiescent bias point.
- The pulse width of 200 ns and the measurement window of 40 ns within these 200 ns is short enough to ensure iso-thermal and iso-dynamic measurement of the pulsed-IV characteristics.




Pulsed – IV chacteristics for multiple quiescent conditions – using TRAPMOD II

# Related Publications

# Publications

| | |
|---|---|
| 1 | S. Khandelwal, Y. S. Chauhan, T. A. Fjeldly, S. Ghosh, A. Pampori, D. Mahajan, R. Dangi, and S. A. Ahsan, "ASM GaN: Industry Standard Model for GaN RF and Power Devices - Part-I: DC, CV, and RF Model", IEEE Transactions on Electron Devices, 2019. |
| 2 | S. A. Albahrani, D. Mahajan, J. Hodges, Y. S. Chauhan, and S. Khandelwal, "ASM GaN: Industry Model for GaN RF and Power Devices - Part-II: Modeling of Charge Trapping", IEEE Transactions on Electron Devices, 2019. |
| 3 | A. Pampori, S. A. Ahsan, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "Physics-based Compact Modeling of MSM-2DEG GaN-based Varactors for THz Applications", IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Kobe, Japan, Mar. 2018. |
| 4 | S. A. Ahsan, A. Pampori, S. Ghosh, S. Khandelwal, and Y. S. Chauhan, "A New Small-signal Parameter Extraction Technique for large gate-periphery GaN HEMTs", IEEE Microwave and Wireless Components Letters, Vol. 27, Issue 10, Oct. 2017. |
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# Thank You!

*Questions*