Negative Capacitance MOSFETs for Future Technology Nodes

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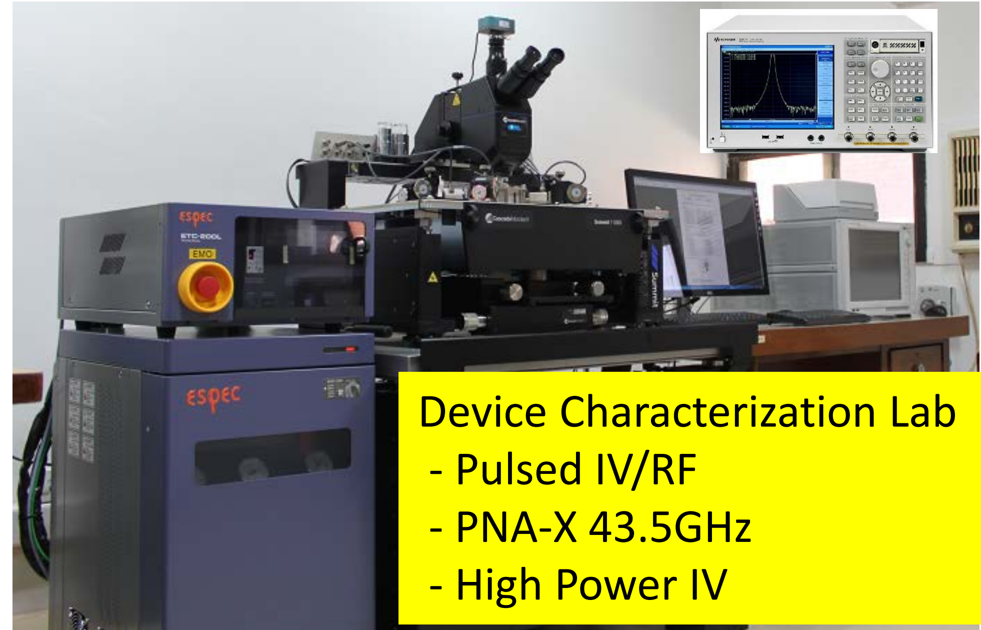
My Group and Nanolab

Current members – 30

- Postdoc – 5
- Ph.D. – 17
- Three PhD graduated
  - Postdocs in UC Berkeley and U. Bordeaux France

	2017	2016	2015	2014	2013	2012
Books	1		1			
Journal	20	18	9	5	3	3
Conference	8	30	30	8	4	6

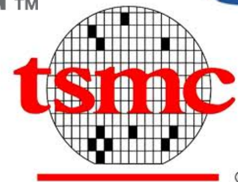


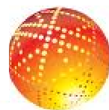
Joint Development & Collaboration

IIT Gandhinagar
Indian Institute of Technology Gandhinagar

UNIVERSITY OF SEOUL

Leading Innovation >>>





GLOBALFOUNDRIES®

ON Semiconductor®

Outline

- MOSFET and Scaling
- Negative Capacitance and Transistor
- Modeling of NC-FinFET
- Impact of Material Parameters
- Switching Delay and Energy
- Conclusion

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- MOSFET and Scaling
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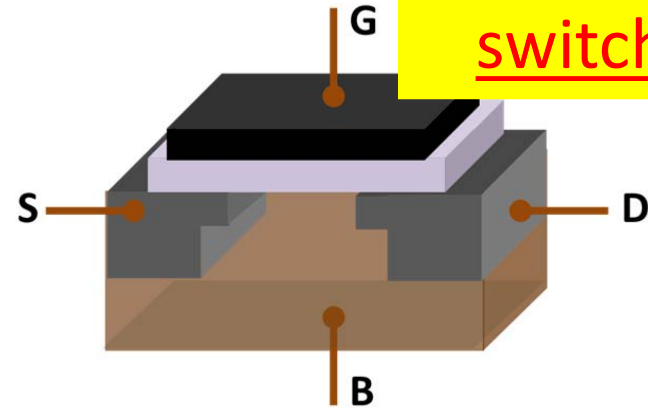
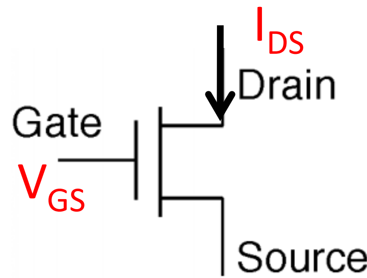
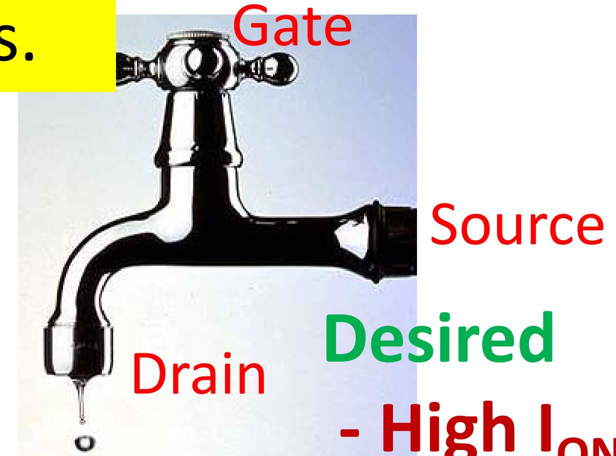
Transistor – The Driving Force

MOSFET is a transistor used for switching electronic signals.

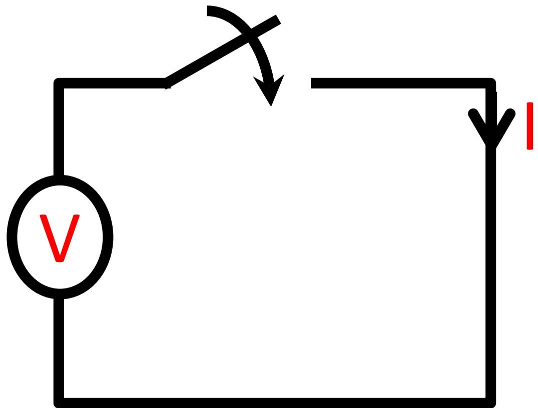


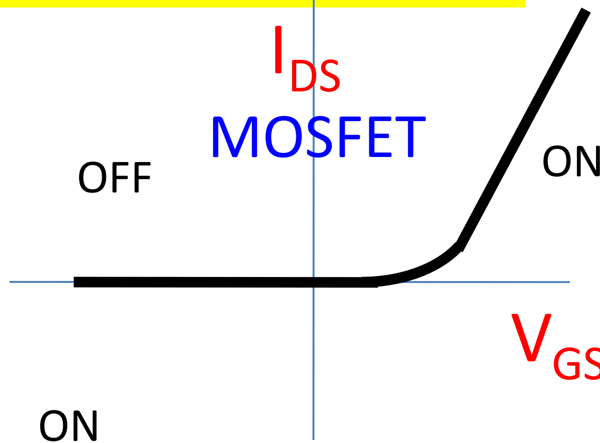


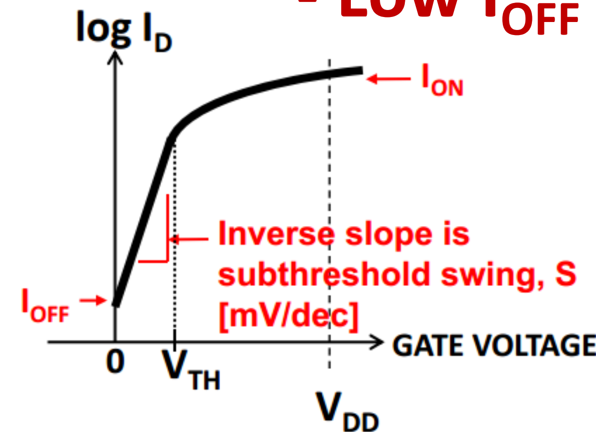


Desired
- High I_{ON}
- Low I_{OFF}

Switch vs. MOSFET



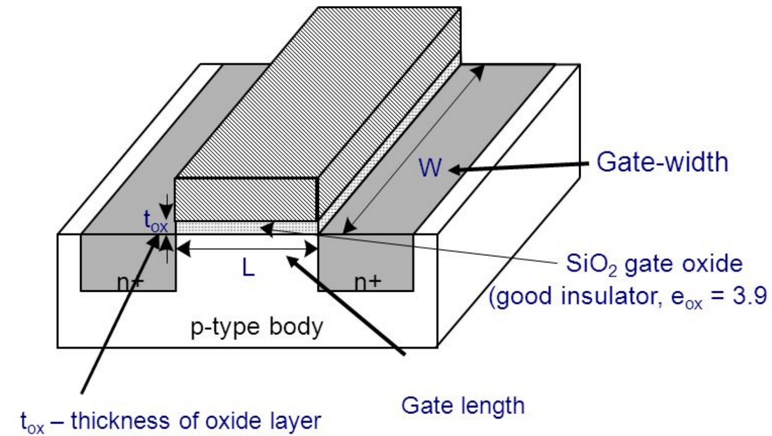




Bulk MOSFET

- Drain current in MOSFET (ON operation)

$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$



- Drain current in MOSFET (OFF operation)

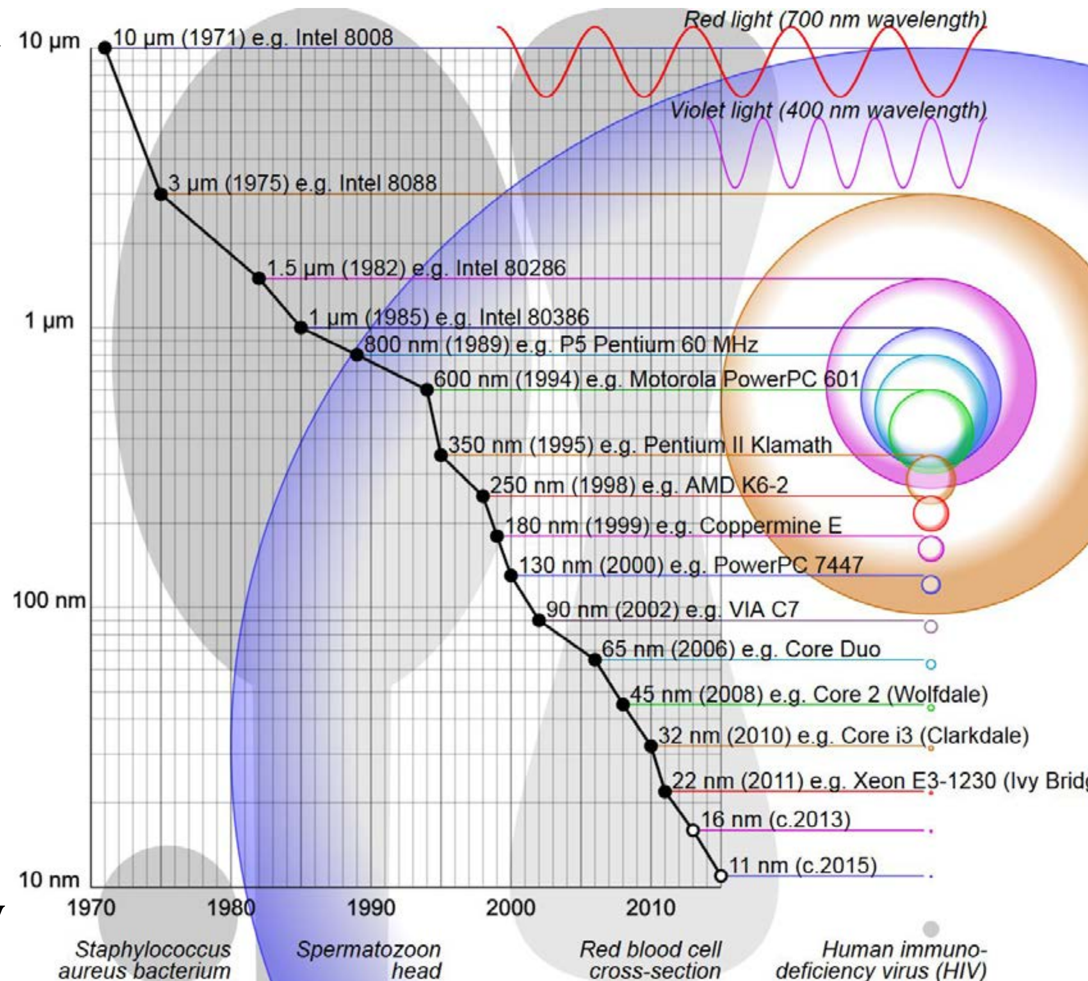
$$I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)}$$

$C_{ox}=\varepsilon_{ox}/t_{ox}$=oxide cap.
S – Subthreshold slope

- **High I_{ON} (↓L, ↑Cox, ↑V_{DD}-V_{TH})**
- **Low I_{OFF} (↑V_{TH}, ↑S)**

Technology Scaling

- Each time the minimum line width is reduced, we say that a new ***technology node*** is introduced.
- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.



Technology Scaling

- Scaling – At each new node, all geometrical features are reduced in size to 70% of the previous node.
- Reward – Reduction of *circuit size by half*. (~50% reduction in area, i.e., $0.7 \times 0.7 = 0.49$.)
  - Twice number of circuits on each wafer
  - Cost per circuit is reduced significantly.

- Ultimately – **Scaling drives down the cost of ICs.**

Scaling and Moore's Law

- Number of components per IC function will double every two years – April 19, 1965 (Electronics Magazine)
- Shorthand for rapid technological change!

Fig. 2 Number of components per Integrated function for minimum cost per component extrapolated vs time.

Microprocessor Transistor Counts 1971-2011 & Moore's Law

Still working!

Source: http://www.intel.com/pressroom/kits/events/moores_law_40th/

Moore's Law

It's not technology! → It's economy.

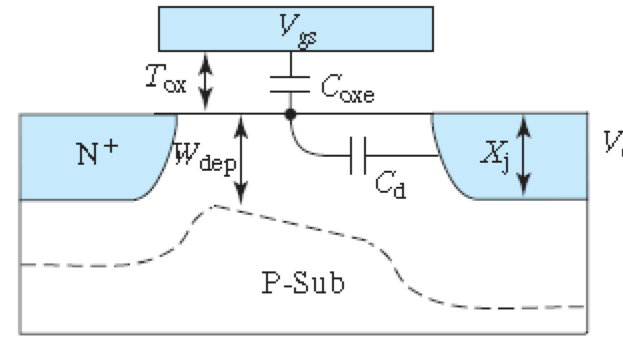
The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

t © 2005 Intel Corporation. All rights reserved.

In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore's Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.

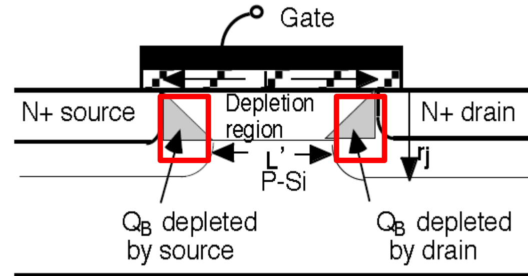
- Ways to Huge Profits
  - High performance and Low Cost
  - Achieved by making everything SMALLER

Scaling Overview

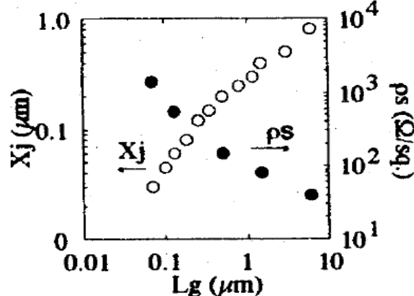


$I_d \propto \sqrt[3]{T_{oxe} W_{dep} X_j}$ *Scale l_d with L for better SCE*

A. Xj :Shallow junctions

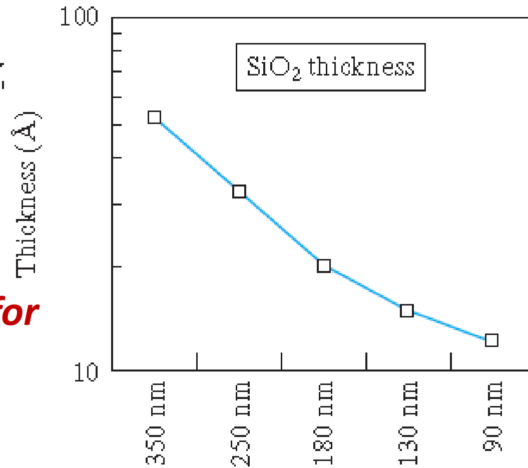


Channel encroachment proportional to X_j

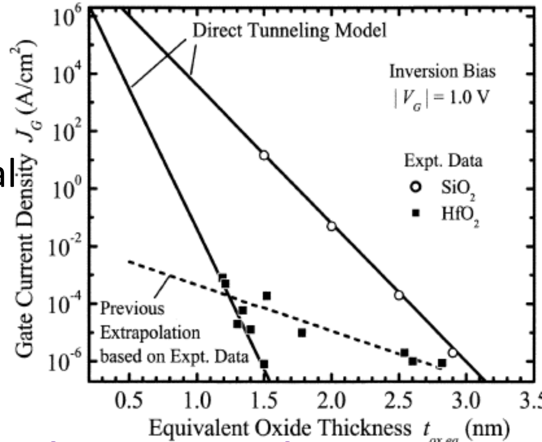


Ohguro, et al., *ULSI Science and Technology 1997*

B. Tox :Scale oxide thickness



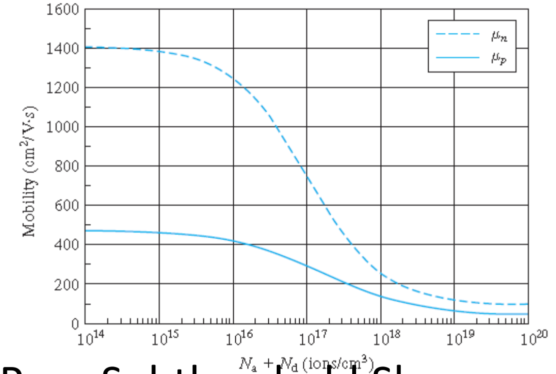
Gate current increases as T_{ox} is reduced



Yeo et.al, IEEE TED, Vol.50, 2003

C. Wdep: Increase doping

1. High scattering



2. Poor Subthreshold Slope

$$S = \frac{dV_{gs}}{d \log I_{ds}} \approx 2.3\, n\, v_t$$

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F + V'_{SB}}}$$ → High I_{OFF}

3. Large junction capacitance

Limit circuit speed

Other Issues

1- Random Dopant Fluctuation

2- Increased Effective T_{ox} (Quantum Mechanical Effect)

3- Polysilicon Gate Depletion

Tsividis, 3rd Edition, 2011

Scaling and Innovations

TABLE 7–1 • Scaling from 90 nm to 22 nm and innovations that enable the scaling.

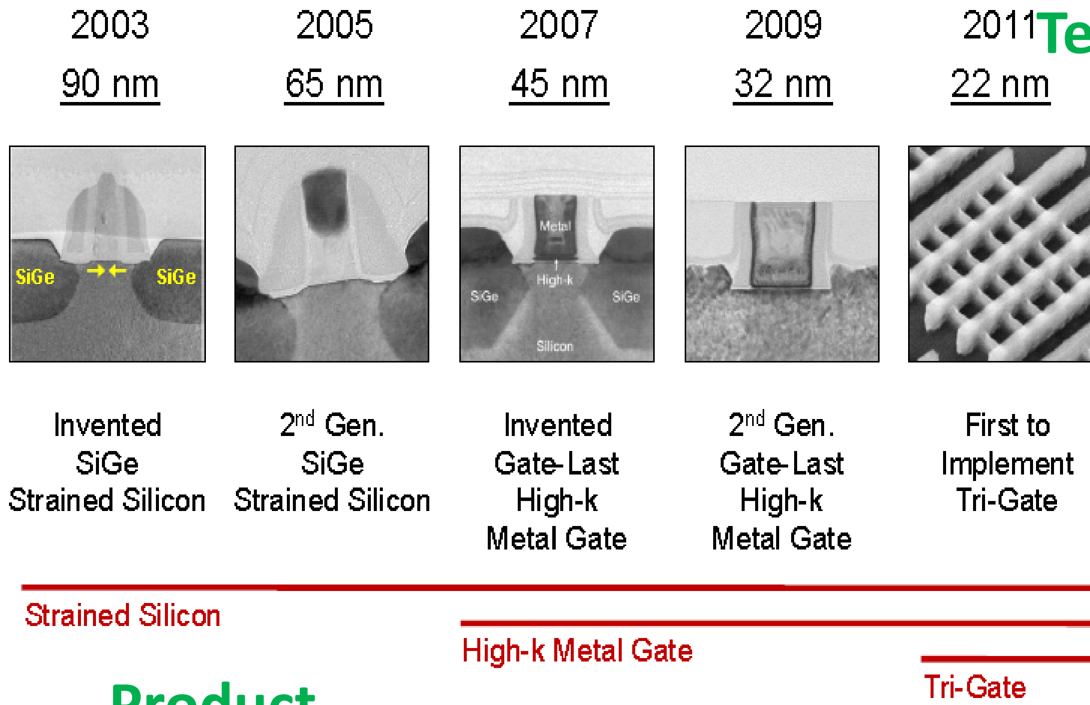
Year of Shipment	2003	2005	2007	2010	2013
Technology Node (nm)	90	65	45	32	22
L_g (nm) (HP/LSTP)	37/65	26/45	22/37	16/25	13/20
EOT_e(nm) (HP/LSTP)	1.9/2.8	1.8/2.5	1.2/1.9	0.9/1.6	0.9/1.4
V_{DD} (V) (HP/LSTP)	1.2/1.2	1.1/1.1	1.0/1.1	1.0/1.0	0.9/0.9
I_{on}, HP (μA/μm)	1100	1210	1500	1820	2200
I_{off}, HP (μA/μm)	0.15	0.34	0.61	0.84	0.37
I_{on}, LSTP (μA/μm)	440	465	540	540	540
I_{off}, LSTP (μA/μm)	1E-5	1E-5	3E-5	3E-5	2E-5
Innovations	→ Strained Silicon		→ High-*k*/metal-gate	→ Wet lithography	→ New Structure

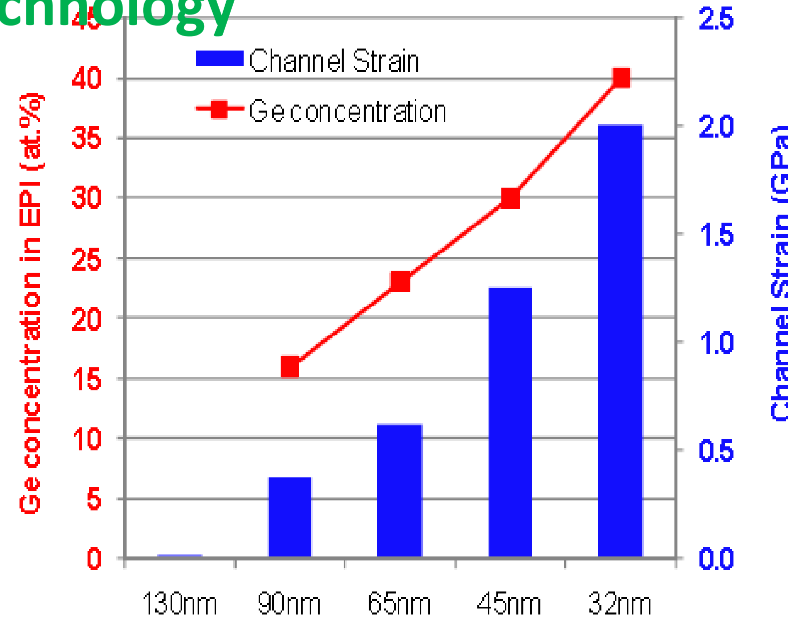
HP: High-Performance technology. LSTP: Low Standby Power technology for portable applications.
EOT_e: Equivalent electrical Oxide Thickness, i.e., equivalent T_{oxe}. I_{on}: NFET I_{on}.

- Scaling For : Cost, Speed and Power
- New technology node every two year
- **Channel length reduction ~30%**
- **Area reduction ~50%**

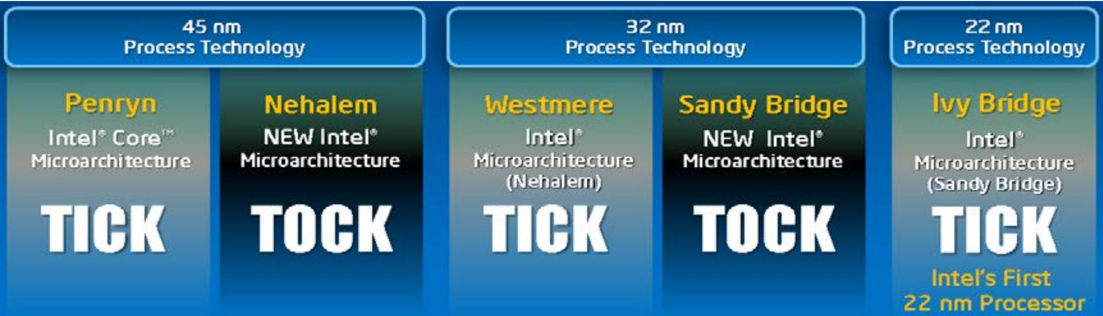
C. Hu, Modern Semiconductor Devices for ICs

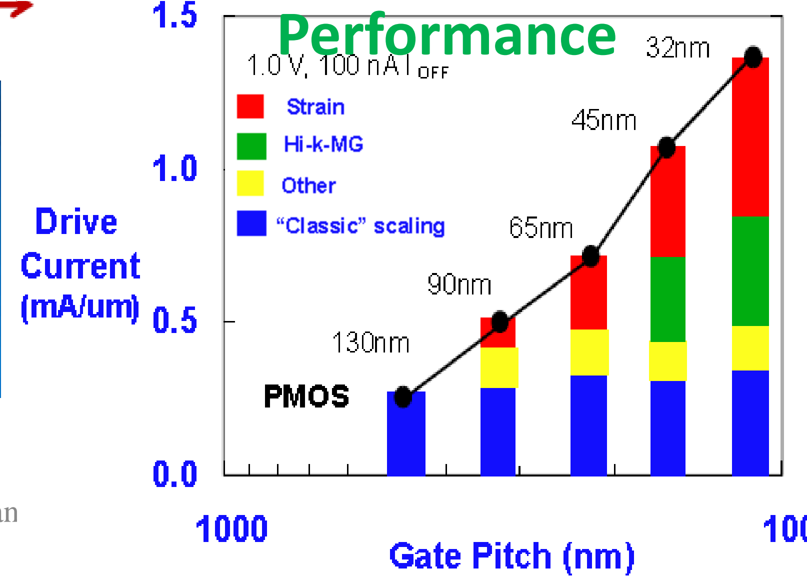
Technology Trend





Product





Source : www.intel.com

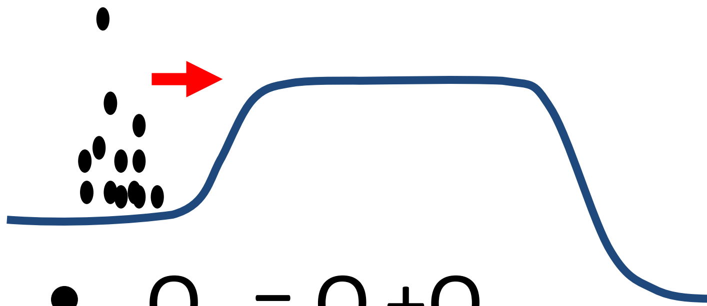
Scaling Issues/Challenges

- V_{TH} not following scaling
- Current Scaling
  - Mobility is not constant
  - Velocity Saturation
  - Higher I_{off}
- Parasitic resistance and capacitance don’t scale linearly
- Process variations
- Affordable Litography
- Heat dissipation and Cooling

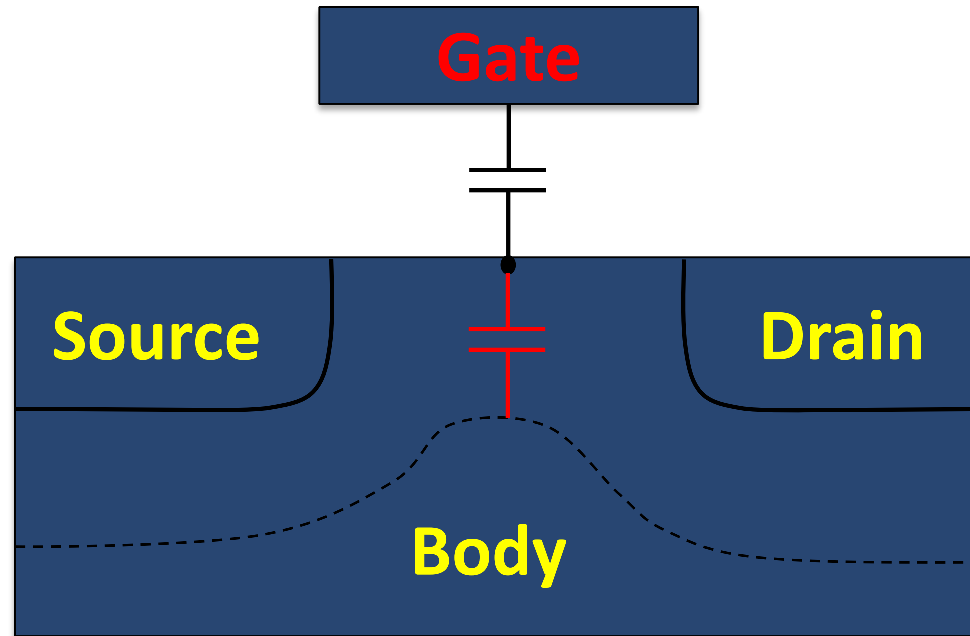
IC industry for >40 years

- Closer distance between elements – *Pitch*
  - *Faster* signal transfer and processing rate
- For the same Chip size (or cost), *more functionality*
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - *Price* of memory/logic gates has dropped 100 million times.
- Miniaturization is key to the improvements in *speed and power consumption* of ICs.

Why divorce after 40 years?

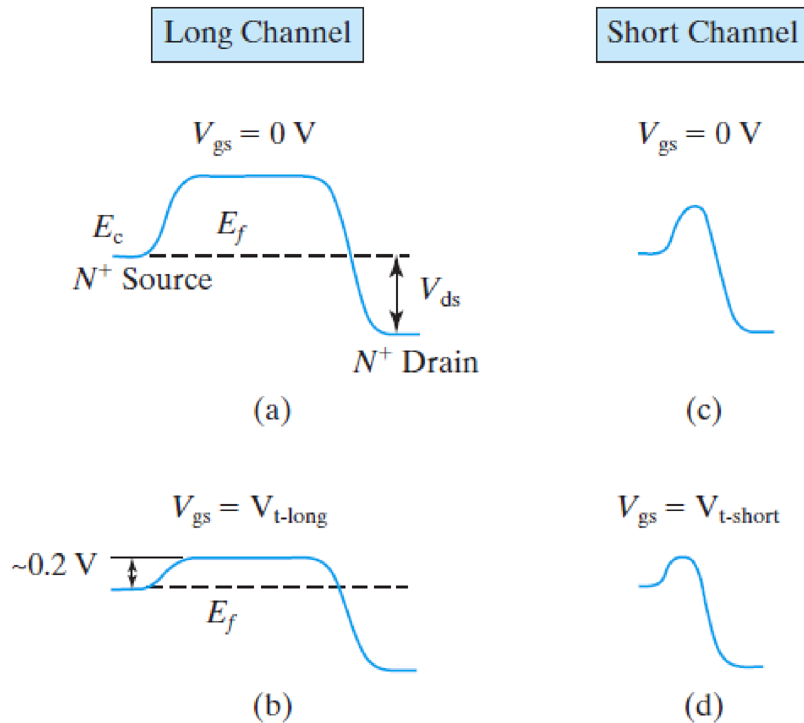


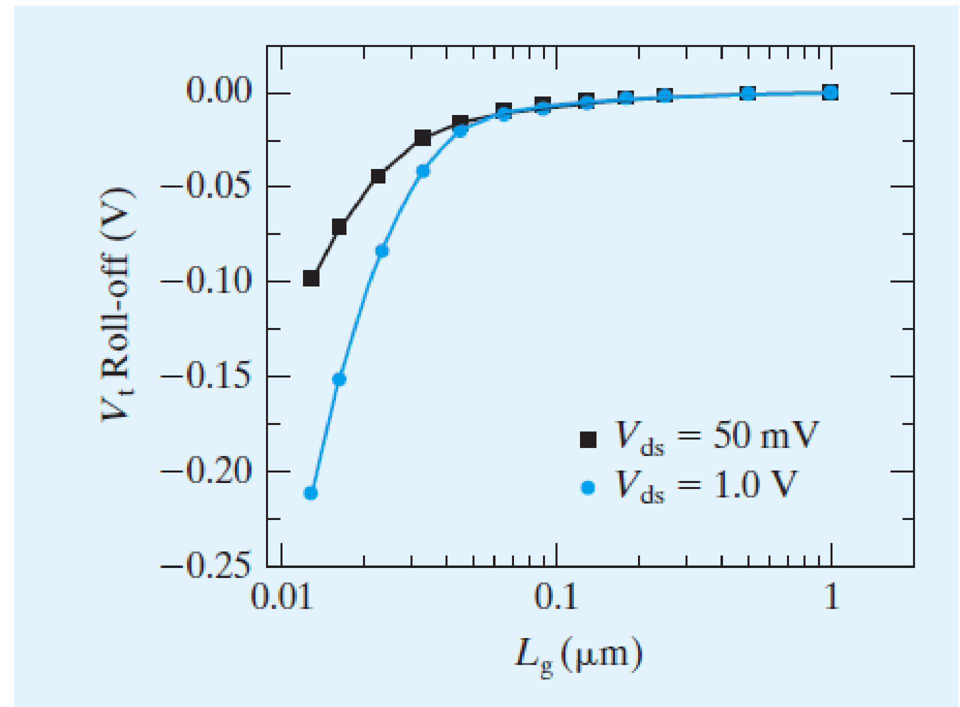
- $Q_G = Q_i + Q_b$
- Charge sharing



Courtesy: Chenming Hu

Threshold Voltage Roll-Off



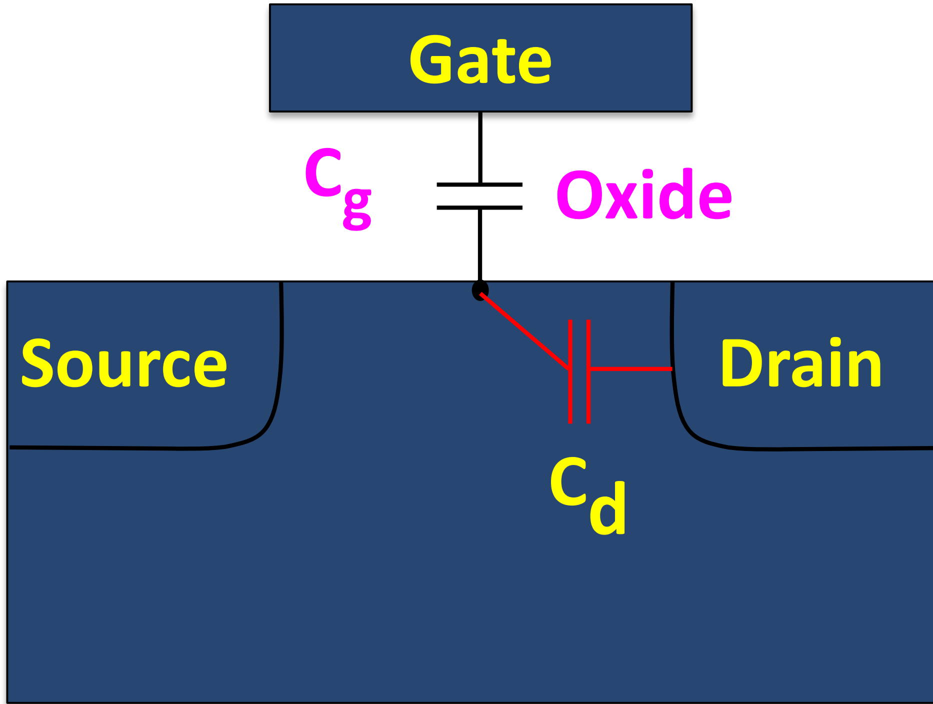


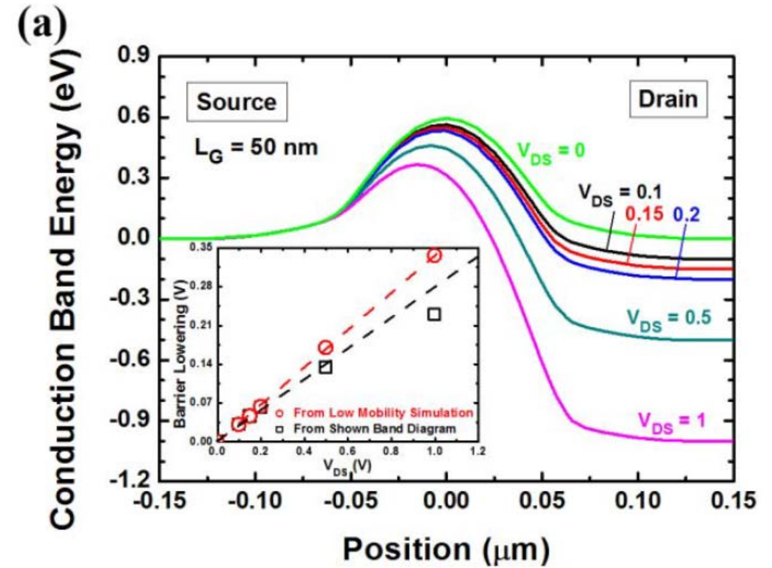
Energy band diagram from source to drain when Vgs=0V and Vgs=Vt.
A-b long channel; c-d short channel.

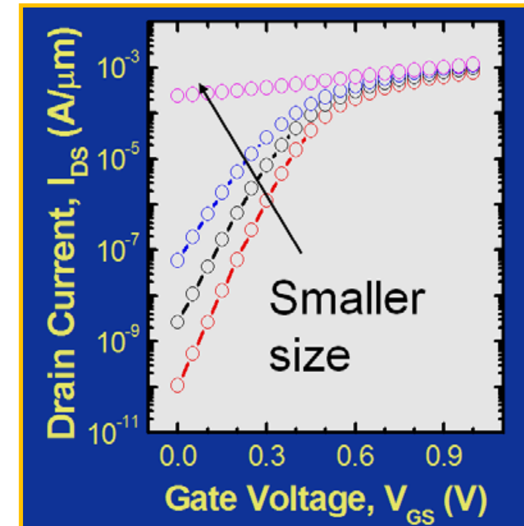
Vt decreases at very small Lg. It determines the minimum acceptable Lg because Ioff is too large when Vt becomes too low or too sensitive to Lg.

Ref. – Modern Semiconductor Devices for Integrated Circuits by Chenming C. Hu

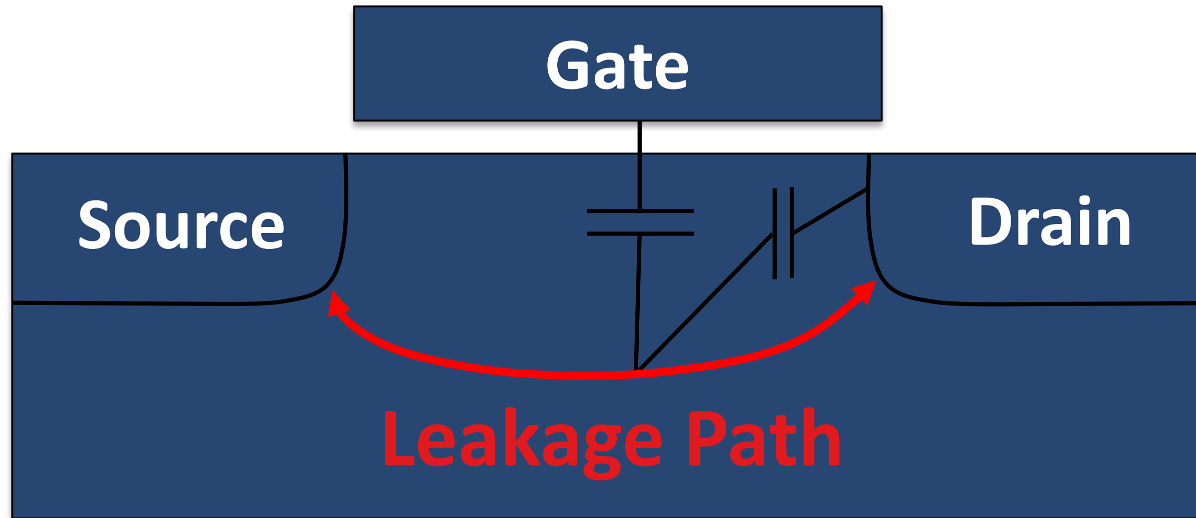
Short Channel Effects





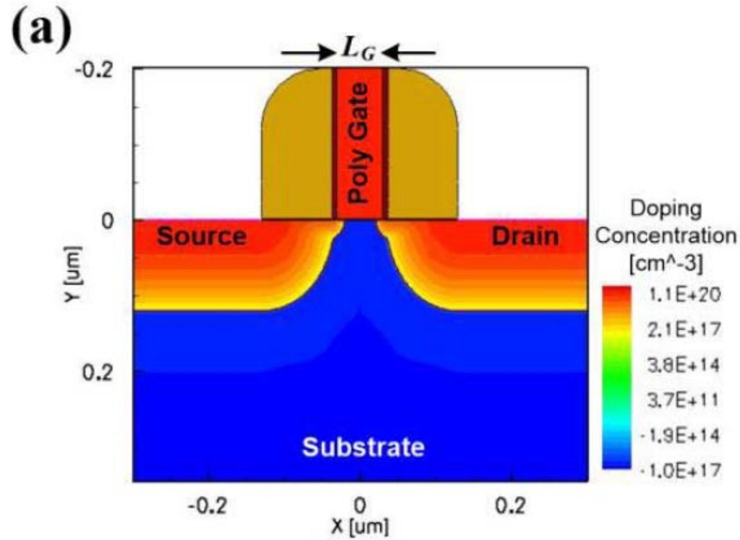


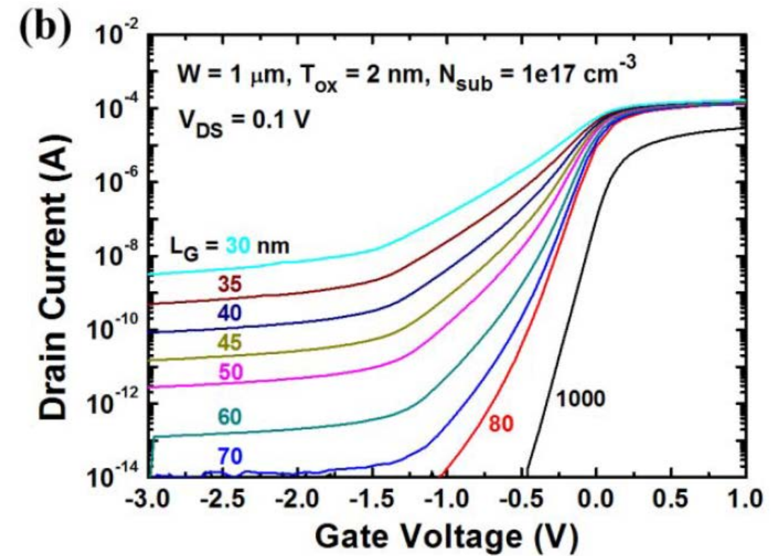
Making Oxide Thin is Not Enough

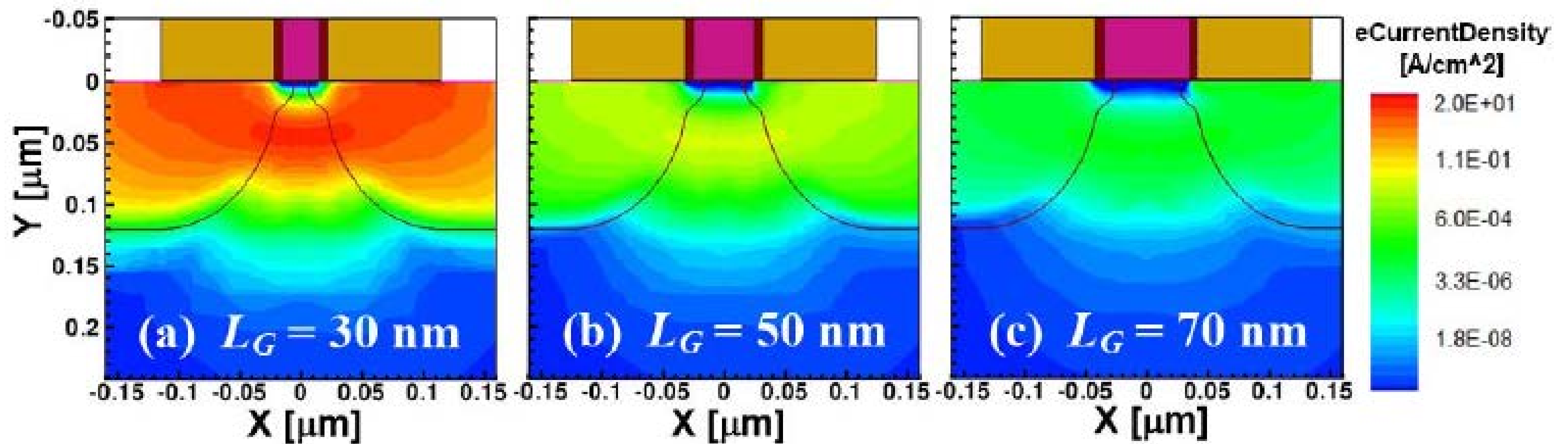


Gate cannot control the leakage current paths that are far from the gate.

Leakage current in MOSFET







Ref. – Y.-K. Lin et. al., "Modeling of Subsurface Leakage Current in Low VTH Short Channel MOSFET at Accumulation Bias", IEEE TED 2016.

MOSFET in sub-22nm era

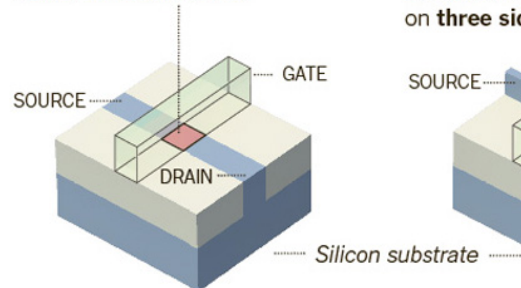
FinFET

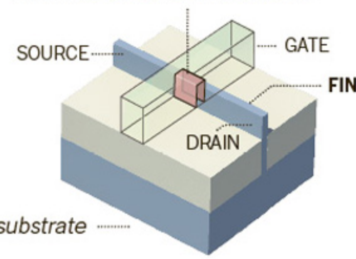
New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

TRADITIONAL TRANSISTOR
Planar **conductive area**

NEW INTEL TRANSISTOR
Conductive area is expanded on **three sides of a raised fin**

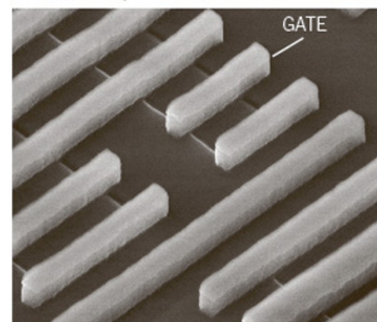




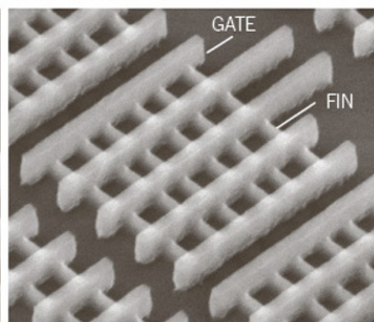
Silicon substrate

The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

Traditional planar transistor



Intel Tri-Gate transistor



Source: Intel

THE NEW YORK TIMES

NY Times

FDSOI

Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices

New platform enables planar FD technology, the only planar solution to sustain Moore's law

From the Semicon West trade show, San Francisco, July 12, 2010 – The Soitec Group (Euronext Paris), the world's leading supplier of engineered substrates for the microelectronics industry, announced today that the company is ready with the Ultra-Thin Buried Oxide (UTBOX) extension to its Ultra-Thin (UT) silicon-on-insulator (SOI) platform, thereby providing a robust substrate solution for chip designers tackling the performance, power and density challenges of mobile consumer devices. Fully Depleted (FD) planar body transistors are now recognized as the right path on the CMOS roadmap for the 22nm generation and beyond. With FD planar transistor technology on UTBOX wafers, chip designers can enhance their usual design flows and techniques. High-volume capacity is available for the 22nm node at Soitec's manufacturing sites in France and Singapore.

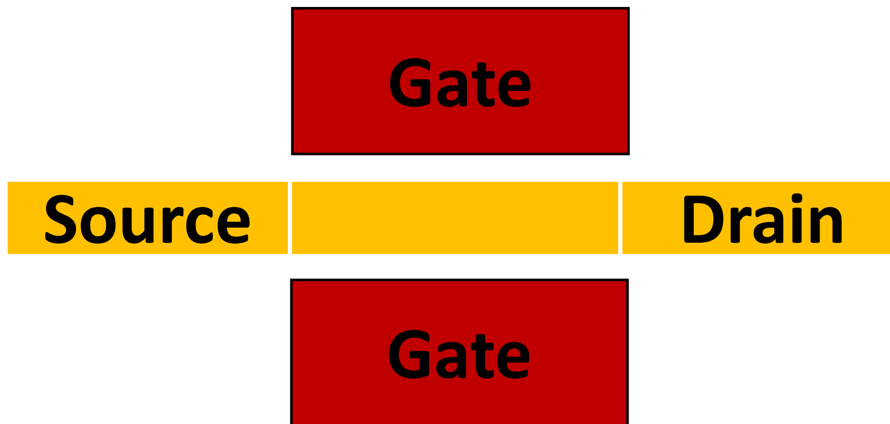
"Soitec is ready with the UTBOX wafers for planar FD architectures: the infrastructure, the process maturity, yield and the capacity are all in place to support demand," said Soitec president and chairman, André-Jacques Auberton-Hervé. "Industry leaders confirm that FD planar technology is the right choice for mobile consumer products, which need higher performance without compromising power. Our UTBOX offering shows the critical role our materials play as the starting point for energy-efficient, state-of-the-art electronics."

SOITEC

Eliminate Si Far from Gate

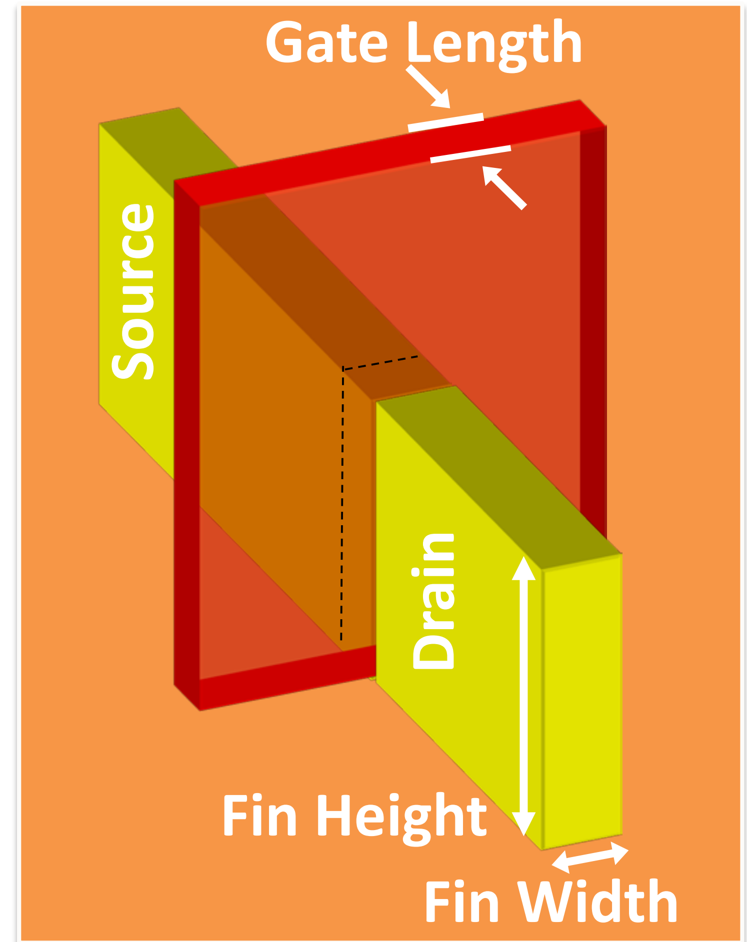
Thin body controlled

By multiple gates.



FinFET body

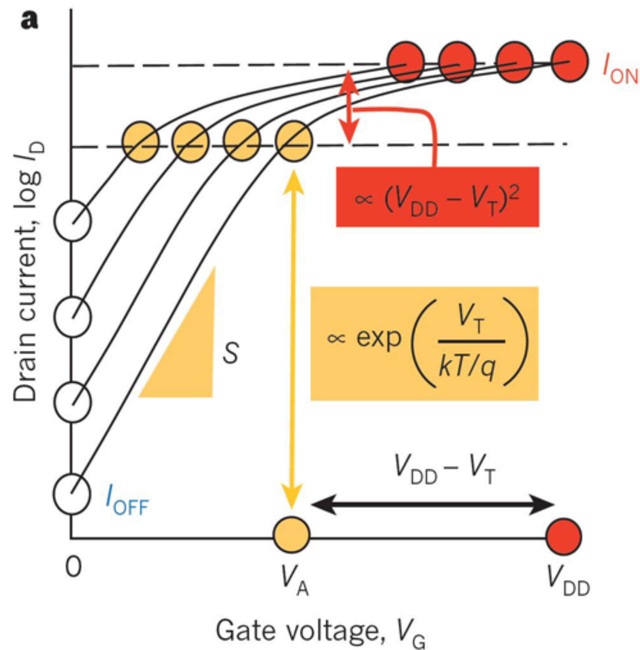
is a thin Fin.



N. Lindert et al., DRC paper II.A.6, 2001

Challenges & Solutions

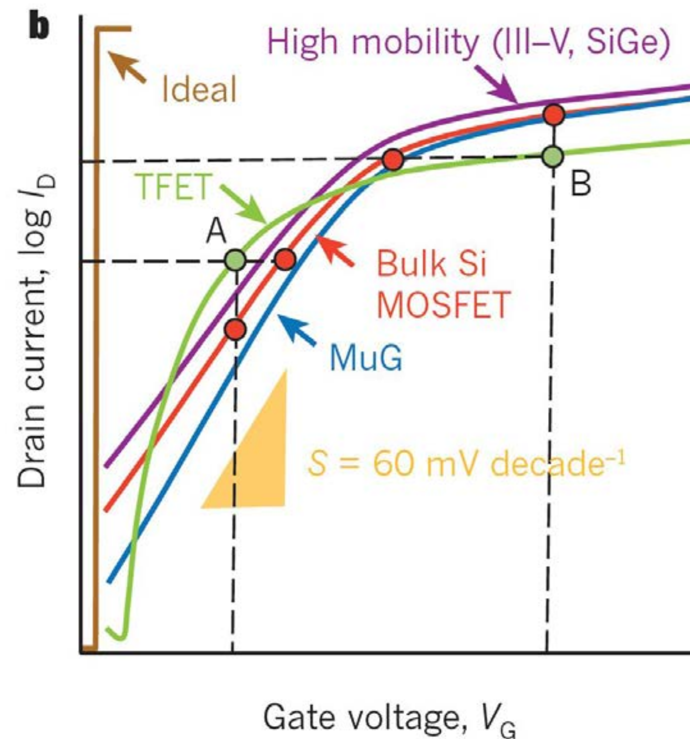
Power challenge



Scaling both the V_{DD} and V_T maintains same performance (I_{ON}) by keeping the overdrive (V_{DD} - V_T) constant.

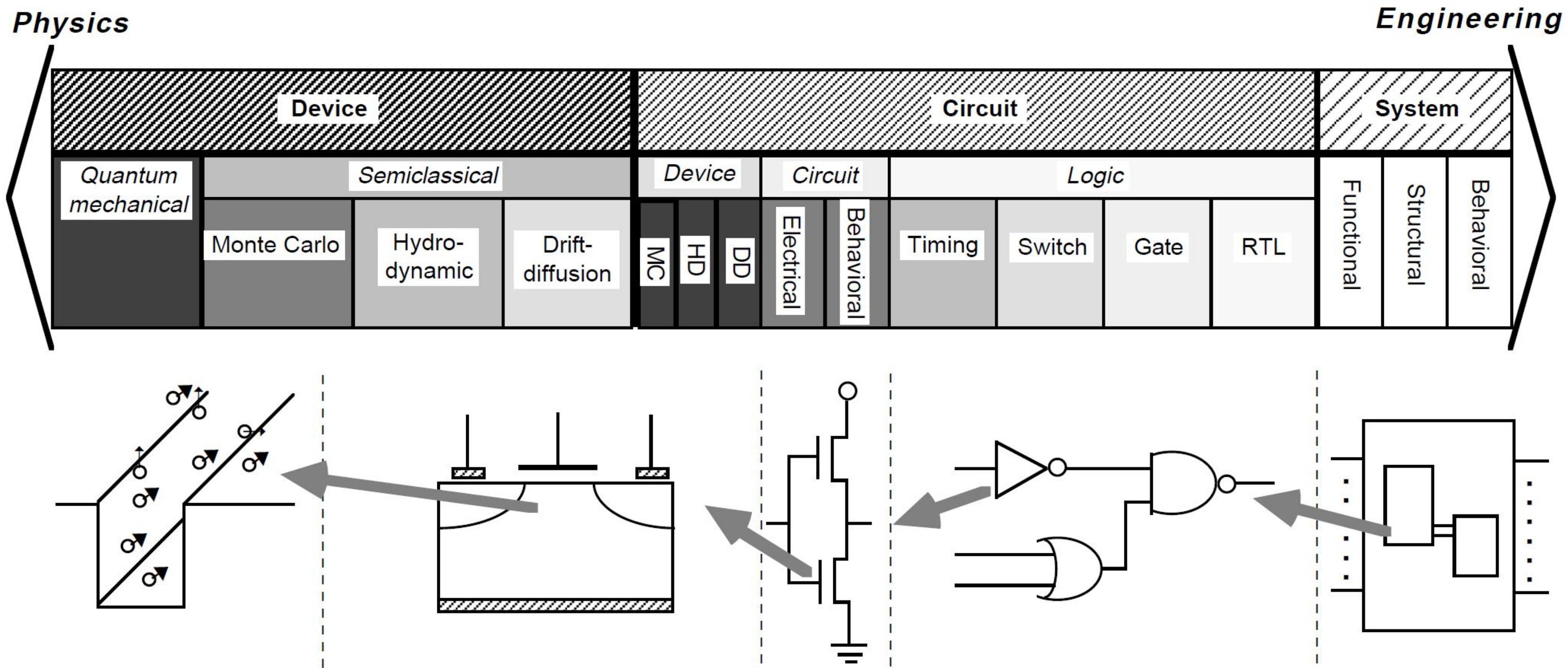
$$I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$$

$$I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)}$$

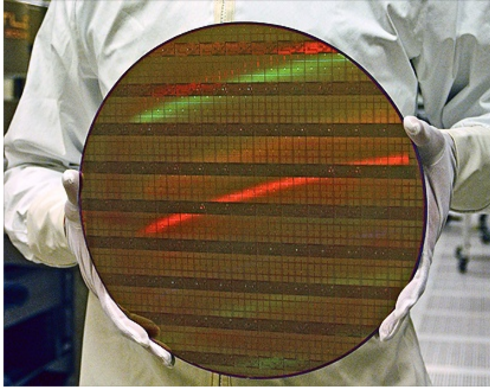


Adrian Ionescu et al., Nature 2011

Spectrum of Approaches to Analyzing Electronic System



Compact Modeling or SPICE Modeling

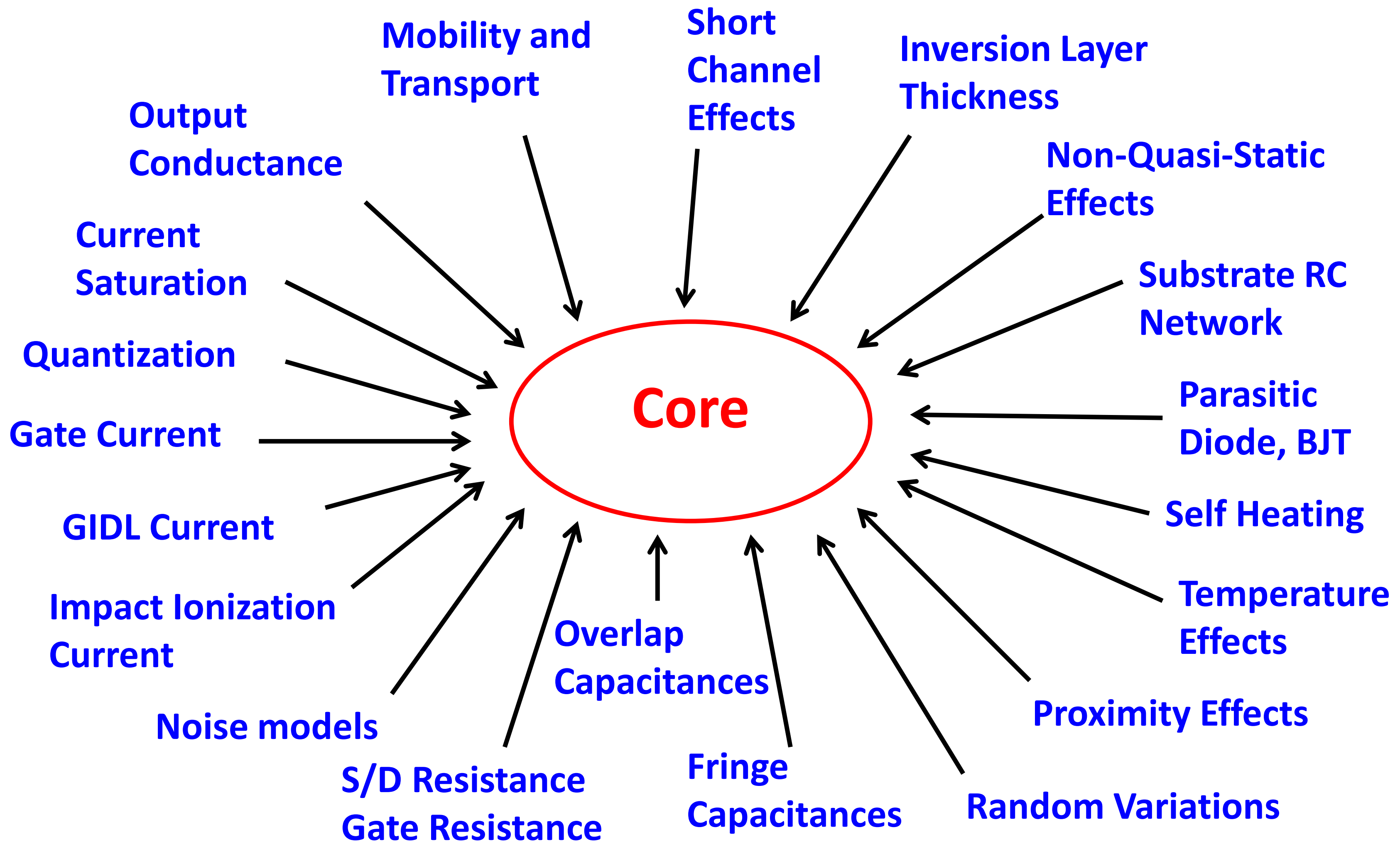


Medium of information exchange

- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Easy Parameter extraction.
- Balance between accuracy and simplicity depends on end application

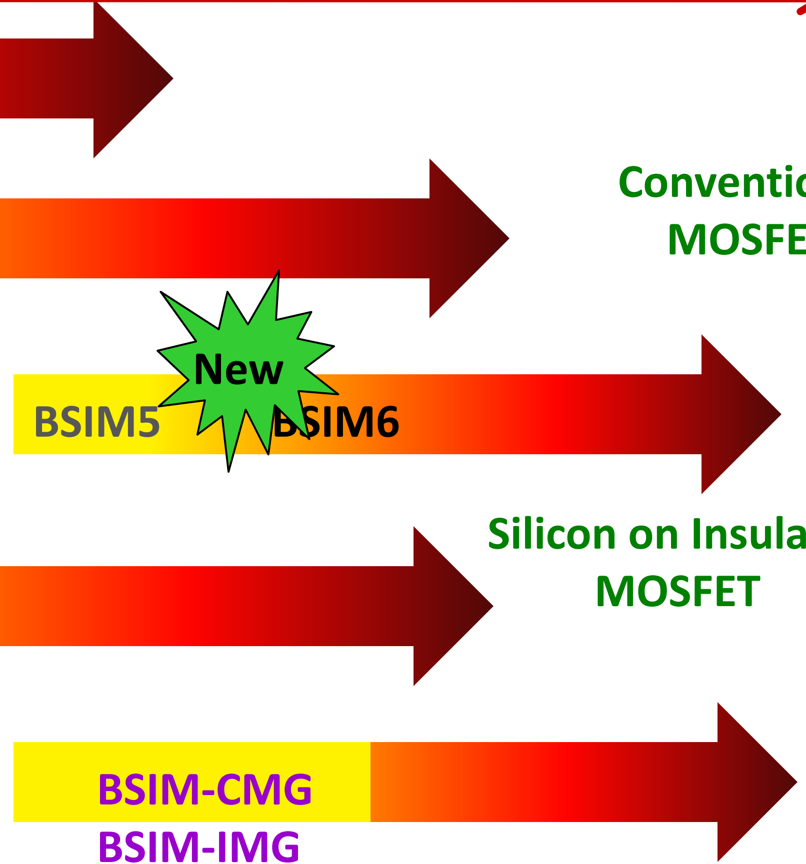
- Excellent Convergence
- Simulation Time – ~µ*sec*
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

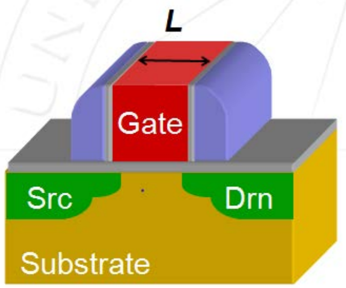
Compact Model is Art Based on Science

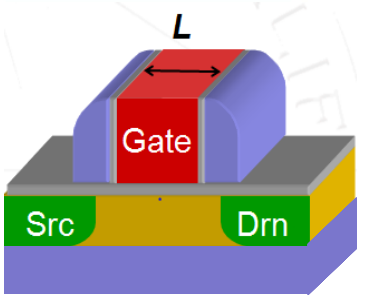


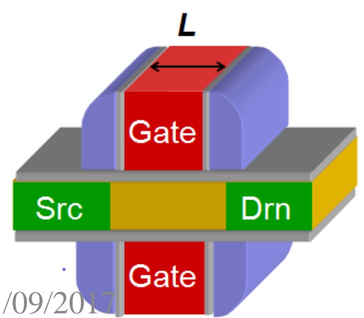
Y. S. Chauhan et.al., "BSIM6: Analog and RF Compact Model for Bulk MOSFET," IEEE TED, 2014.

BSIM Family of Compact Device Models









BSIM: Berkeley Short-channel IGFET Model

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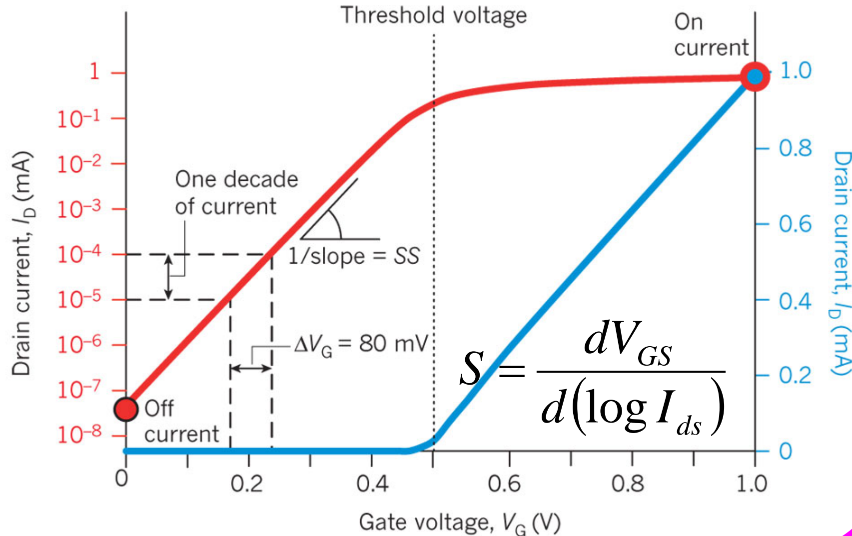
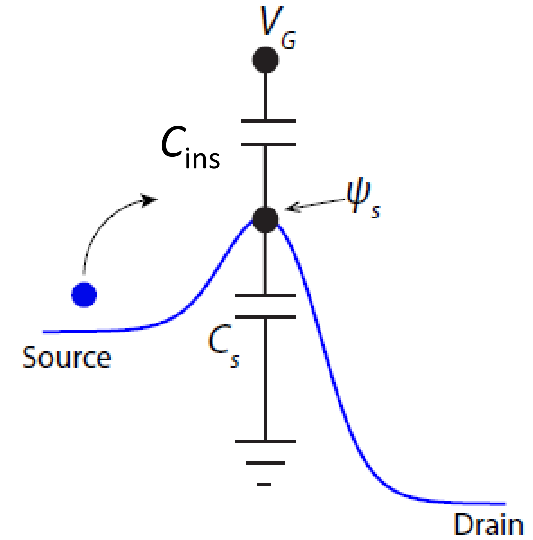
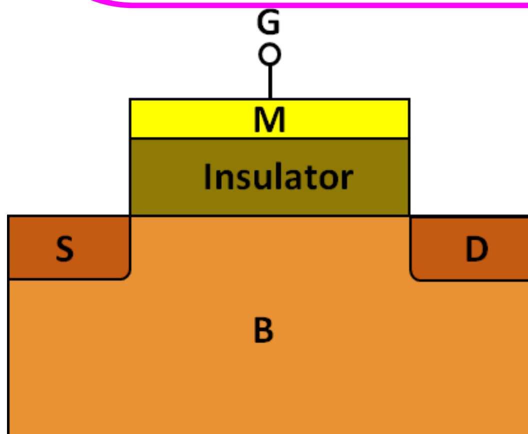
- Conclusion

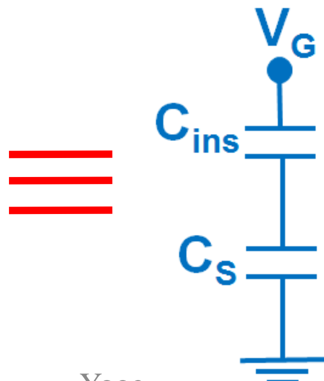
Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.









$$S = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial V_G}{\partial \psi_S} \frac{\partial \psi_S}{\partial \log_{10} I_D}$$

$$= \left(1 + \frac{C_S}{C_{ins}}\right).60\text{mV/decade}$$

As $1 + \frac{C_S}{C_{ins}} \geq 1, S \geq 60mV/decade$

Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as

- Definition 1: $C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1}$ = inverse curvature of free energy density
- Definition 2: $C_{ins} = \frac{\partial P}{\partial E}$ = slope of the polarization vs electric field curve

where P = Polarization in dielectric, G = Free energy density and
E = Externally applied electric field

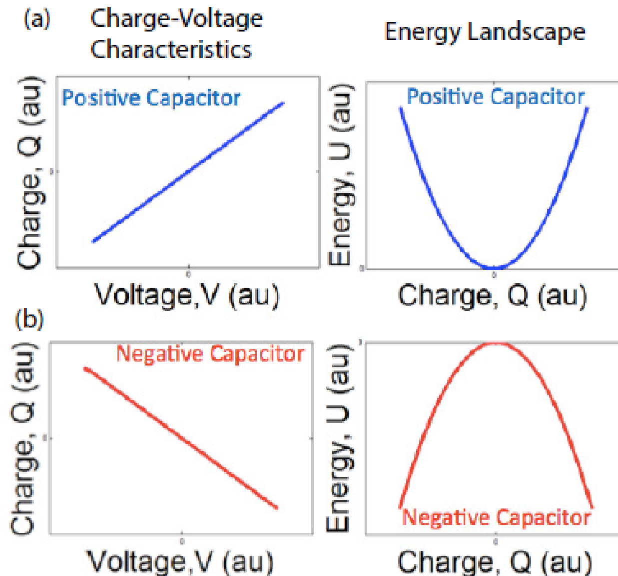
- Two types of non-linear dielectrics:
  - Paraelectric : No polarization when electric field is removed.
  - Ferroelectric : Two possible states of polarization when electric field is removed.

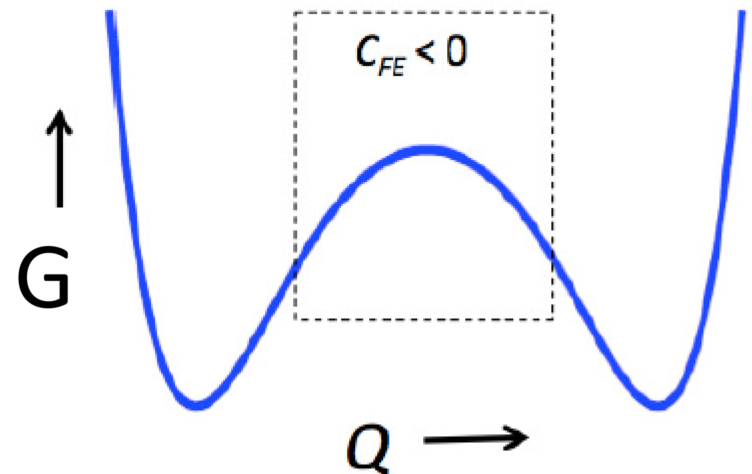
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!

  $C_{ins} < 0$ and $\frac{C_S}{C_{ins}} < 0$, then $\left(1 + \frac{C_S}{C_{ins}}\right) < 1 \rightarrow S < 60\text{mV/decade}$

- For a linear capacitor
  - Energy $G = \frac{Q^2}{2C} \rightarrow$ Capacitance $C = {}^{1}\!\Big/\!{}_{\frac{d^2G}{dQ^2}} = 1/Curvature$
  - The same holds also for a non-linear capacitor.





Energy landscape of ferroelectric materials.

$Q = \epsilon E + P \cong P$

Ref. – S. Salahuddin et. al., *Nano Letters*, 2008.

Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

- In general, α and β can be +ve or –ve but γ is always +ve for stability reasons.
- Dynamics of G is given by $\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$

δ = Polarization damping factor

- In the steady state, $\frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

For $\alpha > 0$ and at $E = 0$, there exit only one real root

$P = 0$

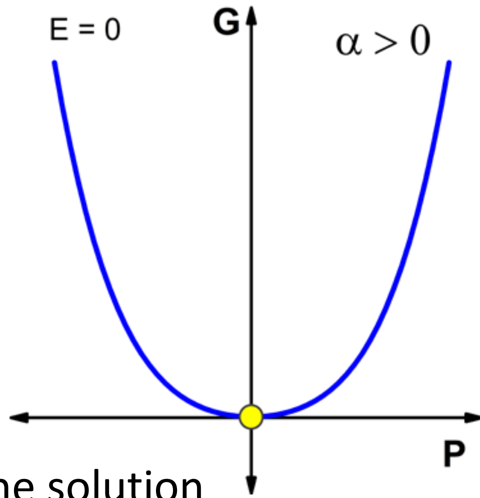
A Paraelectric Material

For $\alpha < 0$ and at $E = 0$, there exit three real roots

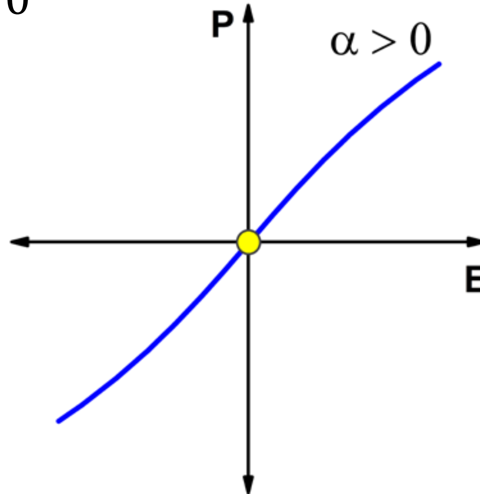
$P = 0, \pm P_r$ where $P_r = \sqrt{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$

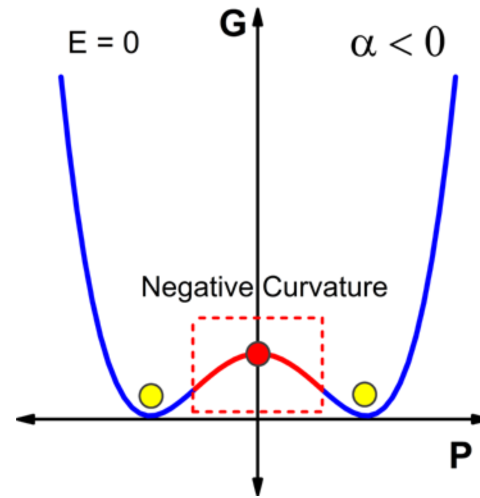
A Ferroelectric Material has a non-zero P at zero E.

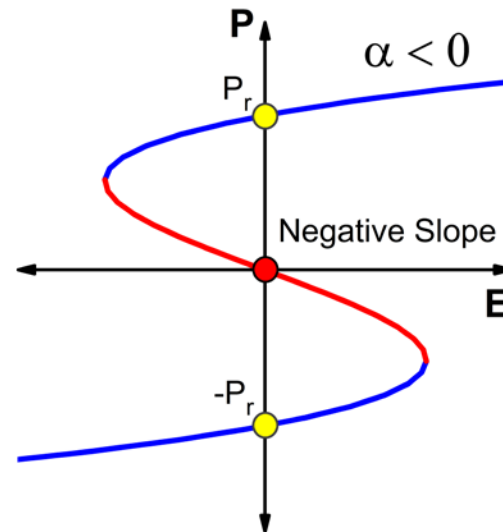
Positive and Negative Capacitances



Only one solution at $E = 0$







Three possible solutions at $E = 0$

$P = 0$ is not possible in a isolated Ferroelectric due to maxima of energy or a negative capacitance

$$C_{ins} = \left(\frac{\partial^2 G}{\partial P^2}\right)^{-1} = \frac{\partial P}{\partial E} < 0$$

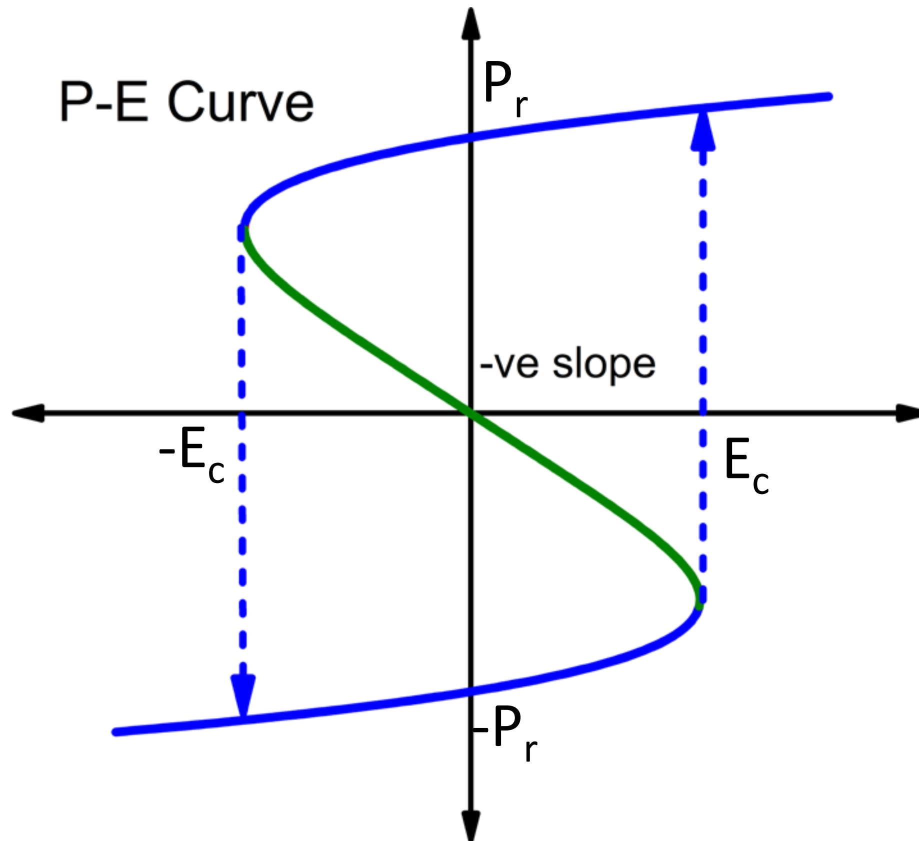
Paraelectric

A Positive Capacitor

Ferroelectric

A Conditionally Negative Capacitor

Negative Capacitance in Ferroelectric



$$C_{ins} = C_{fe}$$

-ve slope region can be stabilized if

$$C_{GG} = \left(\frac{1}{-|C_{fe}|} + \frac{1}{C_S}\right)^{-1} > 0$$

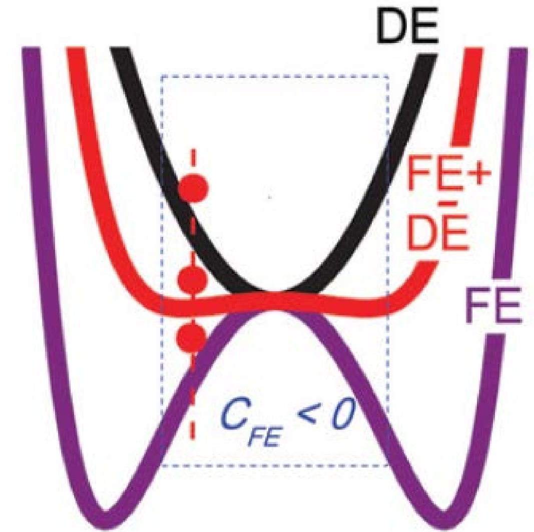
or,

$$|C_{fe}| > C_S$$

S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008.

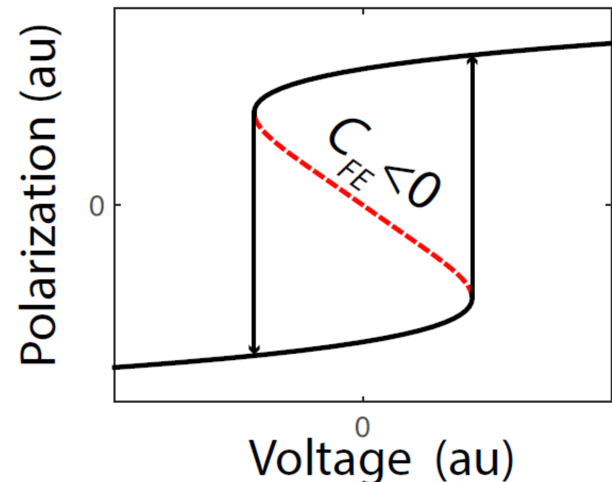
How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

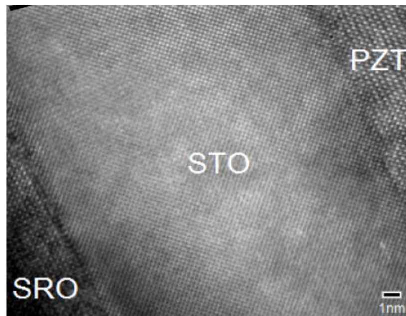


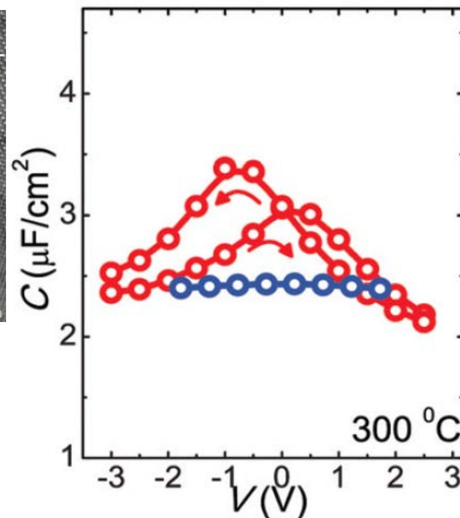
A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011

- $\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0$
- $C_{DE} < |C_{FE}|$ and $C_{FE} < 0$
- $C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0$

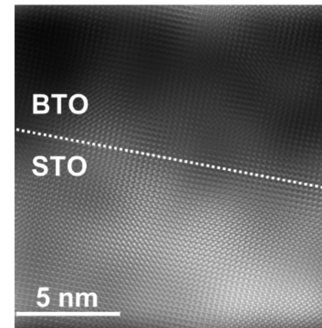


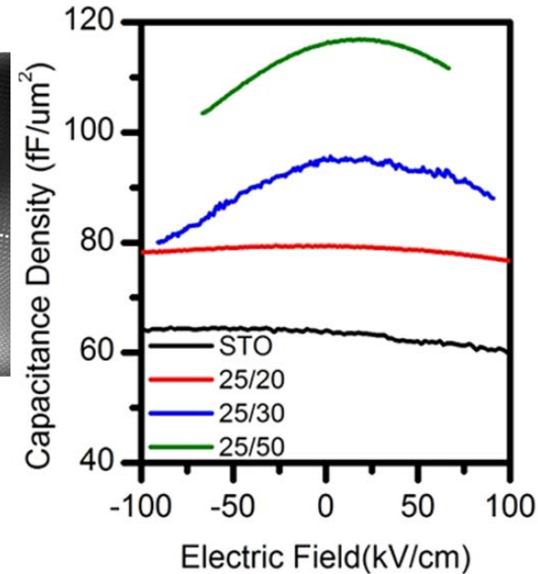
Ferroelectric-Dielectric Systems





A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011.





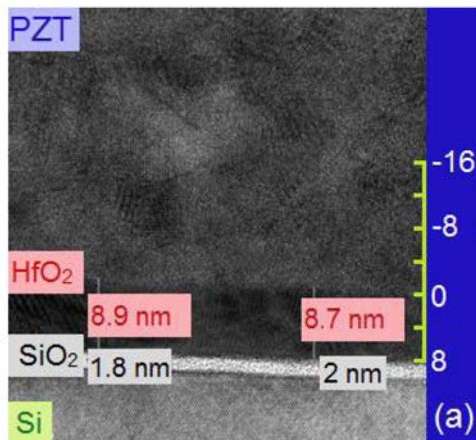
D. J. Appleby et al., Nano Letters, vol. 14, no.7, pp. 3864–3868, 2014.

Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.

$$C_{tot} = \frac{C_{DE}.|C_{FE}|}{|C_{FE}| - C_{DE}} > 0$$

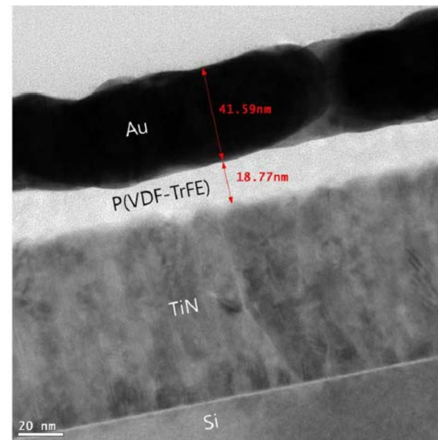
Negative Capacitance FETs

$PbZr_{0.52}Ti_{0.48}O3$ FE with HfO_2 buffer interlayer



S. Dasgupta et al., IEEE JESCDC, 2015.

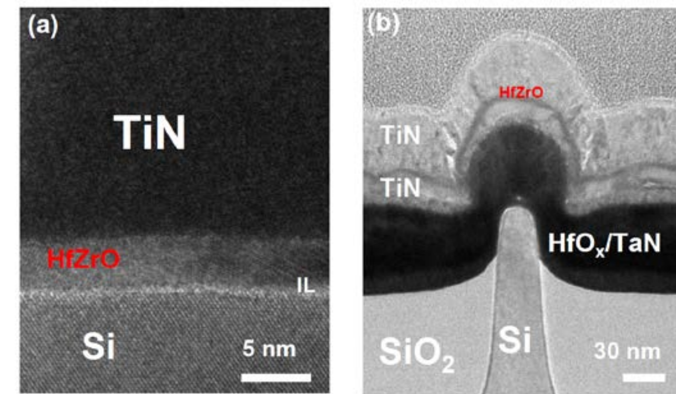
$P(VDF_{0.75}\text{-}TrFE_{0.25})$ Organic Polymer FE



J. Jo et al., Nano Letters, 2015

HfZrO FE

CMOS compatible FE



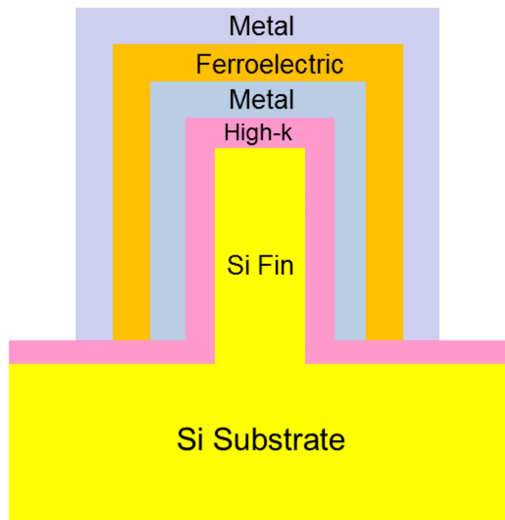
K.-S. Li et al., in IEEE IEDM, 2015.

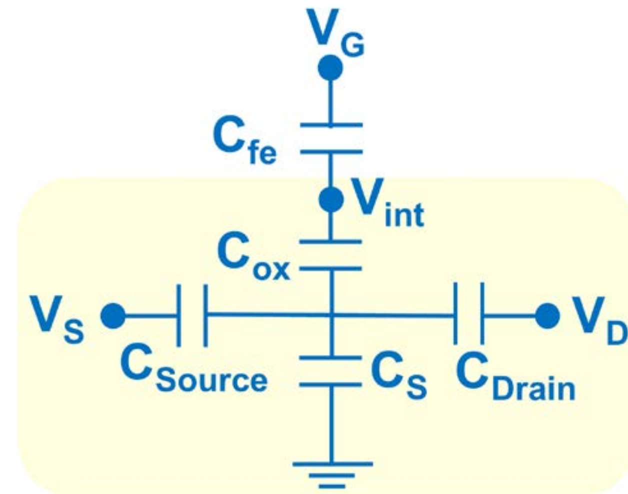
Outline

- MOSFET and Scaling
- Negative Capacitance and Transistor
- Modeling of NC-FinFET
- Impact of Material Parameters
- Switching Delay and Energy
- Conclusion

Device Structure

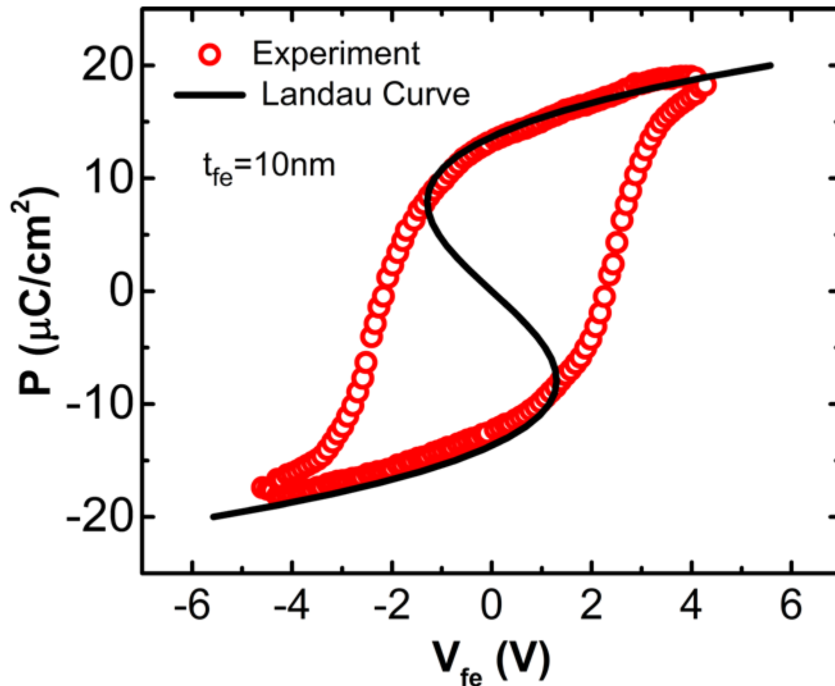
Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)





- Metal internal gate provides an equipotential surface with a spatially constant V_{int}.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.

Experimental Calibration of L-K Model



Calibration of L-K with P-V_{fe} curve for Y-HfO2 with 3.6 mol% content of $YO_{1.5}$[3]

$$\alpha = -1.23 \times 10^9 \text{ m/F}$$

$$\beta = 3.28 \times 10^{10} \text{ m/F}$$

$\gamma = 0$ (2nd order phase transition)

[3] J. M¨uller et al., JAP, vol. 110, no. 11, pp. 114113, 2011.

Gibb's Energy,

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP$$

Dynamics of G is given by

$$\delta \frac{dP}{dt} = -\frac{\partial G}{\partial P}$$

In the steady state, $\frac{dP}{dt} = 0$

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

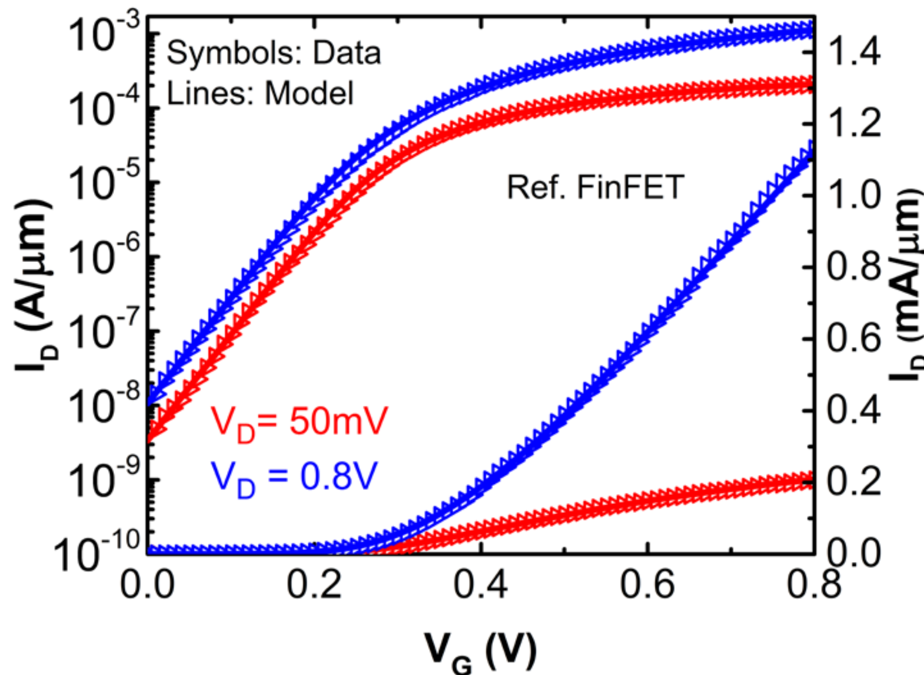
$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$

[1] Devonshire et al., The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 40, no. 309, pp. 1040–1063, 1949.

*[2] Landau, L. D. & Khalatnikov, I. M. On the anomalous absorption of sound near a second order phase transition point. Dokl. Akad. Nauk **96,** 469472 (1954).*

Calibration of Baseline FinFET

Calibration of baseline FinFET with
22 nm node FinFET.



BSIM-CMG model is used to model baseline FinFET.

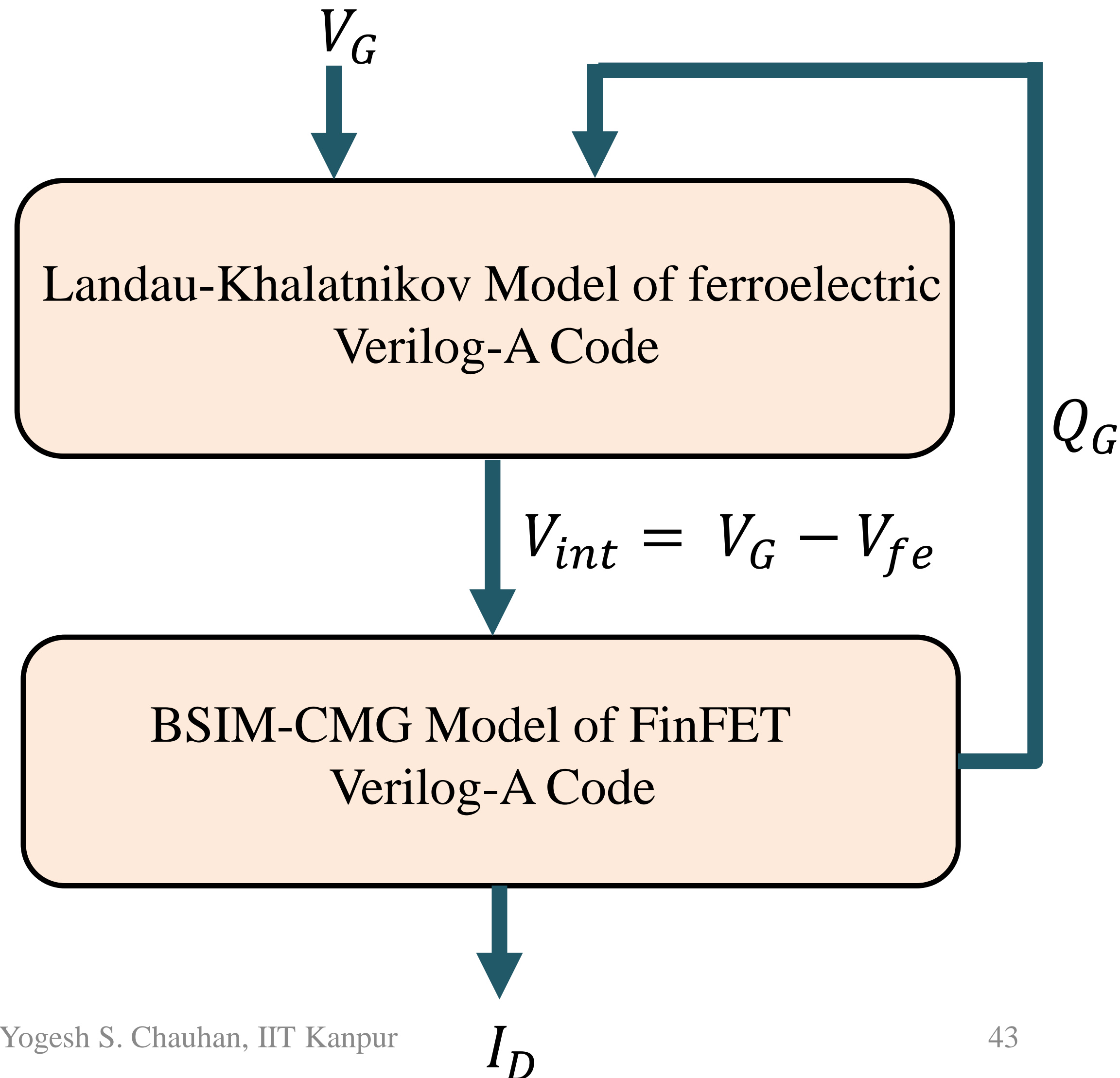
Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

C. Auth et al., in VLSIT, 2012, pp. 131–132.

Complete Modeling Flowchart

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}$$



Outline

- MOSFET and Scaling
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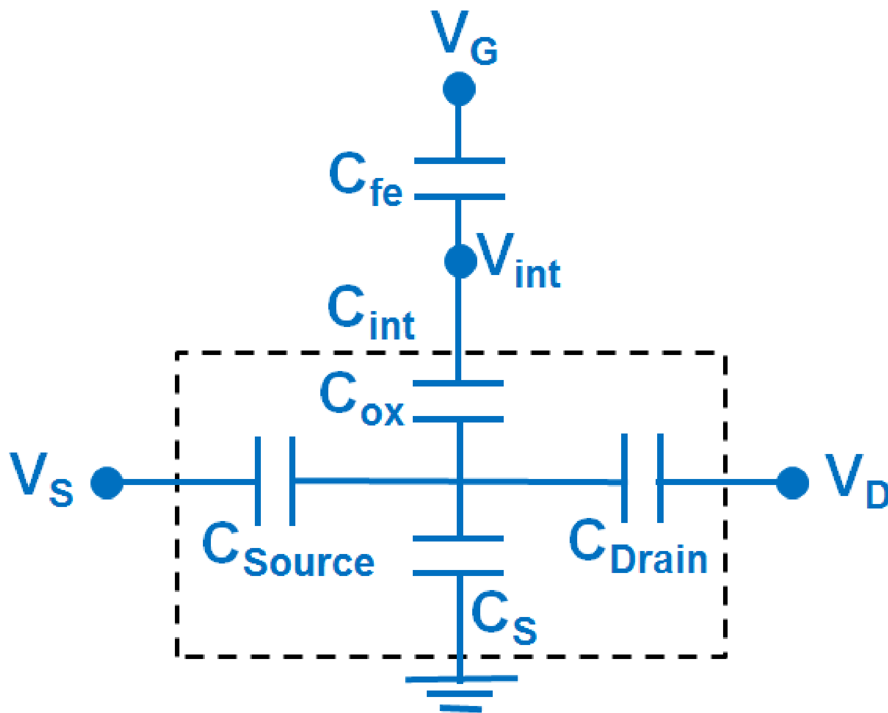
- Impact of Material Parameters
  - Impact of ferroelectric thickness
  - Ferroelectric Parameters Variation
- Switching Delay and Energy
- Conclusion

Capacitances and Voltage Amplification



Capacitance matching between $|C_{fe}|$ and C_{int} increases the gain.

$$E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5$$

$$V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5)$$

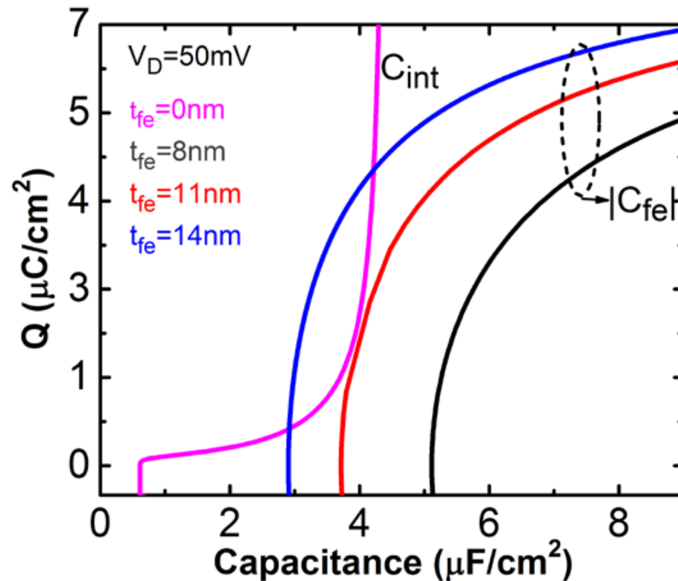
$$C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)}$$

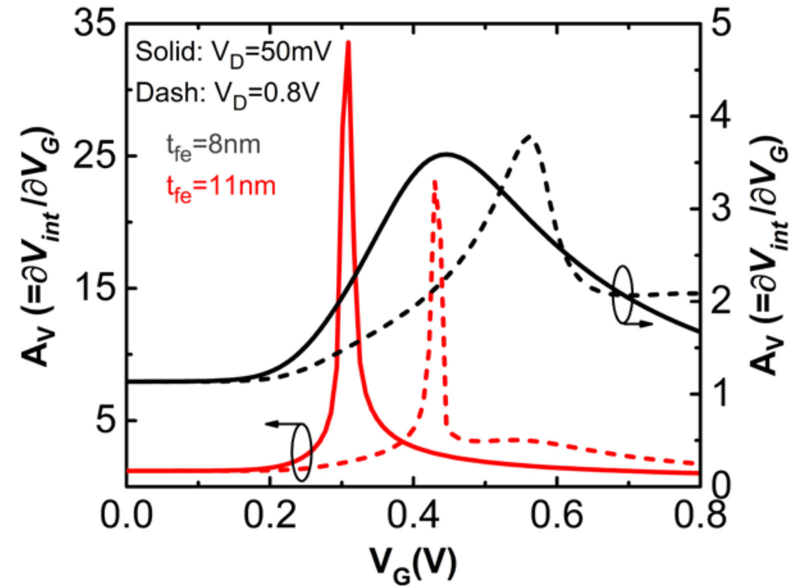
$$\frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}}$$

Internal Voltage Gain,

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

Capacitance Matching



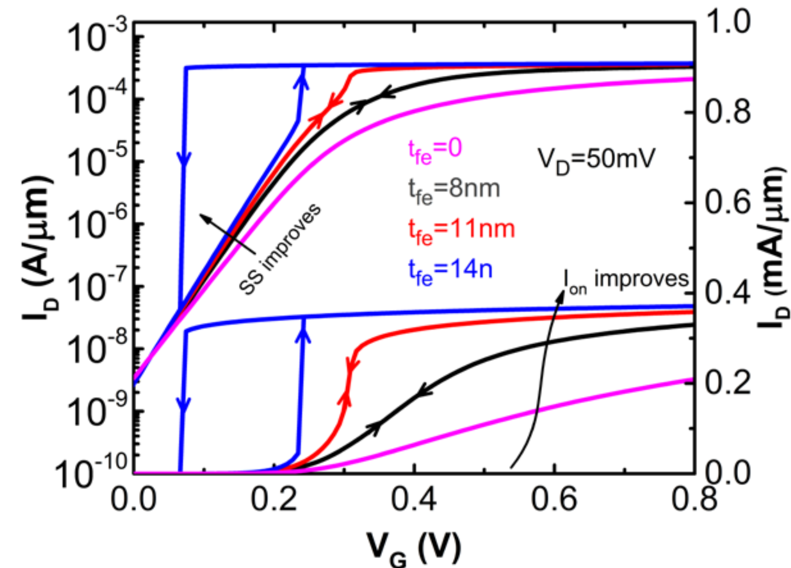


- Capacitance matching increases with t_{fe} which increases the gain.
- Hysteresis appears for $|C_{fe}| < Cint$ which is region of instability.

- Increase in V_D reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.

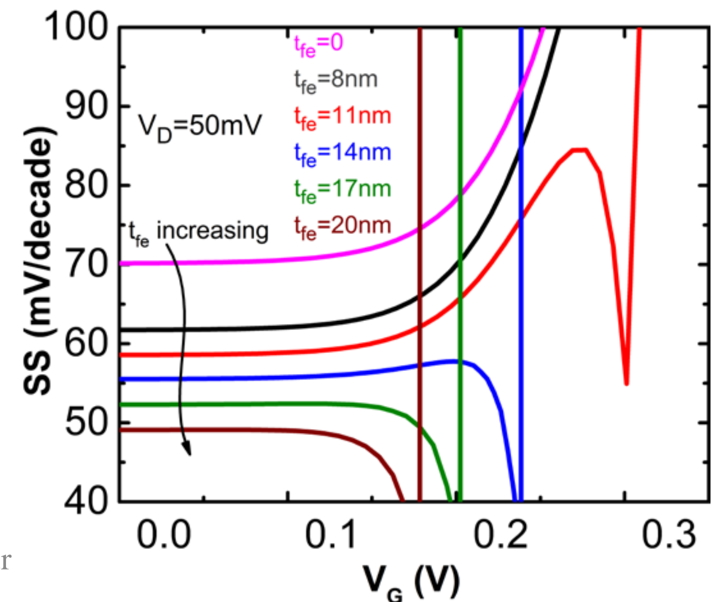
I_D-V_G Characteristics – SS region

- As t_{fe} increases
  - Capacitance matching is better
  - C_S and C_{ins} are better matched



$$S = \left(1 - \frac{C_S}{|C_{ins}|}\right).60\text{mV/dec}$$

- As $t_{fe}\uparrow \rightarrow SS\downarrow$

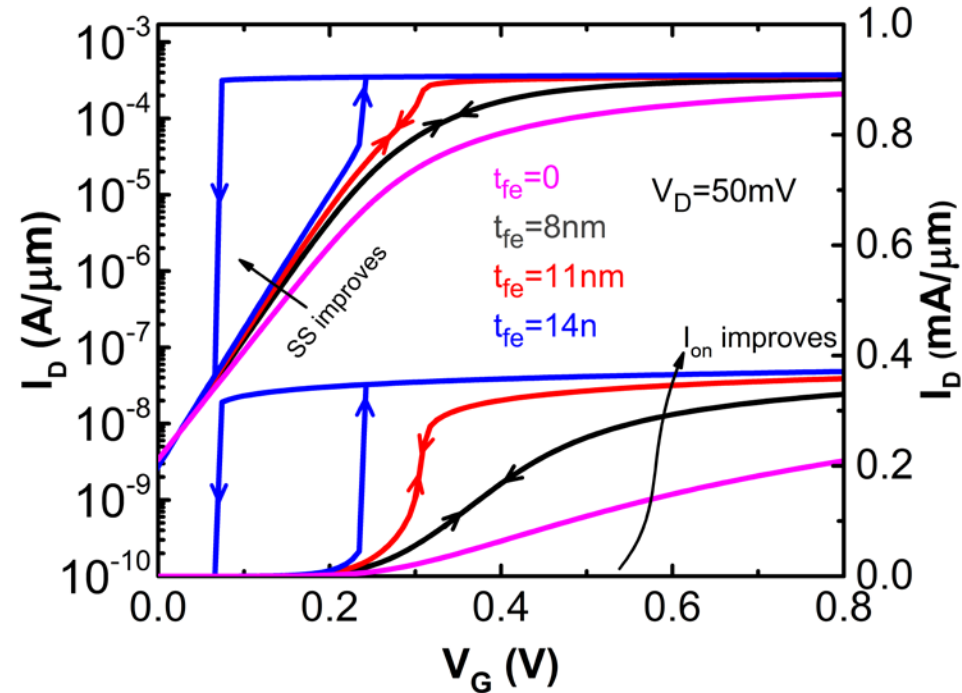


I_D-V_G Characteristics – ON region

- As t_{fe} increases
  - Capacitance matching is better

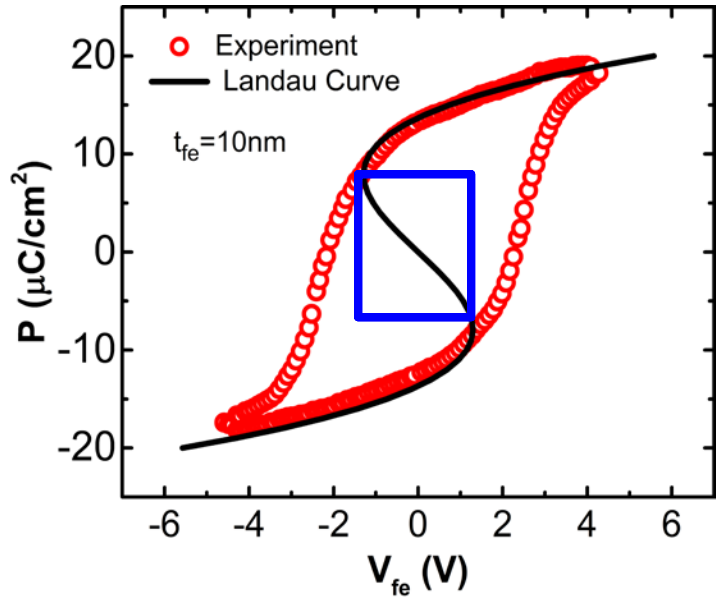
$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, I_{ON} increases.

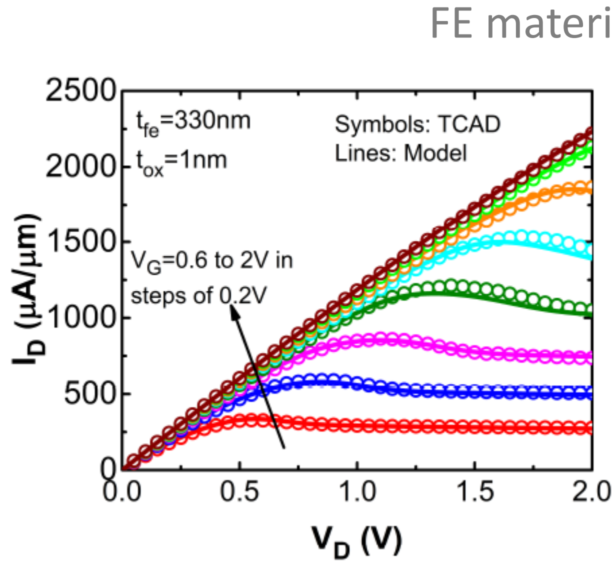


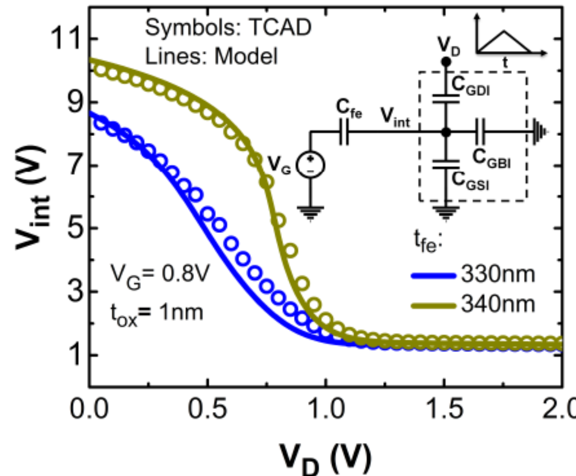
Note the significant improvement in I_{ON} compared to SS.

I_D-V_D Characteristics



FE material is different.





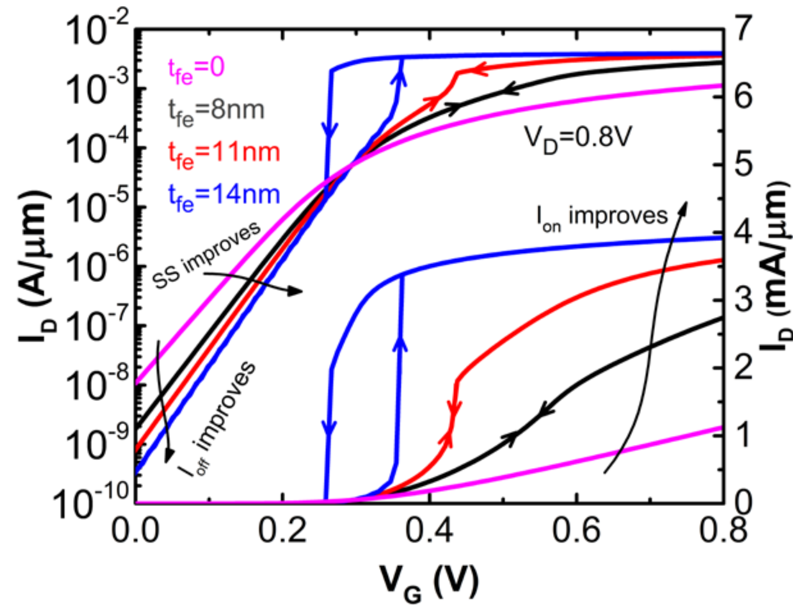
- NCFET is biased in negative capacitance region.
  - Q_G or P is positive → V_{fe} is negative.

- V_{DS}↑ → Q_G or P↓ → $|V_{fe}|$ ↓ → $V_{int}=V_G+|V_{fe}|$ ↓ → A_V ↓ → Current reduces

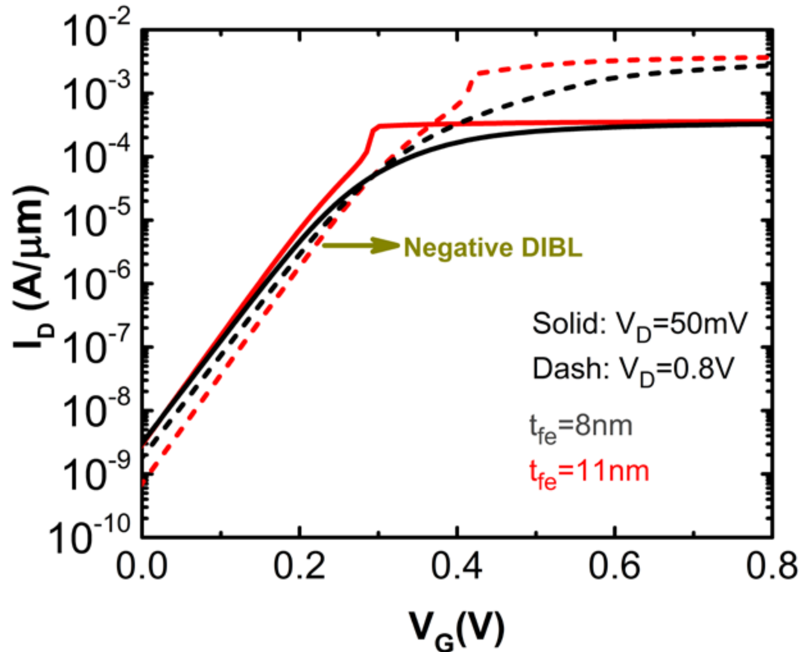
G. Pahwa, …, Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance", IEEE TED, Dec. 2016.

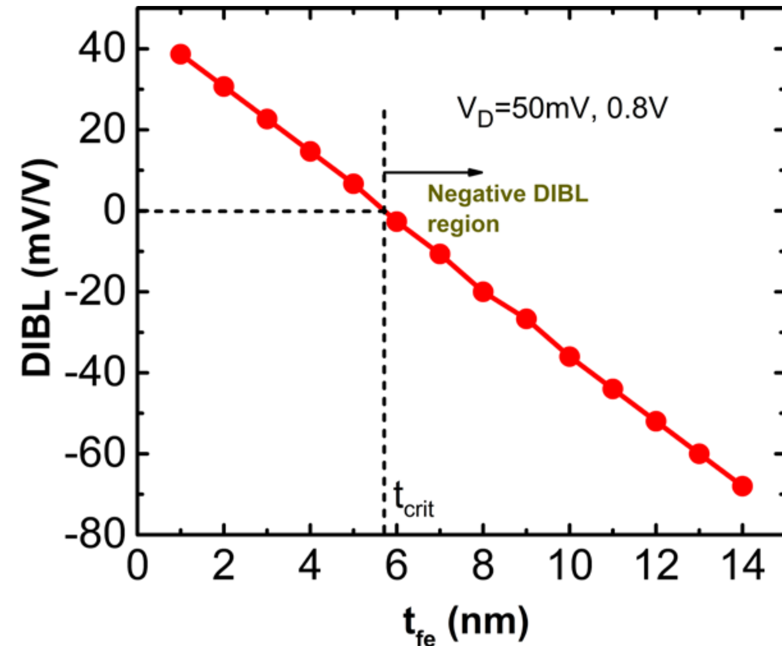
I_D-V_G Characteristics – High V_{DS}

- Hysteresis appears for $|C_{fe}| < C_{int}$ which is the region of instability.
- As t_{fe} increases
  - SS reduces, I_{ON} increases.
  - I_{OFF} reduces for high V_D.
- Width of hysteresis at larger thicknesses can be controlled with V_D.



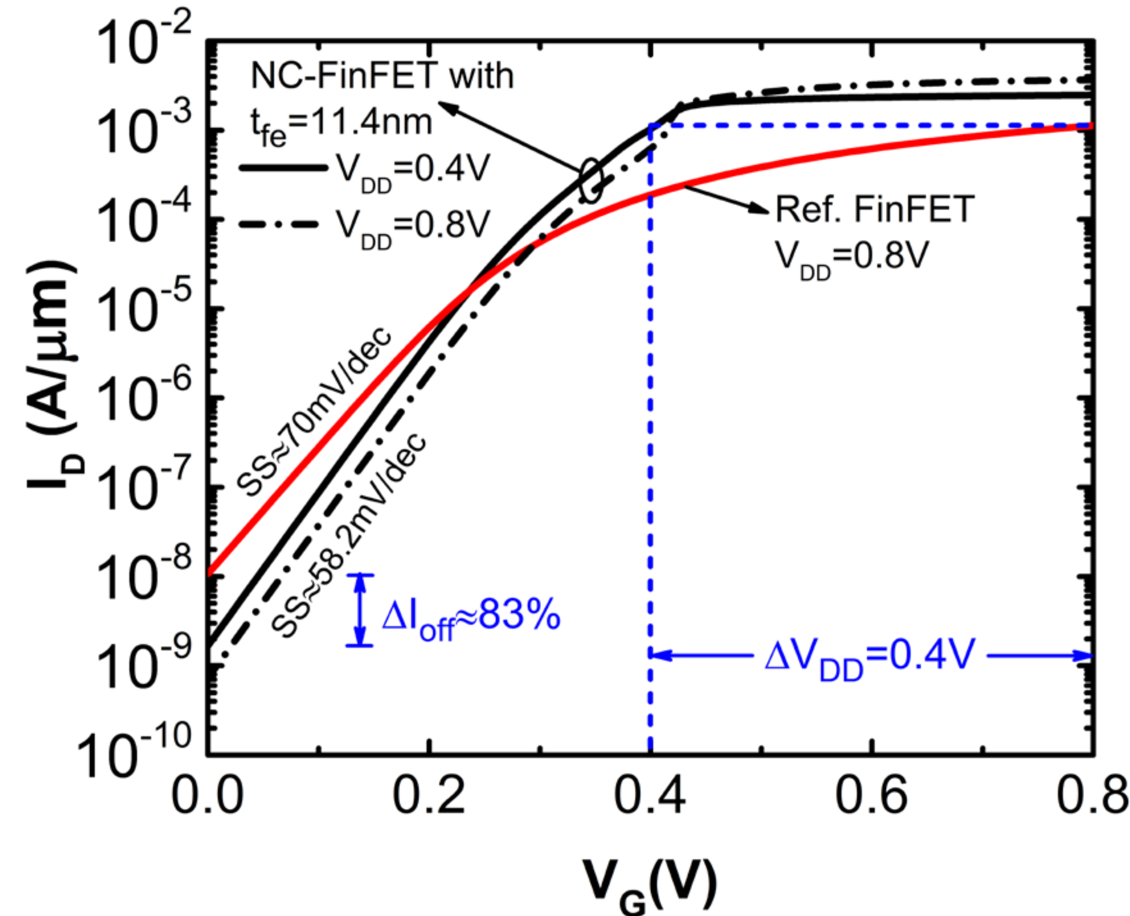
Negative DIBL





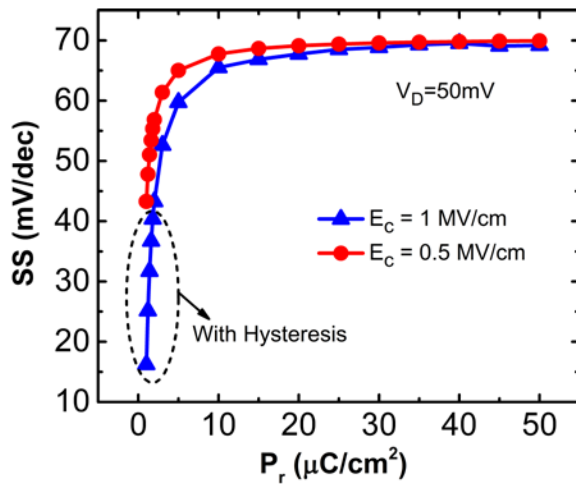
- V_D reduces Q_G which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with t_{fe} due to increased V_{fe} drop.
- V_{th} increases with V_D instead of decreasing.
  - Higher I_{ON} still lower I_{OFF}!

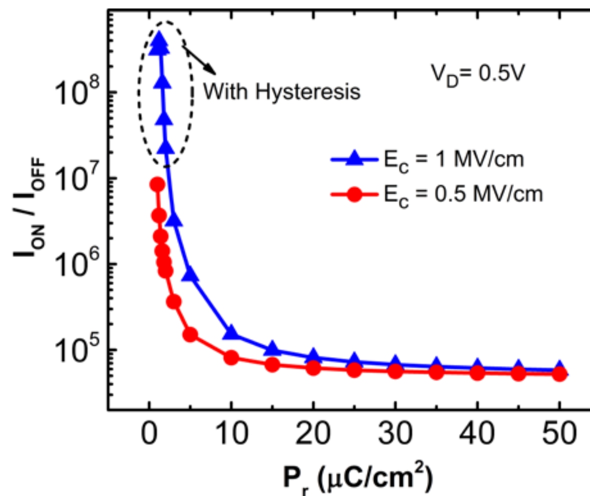
Optimum NC-FinFET

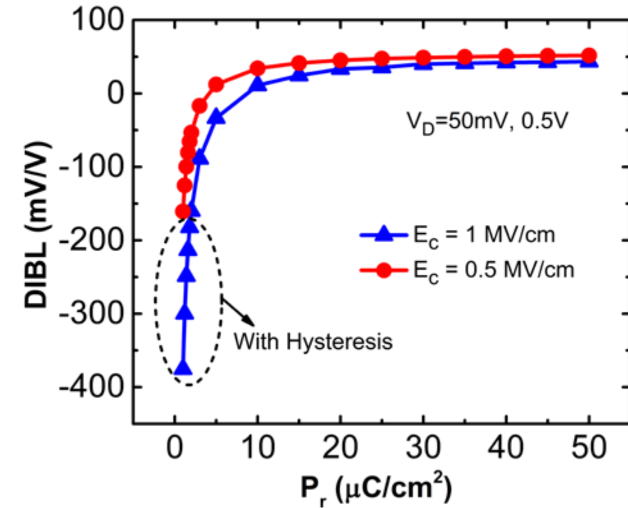


- Same I_{ON} as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- V_{DD} reduction by 0.4 V.
- I_{OFF} reduction by 83 %.

Ferroelectric Parameters Variation







If $\gamma = 0$,

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{{P_r}^3}$$

P_r = Remnant Polarization

E_c = Coercive Field

$$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$$

- Low P_r and high E_c
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I_{ON} but reduce I_{OFF} due to a more negative DIBL ⇒ high I_{ON}/I_{OFF}.

D. Ricinschi et al., JPCM, vol. 10, no. 2, p. 477, 1998.

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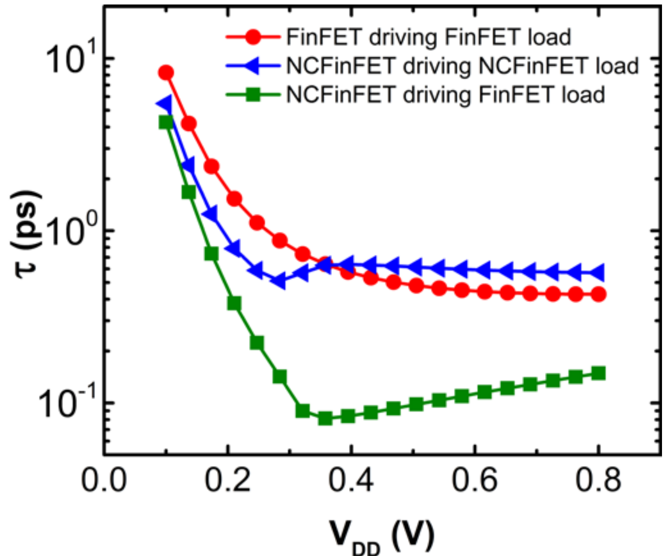
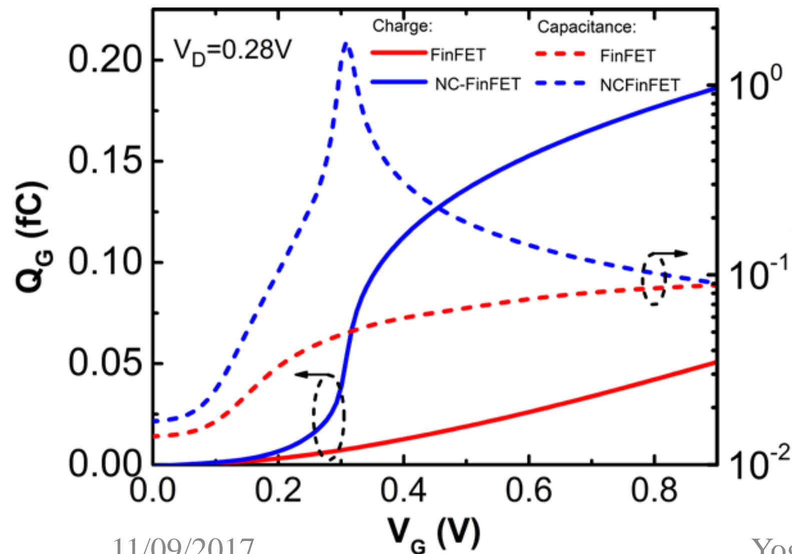
Intrinsic Delay



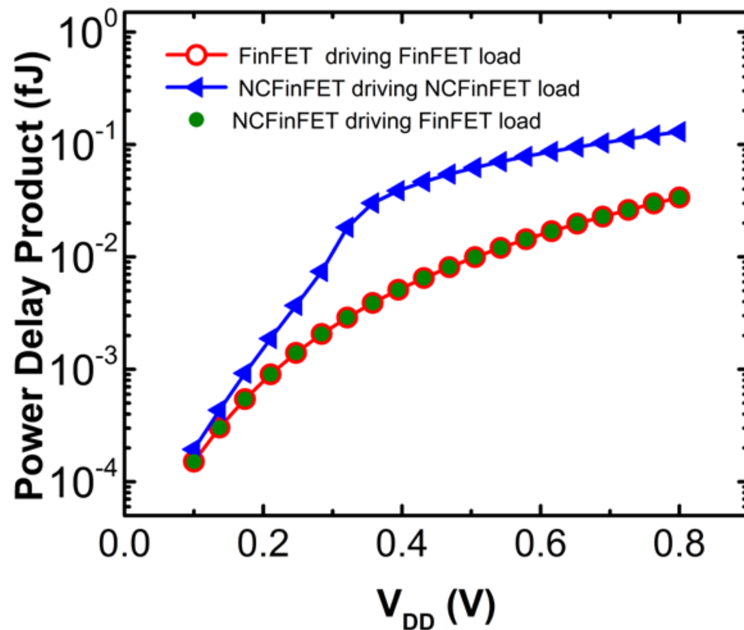


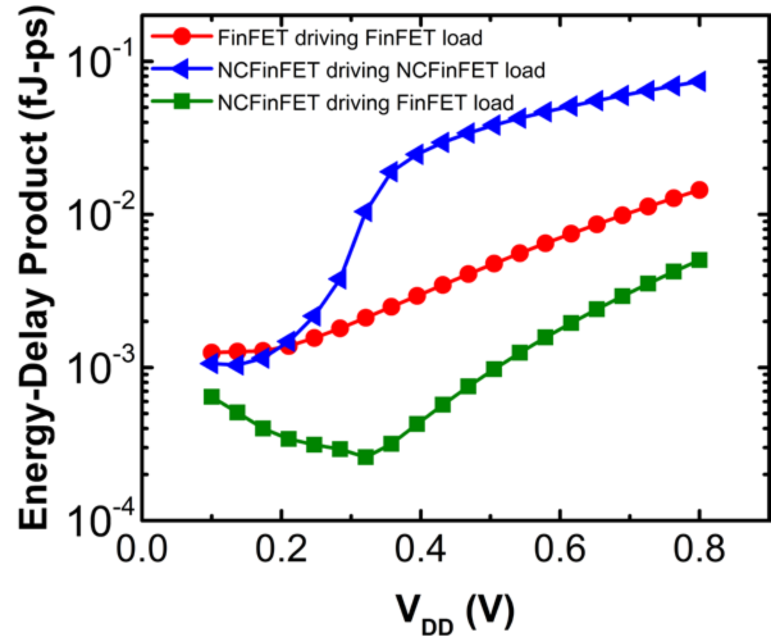
$$\text{Delay, } \tau = \frac{\Delta Q_G}{I_{ON}}$$

$$\Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD})$$

- NC-FinFET driving NC-FinFET
  - For high V_{DD}, high I_{ON} advantage is limited by large amount of ΔQ_G to be driven.
  - Outperforms FinFET at low V_{DD}.
  - Minimum at $V_{DD} \approx 0.28$ V corresponds to a sharp transition in Q_G.
- NC-FinFET driving FinFET load provides full advantage of NC-FinFET.

Power and Energy Delay Products



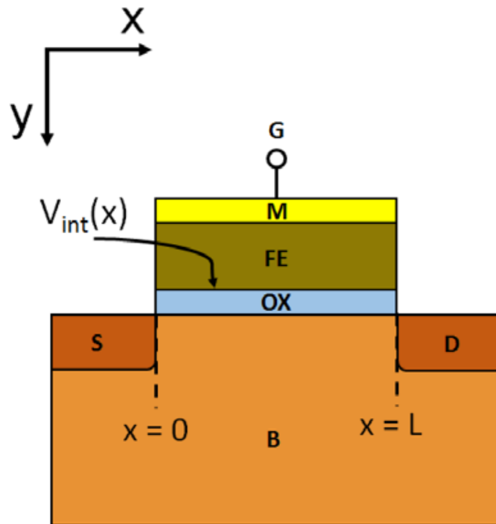


$$PDP = \Delta Q_G . V_{DD}$$

$$EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}}$$

- NC-FinFET driving NC-FinFET shows advantage only for low V_{DD}.
- NC-FinFET driving FinFET load is the optimum choice.

Modeling of MFIS NCFET



Contrast with MFIMS structure:

- P and V_{int} vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models[1,2]:

Implicit equations – tedious iterative numerical solutions

[1] H.-P. Chen, V. C. Lee, A. Ohoka, J. Xiang, and Y. Taur, "Modeling and design of ferroelectric MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2401–2405, Aug. 2011.
[2] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2405–2409, Oct. 2010.

Explicit Modeling of Charge

$$V_{\text{fe}} = Et_{\text{fe}} = aQ_G + bQ_G{}^3$$

Voltage Balance:

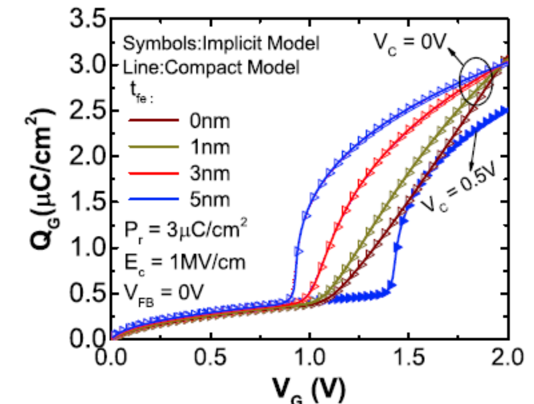
$$V_G - V_{\text{FB}} = V_{\text{fe}} + \frac{Q_G}{C_{\text{ox}}} + \psi_S = a_{\text{eff}}Q_G + bQ_G{}^3 + \psi_S$$

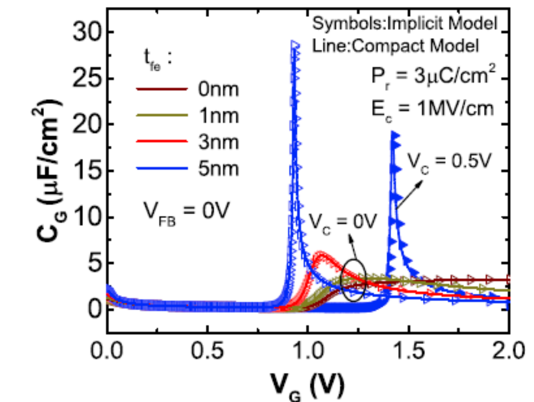
$Q_G - \psi_S$ relation[1]

$$Q_G = \text{sign}(\psi_S)\gamma C_{ox}\left[\psi_S + V_t(e^{-\psi_S/V_t} - 1) + e^{-(2\phi_F + V_C)/V_t}(V_t e^{\psi_S/V_t} - \psi_S - V_t)\right]^{1/2}$$

→ Implicit equation in Q_G

→ **Goal:** Explicit Model with good initial guesses for each region of NCFET operation



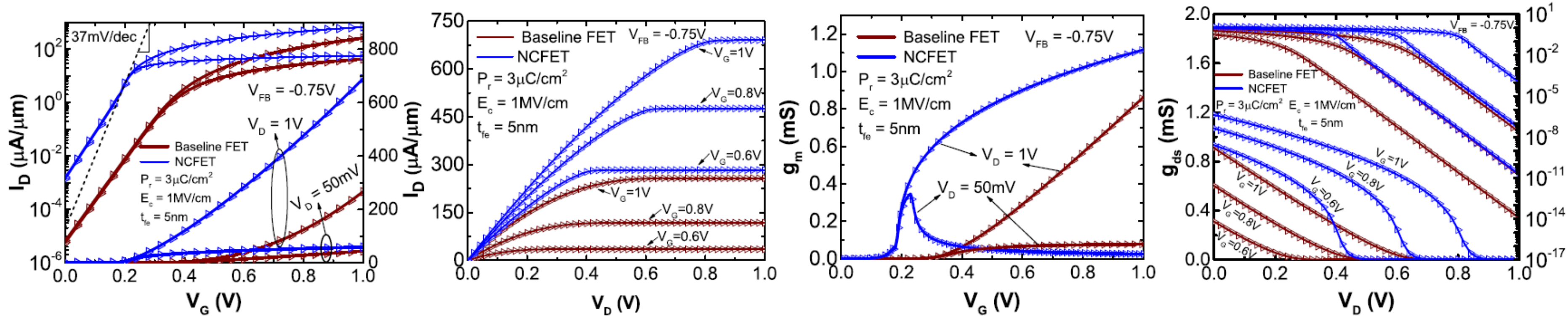


Both the Q_G and its derivatives match well with implicit model

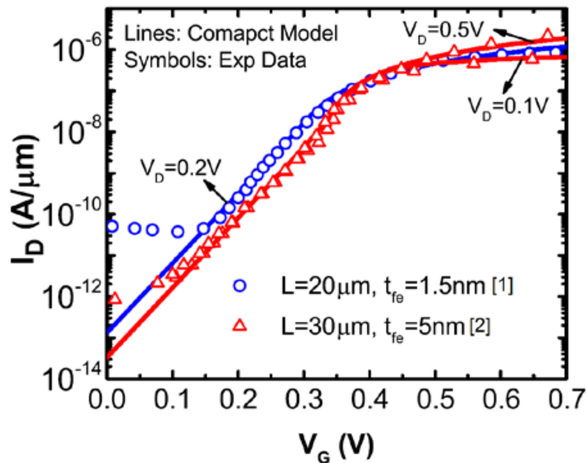
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," in *IEEE Transactions on Electron Devices*, March 2017.

Drain Current Model Validation

Against Full Implicit Calculations



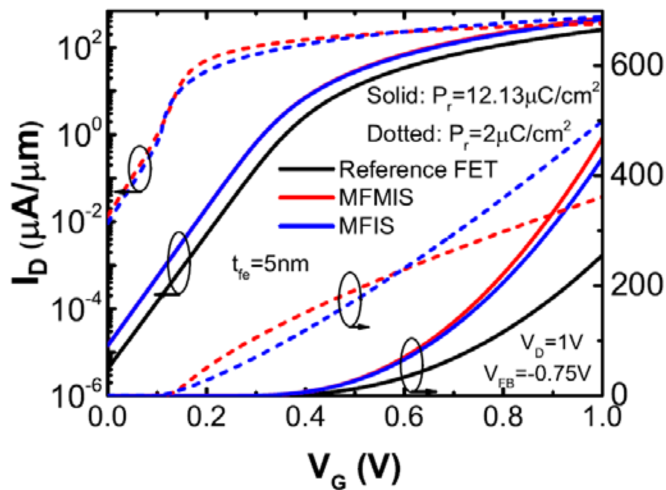
Against Experimental Data

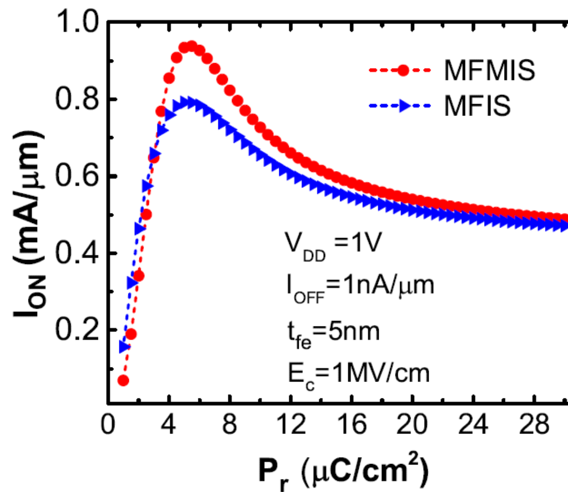


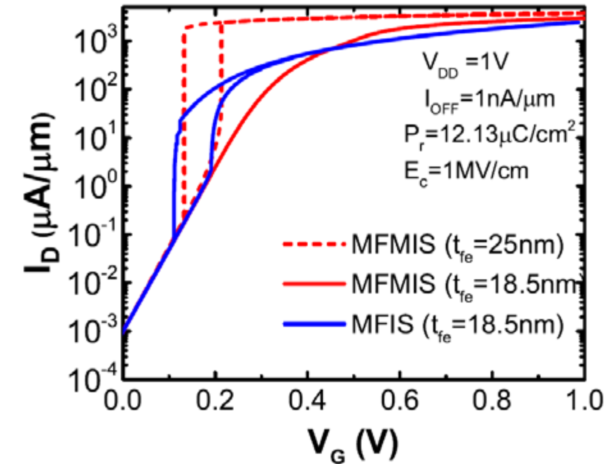
G. Pahwa, T. Dutta, A. Agarwal and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," *IEEE Transactions on Electron Devices*, March 2017.

[1] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2016, pp. 12.1.1–12.1.4. [2] M. H. Lee *et al.*, in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.5.1–22.5.4.

MFIS Vs MFMIS



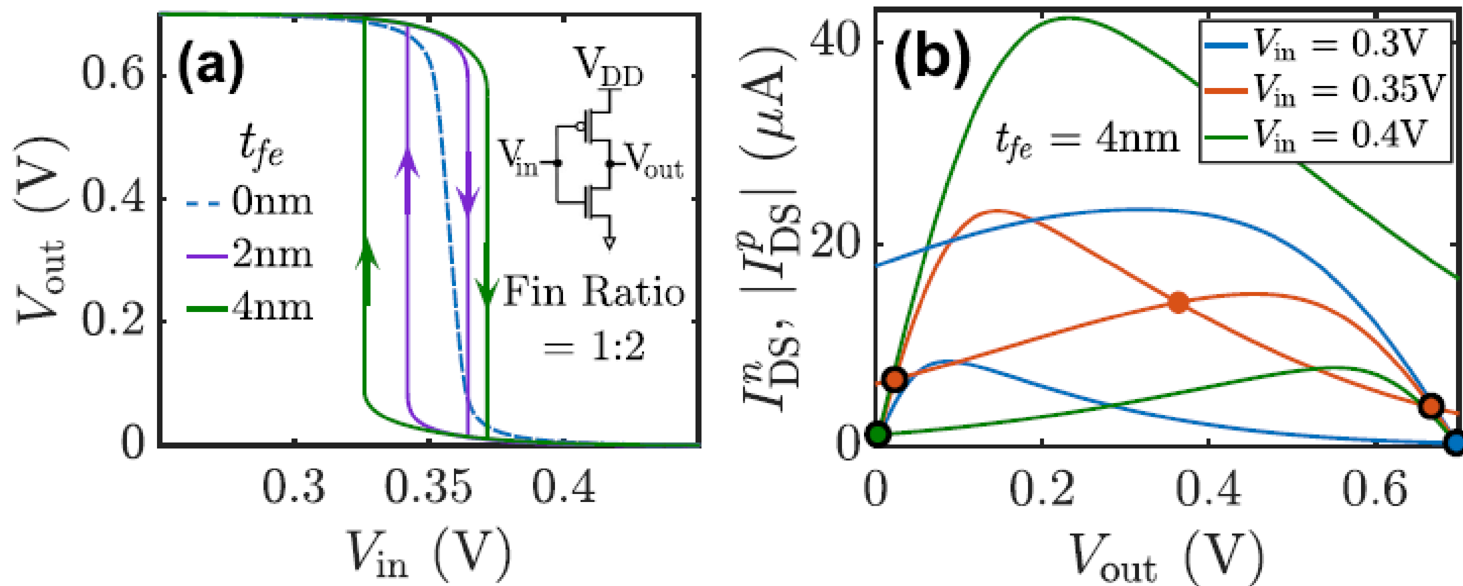




- MFIS excels MFMIS for low P_r ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", accepted in *IEEE Transactions on Electron Devices*, 2018.

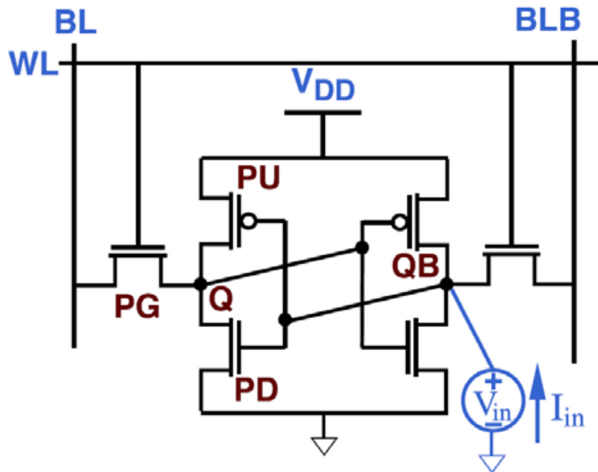
NC-FinFET based inverters

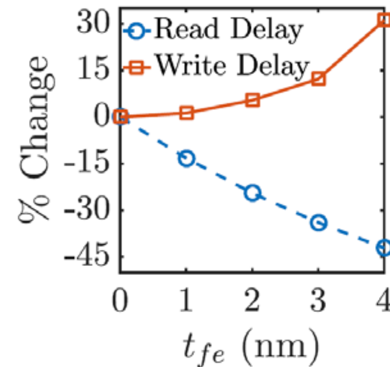


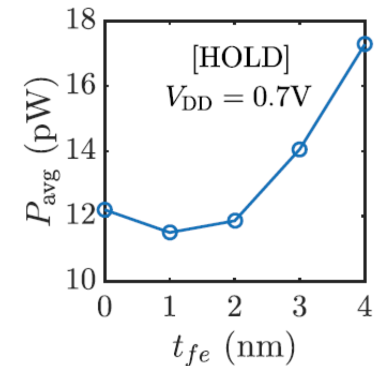
- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

NC-FinFET based SRAM



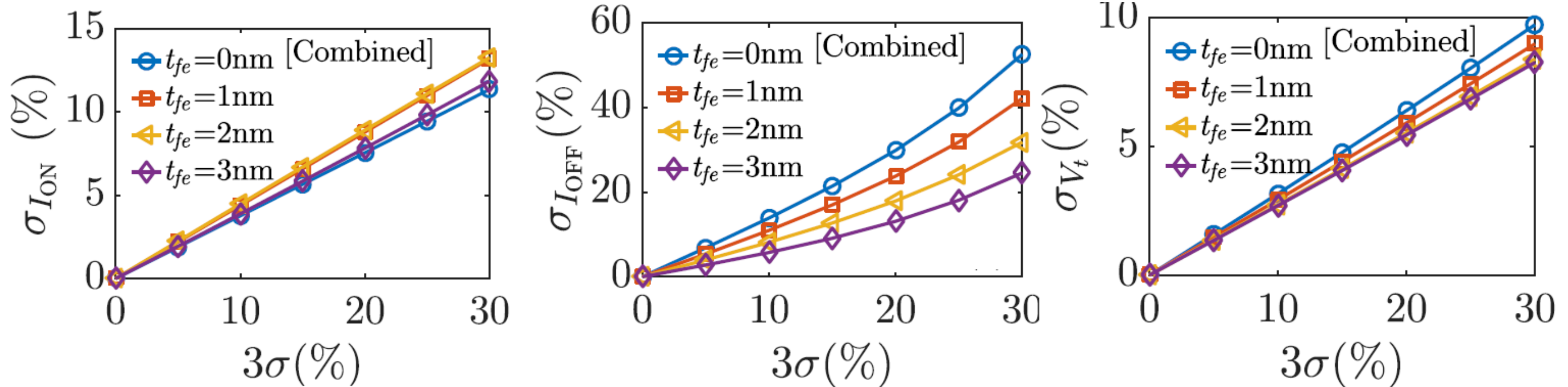




- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- P_{avg}: NC-SRAM performs better with lower standby leakage only at small t_{fe}, taking advantage of the lower subthreshold currents

T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.

Impact of Process Variations

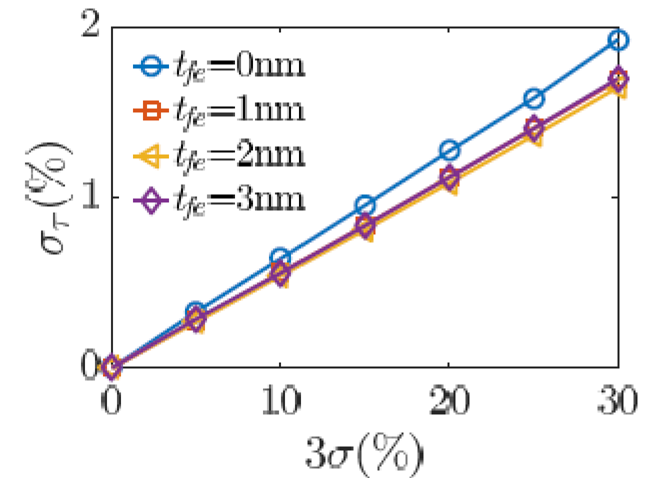


- Variability in I_{ON}, I_{OFF}, and V_t due to combined impact of variability in L_g, T_{fin}, H_{fin}, EOT, t_{fe}, E_c, and P_r
- I_{ON}: Improvement is non-monotonic with t_{fe}
- I_{OFF}: Decreases monotonically with t_{fe}
- V_t: Decreases monotonically with t_{fe}

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", accepted in IEEE Electron Device Letters, 2018.

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.



11-stage Ring-Oscillator: Variation in τ due to combined variation

T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", accepted in IEEE Electron Device Letters, 2018.

Conclusion

- Maintaining I_{ON}/I_{OFF} is the biggest challenge in new technology nodes

- Negative capacitance FET is one of the best choice
  - Need to find sweet material ($HfZrO_2$)
  - Integration in conventional CMOS process remains a challenge (lot of progress)
  - Speed/Switching need more research

Relevant Publications

- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Physical Insights on Negative Capacitance Transistors in Non-Hysteresis and Hysteresis Regimes: MFMIS vs MFIS Structures", accepted in IEEE Transactions on Electron Devices, 2018.
- T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits", accepted in IEEE Electron Device Letters, 2018.
- T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance Evaluation of 7 nm Node Negative Capacitance FinFET based SRAM", IEEE Electron Device Letters, Aug. 2017.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor with MFIS Structure", IEEE Transactions on Electron Devices, Mar. 2017.
- G. Pahwa, …, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part I, Model description", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, …, and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance - Part II, Model validation", IEEE Transactions on Electron Devices, Dec. 2016.
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Energy-Delay Tradeoffs in Negative Capacitance FinFET based CMOS Circuits", IEEE ICEE, Dec. 2016. (Best Paper Award)
- G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing Energy Efficient and Hysteresis Free Negative Capacitance FinFET with Negative DIBL and 3.5X ION using Compact Modeling Approach", IEEE ESSDERC, Switzerland, Sept. 2016. (Invited)

Thank You