Changes in the Editorial Board

AFTER nine years (the maximum three consecutive terms) on the Editorial Board of the IEEE TRANSACTIONS ON ELECTRON DEVICES (T-ED), Prof. David Esseni from the University of Udine, Prof. Jason Woo from the University of California at Los Angeles, and Prof. Ru Huang from Peking University have stepped down from their Editor positions in MOS Devices and Technology. I would like to express my sincere gratitude—and the gratitude of the Electron Device Society community at large—to David, Jason, and Ru for their commitment, dedication, and hard work during their term of service. Our very best wishes to them in their future endeavors.

At the same time, I am more than glad to announce that four new Editors have joined the T-ED Editorial Board. They are not only meant to replace some of the retiring ones, but also to bring within T-ED new expertise and enthusiasm to the job and to further strengthen their areas. All of them are recognized experts in their own field.

They are Prof. Yogesh Singh Chauhan from the Indian Institute of Technology, Kanpur (Device and Process Modeling); Prof. Karol Kalna from Swansea University (Device and Process Modeling); Prof. Giovanni Verzellesi from the University of Modena and Reggio Emilia (Compound Semiconductor Devices); Prof. Runsheng Wang from Peking University (MOS Devices and Technology).

A warm welcome to the newly appointed Editors!

GIOVANNI GHIONE, *Editor in Chief*
Torino, Italy

Yogesh Singh Chauhan (SM'12) was with the Semiconductor Research and Development Center, IBM, Bangalore, India, from 2007 to 2010, the Tokyo Institute of Technology, Tokyo, Japan, in 2010, and the University of California at Berkeley, Berkeley, CA, USA, from 2010 to 2012. He is currently an Associate Professor with IIT Kanpur, Kanpur, India. He is the Lead Developer of the industry standard BSIM-BULK model. He is also the Co-Developer of the ASM-high electron mobility transistor (HEMT) model for GaN HEMTs, which is under industry standardization at the compact model coalition. His current research interests include characterization, modeling, and simulation of semiconductor devices.

Dr. Chauhan was a Technical Program Committee Member of the IEEE International Conference on Simulation of Semiconductor Processes and Devices in 2013 and the IEEE European Solid-State Device Research Conference 2016/2017. He is a member of the IEEE-EDS Compact Modeling Committee. He received the Ramanujan Fellowship in 2012, the IBM Faculty Award in 2013, and the P. K. Kelkar Fellowship in 2015.

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Karol Kalna (SM'13) received the M.Sc. degree (Hons.) in solid-state physics and the Ph.D. degree in condensed matter physics from Comenius University, Bratislava, Slovakia, in 1990 and 1998, respectively.

In 1994, he joined the Institute of Electrical Engineering, Bratislava, as a Research Scientist. He was a Visiting Postgraduate Student with the Department of Physics, UIA University of Antwerp, Antwerp, Belgium, in 1994 and 1997, where he was involved in semiconductor lasers modeling. From 1999 to 2010, he was with the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow, U.K., where he was studying the scaling of high electron mobility transistor (HEMT) into sub-100-nm dimensions performing dc and RF analysis within ensemble Monte Carlo simulations. Since 2002, he has been pioneering III–V MOSFETs for future digital technology studying transistor scaling with Monte Carlo simulations. From 2007 to 2012, he was an Engineering and Physical Sciences Research Council Advanced Research Fellow carrying out the Monte Carlo modeling of deep sub-100-nm, ultrathin body transistors with Si and high-mobility materials in a channel. He was involved in several research projects on III–V MOSFETs for digital applications funded by ESPRC and European Community (DualLogic). He became a Senior Lecturer in 2010 and an Associate Professor in 2013 at the College of Engineering, Swansea University, Wales, U.K., establishing his own Nanoelectronic Devices Computational Group. He has over 200 publications, including 81 papers in peer-review journals and three book chapters and more than 20 invited talks. His current research interests include finite element 2-D and 3-D Monte Carlo simulations of nanoscaled MOSFETs, including FinFETs and gate-all-around nanowires with a channel based on Si, strain Si, and III–V semiconductors; quantum transport simulations using nonequilibrium Green's functions; multiscale modeling coupling density functional theory calculations with Monte Carlo simulations; and simulations of GaN-based HEMTs and ZnO nanowires.

Giovanni Verzellesi (S'92–M'93–SM'08) was born in Reggio Emilia, Italy in 1964. He received the Laurea (*summa cum laude*) degree in electrical engineering from the University of Bologna, Bologna, Italy, in 1989, and the Ph.D. degree in electrical engineering from the University of Padova, Padua, Italy, in 1994.

From 1993 to 1994, he was a Visiting Graduate Student with the University of California at Santa Barbara, Santa Barbara, CA, USA. From 1994 to 1999, he was with the University of Trento, Trento, Italy, as a Research Associate. In 2000, he joined the University of Modena and Reggio Emilia, Modena, Italy, where he became an Associate Professor in 2001 and a Full Professor of electronics in 2006. He has co-authored over 100 papers in international journals and over 110 papers in the proceedings of international conferences. His research activity has been concerned with the modeling, simulation, and characterization of semiconductor devices and sensors and has covered, over the years, the following topics: impact-ionization effects in Si bipolar transistors, Si- and SiC-based radiation detectors, GaN LEDs, and III–V-based FETs. His current research interests include GaN FETs for RF and power switching applications and III–V MOSFETs for logic ICs.

Dr. Verzellesi has served in the technical program committee of the following conferences: the IEEE IEDM, the IEEE IRPS, ESREF, ESSDERC, EXMATEC, and HETECH.

Runsheng Wang (S'07–M'11) received the B.S. and Ph.D. (Hons.) degrees from Peking University, Beijing, China, in 2005 and 2010, respectively.

From 2008 to 2009, he was a Visiting Scholar with Purdue University, West Lafayette, IN, USA. He joined Peking University in 2010, where he is currently an Associate Professor with the Institute of Microelectronics. He has authored or co-authored one book, three book chapters, and over 100 scientific papers, including more than 30 papers published in International Electron Devices Meeting (IEDM) and Symposium on VLSI Technology. He holds 12 U.S. patents and 29 Chinese patents. His current research interests include nanoscale CMOS devices and characterization, circuit and device interaction, and emerging technologies for new-paradigm computing.

Dr. Wang received the IEEE Electron Device Society (EDS) Early Career Award by the IEEE EDS, the National Natural Science Foundation of China (NSFC) Award for Excellent Young Scientists by NSFC, the Natural Science Award (First Prize) by the Ministry of Education of China, and many other awards. He has served on the Technical Program Committee of many IEEE conferences, including IEDM, IRPS, ICSICT, IPFA, and INEC. He serves on the Editorial Board of *Scientific Reports* and *SCIENCE CHINA: Information Sciences*.