Semiconductor industry – Challenges and Opportunities

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Outline

• Hyperconnected Age
  – Role of semiconductors

• What is semiconductor
  – MOSFET and Scaling
  – Multigate Transistors
    • FinFET
    • Thin-Body Transistor

• Compact Modeling of FinFET and UTB FET

• What next?
Hyperconnected Age

- We are living in an unprecedented era of hyperconnectivity that is redefining our societies, cultures, and communications.
- And it has only just begun!
Hyperconnected Age

• Present
  – Facebook has more than 1.4 billion users worldwide, creating a hyperconnected, global social network
  – Human to Device interaction

• Future
  – Device to Human interaction
  – Device to Device interaction

CISCO – By 2020, there will be 50 billion networked devices.
Electronics industry

• Playing important role in making this planet smarter!
• Key enabling technologies
  – Internet of things
  – Cloud
  – Healthcare
  – Robotics
  – Automobile
  – Food

Source: European Commission
Internet of things

**Electric Toothbrush:**
Automatically reorders brush heads, shares
brushing habits with your dentist

**Alarms Clock:**
Remote programs, custom tones, turns
on coffee maker

**Refrigerator:**
RFID tags reorders groceries as
needed, and suggests recipes

**Coffee Maker:**
Custom setting for each coffee type,
starts when alarm goes off

**Automobile:**
Maps traffic in real time; others can
track your location

**Oven:**
Oven settings from computer or phone
if running late

**Computer:**
Centralized control for remote interface to
any other device

**HVAC:**
Controls temperature & lights for maximum
efficiency

**Cell Phone:**
Secure performs identification & verification for
payments

**Building Security:**
Security cameras interact with facial
recognition database

**Vending:**
Automatically reorders supplies before it's empty

**Exercise Equipment:**
Recognizes individual user and tracks
workout schedule

**Media Player:**
Remotely orders new songs & video

**Microwave:**
Automatically sets cook cycle with
RFID recognition

**Television:**
Immediate “one-click” ordering of products
seen on commercials

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IoT & Cloud – Data and Computation
Automobile – Driverless car

Radar Eyes on All Sides

Wearable Electronics

With chips shrinking and sensors becoming cheaper, personal computing is moving from that smartphone in your pocket to your arm, your wrist, right out to your fingertips.

Smart Watch

Google Glass

Need ultra-low power devices and sensors
Healthcare – Implantable Electronics

Wireless Implantable Medical Devices

- Deep Brain Neurostimulators
- Cochlear Implants
- Gastric Stimulators
- Cardiac Defibrillators/Pacemakers
- Insulin Pumps
- Foot Drop Implants

Microphone and Sound Processor
Cable Connector
Implantable Cochlea
5G – Machine communication

- Communication
  - Device to device
  - Machine to machine
  - Vehicle to vehicle
- UHD live video
The Deconstructed Cell Phone

Hint: It’s All About the Microelectronics!
Semiconductors – Heart of technological progress and innovation

• The semiconductor is one of the most pervasive and powerful inventions in human history.

Nobel Prize in Physics 2014
"invention of efficient blue LEDs"
Economic impact of semiconductors

- Semiconductors touch every sphere of economic activity.

- Direct: ~$300 bn
- Indirect
  - Material/equipment
- Induced
  - consumer market
- Downstream
  - Other industry

Source: Global Semiconductor Alliance and Oxford Economics
What is semiconductor?

[Diagram showing energy band diagram, density of states, occupancy probability, and carrier distributions.]

Source: Anandtech
Semiconductor Devices – Junction

- Doping
- Junction
Semiconductor Devices – MOSFET

![Diagram of MOSFET](image)

- **Linear operating region (ohmic mode)**
  - $V_{DS} < V_{GS} - V_{TH}$
  - Source $\rightarrow$ Gate $\rightarrow$ Drain

- **Saturation mode at point of pinch-off**
  - $V_{GS} > V_{TH}$
  - Source $\rightarrow$ Gate $\rightarrow$ Drain

- **Saturation mode**
  - $V_{GS} > V_{TH}$
  - Source $\rightarrow$ Gate $\rightarrow$ Drain

- **Conduction edge**
  - $Q = Q_n + Q_A$

- **Valence edge**
  - $Q = Q_A$

- **Insulator**
  - $-Q_A$

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Semiconductor devices to circuits

NOT gate

Flip-flop

Full Adder

Memory
Semiconductor circuits to Products

CPU

GPU – Graphics Processing Unit

10-100X faster than CPU for parallel calculations

Source: Anandtech, Intel, Nvidia
Today’s ICs

Multiple metal layers

3D ICs

System in Package (SIP)

Enabling Technologies
- Flip Chips
- Multi-Chip Modules
- 3-D Packaging
How do you make these?

Start

Silicon Crystals

Bunny Suits!

10B Transistors per cm²

Silicon “Wafers”

$5B Fabrication Facility

Finish
Building block – (tiny) MOSFET!

- MOSFET is a transistor used for **amplifying** or **switching** electronic signals.
Invention of Transistor

• First Transistor (1947-1948) at AT&T’s Bell Labs
  – Point Contact Transistor
  – First transistor was bipolar contact transistor
  – Material – Germanium
Invention of Transistor

- Worked on theory of Diode, Transistor, Thyristor etc.
  - Invented First transistor at Bell Labs
  - Received Nobel Prize in 1956
- Formed Shockley semiconductor in Mountain View, California in 1956
- Employees of Shockley semiconductor (Robert Noyce, Gordon Moore, ….)
  - These employees opened 65 companies in next 20 years including Intel, AMD, Fairchild,…
Integrated Circuit (IC)

- IC – Electronic circuit manufactured on the surface of a thin substrate of semiconductor material.
- Additional materials are deposited and patterned to form interconnections between semiconductor devices.

- ICs are used in virtually all electronic equipment today and have revolutionized the world of electronics.
Invention of Integrated Circuits

• **Jack Kilby** (at *Texas Instruments*) demonstrated first working IC in 1958.
  – Jack Kilby was awarded the Nobel Prize in Physics 2000.
  – Kilby's work was named an IEEE Milestone in 2009.

• **Robert Noyce** (at *Fairchild Semiconductor*) also invented IC separately six months later than Kilby.
  – It was made of silicon, whereas Kilby's chip was made of germanium.
  – Fairchild Semiconductor was also home of the first silicon gate IC technology with self-aligned gates, which stands as the basis of all modern CMOS computer chips.
Bulk MOSFET

**Schematic Cross Section**

- Gate
- N+ (Source)
- P-
- N+ (Drain)
- Gate oxide

**Barrier height is controlled by gate voltage**

\[ n(E) \propto \exp\left(-\frac{E}{kT}\right) \]

- Increasing \( E \) (energy level)
- Increasing \( V_{GS} \) (gate-source voltage)

**ID_{DS} controlled by V_{GS}**

- \( I_{ON} \) (on current)
- \( I_{OFF} \) (off current)
- Inverse slope is subthreshold swing, \( S \) [mV/dec]

**Desired**
- High \( I_{ON} \)
- Low \( I_{OFF} \)

Figures: T. Liu, SRC/GRC e-Workshop, November 2012
Bulk MOSFET

• Drain current in MOSFET (ON operation)
  \[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

• Drain current in MOSFET (OFF operation)
  \[ I_{OFF} \propto 10^{\left(\frac{V_{GS}-V_{TH}}{S}\right)} \]

• Desired
  • High \( I_{ON} \) (↓L, ↑Cox, ↑\( V_{DD} - V_{TH} \))
  • Low \( I_{OFF} \) (↑\( V_{TH} \), ↑S)

\( C_{ox} = \varepsilon_{ox}/t_{ox} = \text{oxide cap.} \)
\( S = \text{Subthreshold slope} \)
Moore’s Law:
The defining features of the integrated circuit technology (size, speed, cost) follow an exponential growth pattern over time.

Moral: Computing power ↑ while cost ↓ exponentially!
Technology Scaling drives down the cost

• **Scaling:** At each new node, all geometrical features are reduced in size to 70% of the previous node.

• **Reward:** Reduction of *circuit size by half.*
  – Twice number of circuits on each wafer
  – Cost per circuit is reduced significantly.

Moore’s Law  It’s not technology! → It’s economy.

\[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

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*In 1978, a commercial flight* between New York and Paris cost around $900 and took seven hours. If the principles of Moore’s Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.

• **Ways to Huge Profits**
  – High performance and Low Cost
  – Achieved by making everything SMALLER
“Microelectronics” = μm-scale electronics

“Nanotechnology” = nm-scale “stuff”
Strained Silicon $I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2$

Silicon is placed on substrate having large atomic spacing

Methods of straining
- Burried SiGe – Biaxial
- Uniaxial Stress S/D SiGe
Technology Trend

2003  90 nm
2005  65 nm
2007  45 nm
2009  32 nm
2011  22 nm

Invented SiGe Strained Silicon  2nd Gen. SiGe Strained Silicon  Invented Gate-Last High-k Metal Gate  2nd Gen. Gate-Last High-k Metal Gate  First to Implement Tri-Gate

Strained Silicon

Product

45 nm Process Technology
Pentium Intel® Core™ Microarchitecture
TICK

32 nm Process Technology
Nehalem NEW Intel® Microarchitecture
TOCK

Westmere Intel® Microarchitecture (Nehalem)
TICK

Sandy Bridge NEW Intel® Microarchitecture
TOCK

Ivy Bridge Intel® Microarchitecture (Sandy Bridge)
TICK

Intel’s First 22 nm Processor

Performance

Drive Current (mA/um)

1.5
1.0
0.5
0.0
1000
Gate Pitch (nm)
100

Technology

Channel Strain
Ge concentration

130nm  90nm  65nm  45nm  32nm

Source: www.intel.com

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Thin Depletion Layer - Problem

- $Q_G = Q_i + Q_b$
- Charge sharing
Current in MOSFET

- $I_{off}$ is not zero $\rightarrow$ Standby Power Loss

The diagram shows the relationship between $I_D$ (drain current), $V_{GS}$ (gate-to-source voltage), and $V_t$ (threshold voltage). The log scale indicates the non-linear nature of the MOSFET's current-voltage characteristics.
Short Channel – Big Problem

MOSFET becomes “resistor” at small L.

Chenming Hu, “Modern Semiconductor Devices for ICs” 2010, Pearson
Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.
Good Old MOSFET has reached its Limits

- Ioff is bad
- Size and dopant variations

High Vdd, Power, Design Cost
What can we do?

![Diagram showing Gate, Source, Drain, and Leakage Path]
Intel will use 3D FinFET at 22nm

Most radical change in decades

There is a competing SOI technology
One Way to Eliminate Si Far from Gate

**Thin body controlled**
By multiple gates.

FinFET body is a thin Fin.

N. Lindert et al., DRC paper II.A.6, 2001
40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.

X. Huang et al., IEDM, p. 67, 1999
Introduced New Scaling Rule

Leakage is well suppressed if

Fin thickness < Lg

<table>
<thead>
<tr>
<th>10nm Lg</th>
<th>AMD</th>
<th>2002 IEDM</th>
</tr>
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<tbody>
<tr>
<td>5nm Lg</td>
<td>TSMC</td>
<td>2004 VLSI</td>
</tr>
<tr>
<td>3nm Lg</td>
<td>KAIST</td>
<td>2006 VLSI</td>
</tr>
</tbody>
</table>

NiSi
Poly-Si
220Å SiO2

Si fin
Lg=10nm

Gate
State-of-the-Art 14nm FinFET

Transistor Fin Improvement

Taller and Thinner Fins for increased drive current and performance

Source: Anandtech

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2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI)

Source | UTB | Drain
--- | --- | ---
SiO2 | | Si


Drain Current [A/um]

Gate Voltage [V]

T_{si}=8nm
T_{si}=6nm
T_{si}=4nm

1.E-12 1.E-10 1.E-08 1.E-06 1.E-04 1.E-02
FDSOI Roadmap

- From a global cooperation ST-IBM-LETI have enabled an FD-SOI 3-node roadmap.

![FD-SOI Roadmap Diagram](image-url)
Main Differences

**FinFET**
- Body thickness $< L_g$
- Investment by fab
- Has larger Ion

**UTB-SOI**
- Thickness $< \frac{1}{3} L_g$
- Investment by SOI suppliers
- Has good back-gate bias option
Compact Modeling or SPICE Modeling

- Excellent Convergence
- Simulation Time – ~\(\mu\)sec
- Accuracy requirements
  – ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

Good model should be
- **Accurate:** Trustworthy simulations.
- **Simple:** Parameter extraction is easy.

Balance between accuracy and simplicity depends on end application
BSIM-CMG and BSIM-IMG

- Berkeley Short-channel IGFET Model
- First industry standard SPICE model for IC simulation
- Used by hundreds of companies for IC design since 1997
- BSIM FinFET model became industry standard in March 2012

It’s Free
**BSIM-IMG:** Length scaling @ low Vds

Vbg = 1.0V

Vbg = -1.0V

**UTBBSOI FET, Tsi=12nm**

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Common-Multi-Gate Modeling

- Common Multi-gate (BSIM-CMG):
  - All gates tied together
  - Surface-potential-based core I-V and C-V model
  - Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates
Global fitting with 30nm–10µm FinFETs
What Next?

Transistor Pathway

Si/Ge Gate All Around (GAA) Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET
Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

Vertical TFET
Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP

Source: Applied Materials
Modeling of III-V FinFET

Quantum Capacitance Modeling

Modeling of III-V FinFET

Forward Looking Modeling of 2D Semiconductor FET

ID-VG
VD = 2 V

GM-VG
Joint Development & Collaboration

• Working closely with universities/companies on model development and support
Upcoming Book on FinFET Model

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects
Summary

• Future is beyond imagination.
• Challenges
  – Technology – Hardware and Software
  – Need Innovation
• Opportunities
  – Entrepreneurship
  – Research
  – Jobs (private/public)
• Knowledge economy
Are you ready?

Present

Future