High Performance Transistors: Present & Future trends

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Outline

• Semiconductor industry
• What is semiconductor
  – MOSFET and Scaling
  – Multigate Transistors
    • FinFET
    • Thin-Body Transistor
• Compact Modeling of FinFET and UTB FET
• What next?
Semiconductor Industry

- One of the key driving force in today’s global economy.
- >$300 billion industry.

Types of semiconductor companies

Integrated Device Manufacturers (IDMs)
- Integrated Device Manufacturers (IDMs) have their own fabs to fully or partially support their product manufacturing.

Fabless Companies
- Fabless companies have no manufacturing capabilities, and have to outsource all the manufacturing activities from foundries.

Pure-players (Foundries)
- Pure-players (foundries) have no intention to design their own ICs, even though they may also design some simple IP blocks, and ESD devices for I/O.
Global semiconductor companies ranking (2013) – dynamic industry!

<table>
<thead>
<tr>
<th>Rank</th>
<th>Company</th>
<th>Headquarters</th>
<th>Type</th>
<th>Revenue</th>
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<tr>
<td>1</td>
<td>Intel</td>
<td>U.S.</td>
<td>IDM</td>
<td>~$48B</td>
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<tr>
<td>2</td>
<td>Samsung</td>
<td>South Korea</td>
<td>IDM</td>
<td>~$33B</td>
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<td>3</td>
<td>TSMC</td>
<td>Taiwan</td>
<td>Foundry</td>
<td>~$19B</td>
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<td>4</td>
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<td>U.S.</td>
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<td>SK Hynix</td>
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<td>Toshiba</td>
<td>Japan</td>
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<td>TI</td>
<td>U.S.</td>
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<td>9</td>
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<td>IDM</td>
<td>~$8B</td>
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<td>U.S.</td>
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<td>13</td>
<td>AMD</td>
<td>U.S.</td>
<td>Fabless</td>
<td>~$5B</td>
</tr>
</tbody>
</table>

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Device engineering groups in a typical IDM

TCAD Support Group (T)

Process Integration Group (T)

ESD Design Group (T)

Device Design Group (T)

Reliability Group

IC Design Group

Packaging Group

Compact Modeling Group (T)

Process Design Kit Group

T-TCAD users
Process flow of analog and power technology development

- Results from previous technologies and other measurements can serve as a guideline.
- Engineers should foresee the future need (2–5 years), to make sure the new technology is neither too advanced (costly!) nor too conservative (obsolete even before release!).
- Keep applications in mind.
- **The choice of technology node is an important but risky task.**

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What is semiconductor?
Semiconductor Devices – MOSFET
Devices to circuits

- NOT gate
- Flip-flop
- Full Adder
- Memory
Today’s ICs

Multiple metal layers

3D ICs

System in Package (SIP)

Enabling Technologies
- Flip Chips
- Multi-Chip Modules
- 3-D Packaging

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How do you make these?

Start

Silicon Crystals

Bunny Suits!

10B Transistors per cm²

Silicon “Wafers”

$5B Fabrication Facility

Finish
Building block – (tiny) MOSFET!

- MOSFET is a transistor used for **amplifying** or **switching** electronic signals.
Invention of Transistor

• First Transistor (1947-1948) at AT&T’s Bell Labs
  – Point Contact Transistor
  – First transistor was bipolar contact transistor
  – Material – Germanium
Invention of Transistor

- Inventors
  - Walter H. Brattain (1902–1987)
  - John Bardeen (1908–1991)
  - William B. Shockley (1910–1988)
Silicon Valley

- Started with Shockley Semiconductor in 1956
Integrated Circuit (IC)

- IC – Electronic circuit manufactured on the surface of a thin substrate of semiconductor material.
- Additional materials are deposited and patterned to form interconnections between semiconductor devices.
- Jack Kilby (at Texas Instruments) demonstrated first working IC in 1958.
  - Jack Kilby was awarded the Nobel Prize in Physics 2000.
Building Block – Tiny MOSFET!

Desired
- High $I_{ON}$
- Low $I_{OFF}$

Barrier height is controlled by gate voltage
$n(E) \propto \exp(-E/kT)$

$IDS$ controlled by $V_{GS}$

Inverse slope is subthreshold swing, $S$ [mV/dec]
Bulk MOSFET

• Drain current in MOSFET (ON operation)

\[ I_{ON} = \frac{W}{L} \mu C_{ox} (V_{DD} - V_{TH})^2 \]

• Drain current in MOSFET (OFF operation)

\[ I_{OFF} \propto 10^{\left(\frac{V_{GS}-V_{TH}}{S}\right)} \]

• Desired

• High \( I_{ON} \) (↓L, ↑Cox, ↑\( V_{DD}-V_{TH} \))
• Low \( I_{OFF} \) (↑\( V_{TH} \), ↑\( S \))

\( C_{ox} = \varepsilon_{ox}/t_{ox} = \text{oxide cap.} \)
\( S = \text{Subthreshold slope} \)
Technology Scaling

- Each time the minimum line width is reduced, we say that a new technology node is introduced.

- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.
Technology Scaling

• Scaling – At each new node, all geometrical features are reduced in size to 70% of the previous node.

• Reward – Reduction of circuit size by half. (~50% reduction in area, i.e., $0.7 \times 0.7 = 0.49$.)
  – Twice number of circuits on each wafer
  – Cost per circuit is reduced significantly.

• Ultimately – Scaling drives down the cost of ICs.
Scaling and Moore’s Law

• Number of components per IC function will double every two years – April 19, 1965 (Electronics Magazine)
• Shorthand for rapid technological change!

Source: http://www.intel.com/pressroom/kits/events/moores_law_40th/
Moore’s Law:
The defining features of the integrated circuit technology (size, speed, cost) follow an exponential growth pattern over time.

Moral: Computing power ↑ while cost ↓ exponentially!
Moore’s Law

It’s not technology! → It’s economy.

• Ways to Huge Profits
  – High performance and Low Cost
  – Achieved by making everything SMALLER

The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore’s Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.
1 Nano-$ / Transistor!

Can any other industry match it?

2x per 18 months decrease

Average Transistor Cost (Cents)

Year

Ways to drive performance & decrease cost?

• Closer distance between elements – *Pitch*
• *Faster* signal transfer and processing rate
• For the same Chip size (thus material cost), *more functionality*
• *Mass production*
  – Wafer size is doubled every 10 years.
  – Currently it’s 300mm.
• Use less energy (or *less power*) to achieve the same function
Technology Scaling
(Cost, Speed & Power Consumption)

• In the last 45 years since 1965
• *Price* of memory/logic gates has dropped 100 million times.
  – Rapid price drop has stimulated *new applications*.
• The primary engine that powered the proliferation of electronics is “*miniaturization*”.
• More circuits on each wafer → cheaper circuits.
• Miniaturization has also been instrumental to the improvements in *speed and power consumption* of ICs.
Threshold Voltage Roll-Off

V_t decreases at very small L_g. It determines the minimum acceptable L_g because I_off is too large when V_t becomes too low or too sensitive to L_g.
Channel Length Modulation

Pinch off point moves towards the source as $V_{ds}$ increases

$$I_{Dsat} \propto \frac{1}{L - \Delta L} \approx \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right)$$

$$I_{Dsat} = I_{Dsat0} \left(1 + \frac{\Delta L}{L}\right) = I_{Dsat0} \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right)$$

This model is simple and acceptable for some digital applications

More Accuracy for better $g_{ds}$ matching

$$\Delta L = l \ln\left(\frac{V_{ds} - V_{dsat}}{l E_{sat}} + \frac{E_m}{E_{sat}}\right)$$

$g_{ds}$ reduces

$g_{ds} = \frac{dI_{dsat}}{dV_{ds}}$
Velocity Saturation

State of the art MOSFET, channels are short enough to cause velocity saturation.

Long channel current is well predicted by model.

For short channel, current is saturated well below $V_{dsat}$.

Measured carrier velocity

Long channel behavior

Modeling

$E < E_c$, $v = \mu E$ : For low field, velocity is proportional to mobility.

$E > E_c$, $v = \mu E_c = V_{sat}$: High $E_{\text{vertical}}$ ----> Low $\mu$ ----> High $E_c$
Subthreshold slope

- It is defined as the amount of gate voltage required to change the gate current by 1-decade.

\[ S = \frac{dV_{GS}}{d(\log I_{ds})} \]

\[ S = \frac{kT}{q} \ln(10) \left( 1 + \frac{C_{dep}}{C_{ox}} \right) \]

At room temperature

\[ S = (25.85)(2.30) \left( 1 + \frac{C_{dep}}{C_{ox}} \right) \approx 60mV \left( 1 + \frac{C_{dep}}{C_{ox}} \right) \]
Subthreshold slope

- Minimum value of $S$ is 60mV/decade.
- $I_{\text{off}}$ is determined by $V_{\text{TH}}$ and $S$.
- If $I_{ds}$ at $V_{\text{TH}}$ is $100nA \frac{W}{L}$

$$I_{ds}(nA) = 100 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nkT/q}} = 100 \frac{W}{L} 10^{\frac{V_{GS}-V_{TH}}{S}}$$

- To minimize $I_{\text{off}}$
  - Increase $V_{\text{TH}}$ – Not good as $I_{\text{ON}}$ decreases (low speed!)
  - Reduce $S$
    - Increase $C_{ox}$ – Thin oxide
    - Decrease $C_{\text{dep}}$ (Increase $W_{\text{dep}}$) – Use substrate bias or low doping
    - Decrease Temperature – cost?

\[ S = \frac{kT}{q} \ln(10) \left( 1 + \frac{C_{\text{dep}}}{C_{ox}} \right) \]
Channel Engineering : Lateral Non Uniform Doping

The encroachment of depletion layer in the channel is the prime cause of Vt Roll off

Sol: Control depletion region by increasing doping of the substrate, but will have adverse effect on other parameters

Locally increase doping near S/D : Halo doping

Okumura et al, “Novel Source to Drain Non Uniformly Doped channel MOSFET for High Current Drivability and Threshold Voltage Controllability”, IEDM, 1990
Strained Silicon \( I_{ON} = \frac{W}{L} \mu C_{ox} (V_{DD} - V_{TH})^2 \)

Silicon is placed on substrate having large atomic spacing

Methods of straining
- Burried SiGe
- Biaxial
- Uniaxial Stress S/D SiGe
High-K Metal Gate Technology

- “The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s” - Moore

What is HKMG

\[ C_{ox} = \frac{\varepsilon_{ox} \cdot \varepsilon_0}{T_{ox}} \]

\( T_{ox} \downarrow \), \( C_{ox} \) increases

- Better Gate Control
- Gate Leakage Increases

\( C_{ox} \) can alternatively be increased by using high K material: HKMG

\( \text{Lateral and vertical dimensions squeezed} \)
High-K Metal Gate Technology

Intel began volume production of HKMG in 2008 at 45nm

Metal Gate
- Increases the gate field effect

High-k Dielectric
- Increases the gate field effect
- Allows use of thicker dielectric layer to reduce gate leakage

HK + MG Combined
- Drive current increased >20%
  (>20% higher performance)
- Source-drain leakage reduced >5x
- Gate oxide leakage reduced >10x

 Requires interface engineering

High K Material used – HfO₂

EOT @ 45nm = 1.0nm
@ 32nm=0.9nm
Technology Trend

2003: 90 nm
2005: 65 nm
2007: 45 nm
2009: 32 nm
2011: 22 nm

Invented SiGe Strained Silicon
Invented 2nd Gen. SiGe Strained Silicon
Invented 2nd Gen. Gate-Last High-k Metal Gate
First to Implement Tri-Gate

Strained Silicon
High-k Metal Gate
Tri-Gate

Product

Performance

Drive Current (mA/um)

Technology

Channel Strain
Ge concentration

130nm 90nm 65nm 45nm 32nm

1.5
1.0
0.5
0.0

1000 650 450 320 220

PMOS

10/31/2014

Source: www.intel.com

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Wasn’t that smooth ride?

- Where is the bottleneck?

\[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

- \( V_{TH} \) can’t be decreased – why?
Thin Depletion Layer - Problem

- $Q_G = Q_i + Q_b$
- Charge sharing
Current in MOSFET

- $I_{\text{off}}$ is not zero $\Rightarrow$ Standby Power Loss

$V_{GS}$ $V_t$ $I_{DS}$ $I_{\text{off}}$
Short Channel – Big Problem

MOSFET becomes “resistor” at small $L$.

Chenming Hu, “Modern Semiconductor Devices for ICs” 2010, Pearson
Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.
Good Old MOSFET has reached its Limits

- Ioff is bad
- Size and dopant variations

High Vdd, Power, Design Cost
What can we do?

Gate

Source - Drain

Leakage Path
May 4, 2011
The New York Times Front Page

• Intel will use 3D FinFET at 22nm

• Most radical change in decades

• There is a competing SOI technology

Intel Increases Transistor Speed by Building Upward
By JOHN MARKOFF
Published: May 4, 2011

HILLSBORO, Ore.—Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

The transistors on computer chips—whether for PCs or smartphones—have been designed in essentially the same way since 1959 when Robert Noyce, Intel’s co-founder, and Jack Kilby of Texas Instruments independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.
One Way to Eliminate Si Far from Gate

Thin body controlled
By multiple gates.

FinFET body is a thin Fin.

Gate Length

Source
Drain

Gate

N. Lindert et al., DRC paper II.A.6, 2001
40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.

X. Huang et al., IEDM, p. 67, 1999

66mV/dec
Introduced New Scaling Rule

Leakage is well suppressed if

Fin thickness < Lg

10nm Lg   AMD
2002 IEDM

5nm Lg   TSMC
2004 VLSI

3nm Lg     KAIST
2006 VLSI
Two Improvements Since 1999

- **2002** FinFET with thin oxide on Fin top
  F.L. Yang et al. (TSMC) 2002 IEDM, p. 225.

- **2003** FinFET on bulk substrate
  T. Park et al. (Samsung) 2003 VLSI Symp. p. 135.
State-of-the-Art 14nm FinFET

Transistor Fin Improvement

Taller and Thinner Fins for increased drive current and performance

Source: Anandtech

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2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI)

Ultra Thin Body on Thin Box

• Problem in thin BOX without Back-Plane: Depleted zone can extend under the BOX.
  – Increased short channel effects compared to Bulk devices.

• Benefit of Thin BOX with Back-Plane:
  – Doped & Biased Back Plane eliminates this depletion effect under the BOX.

High K-HfZrO₂, EOT=1.4nm, L₉=32nm, Lₜ₇=10nm, Nₜ₇=10¹⁹ cm⁻³, Tsi=7nm
Compact Modeling or SPICE Modeling

- Excellent Convergence
- Simulation Time – ~μsec
- Accuracy requirements – ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG

- Good model should be
  - **Accurate**: Trustworthy simulations.
  - **Simple**: Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application
Industry Standard Compact Models

• Standardization Body – Compact Model Coalition

• CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

• CMC is by the industry and for the industry
BSIM-CMG and BSIM-IMG

• Berkeley Short-channel IGFET Model

• First industry standard SPICE model for IC simulation

• Used by hundreds of companies for IC design since 1997

• BSIM FinFET model became industry standard in March 2012

It’s Free
Common-Multi-Gate Modeling

• Common Multi-gate (BSIM-CMG):
  – All gates tied together
  – Surface-potential-based core I-V and C-V model
  – Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates
BSIM-CMG

Global fitting with 30nm–10µm FinFETs
Modeling of Germanium FinFETs @10nm

• Ge FinFET may be used in 10nm node for better P-FinFET.
• Industry standard BSIM FinFET model can now model Ge FinFET.
• Early availability of a unified Si/Ge FinFET model facilitates technology-circuits co-development.
**Verification of Ge FinFET Model**

- Due to the lower $m^*$ of holes in Ge the charge-centroid is farther away from the oxide interface resulting in a weaker SR scattering.

- Ge mobility has a weaker dependence on $E_{\text{eff}}$ up-to ~0.5 MV/cm as the impact of SR scattering is only seen at much higher $E_{\text{eff}}$ in Ge as compared to Si.

Modeling of **InGaAs FinFET @10nm**

$L = 20 \text{ nm}, H = 30 \text{ nm}, W = 20 \text{ nm}, N_{\text{fin}} = 4.$

Data from: J. J. Gu et al. IEDM 2012

Transistor Pathway

Si/Ge Gate All Around (GAA) Vertical or Horizontal
- Improved electrostatics
  - Precision etch and CMP
  - Scaled metals
  - High Aspect Ratio ALD

III-V FinFET
- Improved mobility
  - Epi structure
  - III-V gate interface
  - New material CMP

Vertical TFET
- Improved SS
  - Epi structure
  - Multi-pass CMP
  - Precision etch & CMP
Future devices – Beyond CMOS

Power challenge

Scaling down of both the $V_{DD}$ and $V_T$ maintains same performance ($I_{ON}$) by keeping the overdrive ($V_{DD} - V_T$) constant.

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Adrian Ionescu et al., Nature 2011
Future devices – Beyond CMOS

• Alternate channel material
Future devices – Beyond CMOS

Suspended Gate/body FET

Tunnel FET

Magnetic devices

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My Two years at IIT Kanpur

- Received IBM Faculty Award (2013)
- Awarded Ramanujan Fellowship (2012)
- **Group:** Postdoc–1, Ph.D.–7, M.Tech–6, R.A.–4
- **Funding > Rs. 3crore**
  - Device Characterization Lab (1.75crore)
  - Upgraded computational infra. (50Lac)
- **Collaboration:** >20 companies/labs

**Publications:**
10 journal papers, 13 conference papers, 10 invited talks
Joint Development & Collaboration

- Working closely with universities/companies on model development and support
FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects
Summary

• Future is beyond your imagination.

• Challenges
  – Technology – Hardware and Software
  – Need Innovation

• Opportunities
  – Entrepreneurship
  – Research
  – Jobs (private/public)

• Knowledge economy
Check my homepage!

- **Recent publications**

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