FinFET Modeling for 10nm and beyond
- Si, Ge and III-V channel

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About me

• Joined IIT Kanpur in 2012
• Awarded Ramanujan Fellowship (2012)
• Received IBM Faculty Award (2013)
• **Funding**
  – Device characterization laboratory (1.75 crore)
  – Upgraded computational infra.
• **Group**: Postdoc–3, Ph.D.–9, M.Tech–8, R.A.–3
• Collaboration: >25 companies/universities

Publications in last 3 years:
• 17 journal papers
• 18 conference papers

Lab website – [http://www.iitk.ac.in/nanolab](http://www.iitk.ac.in/nanolab)
Joint Development & Collaboration

• Working closely with universities/companies on model development and support
Outline

• Bulk MOSFET and Scaling

• FinFET and Compact Modeling

• Unified Compact Model for arbitrary geometry

• What next?
IC industry for >40 years

- Closer distance between elements – *Pitch*
  - *Faster* signal transfer and processing rate
- For the same Chip size (or cost), *more* functionality
- *Mass production* – Wafer size doubled every 10 years.
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - *Price* of memory/logic gates has dropped 100 million times.
- The primary engine that powered the proliferation of electronics is “*miniaturization*”.
- More circuits on each wafer → cheaper circuits.
- Miniaturization is key to the improvements in *speed and power consumption* of ICs.

It’s not technology! → It’s economy.
Why divorce after 40 years?

- $Q_G = Q_i + Q_b$
- Charge sharing

Short Channel — Big Problem

Source: Chenming Hu
Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.
MOSFET in sub-22nm era

**FinFET**  
**FDSOI**

### New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

#### Traditional Transistor
- Planar conductive area
- Silicon substrate

#### New Intel Transistor
- Conductive area is expanded on three sides of a raised fin

The new transistor with its raised fin requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

### Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices

New platform enables planar FD technology, the only planar solution to sustain Moore’s law.

*From the Semicon West trade show, San Francisco, July 12, 2010* – The Soitec Group (Euronext Paris), the world’s leading supplier of engineered substrates for the microelectronics industry, announced today that the company is ready with the Ultra-Thin Buried Oxide (UTBOX) extension to its Ultra-Thin (UT) silicon-on-insulator (SOI) platform, thereby providing a robust substrate solution for chip designers tackling the performance, power and density challenges of mobile consumer devices. Fully Depleted (FD) planar body transistors are now recognized as the right path on the CMOS roadmap for the 22nm generation and beyond. With FD planar transistor technology on UTBOX wafers, chip designers can enhance their usual design flows and techniques. High-volume capacity is available for the 22nm node at Soitec’s manufacturing sites in France and Singapore.

“Soitec is ready with the UTBOX wafers for planar FD architectures: the infrastructure, the process maturity, yield and the capacity are all in place to support demand,” said Soitec president and chairman, André-Jacques Auberton-Hervé. “Industry leaders confirm that FD planar technology is the right choice for mobile consumer products, which need higher performance without compromising power. Our UTBOX offering shows the critical role our materials play as the starting point for energy-efficient, state-of-the-art electronics.”
One Way to Eliminate Si Far from Gate

**Thin** body controlled
By multiple gates.

FinFET body is a thin Fin.

![Diagram](image)

N. Lindert et al., DRC paper II.A.6, 2001

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Transistor Compact Model

Is the vehicle of information transfer

Technology

- Fast
  - \(\sim 10\mu s / \text{bias point}\)
- Accurate
  - \(\sim 1\% \text{ error}\)

EDA / Design

- Robust
  - Crash free for all circuits.

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Compact Model is Art Based on Science

Output Conductance
Current Saturation
Quantization
Gate Current
GIDL Current
Impact Ionization Current
Noise models
S/D Resistance
Gate Resistance
Mobility and Transport
Short Channel Effects
Inversion Layer Thickness
Non-Quasi-Static Effects
Substrate RC Network
Parasitic Diode, BJT
Self Heating
Temperature Effects
Proximity Effects
Random Variations
Overlap Capacitances
Fringe Capacitances

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BSIM-CMG: Industry standard FinFET model

- Selected as Industry standard 2012

FinFETs on Bulk and SOI Substrates
BSIM-CMG

- Common Multi-gate (BSIM-CMG):
- All gates tied together

- Surface-potential-based core I-V and C-V model
- Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates

Y. S. Chauhan et. al., Workshop on Compact Modeling, 2011, Boston.
Verification: 30nm to 10µm FinFETs

Each curve is for one Lg

Symbols: Data; Lines: BSIM-CMG Model
$g_m'$ & $g_m''$ of 30nm to 10µm FinFETs
Temperature Model verified for FinFET

Drain Current ($\mu$A) vs. $V_{gs}$ (V)

-50C $\rightarrow$ 200C in steps of 50C

Increasing T

$L_g$ = 60nm
20 fins

Drain Current (A) vs. $V_{gs}$ (V)

-50C $\rightarrow$ 200C in steps of 50C

Increasing T

$L_g$ = 60nm
20 fins
FinFET’s Various Complex Cross-Sections

TSMC, IEDM 2010

IBM, VLSI 2012

Leti, VLSI 2012

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Prior Models Available for Two Simple Cross-Sections Only – Deductive model

1. **Double-Gate FinFET:**

Charge Equation:

\[
V_G - V_{FB} + \frac{t_{ox}}{2\varepsilon_{ox}} Q_d - V = -\frac{t_{ox}}{2\varepsilon_{ox}} Q_e \\
+ v_T \ln \frac{Q_e (Q_e + Q_d) / (4v_T\varepsilon_{si}/W_{si})}{q \frac{n_i^2}{N_{si}} W_{si} \left[ 1 - \exp \frac{W_{si}}{4v_T\varepsilon_{si}} (Q_e + Q_d) \right]}
\]

2. **Cylindrical FinFET:**

Charge Equation:

\[
V_G - V_{FB} + \ln(1+t_{ox}/R) \frac{Q_{d,Cy}}{2\pi\varepsilon_{ox}} - V = -\ln(1+t_{ox}/R) \frac{Q_{e,Cy}}{2\pi\varepsilon_{ox}} \\
+ v_T \ln \frac{-Q_{e,Cy}}{q \frac{n_i^2}{N_{si}} \pi v_T R^2} + v_T \ln \frac{-(Q_{d,Cy}+Q_{e,Cy})/4\varepsilon_{si}\pi}{1-\exp \frac{Q_{d,Cy}+Q_{e,Cy}}{4\varepsilon_{si}\pi v_T}}
\]

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New Unified Model for Complex FinFET Cross-Sections – Inductive model

\[ v_G - v_O - v_{CH} = -q_m + \ln(-q_m) + \ln\left(\frac{q_t^2}{e^{-q_t} - q_t - 1}\right) \]

\[ v_O = v_{FB} - q_{dep} - \ln\left(\frac{2qn_i^2 A_{ch}}{n_T C_{ins} N_{ch}}\right) \]

\[ q_t = (q_m + q_{dep}) \frac{A_{ch} C_{ins}}{\varepsilon_{ch} W^2} \]

Model Parameters:

- Fin Area: \( A_{ch} \)
- Channel Doping: \( N_{ch} \)
- Channel Width: \( W \)
- Insulator Cap: \( C_{ins} \)

Unified Model for various Fin shapes

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Even FinFET with this “fin” shape

J. P. Duarte et. al., SRC TECHCON 2014.
Experimental FinFET Example: I-V

*FinFET fabricated by SEMATECH

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BSIM-CMG Model Speed Improvement

- Model Speed Improvement ~ 30%
- New core model used in BSIM-CMG109

<table>
<thead>
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<th></th>
<th>Calls</th>
<th>Total*</th>
<th>Bias-indep</th>
<th>Temp-dep</th>
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<th>SPE</th>
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<td>61.59</td>
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</tbody>
</table>

*Total = Bias-indep + Temp-dep + Bias-dep + Loading
*Bias-indep = SPE + Rest

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3D Model for Short Channel Effects

- SCEs are 3-D effects
  - Need to solve the 3-D Poisson’s equation.

\[ \nabla^2 \psi(x, y, z) = -\frac{q N_{ch}}{\varepsilon_{ch}} \]

- DIBL Equations:
  \[ \Delta V_{TH} = f(\vec{V}, \lambda) \quad SS = g(\vec{V}, \lambda) \]

\( \lambda \): characteristic field penetration length

\[ \lambda_{DG} \approx \frac{\varepsilon_{ch} T_{ch} t_{ins}}{\varepsilon_{ins}} \]

K. Suzuki, EDL 1996

\[ \lambda_{C_y G} \approx \sqrt{\frac{2 \varepsilon_{ch} R^2 \ln (1 + \frac{t_{ins}}{R})}{\varepsilon_{ins}}} \]

C. P. Auth, EDL 1997

Unified \( \lambda \)
TCAD FinFET Example: I-V: Scaling

Bulk FinFET
Lines: Model
Symbols: TCAD
Vds = 0.05 V

LG = 1000, 500, 100, 75, 50 nm

HFin = 40 nm, EOT = 1 nm
TFin, top = TFin, base = 15 nm, VDS = 0.5 V
TFin, top = TFin, base = 15 nm, VDS = 1 V
TFin, top = 15 nm, TFin, base = 25 nm, VDS = 0.5 V
TFin, top = 15 nm, TFin, base = 25 nm, VDS = 1 V

\[ \lambda \approx \sqrt{\frac{\varepsilon_{ch} A_{ch}}{C_{ins}}} \]
Experimental FinFET on Bulk Example:
New QM Effects + Body Bias model

Lines: Old BSIM-CMG

Lines: New BSIM-CMG

QM Improvement

Bulk effect Improvement

C_{gg}

\[ V_g \]

Gate Voltage (V)
State-of-the-Art 14nm FinFET

Taller and Thinner Fins for increased drive current and performance

Source: Anandtech
Future – 10nm and beyond

Transistor Pathway

Si/Ge Gate All Around (GAA)
Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET
Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

Vertical TFET
Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP

Source: Applied Materials
Key points for 10nm and beyond

• Reduced leakage – Better sub-threshold slope
  – Ultra-thin channel
  – Electrostatic control → Nanowire transistor

• Higher mobility channel
  – Si NMOS and PMOS
  – Ge PMOS
  – SiGe
  – III-V materials NMOS – InAs, InGaAs etc.

\[ I_{off} \ (nA) = 100 \frac{W}{L} \times \frac{V_{TH}}{S} \]

\[ I_{dsat} = \frac{W}{2L} C_{ox} \mu_{eff} (V_{gs} - V_t)^2 \]
InGaAs FinFET Modeling

- BSIM-CMG with the new Quantum Effects model used to model InGaAs FinFETs

\[ L = 20 \text{ nm}, \ H = 30 \text{ nm}, \ W = 20 \text{ nm}, \ N_{\text{fin}} = 4. \]

InGaAs FinFET Modeling

L = 20 nm, H = 30 nm, W = 20 nm, Nfin = 4.

Data from: J. J. Gu et al. IEDM 2012

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InGaAs FinFETs with Triangular Cross-section

High mobility InGaAs-(111) channel + Multi-Gate structure w/ -OI substrate on Si

T. Irisawa et al. IEDM 2013

Importance of accurate modeling of Quantum Effects
Modeling of **Germanium FinFETs @10nm**

- Ge FinFET may be used in 10nm node for better P-FinFET.
- Industry standard BSIM FinFET model can now model Ge FinFET.
- Early availability of a unified Si/Ge FinFET model facilitates technology-circuits co-development.
Modeling Germanium FinFETs

• User selectable MOD to model Ge FinFETs
  – Material Mode “MTRLMOD” = Si (Default) or Ge
• “MTRLMOD”=Ge invokes new mobility model for Ge
• MTRLMOD = Ge sets key parameters for Ge
  – Band-Gap, Mobility …
• MTRLMOD=Ge model verified with experimental data
  – Excellent Model Calibration Results
  – Scalable Ge FinFET Model
• Due to the lower $m^*$ of holes in Ge the charge-centroid is farther away from the oxide interface resulting in a weaker SR scattering.
• Ge mobility has a weaker dependence on $E_{\text{eff}}$ up-to $\sim 0.5$ MV/cm as the impact of SR scattering is only seen at much higher $E_{\text{eff}}$ in Ge as compared to Si.
BSIM-CMG Model Results for Ge pFinFETs


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BSIM-CMG Model Scalability for Ge pFinFETs

L varying from 20 nm to 90 nm

Scalable Model

L increasing

L varying from 20 nm to 90 nm

Scalable Model
Forward Looking Modeling of Pillar/Nanowire FET

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Validation on Asymmetric Nanowire FET

Symbols – experimental data

Ids-Vgs for N-type Nanowire for different temperatures

S. Venugopalan et. al., "Modeling Intrinsic and Extrinsic Asymmetry of 3D Cylindrical Gate/ Gate-All-Around FETs for Circuit Simulations", IEEE Non-Volatile Memory Technology Symposium, Shanghai, China, Nov. 2011.
Modeling of III-V FinFET

Fig. 1. Schematic showing sidewall channels and 2-DEG channel in AlGaN/GaN based FinFET devices; (a) Wide fin-width device, (b) Narrow fin-width device [12].


Fig. 3. Subthreshold behaviour of model with experimental data [12], for $W_{fin}=80\text{nm}$, $120\text{nm}$, $140\text{nm}$, $180\text{nm}$ and $200\text{nm}$ and $L_g = 1.0\mu\text{m}$. Drain current is normalized with total gate width $(W_{fin} + 2H_{fin})$, where $H_{fin} = 120\text{nm}$.
7nm & beyond – Would it be a smooth ride?

- Effects in ultra-thin Si/Ge/III-V Transistors
  - Quantum Capacitance
  - Charge centroid
  - Source to Drain Tunneling
  - Bandgap variation with thickness
  - Effective mass variation with thickness
Quantum Capacitance

- Concept of the quantum capacitance was given by S. Luryi, which originates when vertical electric field partially penetrates the inversion charge in channel.
- The quantum capacitance depends on 2-D density of states $\rho_{2D} = \frac{m^*}{\pi \hbar^2}$ and valley degeneracy factor ($g_v$).
- Quantum Capacitance
  \[ C_Q = \frac{q^2 g_v m^*}{\pi \hbar^2} \]
Thin body device is a 2D system.
Quantum Capacitance & III-V

- Very strong impact on gate capacitance with low effective mass channel
Charge centroid

- Charge centroid in conjunction with Quantum capacitance can deteriorate C-V further.
Modeling of Quantum Capacitance in III-V FinFET

Avirup Dasgupta et. al., “Modeling of Quantum Capacitance in III-V Transistors”, being submitted in IEEE EDL.
Source to Drain Tunneling in III-V FETs

• Under the barrier transport

\[ T(E) = \exp \left( \frac{-2}{\hbar} \int \sqrt{2m^*_e(E_{\text{barrier}}(x) - E)} \, dx \right) \]

Fig. 2. Bandstructure of 2.43 nm thick InAs slab (16 atomic layers) calculated using DFT \( (m^*_e = m_{DFT} = 0.0944 m_0, E_g = 0.91 \text{ eV}) \). Insert: InAs Bulk Bandstructure \( (m^*_e = m_{Bulk} = 0.023 m_0, E_g = 0.35 \text{ eV}) \)


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Modeling SiGe FinFETs with Thin Fin

• Current Dependent Source/Drain Resistance


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High Mobility channel

- Different materials for NMOS and PMOS
  - Complex integration
- NMOS
  - III-V materials NMOS – InAs, InGaAs etc.
- PMOS
  - Ge PMOS
  - SiGe
- Bulk mobility of Ge = 4000 > Si 1450 cm^2/V-s
- How about using Ge based CMOS?
First Experimental Demonstration of Ge CMOS Circuits from Purdue (IEDM 2014)

Fig. 1. Illustration of GeOI device under discussion. The device has channel length L=50nm, thickness TSI=15nm, EOT1=1.5nm, EOT2=4.0nm. In this letter, we are modeling the GeOI devices with industry standard BSIM-IMG model, which is a surface potential based model.

BSIM-IMG vs. Experimental Ge circuit

Ge CMOS Inverter VTC

Fig. 3. BSIM-IMG model validation with GeOI CMOS inverter for \( V_{DD} \) ranging from 0.2V to 1.4V: (a) Voltage transfer characteristics, (b) CMOS inverter gain vs input voltage, and (c) device characteristics simulated with parameter set optimized for \( I_{DS}-V_{DS} \). The BSIM-IMG accurately models the inverter behaviour, especially for \( V_{DD} \) up to 1V. It is important to note that the static characteristics are available up to \( V_{DD} = 1V \), and the model is optimized till that bias range. Inverter gain is an important parameter as it determines noise margin, and is a function of \( g_m \) and \( g_{ds} \) which are accurately modeled. Inset figure in (c) compares \( I_{DS} \) obtained from \( I_{DS}-V_{GS} \) measurement and extracted from \( I_{DS}-V_{DS} \), highlighting the device degradation. It is observed that the threshold voltage shift is more prominent in PMOS as compared to NMOS.

FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects

Available online on Elsevier.
Relevant Publications


• C. Yadav, A. Agarwal, Y. S. Chauhan, "Simulation study of gate capacitance with back bias effects in III-V UTB devices", SRC TECHCON, Austin, USA, September 2015.


