Fundamentals and Recent Progress in Negative Capacitance Transistors

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Current members – 30
- Postdoc – 3
- Ph.D. – 19
- Seven PhD graduated

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<thead>
<tr>
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<tbody>
<tr>
<td>Books</td>
<td>1</td>
<td></td>
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<td>1</td>
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<tr>
<td>Journal</td>
<td>13</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>9</td>
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<tr>
<td>Conference</td>
<td>11</td>
<td>19</td>
<td>11</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

Funding:
DST, SERB, CSIR, ISRO, DRDO, SRC, IBM, UCB, CMC, Maxlinear, ...

Equipment: DST-FIST, IITK, UP Govt.

Device Characterization Lab
- Pulsed IV/RF
- PNA-X 43.5GHz
- High Power IV
- Load Pull, Noise Analyzer
Nanolab@IITK: From Theory to Applications

**Theory**
- Materials
- Atomistic Sim.
- Semiconductors
- Transport

**Applications**
- Fabrication
- Characterization
- SPICE Models
- Circuit Design
Joint Development & Collaboration
What is a Compact Model?
Compact MOSFET Model

J_{ds} = f_{1}(V_{ds}, V_{gs})

C_{gs} = f_{3}(V_{gd}, V_{gs})

C_{gd} = f_{2}(V_{gd}, V_{gs})

Compact Model

TCAD Model
Compact Modeling or SPICE Modeling

- Excellent Convergence
- Simulation Time – \(\sim \mu\text{sec}\)
- Accuracy requirements – \(\sim 1\%\) RMS error after fitting
- Example: BSIM-BULK, BSIM-CMG, BSIM-IMG

Good model should be
- **Accurate:** Trustworthy simulations.
- **Simple:** Parameter extraction is easy.

Balance between accuracy and simplicity depends on end application

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Industry Standard Compact Models

• Standardization Body – Compact Model Coalition

• CMC Members – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

http://www.si2.org/cmc/
Challenges in Compact Modeling

- **Materials** (Si, Ge, III-V)
- **Physics** (Quantum Mechanics, Transport)
- **Maths/Computer Sc.** (Compiler, Function speed, implementation, algorithms, smoothing, integration, PDE)
- **Electronics** (Circuit considerations – Digital/Analog/RF/noise)

**SPICE Model**
Some Snapshots from recent work
BSIM Family of Compact Device Models


BSIM1,2 BSIM3

BSIM4

Conventional MOSFET

BSIM5 BSIM-BULK

Silicon on Insulator MOSFET

BSIM-CMG BSIM-IMG

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model
Modeling of TMD transistor

- 2D density of state
- Fermi–Dirac statistics
- Trapping effects

Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

C. Yadav et. al., Compact Modeling of Charge, Capacitance, and Drain Current in III-V Channel Double Gate FETs, IEEE TNANO, 2017.
Modeling of Quasi-ballistic Nanowire FETs

Key features of the model

- **Geometry**: The model is valid for different cross-section geometries captured through effective $C_g$ and $W_{eq}$.
- **Material**: Different materials are taken into account through $n^*$, mobility, and band gap parameters.
- **Doping**: The model works for both, p- and n-type dopings.

- **Subband quantization**: The model takes multiple subbands into account.
- **Thickness**: Effects of semiconductor thickness scaling is built into diffusive to ballistic regimes.
- **Quasi-ballistic**: The model is valid from drift-diffusive to ballistic regimes.
- **Temperature**: Characteristic features of 1D electrostatics at different temperatures are captured.


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Fig. 12: Circular quasi-ballistic InAs nanowire: Drain current as a function of the gate and drain voltages for n-type InAs nanowires, with a circular cross-section ($r = 7.5nm$), $L_g = 100nm$ and $EOT = 0.92nm$ (Device 5)\[44\], are shown in (a) and (b) respectively. Device works in the quasi-ballistic regime. Relevant parameter values are specified in Table II. Short channel effect related parameters have been used as in \[19\], \[20\].
FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

Chapters

1. FinFET- from Device Concept to Standard Compact Model
2. Analog/RF behavior of FinFET
3. Core Model for FinFETs
4. Channel Current and Real Device Effects
5. Leakage Currents
6. Charge, Capacitance and Non-Quasi-Static Effect
7. Parasitic Resistances and Capacitances
8. Noise
10. Benchmark tests for Compact Models
11. BSIM-CMG Model Parameter Extraction
12. Temperature Effects
Industry Standard FDSOI Compact Model BSIM-IMG for IC Design

Chapters

1. Fully Depleted Silicon on Oxide Transistor and Compact Model
2. Core Model for Independent Multigate MOSFETs
3. Channel Current Model With Real Device Effects in BSIM-IMG
4. Leakage Current and Thermal Effects
5. Model for Terminal Charges and Capacitances in BSIM-IMG
6. Parameter Extraction With BSIM-IMG Compact Model
7. Testing BSIM-IMG Model Quality
8. High-Frequency and Noise Models in BSIM-IMG
News (March 2018)

- Our ASM-GaN-HEMT Model is world’s first industry standard SPICE Model for GaN HEMTs
- Download – http://iitk.ac.in/asm/

Si2 Approves IC Design Simulation Standards for Gallium Nitride Devices

March 14, 2018 / 0 Comments / in Compact Model, Frontpage /

Si2 Approves Two IC Design Simulation Standards for Fast-Growing Gallium Nitride Market

Compact Model Coalition Models Expected to Reduce Costs, Speed Time-to-Market

http://www.si2.org/cmc/

http://www.si2.org/2018/03/14/gallium-nitride-models/
Outline

• Motivation
• Understanding Negative Capacitance
• Experimental realization of Negative Capacitance
• NCFETs: Modeling and Analysis
  – MFIS vs MFMIS configurations
    – Long Channel
    – Short Channel
• Performance of NCFET based Circuits
• Conclusion
Power challenge

\[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

\[ I_{OFF} \propto 10^{\left(-\frac{V_{TH}}{SS}\right)} \]

\[ P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC} \]

Scaling both the \(V_{DD}\) and \(V_{T}\) maintains same performance (\(I_{ON}\)) by keeping the overdrive (\(V_{DD} - V_{T}\)) constant.


A. M. Ionescu, Kathy Boucart, “Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch”, IEDM 2009.
Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.

\[ S = \frac{dV_{GS}}{d(\log I_{ds})} \]

\[ = \frac{1}{\text{slope}} = 60 \text{mV/decade} \]

As \( 1 + \frac{C_S}{C_{\text{ins}}} \geq 1 \), \( S \geq 60 \text{mV/decade} \)
Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as

  1: \( C_{\text{ins}} = \left( \frac{\partial^2 G}{\partial P^2} \right)^{-1} \) = inverse curvature of free energy density

  2: \( C_{\text{ins}} = \frac{\partial P}{\partial E} \) = slope of the polarization vs electric field curve

\( P \) = Polarization in dielectric, \( G \) = Free energy density, \( E \) = Externally applied electric field

- Two types of non-linear dielectrics:
  - Paraelectric: No polarization when electric field is removed.
  - Ferroelectric: Two possible states of polarization when electric field is removed.
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!
  
  \[ C_{\text{ins}} < 0 \] and \[ \frac{C_S}{C_{\text{ins}}} < 0 \], then \[ 1 + \frac{C_S}{C_{\text{ins}}} < 1 \rightarrow S < 60\text{mV/decade} \]

- For a capacitor
  
  - Energy \( G = \frac{Q^2}{2C} \rightarrow \text{Capacitance } C = \frac{1}{\frac{d^2G}{dQ^2}} = \frac{1}{\text{Curvature}} \)

Capacitance Definition

Charge-Voltage Relation

\[ C = \frac{dQ}{dV} \]

If \( C < 0 \) \( \rightarrow \) As \( V \downarrow \), \( Q \uparrow \)

More Definitions

Capacitance of a general dielectric:

\[ C = \left( \frac{\partial^2 G}{\partial Q^2} \right)^{-1} \]

Inverse curvature of free energy density

\[ G = \text{Free energy density} \]

Para- and Ferro-electric Materials

• **Paraelectric**: No polarization when electric field is removed.

• **Ferroelectric**: Two possible states of polarization when electric field is removed – Spontaneous/Remnant Polarization.
Ferroelectricity

Requirements:
• Spontaneous electric polarization: Non-Centrosymmetricity (for crystalline materials)
• Reversible polarization state by the application of electric field

e.g. Lead titanate PbTiO$_3$, HZO

Centrosymmetric: Paraelectric

Non-Centrosymmetric: Ferroelectric

$P=0$ at $E=0$

$E=0$

$P \neq 0$ at $E=0$

---

Paraelectric to Ferroelectric Phase Transition

e.g. Pb[Zr$_x$Ti$_{1-x}$]O$_3$ Lead Zirconium Titanate (PZT)

Paraelectric phase

T > $T_C$
Cubic

Ferroelectric phase

T < $T_C$
Tetragonal

$T_C$ = Curie Temperature

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Landau-Khalatnikov Theory of Non-Linear Dielectrics

• Free energy of a non-linear dielectric is given as
  \[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]

• In general, \( \alpha \) and \( \beta \) can be +ve or –ve but \( \gamma \) is always +ve for stability reasons.

• Dynamics of \( G \) is given by
  \[ \delta \frac{dP}{dt} = -\frac{\partial G}{\partial P} \]
  \( \delta = \) Polarization damping factor

• In the steady state, \( \frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \)

For \( \alpha > 0 \) and at \( E = 0 \), there exit only one real root

\[ P = 0 \]

A Paraelectric Material

For \( \alpha < 0 \) and at \( E = 0 \), there exit three real roots

\[ P = 0, \pm P_r \text{ where } P_r = \frac{\sqrt{\beta^2 - 3\alpha\gamma - \beta}}{3\gamma} \]

A Ferroelectric Material has a non-zero \( P \) at zero \( E \).
Assumptions

Free energy of a non-linear dielectric

\[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]

• Polarization and Electric field are uniaxial. (perpendicular to electrodes)
• Polarization and Electric field magnitudes are uniform throughout the ferroelectric.
• Piezo-electricity is ignored.
L-K explanation of Phase Transition

For $E = 0$, $G = \alpha P^2 + \beta P^4 + \gamma P^6$ and $\alpha = \alpha_0 (T - T_0)$, $\alpha_0 > 0$

Paraelectric Material

$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

- $\alpha > 0$ i.e. for $T > T_0$; at $E = 0$, there exists only one real root, $P = 0$
- i.e. No polarization when electric field is removed

$[P = 0 \text{ at } E = 0]$

Ferroelectric Material

$0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5$

- $\alpha < 0$ i.e. for $T < T_0$; at $E = 0$, there exist three real roots $P = 0, \pm P_r$ where

$$P_r = \sqrt[3]{\frac{\sqrt{\beta^2 - 3\alpha\gamma} - \beta}{3\gamma}}$$

- Two possible states of polarization when electric field is removed.

Positive and Negative Capacitances

**Paraelectric**
A Positive Capacitor

**Ferroelectric**
A Conditionally Negative Capacitor

Only one solution at $E = 0$.

Three possible solutions at $E = 0$.

$P = 0$ is not possible in an isolated Ferroelectric due to maxima of energy or a negative capacitance.

\[ C_{ins} = \left( \frac{\partial^2 G}{\partial P^2} \right)^{-1} = \frac{\partial P}{\partial E} < 0 \]
Application of Electric Field

\[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]
\[ E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

![Diagram of electric field and polarization](image)

Paraelectric
[A Positive Capacitor]

Isolated Ferroelectric
[A Conditionally Negative Capacitor]


How to stabilize a Negative Capacitance?

Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

Total energy of the FE + DE system

\[ G = G_f + G_d \]

\[ Q = \varepsilon_0 E_f + P_f = \varepsilon_0 E_d + P_d \]

Assuming V is small

\[ Q \approx P_f \approx P_d \]

\[ \Rightarrow \frac{\partial^2 G}{\partial Q^2} = \frac{\partial^2 G_f}{\partial Q^2} + \frac{\partial^2 G_d}{\partial Q^2} \]

For a stable system

\[ \frac{\partial^2 G}{\partial Q^2} > 0 \text{ (minimum)} \]

\[ \Rightarrow \frac{1}{C_{tot}} = \frac{1}{C_f} + \frac{1}{C_d} > 0 \]

For a stable system

\[ |C_f| > C_d \]

\[ C_{tot} = \frac{C_d \cdot |C_f|}{|C_f| - C_d} > 0 \]

\[ C_{tot} > C_d \]

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Negative Capacitance in Ferroelectric

Negative slope region can be stabilized if

\[ \frac{1}{C_{ins}} = C_{fe} \]

or,

\[ |C_{fe}| > C_{S} \]

\[ C_{total} = \left( \frac{1}{-|C_{fe}|} + \frac{1}{C_{S}} \right)^{-1} > 0 \]

How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

\[
\frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0
\]

- \(C_{DE} < |C_{FE}|\) and \(C_{FE} < 0\)

- \(C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0\)

A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011


**Total Capacitance of Ferroelectric-dielectric hetero-structure becomes greater than the dielectric capacitance.**

\[
C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0
\]
Ferroelectric-Resistor System

NC is observed only for a small duration (~μs) during polarization switching.

Difficult to stabilize.

First ever demonstration of S-curve

Hoffmann et al. *IEDM*, Dec 2018

Negative Capacitance FETs

$\text{PbZr}_{0.52}\text{Ti}_{0.48}\text{O}_3$ FE with HfO$_2$ buffer interlayer

$\text{P(VDF}_{0.75}\text{-TrFE}_{0.25})$ Organic Polymer FE

HfZrO FE
CMOS compatible FE


J. Jo et al., Nano Letters, 2015

K.-S. Li et al., in IEEE IEDM, 2015.
NCFET Structures

**MFMIS Structure**

- **Metal Ferroelectric Metal Insulator Semiconductor**
- **NC-FinFET**
  - Material: $\text{Hf}_{0.42}\text{Zr}_{0.58}\text{O}_2$
  - $L_g = 30$ nm
- Reference: [Li et al. IEDM '15]

**MFIS Structure**

- **Metal Ferroelectric Insulator Semiconductor**
- **MFIS**
  - $t_{fe} = 1.5$ nm
- **PZT**
  - $V_{int}(x)$
- **13 mV/decade**
- **Lg = 10 µm**
- Reference: [Lee et al., IEDM '16]

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**46 mV/decade**
- Reference: [Rusu et al. IEDM '10]

**13 mV/decade**
- Reference: [Dasgupta et al., IEEE JESCDC, '15]

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**52 mV/decade**
- Reference: [Lee et al., IEDM '16]
MFMIS NCFET Modeling

MFMIS Structures

• Metal internal gate $\rightarrow$ equipotential surface with a spatially constant $V_{\text{int}}$.

• Ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire $\rightarrow$ Simplified modeling.
Device Structure

Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)

- Metal internal gate provides an equipotential surface with a spatially constant $V_{\text{int}}$.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.
Experimental Calibration of L-K Model

\[ \delta \frac{dP}{dt} = \frac{dG}{dP} \]

In the steady state, \( \frac{dP}{dt} = 0 \)

\[ E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

\( P = Q - \varepsilon E \approx Q \) (Gate Charge)

\( \alpha = -1.23 \times 10^9 \text{ m/F} \)
\( \beta = 3.28 \times 10^{10} \text{ m/F} \)
\( \gamma = 0 \) (2nd order phase transition)


Calibration of Baseline FinFET

Calibration of baseline FinFET with 22 nm node FinFET.

BSIM-CMG model is used to model baseline FinFET.

Gate length (L) = 30nm, Fin height (Hfin) = 34nm, Fin thickness (Tfin) = 8nm

Complete Modeling Flowchart

\[
E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5
\]

\[
P = Q - \varepsilon E \approx Q \text{ (Gate Charge)}
\]

\[
V_G
\]

\[
V_{int} = V_G - V_{fe}
\]

Landau-Khalatnikov Model of ferroelectric
Verilog-A Code

BSIM-CMG Model of FinFET
Verilog-A Code

\[
I_D \quad Q_G
\]
Capacitances and Voltage Amplification

\[ E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

\[ V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5) \]

\[ C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)} \]

\[ \frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}} \]

Internal Voltage Gain,

\[ A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}} \]

Capacitance matching between \(|C_{fe}|\) and \(C_{int}\) increases the gain.
Capacitance Matching

- Capacitance matching increases with $t_{fe}$ which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.

- Increase in $V_D$ reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.
$
I_D - V_G$ Characteristics – SS region

- As $t_{fe}$ increases
  - Capacitance matching is better
  - $C_S$ and $C_{ins}$ are better matched

$$S = \left(1 - \frac{C_S}{|C_{ins}|}\right) \cdot 60\text{mV/dec}$$

- As $t_{fe} \uparrow \rightarrow \text{SS} \downarrow$
**I_D-V_G Characteristics – ON region**

- As $t_{fe}$ increases
  - Capacitance matching is better

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, $I_{ON}$ increases.

Note the significant improvement in $I_{ON}$ compared to SS.
**$I_D-V_G$ Experimental Demonstration**

**M. H. Lee et al., in IEEE JEDS, July 2015.**

**K. S. Li et al., in IEEE IEDM, 2015**

**J. Zhou et al., in IEEE IEDM, 2016.**

**D. Kwon et al., in IEEE EDL, 2018**

**Jing Li et al., in IEEE EDL, 2018**
**I_D-V_D Characteristics**

- NCFET is biased in negative capacitance region.
  - \( Q_G \) or \( P \) is positive \( \rightarrow \) \( V_{fe} \) is negative.

- \( V_{DS} \uparrow \) \( \rightarrow \) \( Q_G \) or \( P \downarrow \) \( \rightarrow \) \( |V_{fe}| \downarrow \) \( \rightarrow \) \( V_{int} = V_G + |V_{fe}| \downarrow \) \( \rightarrow \) \( A_V \downarrow \) \( \rightarrow \) Current reduces

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Experimental Demonstration

1.5 nm HZO
Compatible with sub-10nm technology node

M. H. Lee et al., *IEDM*, pp. 12.1.1–12.1.4., 2016


K. S. Li et al., in *IEEE IEDM*, 2015

K. S. Li et al., in *IEEE IEDM*, 2018

14nm node NCFinFET by Global Foundries


Negative DIBL

- $V_D$ reduces $Q_G$ which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with $t_{fe}$ due to increased $V_{fe}$ drop.
- $V_{th}$ increases with $V_D$ instead of decreasing.
  - Higher $I_{ON}$ still lower $I_{OFF}$!
Negative DIBL/DIBR Effect

\( V_D \uparrow, Q_G \downarrow, V_{fe} \uparrow, V_{int} \downarrow, V_{th} \uparrow \)

- \( V_{th} \) increases with \( V_D \) instead of decreasing. Higher \( I_{ON} \) still lower \( I_{OFF} \).
- Negative DIBL increases with \( t_{fe} \) due to increased \( V_{fe} \) drop.


Xu et al., *ACS Nano*, 2018

I_D-V_G Characteristics – High V_DS

- Hysteresis appears for |C_{fe}| < C_{int} which is the region of instability.

- As t_{fe} increases
  - SS reduces, I_{ON} increases.
  - I_{OFF} reduces for high V_D.

- Width of hysteresis at larger thicknesses can be controlled with V_D.
Negative Output Differential Resistance


Mengwei Si et al., Nature Nanotechnology, 2018

J. Zhou et al., IEEE, JEDS, 2018

J. Zhou et al., IEDM 2016
Optimum NC-FinFET

- Same $I_{ON}$ as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- $V_{DD}$ reduction by 0.4 V.
- $I_{OFF}$ reduction by 83%.

Ferroelectric Parameters Variation

If $\gamma = 0$,

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{P_r^3}$$

- Low $P_r$ and high $E_c$
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase $I_{ON}$ but reduce $I_{OFF}$ due to a more negative DIBL $\Rightarrow$ high $I_{ON}/I_{OFF}$.

$P_r$ = Remnant Polarization
$E_c$ = Coercive Field

$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$

Intrinsic Delay

\[ \text{Delay, } \tau = \frac{\Delta Q_G}{I_{ON}} \]

\[ \Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD}) \]

- NC-FinFET driving NC-FinFET
  - For high \( V_{DD} \), high \( I_{ON} \) advantage is limited by large amount of \( \Delta Q_G \) to be driven.
  - Outperforms FinFET at low \( V_{DD} \).
  - Minimum at \( V_{DD} \approx 0.28 \text{ V} \) corresponds to a sharp transition in \( Q_G \).

NC-FinFET driving FinFET load provides full advantage of NC-FinFET.
Power and Energy Delay Products

\[ PDP = \Delta Q_G \cdot V_{DD} \]

\[ EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}} \]

- NC-FinFET driving NC-FinFET shows advantage only for low \( V_{DD} \).
- NC-FinFET driving FinFET load is the optimum choice.
Modeling of MFIS NCFET

Contrast with MFIMS structure:

- \( P \) and \( V_{\text{int}} \) vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models\([1,2]\):
Implicit equations – tedious iterative numerical solutions


Explicit Modeling of Charge

\[ V_{fe} = E_{tfe} = a Q_G + b Q_G^3 \]

Voltage Balance:

\[ V_G - V_{FB} = V_{fe} + \frac{Q_G}{C_{ox}} + \psi_S = a_{eff} Q_G + b Q_G^3 + \psi_S \]

\( Q_G - \psi_S \) relation\(^\text{[1]}\)

\[ Q_G = \text{sign}(\psi_S) \gamma C_{ox} \left[ \psi_S + V_t(e^{-\psi_S/V_t} - 1) \right. \]

\[ + \left. e^{-(2\phi_F + V_C)/V_t} (V_t e^{\psi_S/V_t} - \psi_S - V_t) \right]^{1/2} \]

→ Implicit equation in \( Q_G \)

→ **Goal:** Explicit Model with good initial guesses for each region of NCFET operation

Both the \( Q_G \) and its derivatives match well with implicit model

Drain Current Model Validation

Against Full Implicit Calculations

Against Experimental Data


MFIS Vs MFMIS

- MFIS excels MFMIS for low $P_r$ ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

Compact Modeling of MFIS GAA-NCFET

$$V_{fe} = a_0 Q + b_0 Q^3$$

Radial Dependence in Ferroelectric Parameter:
(Ignored in others work)

$$a_0 = 2aR \ln[1 + t_{fe}/(R + t_{ins})]$$
$$b_0 = 2bR^3[1/(R + t_{ins})^2 - 1/(R + t_{ins} + t_{fe})^2]$$

Mobile Charge Density:

$$Q = \varepsilon_s \left(\frac{d\psi}{d\rho}\right)_{\rho=R} = \left(\frac{2\varepsilon_s}{R}\right) \left(\frac{2kT}{q}\right) \left(\frac{\beta^2}{1-\beta^2}\right)$$

Voltage Balance:

$$V_g - \Delta \phi - \psi_s = (a_0 + 1/C_{ins})Q + b_0 Q^3$$

$\rightarrow$ **Goal:** Explicit Model for $\beta$ with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.
Drain Current Model Validation

Against Full Implicit Calculations

- In contrast to bulk-NCFETs
  - Multi-gate NCFETs with an undoped body exhibit same $I_{OFF}$ and $V_{th}$ due to absence of bulk charges.
  - GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.

Terminal Charges in GAA-NCFET

- Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
- For high $V_{DS}$, the $Q_G$ for GAA-NCFET is saturates to $(4/5)^{th}$ of the maximum value (at $V_{ds} = 0$) in contrast to conventional devices for which it saturates to $(2/3)^{rd}$ of the maximum value.
Comparing $I_D-V_G$ and $I_D-V_D$ Characteristics (long channel)

- MFIS excels MFMIS for low $P_r$ ferroelectrics only, in long channel NCFETs.
Understanding different trends with $P_r$

- Total current in ON regime $\approx$ drift current = inversion charge * horizontal electric field
- For high $P_r$, charge is higher for MFIS, but electric field in channel is low due to a decreasing $V_{int}$ profile from source to drain, which results in lower current than MFMIS.
- For low $P_r$, charge is lower for MFIS, but electric field in channel is high due to a increasing $V_{int}$ profile from source to drain, which results in higher current than MFMIS.

Hysteresis Behavior

- Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
- Source end dipole switches, first, owing to its least hysteresis threshold.
- Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

MFMIS vs MFIS: Short Channel Effects
OFF Regime (low $V_D$)

2D Numerical Simulation Results in COMSOL

NCFETs exhibit reverse trends in $V_t$ and SS with scaling except for very small lengths.


Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.

In MFIS, fringing effect remains localized to channel edges only \(\rightarrow\) Halo Like barriers.

In MFMIS, internal metal extends this effect to the entire channel \(\rightarrow\) larger \(V_t\) than MFIS.

Reverse SS trends with Scaling

\[ SS = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial \psi_c}{\partial \log_{10} I_D} \left( \frac{m}{A_{fe}} \right) \]

\[ m = \frac{\partial V_{int}}{\partial \psi_c} = \text{Body Factor} \]

\[ A_{fe} = \frac{\partial V_{int}}{\partial V_G} = \text{Ferroelectric gain} \]

\[ A_{eff} = m^{-1} A_{fe} = \frac{1}{1 - \frac{C_{int}}{|C_{fe}|}} \]

\[ L \downarrow, \frac{C_{int}}{|C_{fe}|} \uparrow, A_{fe} \uparrow, m \downarrow, A_{eff} \uparrow, SS \downarrow \] (except for very small lengths where \( m \) dominates).

Increasing the spacer permittivity enhances the outer fringing electric field, which leads to a rise in Vt and reduction in SS and DIBL.

OFF Regime (high $V_{DS}$): Negative DIBL

- Negative DIBL effect increases with Scaling.
- More pronounced in MFMIS than MFIS.

Impact of S/D doping

- NCFETs exhibit trends opposite to baseline FET with respect to the increase in $N_D$.
- Strength of fringing field originated from ionized S/D dopant ions increases with $N_D$.


06/21/2019 Yogesh Chauhan, IIT Kanpur
The internal floating metal gate maintains a uniform electrical field distribution throughout the ferroelectric and a uniform potential ($V_{int}$) at ferroelectric-oxide interface.

In the MFIS, however, electric field distribution and $V_{int}$ at the interface are non-uniform.

ON Regime: Electrical Characteristics

\[ P_r = 0.1213 \, \mu C/cm^2 \]

- Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling \( \rightarrow \) lower \( V_{DSat} \) of MFIS results in lower \( I_{DS} \).
- However, internal metal in MFMIS helps \( V_{DS} \) impact to easily reach source side \( \rightarrow Q_{IS} \downarrow \rightarrow \) Larger NDR effect in MFMIS than MFIS.
- In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former for iso-\( V_{FB} \) case only.

ON Regime: Impact of Spacers

- $C_{\text{int}}$ increases with scaling in NCFETs with spacers due to outer fringing capacitances $\rightarrow$ increases gain.
- For W/O spacers, $V_{\text{int}}$ decreases due to absence of outer fringing, uncompensated drain side inner fringing, and increased drain to channel coupling.

Impact of Quantum Mechanical Effects

- The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.


Impact of Ferroelectric Thickness

- NC influence decreases with $t_{fe}$ which also starts to homogenise the internal gate potential.

- Thus, relative difference between MFIS and MFMIS diminishes as $t_{fe}$ is decreased.

Does polarization damping really limit operating frequency of NC-FinFET based circuits?

Recent Demonstration by Global Foundries on 14nm NC-FinFET

- Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power\(^1\).
- Another theoretical study predicted intrinsic delay due to polarization damping in NCFET to be very small (270 fs)\(^2\).

\(^1\) Krivokapic, Z. et al., IEDM 2017

Fig. 3: TEM picture of minimum gate length RMG with 8nm FE. The inset shows the crystallinity of the FE film.

Fig. 13: Active power of FO3 inverter RO vs. effective SS for \(V_{dd} = 1.05\) V.

Fig. 14: Active power of NCFET FO3 inverter RO with \(W_n = W_p = 360\) nm, \(L = 14\) nm.
• Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

NC-FinFET based SRAM

- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- $P_{\text{avg}}$: NC-SRAM performs better with lower standby leakage only at small $t_{fe}$, taking advantage of the lower subthreshold currents

Effects of NCFET on standard cells: 7nm FinFET standard cell library

- Increasing $t_{fe}$ – larger $A_v$ in transistors (i.e., steeper slope and higher ON current) $\rightarrow$ Delay of cells become smaller.
Effects of NCFET on standard cells: 7nm FinFET standard cell library

Using a ferroelectric with 1nm, 2nm, 3nm and 4nm thickness provides a speedup of around 15%, 30%, 40% and 45% respectively, in the delay of gates at the operating voltage of 0.7V.

- Quantifying the relative delay decrease/improvement of cells within the 7nm FinFET standard cell library due to NCFET at $V_{DD} = 0.7V$. 
Effects of NCFET on standard cells: 7nm FinFET standard cell library

- Increase in $t_{fe}$ leads to an increase in the total cells’ capacitance which further increases internal power of the cells.
- Same baseline performance (i.e., frequency) can be achieved at a lower voltage, which leads to quadratic saving in dynamic power and exponential saving in stand-by power, thus, compensating the side effect of NCFET with respect to power.
Effects of NCFET on future processor design

(a) What is the frequency increase due to NCFET under the same voltage constraint?
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?
(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

NC-FinFET based Processor Performance

- NCFET with ferroelectric thickness more than 1nm leads to a noticeable temperature reduction, due to the decrease in the on-chip power density.
NC-FinFET based Processor Performance

Energy harvesting and IOT

- Under very small power budgets harvested from body heat, NCFET technology enables the processor to operate at around 42-127% higher frequency compared to the conventional FinFET technology.
NC-FinFET RF Performance

- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis

NC-FinFET RF Performance

• Current gain ($\propto \frac{g_m}{C_{gg}}$) is almost independent of $t_{fe}$ as both the $g_m$ and $C_{gg}$ increase with $t_{fe}$ almost at a constant rate.
  • Cut-off frequency ($f_T$) remains identical for both the Baseline and NC-FinFET.
• Temperature rise and Power consumption due to self-heating increase with $t_{fe}$ as $I_d$ increases. Reduce $V_{dd}$ to achieve energy efficient performance.
NC-FinFET RF Performance

\[ g_{ds} \] and self heating (\( \Delta G_{SHE} \propto g_{ds}(f) - g_{ds}(dc) \)) both increase with \( t_{fe} \) due to increased capacitance matching between \( C_{fe} \) and \( C_{int} \).

\[ g_{ds} = \frac{\partial l_{ds}}{\partial V_{ds}} = \frac{\partial l_{ds}}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial V_{ds}} = g_{m} \times A_{V}^{D} \]

where \( A_{V}^{D} = \frac{-C_{GDI}}{|C_{fe}| - C_{int}} \)

- Voltage gain \( (A_{V} = g_{m}/g_{ds} = C_{fe}/C_{GDI}) \) decreases with \( t_{fe} \) due to decrease in \( C_{fe} \).
- Maximum oscillation frequency \( (f_{max}) \) also reduces with \( t_{fe} \) which can be compensated by reducing \( V_{dd} \).
Impact of Process Variations

• Variability in $I_{ON}$, $I_{OFF}$, and $V_t$ due to combined impact of variability in $L_g$, $T_{fin}$, $H_{fin}$, EOT, $t_{fe}$, $E_c$, and $P_r$
• $I_{ON}$: Improvement is non-monotonic with $t_{fe}$
• $I_{OFF}$: Decreases monotonically with $t_{fe}$
• $V_t$: Decreases monotonically with $t_{fe}$

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.

11-stage Ring-Oscillator: Variation in \( \tau \) due to combined variation

Open Questions

• Is NC a static or transient phenomenon?
• Physical explanation of NC effect
• Second order effects
  – Impact of grain boundaries and their sizes
  – Impact of multi-domain effects
  – Impact of traps
  – Impact of FE thickness
  – Reliability
• Impact of NDR/NDIBL on circuits
Conclusion

- Maintaining $I_{ON}/I_{OFF}$ is the biggest challenge in new technology nodes
- Negative capacitance FET is one of the best choice
  - Need to find sweet material (HfZrO$_2$?)
  - Integration in conventional CMOS process remains a challenge (lot of progress)
- Compact (SPICE) Models are ready for circuit evaluation
Relevant Publications from our group

Relevant Publications from Our group


Thank You