Physics and Modeling of Nano-Transistors

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Outline

• Compact Modeling
• Bulk MOSFET and FinFET
• Negative Capacitance FET
• ASM-GaN-HEMT Model

My Group and Nanolab

Current members – 35
- Postdoc – 4
- Ph.D. – 19
- Ten PhD graduated

Books

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Journal

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Conference

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Device Characterization Lab
- Pulsed IV/RF
- PNA X 43 GHz
- High Power IV
- Load Pull

Alumni (PhD) of Nanolab

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<td>Girish Pahwa</td>
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<td>Shantanu Agnihotri</td>
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<td>Prateek Jain</td>
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<td>Avirup Dasgupta</td>
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<td>Sheikh Aamir Ahsan</td>
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<td>Harshit Agarwal</td>
<td>Asst. Prof. at IIT Jodhpur</td>
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<td>2017</td>
<td>Pragya Kushwaha</td>
<td>SAC, ISRO</td>
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Compact Modeling – Industrial Research

- **Bulk** MOSFET Modeling (DC to RF)
  - BSIM4 and BSIM6
- **Partially Depleted SOI** MOSFET Modeling (DC to RF)
  - BSIM-SOI
- Multigate MOSFET Modeling
  - FinFET & Nanowire Transistor – BSIM-CMG
  - Fully Depleted SOI (FDSOI) Transistor– BSIM-IMG
- High Voltage LDMOS Modeling using BSIM6 – BSIM-HV
- GaN HEMT Modeling
  - ASM-HEMT: industry standard
- DC, CV and RF Characterization
  - All models are validated on measured data
- Working as BSIM Group member/consultant

Joint Development & Collaboration

Spectrum of Approaches to Analyzing Electronic System

*The “Big Picture”*

Source: Xing Zhou, NTU

Circuit simulation

- Circuit simulation is an important part of any design process.
- Explosive growth of integrated circuit market in the 1970’s resulted in the rise of importance of circuit simulation.
  - With integrated circuits, prototypes were expensive to build and difficult to troubleshoot.
  - As designs became larger and more complicated, the need to use circuit simulators increased.
- Time to market and cost.
SPICE Simulation

• SPICE (Simulation Program with Integrated Circuits Emphasis) is a powerful general purpose circuit simulation program that is used to verify circuit designs and to predict the circuit behavior.

• SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley in early part of 1970.

• SPICE can do several types of circuit analyses.
  • Non-linear DC / Transient analysis, Linear AC Analysis
  • Noise analysis, Sensitivity analysis, Distortion analysis

SPICE Development

• SPICE was developed out of a graduate class project at University of California, Berkeley.

Laurence W. Nagel
Ronald A. Rohrer
Donald O. Pederson


SPICE and Device Models

• Look Up Table – Store measured or simulated data in a table.

• Physical model generally does not have parameters but does not fit with data accurately.

• Empirical models are mathematical models written to reflect measured characteristics
  • Angelov model for HEMT

• Compact SPICE models are the physics based model but parametrized to fit measured data.

Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.

Ron Rohrer
Special Issue on 40th Anniversary of SPICE
SPRING 2011 IEEE SOLID-STATE CIRCUITS MAGAZINE
What is a Compact Model?

Compact model complexity: What’s so hard about fitting Curves?

\[ I = \frac{V}{R} \text{ is a compact model for a resistor} \]

\[ I = V/(q_o + TCR(VTR + T + TR - 25)/(Leff/Weff)) \]

\[ Weff = W + dW \]

\[ Leff = L + dL \]

\[ Jth = \frac{V}{I} \]

\[ Rth = \frac{Rth0}{(Leff/Weff)} + \frac{Rth1}{(Leff/Weff)} + Rth2 \]

Add: Geometric Scaling
Temperature Scaling
Self Heating

PDK and Compact Model

Enablers of a silicon chip design

Source: David HARAMET al. IBM J RES. DEV. MARCH/MAY 2003
Compact Modeling or SPICE Modeling

- Good model should be
  - **Accurate**: Trustworthy simulations.
  - **Simple**: Parameter extraction is easy.
- Balance between accuracy and simplicity depends on end application
- **Excellent Convergence**
- **Simulation Time** – \( \sim \mu \text{sec} \)
- **Accuracy requirements**
  - \( \sim 1\% \) RMS error after fitting
- Example: BSIM-BULK, BSIM-CMG, BSIM-IMG

Medium of information exchange

Industry Standard Compact Models

- **Standardization Body** – Compact Model Coalition
- **CMC Members** – EDA Vendors, Foundries, IDMs, Fabless, Research Institutions/Consortia

Challenges in Compact Modeling

- **Materials** (Si, Ge, III-V)
- **Physics** (Quantum Mechanics, Transport)
- **Maths/Computer Sc.** (Compiler, Function speed, implementation, algorithms, smoothing, integration, PDE)
- **Electronics** (Circuit considerations – Digital/Analog/RF/noise)

Compact Model is Art Based on Science

Outline

- Compact Modeling
- Bulk MOSFET and FinFET
- Negative Capacitance FET
- ASM-GaN-HEMT Model

Bulk MOSFET

- Drain current in MOSFET (ON operation)

\[
I_{ON} = \mu \frac{W}{L} C_{ox} \left( \frac{1}{2} (V_D - V_{TH}) \right)^2
\]

- Drain current in MOSFET (OFF operation)

\[
I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)}
\]

- Desired
  - High \(I_{ON}\) (↓L, ↑Cox, ↑V_D-V_{TH})
  - Low \(I_{OFF}\) (↑V_{TH}, ↑S)

BSIM Family of Compact Device Models

Technology Scaling

- Each time the minimum line width is reduced, we say that a new technology node is introduced.

- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.
IC industry for >40 years

- Closer distance between elements – *Pitch*
- Faster signal transfer and processing rate
- For the same Chip size (or cost), *more functionality*
- Mass production – Wafer size doubled every 10 years.
- Use less energy (or *power*) for same function
- In the last 45 years since 1965
  - Price of memory/logic gates has dropped 100 million times.
- The primary engine that powered the proliferation of electronics is “*miniaturization*”.
- More circuits on each wafer → cheaper circuits.
- Miniaturization is key to the improvements in speed and power consumption of ICs.

*It’s not technology! → It’s economy.*

Wasn’t that smooth ride?

- Where is the bottleneck?
  - $I_{ON} = \mu \frac{W}{L} C_{ox} \frac{1}{2} (V_{DD} - V_{TH})^2$
- $V_{TH}$ and Subthreshold Slope can’t be decreased

Thin Depletion Layer - Problem

- $Q_G = Q_i + Q_b$
- Charge sharing
Short Channel – Big Problem

MOSFET becomes “resistor” at small L.

Chenming Hu, *Modern Semiconductor Devices for ICs* 2010, Pearson

Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.

What can we do?

MOSFET in sub-22nm era

FinFET

FD-SOI

Soitec announces industrial readiness of complete Fully Depleted (FD) platform – Key to higher performance for mobile consumer devices

New platform enables planar FD technology, the only planar solution to sustain Moore’s law from the Semiconductor Trade Show, San Francisco, July 12, 2016 – The silicon foundry leader Unisem, a global leader in silicon wafer fab refurbishment, announced today that the new FD platform is now ready for high-volume manufacturing. The FD platform is designed to meet the needs of high-performance mobile devices such as smartphones, tablets, and servers. The platform is based on the FD-SOI (fully depleted silicon-on-insulator) technology, which is known for its high performance and low power consumption. The FD platform offers performance gains of up to 50% over traditional planar silicon-on-insulator (SOI) technology. The platform is capable of supporting high-performance applications such as artificial intelligence, machine learning, and autonomous driving.
One Way to Eliminate Si Far from Gate

Thin body controlled
By multiple gates.

FinFET body is a thin Fin.

- Gate
- Source
- Drain

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40nm FinFET – 1999

30nm Fin allows 2.7nm SiO2 & undoped body ridding random dopant fluctuation.

- 66mV/dec

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Introduced New Scaling Rule

Leakage is well suppressed if
Fin thickness < Lg

- 10nm Lg AMD 2002 IEDM
- 5nm Lg TSMC 2004 VLSI
- 3nm Lg KAIST 2006 VLSI

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State-of-the-Art 14nm FinFET

Taller and Thinner Fins for increased drive current and performance

Source: Anandtech
2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI)


Another MOSFET architecture – Gate-All-Around or Surround Gate

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- ASM-GaN-HEMT Model

BSIM-CMG and BSIM-IMG

- Berkeley Short-channel IGFET Model
- First industry standard SPICE model for IC simulation
- Used by hundreds of companies for IC design since 1997
- BSIM FinFET model became industry standard in March 2012

It’s Free
BSIM-CMG: Industry standard FinFET model

• Selected as Industry standard 2012

Short Channel (2D) Effects

- Along the channel – 2D
- Quasi-2D analysis

\[ \frac{1}{\rho} \frac{\partial}{\partial r} \left( \frac{\partial \psi}{\partial r} \right) + \frac{\partial^2 \psi}{\partial z^2} = \frac{\Phi_N}{\epsilon_{\text{si}}} \]

Characteristic Length

- Similar expression for Double Gate and FinFET/Trigate
- Analytical expressions model
  - Threshold Voltage roll off
  - Drain induced barrier lowering (DIBL)
  - Sub-threshold swing degradation

Quantum Mechanical Effects

- Predictive model for confinement induced \( V_{th} \) shift due to band splitting present in the model
- Can choose to use an effective \( t_{eq} \) that accounts for charge centroid behavior with bias
- Effective Width model that accounts for reduction in width for a triple / quadruple / surround gate structure

Symbols: TCAD Results; Lines: Model

BSIM-CMG Core Models

- Four device architectures
- Three core models
  - Intrinsic Double Gate Core (Y. Taur et al, IEEE EDL, 2004)
  - Perturbation based DG Core for high-doping
  - Cylindrical Gate Core
- Bulk and SOI Substrate
Verification: 30nm to 10µm FinFETs

Each curve is for one Lg
Symbols: Data; Lines: BSIM-CMG Model

Temperature Model verified for FinFET

FinFET’s Various Complex Cross-Sections

Prior Models Available for Two Simple Cross-Sections Only – Deductive model
1. Double-Gate FinFET:

2. Cylindrical FinFET:
New Unified Model for Complex FinFET Cross-Sections – Inductive model

\[ v_G - v_O - v_{CH} = -q_o + \ln \left( -q_o + \frac{q_i^2}{e^{q_i} - q_i - 1} \right) \]

\[ v_O = v_{CH} - q_{dep} - \ln \left( \frac{2 |q_{dep}|}{q_{ins} v_{CH}} \right) \]

\[ q_i = (q_o + q_{dep}) \left( \frac{A_{CH} C_{dep}}{C_{ch}} e^{-q_{dep} \lambda} \right) \]

Model Parameters:
- Fin Area: \( A_{CH} \)
- Channel Doping: \( N_{CH} \)
- Channel Width: \( W \)
- Insulator Cap: \( C_{ins} \)

Unified Model for various Fin shapes

3D Model for Short Channel Effects

- SCEs are 3-D effects
  - Need to solve the 3-D Poisson’s equation.
- \( V^2 \psi(x, y, x) = -\frac{q N_{CH}}{\varepsilon_{CH}} \)

DIBL Equations:

\[ \Delta V_{TH} = f(\bar{V}, \lambda) \]

\[ SS = g(\bar{V}, \lambda) \]

\[ \lambda: \text{characteristic field penetration length} \]

\[ \lambda_{DG} \approx \frac{\varepsilon_{CH} T_{CH} t_{ins}}{\varepsilon_{ins}} \]

\( K \) Suzuki, 1996

\[ \lambda_{LY} \approx \frac{2 \varepsilon_{CH} R^2 \ln \left( 1 + \frac{t_{ins}}{R} \right)}{\varepsilon_{ins}} \]

\( C. P. Auth, 1997 \)

Unified \( \lambda \)

Experimental FinFET Example: I-V

TCAD FinFET Example: I-V: Scaling
Experimental FinFET on Bulk Example: New QM Effects + Body Bias model

Lines: Old BSIM-CMG
Lines: New BSIM-CMG

QM Improvement
Bulk effect Improvement

$V_g$ vs $C_{gg}$

Modeling SiGe FinFETs with Thin Fin

- Current Dependent Source/Drain Resistance

$R_u = \left(\frac{1}{\mu \tau_{cap}}\right)^{0.5}$

where $I_{src} = Q_C/\tau_{cap}$ is the saturation current in the source region and $R_{u} = \rho_{u} R_{DSS}$ is the body resistance.


FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard

Industry Standard FDSOI Compact Model BSIM-IMG for IC Design
Future – 10nm and beyond

Key points for 10nm and beyond

- Reduced leakage – Better sub-threshold slope
  - Ultra-thin channel
  - Electrostatic control → Nanosheet transistors

- Higher mobility channel
  - Si NMOS and PMOS
  - Ge PMOS
  - SiGe
  - III-V materials NMOS – InAs, InGaAs etc.

\[ I_{\text{off}} (nA) = 100 \frac{W}{L} \frac{\text{Pm}}{T} \]

InGaAs FinFET Modeling

- BSIM-CMG with the new Quantum Effects model used to model InGaAs FinFETs

\[ I_{\text{shunt}} = \frac{W}{2L} C_{\text{as}} \mu_{\text{eff}} (V_{\text{gs}} - V_{\text{t}})^{3} \]

InGaAs FinFETs with Triangular Cross-section

Importance of accurate modeling of Quantum Effects
BSIM-CMG Model Results for Ge pFinFETs

Modeling of GAA Nanowire FET

Validation on Asymmetric Nanowire FET

Modeling of Gate-All-Around FETs


S. Venugopalan et. al., "Modeling Intrinsic and Extrinsic Asymmetry of 3D Cylindrical Gate/ Gate-All-Around FETs for Circuit Simulations", IEEE Non-Volatile Memory Technology Symposium, Shanghai, China, Nov. 2011.

S. Venugopalan et. al., IBM, Nonwire, IEDM 2013

IBM, Stacked Nanosheet, VLSIT 2017
Samsung Multibridge & Twin Nanowire

Samsung, SOI Conf. 2006

Multi-bridge-channel MOSFET

Twin silicon nanowire MOSFET

Stacked GAA Si NW MOSFETs

IMEC, IEDM 2016

TCAD Validation for different cross-sections of GAA Transistors

Ach = 28nm^2, W=18nm, Cin=0.86nF/m

Circular GAA

Ach = 22nm^2, W=18nm, Cin=0.76nF/m

Square GAA

Ach = 14nm^2, W=18nm, Cin=0.73nF/m

Triangular GAA

7nm & beyond – Would it be a smooth ride?

• Effects in ultra-thin Si/Ge/III-V Transistors
  • Quantum Capacitance
  • Charge centroid
  • Source to Drain Tunneling
  • Bandgap variation with thickness
  • Effective mass variation with thickness
Quantum Capacitance

- Quantum capacitance originates when vertical electric field partially penetrates the inversion charge in channel.
- The quantum capacitance depends on 2-D density of states $\rho_{2D} = \frac{m_{||}^*}{\pi \hbar^2}$ and valley degeneracy factor ($g_v$).
- Quantum Capacitance $C_Q = \frac{q^2 g_v m_{||}^*}{\pi \hbar^2}$

Quantum Capacitance in III-V FinFETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands

Modeling of III-V Channel DG-FETs

- Conduction band nonparabolicity
- 2-D density of states
- Quantum capacitance in low DOS materials
- Contribution of multiple subbands
Charge centroid

• Charge centroid in conjunction with Quantum capacitance can deteriorate C-V further.

Modeling of Quasi-ballistic Nanowire FETs

Key features of the model

- Quantum capacitance
- Gate capacitance
- E contribution to C

Outline

• Compact Modeling
• Bulk MOSFET and FinFET
• Negative Capacitance FET
• ASM-GaN-HEMT Model
Microprocessor trends

![Graph showing Microprocessor trends](image)


\[ P = C_L V_{DD} \alpha_f + I_{leak} V_{DD} + P_{SC} \]


Power challenge

- \( I_{ON} = W \frac{L}{C_{ox}} \frac{1}{2} (V_{DD} - V_{TH})^2 \)
- \( I_{OFF} \approx 10^{-10} \frac{(V_{TH})^2}{V_{DD}} \)
- \( P = C_J V_{DD} \alpha_f + I_{leak} V_{DD} + P_{SC} \)

 Scaling both the \( V_{DD} \) and \( V_f \) maintains same performance \( I_{ON} \) by keeping the overdrive \( (V_{DD} - V_f) \) constant.

A. M. Ionescu, Kathy Boucart, “Tunnel FET or Ferroelectric FET to achieve a sub-60mV/decade switch”, IEDM 2009

Subthreshold Swing

- Amount of gate voltage required to change the current by 1-decade.

\[ S = \frac{\partial V_{GS}}{\partial \log I_D} = \frac{\partial V_G}{\partial \log I_D} + \frac{\partial V_D}{\partial \log I_D} \]

As \( 1 + \frac{1}{C_{ins}} \geq 1.5 \geq 60 \text{mV/decade} \)

Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as
  - 1: \( C_{ins} = -\frac{\partial P}{\partial E} \) = inverse curvature of free energy density
  - 2: \( C_{ins} = \frac{\partial P}{\partial E} \) = slope of the polarization vs electric field curve

- Two types of non-linear dielectrics:
  - Paraelectric: No polarization when electric field is removed.
  - Ferroelectric: Two possible states of polarization when electric field is removed.
Negative Capacitance Transistor

• What if insulator has a Negative Capacitance!

$$C_{\text{ins}} < 0$$ and $$\frac{C_{S}}{C_{\text{ins}}} < 0$$, then $$\left(1 + \frac{C_{S}}{C_{\text{ins}}} \right) < 1 \Rightarrow S < 60\text{mV/decade}$$

• For a capacitor

• Energy $$G = \frac{Q^2}{2C}$$ \(\Rightarrow\) Capacitance $$C = \frac{1}{\frac{Q^2}{2G}} = \frac{1}{\text{Curvature}}$$

Para- and Ferro-electric Materials

• Paraelectric: No polarization when electric field is removed.

• Ferroelectric: Two possible states of polarization when electric field is removed –Spontaneous/Remnant Polarization.

Ferroelectricity

Requirements:

• Spontaneous electric polarization: Non-Centrosymmetry (for crystalline materials)
• Reversible polarization state by the application of electric field

e.g. Lead titanate PbTiO₃, HZO

Paraelectric to Ferroelectric Phase Transition

e.g. Pb(ZrxTi1-x)O₃, Lead Zirconium Titanate (PZT)

$$P = 0$$ at $$E = 0$$

$$T > T_C$$ Cubic

$$T < T_C$$ Tetragonal

$$T_C = \text{Curie Temperature}$$
Landau-Khalatnikov Theory of Non-Linear Dielectrics

- Free energy of a non-linear dielectric is given as
  \[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]
  - \( \alpha \) and \( \beta \) can be +ve or –ve but \( \gamma \) is always +ve for stability reasons.
  - Dynamics of \( G \) is given by \( \delta \frac{dP}{dt} = -\frac{\partial G}{\partial P} \)
  - In the steady state, \( \frac{dP}{dt} = 0 \rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \)

For \( \alpha > 0 \) and at \( E = 0 \), there exit only one real root
\[ P = 0 \]
A Paraelectric Material

For \( \alpha < 0 \) and at \( E = 0 \), there exit three real roots
\[ P = 0, \pm P_r \]
A Ferroelectric Material has a non-zero \( P \) at zero \( E \).

L-K explanation of Phase Transition

For \( E = 0 \), \( G = \alpha P^2 + \beta P^4 + \gamma P^6 \) and \( \alpha = \alpha_0(T - T_0), \alpha_0 > 0 \)

Paraelectric Material
\[ 0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]
  - \( \alpha > 0 \) i.e. for \( T > T_c \) at \( E = 0 \), there exists only one real root, \( P = 0 \)
  - i.e. No polarization when electric field is removed
  \[ \{ P = 0 \text{ at } E = 0 \} \]

Ferroelectric Material
\[ 0 = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]
  - \( \alpha < 0 \) i.e. for \( T < T_c \) at \( E = 0 \), there exist three real roots
  \[ P = 0, \pm P_r \]
  where \( P_r = \sqrt{\frac{2\alpha - 3\alpha_0 - \beta}{3\gamma}} \)
  - Two possible states of polarization when electric field is removed.

Assumptions

Free energy of a non-linear dielectric
\[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]

- Polarization and Electric field are uniaxial. (perpendicular to electrodes)
- Polarization and Electric field magnitudes are uniform throughout the ferroelectric.
- Piezo-electricity is ignored.

Positive and Negative Capacitances

For \( E = 0 \), \( P = \delta P + \frac{\partial^2 G}{\partial P^2} \)

- Only one solution at \( E = 0 \)
\[ \alpha > 0 \]
  - \( \alpha > 0 \) i.e. for \( T > T_c \) at \( E = 0 \), there exit only one real root
\[ P = 0 \]
  - Three possible solutions at \( E = 0 \)
\[ P = 0 \text{ is not possible in a isolated Ferroelectric due to maxima of energy or a negative capacitance} \]

Paraelectric
A Positive Capacitor

Ferroelectric
A Conditionally Negative Capacitor

Application of Electric Field

\[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]
\[ E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

Paraelectric
[Positive Capacitor]

Isolated Ferroelectric
[Conditionally Negative Capacitor]

How to stabilize a Negative Capacitance?

Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

For a stable system, \( \frac{\partial^2 G}{\partial Q^2} > 0 \) (minimum)

\[ |C_f| > C_d \]

How to stabilize a Negative Capacitance?

- Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

\[ C_{tot} = C_{fs} + C_{DE} \]
\[ C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0 \]

- \( C_{DE} < |C_{FE}| \) and \( C_{FE} < 0 \)

- \( C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0 \)

Negative Capacitance in Ferroelectric

For a stable system, \( |C_f| > C_d \)

Total energy of the FE + DE system

\[ G = G_f + G_d \]
\[ Q = \epsilon_0 E_f + P_f = \epsilon_0 E_d + P_d \]

Assuming V is small
\[ Q \approx P_f \approx P_d \]

\[ \frac{\partial^2 G}{\partial Q^2} = \frac{\partial^2 G_f}{\partial Q^2} + \frac{\partial^2 G_d}{\partial Q^2} \]
\[ C_{tot} = \frac{C_f}{|C_f|} \cdot \frac{C_d}{|C_d|} > 0 \]

06/15/2020 Yogesh Chauhan, IITK
Ferroelectric-Dielectric Systems

Total Capacitance of Ferroelectric-dielectric hetro-structure becomes greater than the dielectric capacitance.

\[ C_{\text{tot}} = |C_{\text{dielectric}}| > 0 \]

Ferroelectric-Resistor System

NC is observed only for a small duration (~\(\mu s\)) during polarization switching.

Difficult to stabilize.

PZT ferroelectric (\(\text{PbZr}_{0.2}\text{Ti}_{0.8}\text{O}_3\))

First ever demonstration of S-curve

Measuring S-Curve

Negative Capacitance FETs

- PbZr$_{0.52}$Ti$_{0.48}$O$_3$ FE with HfO$_2$ buffer interlayer
- P(VDF$_{0.75}$-TrFE$_{0.25}$) Organic Polymer FE
- HfZrO FE CMOS compatible FE

S. Dasgupta et al., IEEE JEDC, 2015.
J. Jo et al., Nano Letters, 2015
K.-S. Li et al., in IEEE IEDM, 2015.

NCFET Structures

MFMIS Structure

- Metal Ferroelectric Metal Insulator Semiconductor

MFIS Structure

- Metal Ferroelectric Insulator Semiconductor

Device Structure

- Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)

- Metal internal gate provides an equipotential surface with a spatially constant $V_{\text{int}}$.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.

MFMIS NCFET Modeling

- Metal internal gate $\rightarrow$ equipotential surface with a spatially constant $V_{\text{int}}$.
- Ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire $\rightarrow$ Simplified modeling.
Experimental Calibration of L-K Model

Gibb's Energy,
\[ G = \alpha P^2 + \beta P^3 + \gamma P^6 - EP \]

Dynamics of \( G \) is given by
\[ \frac{\delta}{\delta t} = -\frac{\partial G}{\partial P} \]

In the steady state, \( \frac{\delta}{\delta t} = 0 \)

\[ E = \frac{V_{fe}}{t_{fe}} = 2aP + 4\beta P^3 + 6\gamma P^5 \]

\[ P = Q - \epsilon E \approx Q \text{ (Gate Charge)} \]

\( \alpha = -1.23 \times 10^5 \text{ m/F} \)
\( \beta = 3.28 \times 10^{10} \text{ m/F} \)
\( \gamma = 0 \) (2nd order phase transition)


Calibration of Baseline FinFET

BSIM-CMG model is used to model baseline FinFET.

Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

Capacitances and Voltage Amplification

\[ E = \frac{V_{fe}}{t_{fe}} = 2aP + 4\beta P^3 + 6\gamma P^5 \]

\[ V_{fe} = \frac{\partial Q}{\partial V_{fe}} \]

\[ C_{fe} = \frac{1}{t_{fe}(2a + 12\beta Q^2 + 30\gamma Q^4)} \]

\[ 1 = C_{ax} + C_s + C_{drain} + C_{source} \]

Internal Voltage Gain,
\[ A_V = \frac{\partial V_{int}}{\partial V_C} = \frac{V_{fe}}{C_{fe} = C_{int}} \]

Capacitance matching between \( |C_{fe}| \) and \( C_{int} \) increases the gain.
Capacitance Matching

- Capacitance matching increases with $t_{fe}$ which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.
- Increase in $V_D$ reduces the capacitance matching:
  - Reduces gain.
  - Reduces width of hysteresis window.

$\Delta_{SS} = 0.60 \text{mV/dec}$

$I_D-V_G$ Characteristics – SS region

- As $t_{fe}$ increases
  - Capacitance matching is better
  - $C_S$ and $C_{int}$ are better matched

$S = \left(1 - \frac{C_S}{|C_{int}|}\right) \cdot 60 \text{mV/dec}$

- As $t_{fe} \uparrow \rightarrow SS \downarrow$

$I_D-V_G$ Characteristics – ON region

- As $t_{fe}$ increases
  - Capacitance matching is better

$$A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, $I_{ON}$ increases.

Note the significant improvement in $I_{ON}$ compared to SS.

$I_D-V_G$ Experimental Demonstration

M. H. Lee et al., in IEEE IEDM, July 2015.

K. S. Li et al., in IEEE IEDM, 2015.


D. Rusek et al., in IEEE EDL, 2018.

Jing Li et al., in IEEE EDL, 2018.
**I_D-V_D Characteristics**

- NCFET is biased in negative capacitance region.
  - $Q_G$ or $P$ is positive $\Rightarrow V_G$ is negative.
  - $V_{DS} \uparrow \Rightarrow Q_G$ or $P$ $\downarrow \Rightarrow |V_{fe}| \downarrow \Rightarrow V_{int} = V_G + |V_{fe}| \downarrow \Rightarrow A_{v} \downarrow \Rightarrow$ Current reduces


**Negative DIBL**

- $V_D$ reduces $Q_G$ which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with $t_{fe}$ due to increased $V_{fe}$ drop.
  - $V_{th}$ increases with $V_D$ instead of decreasing.
  - Higher $I_{ON}$ still lower $I_{OFF}$.


**Experimental Demonstration**

1.5 nm HZO Compatible with sub-10nm technology node


14nm node NCFinFET by Global Foundries


**Negative DIBL/DIBR Effect**

- $V_{th}$ increases with $V_D$ instead of decreasing. Higher $I_{ON}$ still lower $I_{OFF}$.
- Negative DIBL increases with $t_{fe}$ due to increased $V_{fe}$ drop.

**I<sub>D</sub>-V<sub>G</sub> Characteristics – High V<sub>DS</sub>**

- Hystersis appears for |C<sub>fe</sub>| < C<sub>int</sub> which is the region of instability.
- As t<sub>fe</sub> increases
  - SS reduces, I<sub>ON</sub> increases.
  - I<sub>OFF</sub> reduces for high V<sub>D</sub>.
- Width of hystersis at larger thicknesses can be controlled with V<sub>D</sub>.

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**Negative Output Differential Resistance**

- For low Pr and high Ec
  - reduce |C<sub>fe</sub>| which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I<sub>ON</sub> but reduce I<sub>OFF</sub> due to a more negative DIBL ⇒ high I<sub>ON</sub>/I<sub>OFF</sub>.

---

**Optimum NC-FinFET**

- Same I<sub>ON</sub> as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- V<sub>DS</sub> reduction by 0.4 V.
- I<sub>OFF</sub> reduction by 83%.

---

**Ferroelectric Parameters Variation**

- Low Pr and high Ec
  - reduce |C<sub>fe</sub>| which leads to improved capacitance matching and hence, a high gain.
  - Low SS
  - increase I<sub>ON</sub> but reduce I<sub>OFF</sub> due to a more negative DIBL ⇒ high I<sub>ON</sub>/I<sub>OFF</sub>.
Intrinsic Delay

\[ \Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD}) \]

- NC-FinFET driving NC-FinFET
  - For high \( V_{DD} \), high \( I_{ON} \) advantage is limited by large amount of \( \Delta Q_G \) to be driven.
  - Outperforms FinFET at low \( V_{DD} \).
  - Minimum at \( V_{DD} \approx 0.28 \text{ V} \) corresponds to a sharp transition in \( Q_G \).
- NC-FinFET driving FinFET load provides full advantage of NC-FinFET.

Power and Energy Delay Products

\[ PDP = \Delta Q_G V_{DD} \]
\[ EDP = \frac{(\Delta Q_G)^2}{I_{ON}} \]

- NC-FinFET driving NC-FinFET shows advantage only for low \( V_{DD} \).
- NC-FinFET driving FinFET load is the optimum choice.

Modeling of MFIS NCFET

- \( P \) and \( V_{int} \) vary spatially in longitudinal direction
- Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models\(^{[1,2]}\):
- Implicit equations – tedious iterative numerical solutions

Explicit Modeling of Charge

\[ V_C = E_{It} = aQ_G + bQ_G^3 \]

Voltage Balance:
\[ V_G - V_B = \frac{Q_G}{C_{ox}} + \psi_S = e^{Q_G} + bQ_G^3 + \psi_S \]
\[ Q_G - \psi_S \text{ relation}^{[3]} \]
\[ Q_G = \begin{cases} \text{sign}(V_S) & \text{if } V_S = 0 \text{ or } \psi_S = 0 \\ e^{(\psi_S + \psi_G) / \psi_G} + e^{-\psi_S / \psi_G} - 1 \\ e^{-2\psi_S / \psi_G} + e^{\psi_S / \psi_G} - \psi_S - V_I \end{cases}^{[2]} \]

- Implicit equation in \( Q_G \)
- Goal: Explicit Model with good initial guesses for each region of NCFET operation

Both the \( Q_G \) and its derivatives match well with implicit model

Drain Current Model Validation

Against Full Implicit Calculations

Against Experimental Data


MFIS Vs MFMIS

- MFIS excels MFMIS for low P_r ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.


Compact Modeling of MFIS GAA-NCFET

Voltage Balance:

\[ V_{th} = n_0 Q + h_0 Q^2 \]

Radial Dependence in Ferroelectric Parameter:

\[ n_0 = \frac{2}{(R + t_{ox})} \frac{d}{dR} \left[ \frac{2}{R} \left( \frac{R}{1-R} \right) \right] \]

\[ h_0 = 2d/[(R + t_{ox})^2 - 1/(R + t_{ox} + t_h)^2] \]

Mobile Charge Density:

\[ \bar{Q} = \int_{\alpha}^{\beta} \frac{dP}{dR} dR = \frac{2}{R} \left( \frac{R}{1-R} \right) + \left( 1 - \frac{R^2}{1-R^2} \right) G = 0 \]

Voltage Balance:

\[ V_{th} = \Delta V_F - \bar{Q} = (\alpha + 1/C_{tot})Q + h_0 Q^2 \]

Goal: Explicit Model for \( \beta \) with good initial guess valid in all region of NCFET operation which will be used for further calculation of drain current and terminal charges.

Drain Current Model Validation

Against Full Implicit Calculations

- In contrast to bulk-NCFETs
  - Multi-gate NCFETs with an undoped body exhibit same \( I_{OFF} \) and \( V_{th} \) due to absence of bulk charges.
  - GAA-NCFET characteristics show different bias dependence due to the absence of bulk charge.

Terminal Charges in GAA-NCFET

- Peak in the gate capacitance is observed where the best capacitance matching occurs between the internal FET and the ferroelectric layer.
- For high $V_{DS}$, the $Q_G$ for GAA-NCFET is saturates to $(4/5)th$ of the maximum value (at $V_{ds} = 0$) in contrast to conventional devices for which it saturates to $(2/3)^3$ of the maximum value.

MFMIS Vs MFIS


Comparing $I_D$-$V_G$ and $I_D$-$V_D$ Characteristics (long channel)

- MFIS excels MFMIS for low $P_r$ ferroelectrics only, in long channel NCFETs.

Understanding different trends with $P_r$

- Total current in ON regime = drift current = inversion charge * horizontal electric field
- For high $P_r$, charge is higher for MFIS, but electric field in channel is low due to a decreasing $V_{int}$ profile from source to drain, which results in lower current than MFMIS.
- For low $P_r$, charge is lower for MFIS, but electric field in channel is high due to a increasing $V_{int}$ profile from source to drain, which results in higher current than MFMIS.

**Hysteresis Behavior**

- Continuous switching of dipoles from source to drain results in a smooth hysteresis behavior in MFIS compared to MFMIS where dipoles behave in unison.
- Source end dipole switches, first, owing to its least hysteresis threshold.
- Non-zero drain bias disturbs capacitance matching in MFMIS resulting in a delayed onset of hysteresis.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.


**OFF Regime (low \( V_D \))**

2D Numerical Simulation Results in COMSOL

- NCFETs exhibit reverse trends in \( V_t \) and SS with scaling except for very small lengths.


**Reverse \( V_t \) Shift with Scaling**

- Coupling of inner fringing electric field to the ferroelectric increases with scaling, which increases the voltage drop across ferroelectric and hence, the conduction barrier height.
- In MFIS, fringing effect remains localized to channel edges only → Halo Like barriers.
- In MFMIS, internal metal extends this effect to the entire channel → larger \( V_t \) than MFIS.

Reverse SS trends with Scaling

\[ SS = \frac{\partial V_G}{\partial \log_{10} I_D} = \frac{\partial \psi_c}{\partial \log_{10} I_D} \]  
\[ A_{fe} = \frac{\partial V_{int}}{\partial V_G} \]  
\[ A_{eff} = m^{-1} A_{fe} = \frac{1}{1 - \frac{C_{pol}}{|C_{fe}|}} \]

\[ L, t, C_{pol}, A_{fe} \uparrow, m \downarrow, A_{eff} \uparrow, SS \downarrow \] (except for very small lengths where \( m \) dominates).

OFF Regime (high \( V_{DS} \)): Negative DIBL

- Negative DIBL effect increases with Scaling.
- More pronounced in MFMIS than MFIS.

Impact of S/D doping

- NCFETs exhibit trends opposite to baseline FET with respect to the increase in \( N_D \).
- Strength of fringing field originated from ionized S/D dopant ions increases with \( N_D \).

Impact of Spacer Permittivity

Increasing the spacer permittivity enhances the outer fringing electric field, which leads to a rise in \( V_t \) and reduction in SS and DIBL.
ON Regime: Potential and field distribution

- The internal floating metal gate maintains a uniform electrical field distribution throughout the ferroelectric and a uniform potential (Vint) at ferroelectric-oxide interface.
- In the MFIS, however, electric field distribution and Vint at the interface are non-uniform.


ON Regime: Electrical Characteristics

- Drain side charge pinches-off earlier in MFIS than MFMIS due to strong localized drain to channel coupling → lower VDSat of MFIS results in lower IDS.
- However, internal metal in MFMIS helps Vint impact to easily reach source side → QIS ↓ → Larger NDR effect in MFMIS than MFIS.
- In long channel, MFMIS excels MFIS, however, for short channels vice-versa is true due to substantial NDR effect in former for iso-Vth case only.


ON Regime: Impact of Spacers

- Cint increases with scaling in NCFETs with spacers due to outer fringing capacitances → increases gain.
- For W/O spacers, Vint decreases due to absence of outer fringing, uncompensated drain side inner fringing, and increased drain to channel coupling.


Impact of Quantum Mechanical Effects

- The QME results in an increase in the effective oxide thickness of the internal FET which eventually diminishes the benefits achievable from NC effect for the particular value of ferroelectric thickness.

Impact of Ferroelectric Thickness

- NC influence decreases with $t_{fe}$ which also starts to homogenise the internal gate potential.
- Thus, relative difference between MFIS and MFMIS diminishes as $t_{fe}$ is decreased.


Does polarization damping really limit operating frequency of NC-FinFET based circuits?

- Ring Oscillators with NC-FinFET can operate at frequencies similar to FinFET but at a lower active power[1].
- Another theoretical study predicted intrinsic delay due to polarization damping in NCFinFET to be very small (270 fs)[2].


NC-FinFET based inverters

- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.


NC-FinFET based SRAM

- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- $P_{avg}$: NC-SRAM performs better with lower standby leakage only at small $t_{fe}$, taking advantage of the lower subthreshold currents

Effects of NCFET on standard cells: 7nm FinFET standard cell library

- Increasing $t_{fe}$ – larger $A_c$ in transistors (i.e., steeper slope and higher ON current) → Delay of cells become smaller.

Quantifying the relative delay decrease/improvement of cells within the 7nm FinFET standard cell library due to NCFET at $V_{DD} = 0.7V$.

Effects of NCFET on future processor design

(a) What is the frequency increase due to NCFET under the same voltage constraint?
(b) What is the frequency increase under the same (i.e., baseline) power density constraint?
(c) What is the minimum operating voltage along with the achieved power reduction under the same (i.e., baseline) performance (i.e., frequency) constraint?

NC-FinFET RF Performance

- Baseline Technology: 10 nm node RF FinFET
- RF Parameters extraction using BSIM-CMG model
- BSIM CMG coupled with L-K for NC-FinFET analysis


- Current gain ($\alpha \frac{g_m}{g_d}$) is almost independent of $\tau_{fe}$ as both $g_m$ and $C_{gd}$ increase with $\tau_{fe}$ almost at a constant rate.
- Cut-off frequency ($f_c$) remains identical for both the Baseline and NC-FinFET.
- Temperature rise and Power consumption due to self-heating increase with $\tau_{fe}$ as $I_d$ increases. Reduce $V_{dd}$ to achieve energy efficient performance.

NC-FinFET RF Performance

- Variability in $I_{ON}$, $I_{OFF}$, and $V_c$ due to combined impact of variability in $L_g$, $T_{fin}$, $H_{fin}$, EOT, $t_{fe}$, $F_{ct}$, and $P_r$
- $I_{ON}$: Improvement is non-monotonic with $t_{fe}$
- $I_{OFF}$: Decreases monotonically with $t_{fe}$
- $V_c$: Decreases monotonically with $t_{fe}$

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.

Open Questions

- Is NC a static or transient phenomenon?
- Physical explanation of NC effect
- Second order effects
  - Impact of grain boundaries and their sizes
  - Impact of multi-domain effects
  - Impact of traps
  - Impact of FE thickness
- Reliability, Variability
- Impact of NDR/NDIBL on circuits

Relevant Publications

Outline

• Compact Modeling
• Bulk MOSFET and FinFET
• Negative Capacitance FET
• ASM-GaN-HEMT Model

News (March 14, 2018)

• Our ASM-GaN-HEMT Model is industry standard SPICE Model for GaN HEMTs
• Download – http://iitk.ac.in/asm/

GaN Attractions & Avenues

Size Comparison

Size comparison of Si power MOSFET with GaN HEMT from EPC for same performance

Size comparison of RF HEMTs based on GaAs and GaN technologies from Qorvo

Media Coverage (April 11, 2018)

आईआईटीमें बनाया सिम्यूलेशन सॉफ्टवेयर

Size comparison of Si power MOSFET with GaN HEMT from EPC for same performance

Size comparison of RF HEMTs based on GaAs and GaN technologies from Qorvo

Industry players for power applications as of 2012
GaN HEMT

Some interesting features of III-nitride system:
• Wide bandgap
• High 2-DEG charge density
• High electron mobility
• High breakdown voltage
• Excellent thermal conductivity
• High power density per mm of gate periphery

• GaN HEMTs are able to operate in high frequency, high power as well as high temperature device applications

GaN HEMT Structure

Status of Compact Model – GaN HEMT

CMC candidate models for industry standardization
(Two models selected as industry standard)
• ASM-GaN model: Our Model
• MIT MVSG model: MIT, Prof. D. Antoniadis
Core Model & Parameters

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<td>( n_s )</td>
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<td>Low Field Mobility</td>
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<tr>
<td>( N_{AR} )</td>
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<tr>
<td>( V_{BS} )</td>
<td>AR saturation velocity</td>
<td>157.6 x 3 cm/s</td>
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<tr>
<td>( R_{th} )</td>
<td>Thermal Resistance</td>
<td>22Ω</td>
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</table>

Access Resistance Model

\[ R_{ds} = \frac{V_{ds}}{I_{ds}} = \frac{V_{th}}{\mu_0 W L} \left( 1 + \left( \frac{V_{ds}}{V_{th}} \right)^2 \right) \]

Temperature Scaling

Effect of high access region resistance at high \( V_g \)

Nonlinear source/drain access region resistance model

Fig. 1: Nonlinear variation of source/drain access resistances with \( I_{ds} \) extracted from TCAD simulation and comparison with model.

Fig. 2: \( I_{ds} - V_{ds} \) and trans-conductance for the Toshiba power HEMT. Different slopes above \( V_{th} \) in \( g_{m} \); self-heating governs the first slope while velocity saturation in access region affects second slope.

Fig. 3: (a) \( I_{ds} - V_{ds} \), (b) \( g_{m} \), and (c) reverse \( I_{ds} - V_{ds} \) fitting with experimental data. The non-linear \( R_{ds} \) model shows correct behavior for the higher \( V_g \) curves in the \( I_{ds} - V_{ds} \) plot; the S-P based model can accurately capture the reverse output characteristics.
Modeling of Field-Plates in HEMTs

Field-Plate Capacitance Modeling

Trap Model

RF Model & Extraction (i)

- Model
  - Core surface potential based PDK
  - Access region resistances included in core
  - Bus-inductances in extrinsics

Device Layout

Pad-Level Small Signal Equivalent Circuit Model
RF Parameter Extraction (ii)

Resonant peaks due to interaction of inductances with intrinsic capacitances:

- $L_{10}$, $L_{10}$, $L_{10}$
- $pH = 6.08$
- $pH = 8.25$

Summary

- Industry standard model development @ IITK
- All models are implemented in the Verilog - A code
  - Tested on commercial simulators
  - Validated with real device data
- Working with major semiconductor and EDA companies