BSIM-BULK: Industry Standard SPICE Model for Analog, RF & High Voltage Applications

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Components required for successful IC design

SPICE and Device Compact Models

Don Pederson correctly recognized that device models, not internal algorithms, were the keys to the success of a circuit simulation program.

Ron Rohrer
Special Issue on 40th Anniversary of SPICE

SPRING 2011 IEEE SOLID-STATE CIRCUITS MAGAZINE
Compact Model

• Compact Model is the medium of information exchange between foundry and designer.

• Compact Model must have
  – Convergence on variety of conditions
  – Fast
  – Accuracy
Compact Model Approaches for MOSFET

- Threshold Voltage based Models (e.g. BSIM3, BSIM4)
  - Fully Analytical solution (easy to implement) – Fast
  - Currents expressed as functions of Voltages

\[ I_{ds} = \mu \frac{W}{L} C_{ox} \left[ (V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \]

- Different equations for
  - Sub-threshold and above-threshold
  - Linear/saturation regions
  - Use interpolation function to get smooth current
Compact Model Approaches for MOSFET

• Surface Potential based Models (e.g. ASM-HEMT, PSP, HiSim)

\[ V_G - V_{FB} - \Psi_S = -\frac{Q_{si}}{C_{ox}}, \quad Q_{si} = -\text{sign}(\Psi_S) \Gamma C_{ox} \sqrt{V_t \left( e^{\frac{\Psi_S}{V_t}} - 1 \right) + V_t e^{\frac{2\Phi_F + V_{CH}}{V_t}} \left( e^{\frac{\Psi_S}{V_t}} - 1 \right) + \Psi_S} \]

  – Implicit equation is solved either iteratively or analytically
  – Might be slower than threshold voltage based models

• Charge based Models (e.g. BSIM-BULK, BSIM-CMG)

  – Solve for charge instead of surface potential
  – No iterations
  – Faster than Surface Potential based approach with similar accuracy in charge/current
BSIM Family of Compact Device Models

- BSIM1,2
- BSIM3
- BSIM4
- BSIM5 (Formerly BSIM6)
- BSIM-SOI
- BSIM-CMG
- BSIM-IMG
- Bulk MOSFET
- Silicon on Insulator MOSFET
- Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model
BSIM-BULK Description
BSIM-BULK Developers

• Students –
  – Ravi Goel, IIT Kanpur
  – Chetan Gupta, IIT Kanpur
  – Harshit Agarwal, IIT Kanpur
  – S. Venugopalan, UCB
  – M. A. Karim, UCB

• Professors –
  – Yogesh S. Chauhan, IIT Kanpur
  – Chenming Hu, UCB
Charge based MOSFET model

- Next generation BSIM Bulk MOSFET model
- Charge based core derived from Poisson’s solution
- Physical effects (SCE, CLM etc.) taken from BSIM4
- Parameter names matched to BSIM4 parameters
- Gummel Symmetry (symmetric @ $V_{DS}=0$)
- AC Symmetry
  - Capacitances/derivatives are symmetric @$V_{DS}=0$
- Continuous
  - From accumulation to strong inversion
  - From linear to saturation
- Physical Capacitance model
  - Short channel CV–Velocity saturation & other effects
- No glitches – smooth current and capacitance behavior
BSIM-BULK flow

1. Calculate **pinch-off potential** $\Psi_p$ (function of $V_g$)

2. Calculate source and drain **inversion charge density**

3. Calculate **drain current**
   - Noise is calculated after inversion charge densities and $i_{ds}$ is obtained

4. Calculate **total gate drain source and body charge**

Fig: Solution of the core model
Core Model + Real effects

- Channel Length Modulation and DIBL
- Mobility Degradation
- Short Channel Effects
- Quantum Effects
- Temperature Effects
- Fringe Capacitances
- Overlap capacitances
- Velocity Saturation
- GIDL Current
- Impact Ionization current
- Direct tunneling gate current
- S/D Resistance/Parasitic Resistance
- Noise models

Physics of BSIM6 Model

- Poisson’s solution for long channel MOSFET

\[ V_G - V_{FB} - \Psi_S = -\frac{Q_i + Q_b}{C_{ox}} = -\frac{Q_i}{C_{ox}} + \text{sign}(\Psi_S) \Gamma C_{ox} \sqrt{V_t \left( \frac{\Psi_S}{V_t} - 1 \right)} + \Psi_S \]

- Inversion Charge linearization

\[ -\frac{Q_i}{C_{ox}} = n_q (\Psi_P - \Psi_S) \]

- \( n_q \) is the slope factor

\[ n_q = 1 + \frac{\Gamma}{\sqrt{\Psi_{s0}} + \sqrt{\Psi_P}} \]

\[ V_G - V_{FB} - \Psi_P = \text{sign}(\Psi_P) \Gamma C_{ox} \sqrt{V_t \left( \frac{\Psi_P}{V_t} - 1 \right)} + \Psi_P \]

\( \Psi_P \) is evaluated from implicit equation

- \( \Psi_P = \Psi_S \), when \( Q_i = 0 \)

\( n_q \) is made bias dependent to improve accuracy

Physics of BSIM6 Model

• Using linearization approach and normalization

\[
2q_i + \ln(q_i) + \ln \left( \frac{2n_q}{\gamma} \left( \frac{2n_q}{\gamma} q_i + 2 \sqrt{-2q_i + \psi_p} \right) \right) = \psi_p - 2\phi_f - v_{ch}
\]

• **No approximation** to solve the charge equation

• Solved the charge equation using first & second order Newton-Raphson technique to obtain **analytical expression** of \(q_i\)
Analytical expression of $q_i$

\[ n_{q0} = 1 + \frac{\gamma}{2\sqrt{\psi_p}} \]
\[ T_2 = \psi_p - 2\phi - v_{ch} - \ln \left( 4.0 \cdot \frac{n_{q0}}{\gamma} \cdot \sqrt{\psi_p} \right) \]
\[ \ln q_0 = \frac{1}{2} \left[ T_2 - 0.201491 - \sqrt{T_2 \cdot (T_2 + 0.402982) + 2.446562} \right] \]
\[ q_0 = e^{\ln q_0} \]
if $\ln q_0 \leq -80.0$

\[ q_{s/d} = q_0 \cdot \left[ 1 + \psi_p - 2\phi - v_{ch} - \ln q_0 - \ln \left( 2 \cdot \frac{n_{q0}}{\gamma} \left( 2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0} - 1)} \right) \right) \right] \]

else

\[ T_4 = 2 \cdot q_0 + \ln \left( 2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma} \left( 2 \cdot q_0 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0} - 1)} \right) \right) - \psi_p - 2\phi - v_{ch} \]
\[ T_5 = 2 \cdot q_0 + \frac{\gamma}{2(n_{q0} - 1)} - 2 \cdot \frac{\gamma}{2(n_{q0} - 1)} \cdot q_0 \]
\[ q_1 = q_0 - \frac{T_4}{T_5} \]
\[ T_4 = 2 \cdot q_1 + \ln \left( 2 \cdot q_1 \cdot \frac{n_{q0}}{\gamma} \left( 2 \cdot q_1 \cdot \frac{n_{q0}}{\gamma} + 2 \cdot \frac{\gamma}{2(n_{q0} - 1)} \right) \right) - \psi_p - 2\phi - v_{ch} \]
\[ T_5 = 2 \cdot q_1 + \frac{\gamma}{2(n_{q0} - 1)} - 2 \cdot \frac{\gamma}{2(n_{q0} - 1)} \cdot q_1 \]
\[ T_7 = -\frac{1}{q_1^2} - \frac{1}{\frac{\gamma}{2(n_{q0} - 1)} \cdot q_1 + \frac{\gamma}{2(n_{q0} - 1)}} - \left[ \frac{\gamma}{2(n_{q0} - 1)} \cdot q_1 + \frac{\gamma}{2(n_{q0} - 1)} \right]^2 \]
\[ q_{s/d} = q_1 - \frac{T_4}{T_5} \cdot \left( 1 + \frac{T_4 \cdot T_2}{2 \cdot T_5^2} \right) \]
Drain Current including Current saturation

- **Drain-Source current**
  - Mobility model
  - Current saturation

\[
I_D = \frac{\mu_v}{1 + \left(\frac{\mu_v}{v_{sat}}\right) dx} W\left(-Q_i \frac{d\Psi}{dx} + V_T \frac{dQ_i}{dx}\right)
\]

\[
-I_i = \frac{Q_i}{C_{ox}} = n_q (\Psi_P - \Psi_S), q = -\frac{Q_i}{2n_q C_{ox} V_T}, i_d = \frac{I_D}{2n_q W \mu V_T^2}, \lambda_c = \frac{2\mu V_T}{v_{sat} L}
\]

- **Using charge linearization & normalization**

\[
i_{ds} = \left(\frac{q_s^2 + q_s}{\frac{1}{2}\left[\sqrt{1 + \Gamma^2} + \frac{1}{\Gamma} \ln\left(\Gamma + \sqrt{1 + \Gamma^2}\right)\right]}\right)
\]

\[
\Gamma = 2\lambda_c (q_s - q_d)
\]
Normalized $Q_i-V_G$ & derivatives

$q_i$ vs $V_G$

$1^{st}$ derivative

$2^{nd}$ derivative

$3^{rd}$ derivative

Red – Numerical Surf. Pot. model
Blue – BSIM6 model
Normalized $I_{DS} - V_{GS}$ & derivatives

$I_{SPN}(v_g, v_{fb}, 10, 0)$
$\frac{I_{BSIM6}(v_g, v_{fb}, 10, 0)}{I_{SPN}(v_g, v_{fb}, 10, 0)}$

$I_{DS}$ vs $V_G$

Error (%)

Red – Numerical Surf. Pot. model
Blue – BSIM6 model

$1^{st}$ derivative

$2^{nd}$ derivative

$3^{rd}$ derivative
Short Channel Effects

• Many of the short channel effects are included using threshold voltage shift (same as BSIM4)

\[
\Delta V_{th,V_DN UD} = K_1 \cdot (\sqrt{P_{hist}V_{bs x}} - \sqrt{\psi_{st}}) \cdot \left( 1 + \left( \frac{L_{PEB}}{L_{eff}} \right)^{L_{PEBEXP}} \right) - K_2 \cdot V_{bs x}
\]

\[
\Delta V_{th,SCE} = -\theta_{SCE} \cdot DVT_0 \cdot (V_{bi} - \psi_{st})
\]

\[
\Delta V_{th,DIBL} = -(E_T A_0 + E_T A B \cdot V_{bs x}) \cdot \theta_{DIBL} \cdot V_{ds x}
\]

\[
\Delta V_{th,RSC E} = K_1 \cdot \theta_{RSCE} \cdot \sqrt{\psi_{st}}
\]

\[
\Delta V_{th,NW1} = (K_3 + K_3 B \cdot V_{bs x}) \cdot \left( \frac{T_{ox}}{W_{eff} \cdot W_0} \right)
\]

\[
\Delta V_{th,NW2} = -\theta_{NW2} \cdot (V_{bi} - \psi_{st})
\]

\[
\Delta V_{th,DITS} = -n \cdot \frac{K T}{q} \cdot \ln \left( \frac{L_{eff}}{L_{eff} + DVT_0 \cdot (1 + \exp(-DVT_1 \cdot V_{ds}))} \right)
\]

\[
\Delta V_{th,all} = \Delta V_{th,V_NUD} + \Delta V_{th,SCE} + \Delta V_{th,DIBL} + \Delta V_{th,RSC E} + \Delta V_{th,NW1}
\]

\[+ \Delta V_{th,NW2} + \Delta V_{th,DITS}
\]

\[
V_{gfb} = V_g - V_{fb} - \Delta V_{th,all}
\]
Mobility Model

- Mobility model adopted from BSIM4

\[
\mu_{\text{eff}} = \frac{U_0 \cdot f(L_{\text{eff}})}{1 + (U_A + U_C \cdot V_{t_{\text{dsf}}}) \left[ \frac{V_{\text{gsf}}}{E_{\text{eff}}} + \frac{C_i \cdot (V_{\text{THO}} - V_{\text{FEO}} - \Phi_s)}{TOX} \right] + UD \left( \frac{V_{m} \cdot TOX}{V_{\text{gsf}} + 2V_{m}^2 + 0.0001} \right)}
\]

where

\[
\eta = \begin{cases} 
\frac{1}{2} \cdot ETAMOB & \text{for NMOS} \\
\frac{1}{3} \cdot ETAMOB & \text{for PMOS}
\end{cases}
\]

\[
E_{\text{efffs}} = 10^{-8} \cdot \left( \frac{q_{bs} + \eta \cdot q_{is}}{\varepsilon_{\text{ratio}} \cdot Tox} \right) \quad \text{MV/cm}
\]

\[
V_{\text{dsx}} = \sqrt{V_{\text{ds}}^2 + 0.01 - 0.1}
\]

\[
V_{\text{bsx}} = - \left[ V_s + \frac{1}{2} (V_{\text{ds}} - V_{\text{dsx}}) \right]
\]

BSIM4

BSIM-BULK

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Saturation Voltage $V_{dsat}$

- $V_{ds}$ to $V_{dsat}$ – BSIM4 formulation causes asymmetry in higher order derivatives
- New $V_{dsat}$ evaluation:

$$
\lambda_c = \frac{2 \mu_{effs} V_t}{V_{SAT} \cdot L_{eff}} \quad \Rightarrow \quad q_{dsat} = \frac{1}{2} K_{SATIV} \cdot \lambda_c \cdot \frac{q_s^2 + q_s}{1 + \frac{1}{2} \lambda_c (1 + q_s)}
$$

$$
V_{dsat} = \frac{V_{dsat}}{V_t} = \psi_p - 2 \varphi_f - 2q_{dsat} - \ln \left[ \frac{2q_{dsat} \cdot n_q}{\gamma} \left( \frac{2q_{dsat} \cdot n_q}{\gamma} + \frac{\gamma}{n_q - 1} \right) \right]
$$

$$
V_{dseff} = \frac{V_{ds}}{\left[ 1 + \left( \frac{V_{ds}}{V_{dsat} - V_s} \right)^{1/\Delta} \right]^{\Delta}}
$$
Output conductance – CLM

\[ E_{sat} = \frac{2 \cdot V_{SAT}}{U_0 \cdot D_{mobs}} \]

\[ F = \begin{cases} 
1 & \text{for } FPROUT \leq 0 \\
\frac{1}{\frac{FPROUT \cdot \sqrt{L_{eff}}}{q_{ia} + 2 \cdot n V_t}} & \text{for } FPROUT > 0 
\end{cases} \]

\[ C_{clm} = \begin{cases} 
\frac{F \left( 1 + PCLMG \cdot \frac{q_{ia}}{E_{sat} \cdot L_{eff}} \right)}{PCLM} & \text{for } PCLMG > 0 \\
\frac{F \left( 1 - PCLMG \cdot \frac{q_{ia}}{E_{sat} \cdot L_{eff}} \right)}{PCLM} & \text{for } PCLMG < 0 
\end{cases} \]

\[ V_{asat} = V_{dsat} + E_{sat} L \]

\[ M_{CLM} = 1 + \frac{1}{C_{clm}} \ln \left[ 1 + \frac{V_{ds} - V_{dseff}}{V_{asat}} \cdot C_{clm} \right] \]

Adopted from BSIM4
Output conductance – DIBL Effect

\[
P V A G f a c t o r = \begin{cases} 
1 + P V A G \cdot \frac{q_{im}}{E_{\text{sat}}L_{\text{eff}}} & \text{for } P V A G > 0 \\
\frac{1}{1 - P V A G \cdot \frac{q_{im}}{E_{\text{sat}}L_{\text{eff}}}} & \text{for } P V A G < 0
\end{cases}
\]  \quad (3.104)

\[
\theta_{\text{rout}} = \frac{0.5 \cdot P D I B L 1}{\cosh \left( D R O U T \cdot \frac{L_{\text{eff}}}{L_{t0}} \right) - 1} + P D I B L 2
\]  \quad (3.105)

\[
V_{A D I B L} = \frac{q_{ia} + 2kT/q}{\theta_{\text{rout}}} \cdot \left( 1 - \frac{V_{\text{dsat}}}{V_{\text{dsat}} + q_{ia} + 2kT/q} \right) \cdot P V A G f a c t o r \cdot \frac{1}{1 + P D I B L C B \cdot V_{bsx}}
\]  \quad (3.106)

\[
M_{D I B L} = \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{A D I B L}} \right)
\]  \quad (3.107)
**I_{DS-VX} Gummel Symmetry**

All derivatives are continuous at $V_{DS}=0$
(N+1 derivatives exist, where N=DELTA)
Harmonic Balance Simulation

- Accurate value of slope for all harmonics
Global Extraction Procedure

- Single set of parameters for geometrical scaling
- Step by step approach needed
Validation on Measured Data (Large device)

IDVG @ VDS=50mV

IDVG in saturation

gmVG @ VDS=50mV

IDVD

gdsVD IBVG for different VDS
Validation on Measured Data (Short device)

IDVG @ VDS=50mV

IDVG in saturation

gmvG in saturation

IDV

IDVG in saturation

IDVD gdsVD

gmvG in saturation

IBVG for different VDS
Model Validation on Measurements

$I_D V_{GS}$ at $V_{DS} = 0.05V$ for different $V_{BS}$

Geometrical Scaling
Model Validation on Measurements

$g_{mV_{GS}}$ at $V_{DS}=0.05V$ for different $V_{BS}$

Geometrical Scaling
Model Validation on Measurements: $I_{DS}V_{DS}$ at $V_{BS}=0V$

Geometrical Scaling

1. $W/L=10\mu m/0.07\mu m$
2. $W/L=10\mu m/0.08\mu m$
3. $W/L=10\mu m/0.09\mu m$
4. $W/L=10\mu m/0.10\mu m$
5. $W/L=10\mu m/0.12\mu m$
6. $W/L=10\mu m/0.16\mu m$
7. $W/L=10\mu m/0.24\mu m$
8. $W/L=10\mu m/0.50\mu m$
9. $W/L=10\mu m/2.00\mu m$
CV Model

- Physical Capacitance Model
- Poly-depletion & Quantum Mechanical Effect
- Channel Length Modulation
- Velocity Saturation Effect
- Charge conservation
Physical Capacitance Model

Also available in CV Model
- PDE
- QME
- SCE

Bulk terminal

\[ Q_b = T_1 + T_2 + \left[ T_4 \cdot T_7 - n_q \cdot \left( q_s + q_{deff} + \frac{(q_s - q_{deff})^2}{3(1 + q_s + q_{deff})} \right) \right] \]

Source terminal

\[ Q_s = \frac{n_q}{3} \left[ 2 \cdot q_s + q_{deff} + \frac{1 + 0.8 \cdot q_s + 1.2 \cdot q_{deff}}{2} \left( \frac{q_s - q_{deff}}{1 + q_s + q_{deff}} \right)^2 \right] \]

Drain terminal

\[ Q_d = \frac{n_q}{3} \left[ q_s + 2 \cdot q_{deff} + \frac{1 + 1.2 \cdot q_s + 0.8 \cdot q_{deff}}{2} \left( \frac{q_s - q_{deff}}{1 + q_s + q_{deff}} \right)^2 \right] \]
Normalized $Q_G$, $Q_B$ and $Q_S$ vs. $V_{GS}$
Normalized Capacitance

Normalized to $W^*L^*C_{OX}$
Normalized Capacitance (No QME & PDE)

- $C_{GD}$ vs. $V_{GS}$
- $C_{GG}$ vs. $V_{GS}$
- $C_{GS}$ vs. $V_{GS}$

$V_{DS} = 0, 0.2, 0.5, 1V$
Normalized $C_{GG}$ vs. $V_{GS}$ (with PDE only)
QME model for Capacitance

Charge centroid

\[
X_{DC}^{inv} = \frac{ADOS \cdot (1.9 \cdot 10^{-9})}{1 + \left[ \frac{Q_i + ETAQM \cdot Q_B}{QM0} \right]^{0.7 \cdot BDOS}}
\]

\[
C_{ox}^{inv} = \frac{3.9 \cdot \varepsilon_0}{TOXP \cdot \frac{3.9}{EPSROX} + \frac{X_{DC}^{inv}}{\varepsilon_{ratio}}}
\]

Intrinsic Charge expressions:

\[
WLCOXV t_{inv} = NF \cdot Wact \cdot Lact \cdot C_{ox}^{inv} \cdot nVt
\]

\[
QB_i = -NF \cdot Wact \cdot Lact \cdot \left( \frac{\varepsilon_0 \cdot EPSROX}{TOXP} \right) \cdot nVt \cdot Qb
\]

\[
QS_i = -WLCOXV t_{inv} \cdot Qs
\]

\[
QD_i = -WLCOXV t_{inv} \cdot Qd
\]

\[
QGi = QS_i + QD_i + QB_i
\]
Normalized $C_{GG}$ vs. $V_{GS}$ (with QME only)
Normalized $C_{GG}$ vs. $V_{GS}$ (QME and PDE)

Normalized to $W*L*C_{OX}$
Normalized Caps vs. $V_{DS}$

Normalized to $W*L*C_{OX}$
Capacitance Quality Test

\[ C_{SG} = C_{DG} \quad @V_{DS} = 0 \]

\[ C_{GD} = C_{GS} \quad @V_{DS} = 0 \]
Junction capacitance model

- BSIM4 junction capacitance model causes asymmetry
- Updated junction capacitance model for AC symmetry

\[ Q_{j_{\text{old}}}(V_j) :\]

\[
\begin{cases} 
    1 - \left(1 - \frac{V_j}{P_{\text{BS}}} \right)^{1-M_{\text{JS}}} & \text{if } V_j < 0 \\
    0 & \text{if } V_j = 0 \\
    V_j \cdot C_j + V_j^2 \cdot \frac{M_{\text{JS}} \cdot C_j}{2 \cdot P_{\text{BS}}} & \text{if } V_j > 0 
\end{cases}
\]

Transition point is at \( V_j = 0 \)

\[ Q_{j_{\text{new}}}(V_j) :\]

\[
\begin{cases} 
    x_0 \leftarrow 0.9 \\
    \frac{1 - \left(1 - \frac{V_j}{P_{\text{BS}}} \right)^{1-M_{\text{JS}}}}{C_j \cdot P_{\text{BS}}} & \text{if } \frac{V_j}{P_{\text{BS}}} < x_0 \\
    \frac{1}{(1-x_0)^{M_{\text{JS}}}} \cdot \left(1 - \frac{V_j}{P_{\text{BS}}} \right) \left[ \frac{1}{2} \cdot M_{\text{JS}} \cdot \frac{1}{1-x_0 \cdot \left(1 - \frac{V_j}{P_{\text{BS}}} \right) - (1 + M_{\text{JS}})} + C_j \right] & \text{otherwise} 
\end{cases}
\]

Transition point is at \( V_j = 0.9V \)
Junction capacitance model

- Symmetry problem using old $Q_j$
- New model is infinitely differentiable @ $V_{DS}=0$
AC Symmetry test

Capacitance & derivatives are symmetric

\[ V_S \quad (+) \quad I_S \quad (+) \quad V_b \quad (+) \quad I_b \quad (+) \quad V_d \quad (+) \quad I_d \quad (+) \]

\[ \text{anti-phase} \quad v_s = -1 + j0 \quad \text{in-phase} \quad v_s = 1 + j0 \]

\[ v_d = +1 + j0 \quad \text{anti-phase} \quad v_d = -1 + j0 \quad \text{in-phase} \]

Ref. - C. McAndrew, IEEE TED, 2006
BSIM6 Validation – Gate Capacitance

PMOS

NMOS

\[ C_{gg} \text{ normalized to } C_{ox} \cdot \text{WL} \]
RF Validation

Fig. 12. Smith chart of $S_{11}$ and $S_{22}$ parameters at $V_G - V_{T_{0,sat}} = [0.125, 0.225, 0.425, 0.725]$ V and $V_D = 1.1$ V.
Modeling of Self-Heating Effect

Self Heating Effect is modeled by using Thermal Network.

Voltage at thermal node ‘ΔT’ is rise in temperature.

This Voltage (ΔT) is added to the temperature variable in the model.

Ref.: BSIM-SOI Model
Self Heating Model – Quality Test

- **Step 1**: For transistor biased in saturation, sweep $R_{TH}$ (thermal resistance) with self-heating ON, observe current and temperature.

- **Step 2**: Switch off self-heating model, simulate the same circuit for temperature range obtained in step 1.

- **Drain current obtained from both the steps should be same.**

Self Heating Effect: **Output Characteristics**

- Drain current reduces in high power region.
  - Negative ‘gds’

![Graph showing output characteristics](image)

**Graph Legend:**
- **With Self Heating**
- **Without Self Heating**

**Key Points:**
- Drain Voltage (V)
- Drain Current (mA)
- \( V_G = 4V \)
- \( V_G = 3V \)
- \( V_{DS} \) (V)
Modeling of Gate Resistance and NQS in BSIM-BULK Model
Figure 2: Gate resistance network for (a) $RGATEMOD = 0$ (b) $RGATEMOD = 1$
(b) $RGATEMOD = 2$ (d) $RGATEMOD = 3$.
NQS (Non-Quasi-Static) Effect

In QS modeling: charge is a function of terminal voltages only.

\[ Q(t) = Q(V_G(t), V_D(t), V_S(t), V_B(t)) \]

In NQS modeling: charge is not only a function of terminal voltages but also an explicit function of time.

\[ Q(t) = Q(V_G(t), V_D(t), V_S(t), V_B(t), t) \]

- The onset frequency of NQS \( (f_{nqs}) \) is typically around \( \approx \frac{f_t}{3} \).
NQS (Non-Quasi-Static) Effect

This is first order NQS model

\[ \frac{1}{R_{ii}} = XRCRG1 \cdot NF \cdot \left( \frac{I_{ds}}{V_{dseff}} + XRCRG2 \cdot \frac{W_{eff}\mu_{eff}C_{oxeff}V_t}{L_{eff}} \right) \]

\( R_{ii} \) is the channel reflected NQS resistance

\( R_{geltd} \) is used as the Gate Electrode Resistance

- Segmentation model with segments ≥ 17 can capture the NQS trend
- Increases the computational time

This approach has been there in the present BSIM-BULK model
NQS: Improved Model

✓ Modeling of Channel RC Network
✓ Modeling of Gate Electrode RC Network

\[ R_1 = \frac{R_{ch}}{40}, R_2 = \frac{7R_{ch}}{120}, R_3 = \frac{R_g}{3}, C_2 = \frac{20C_{ox}}{49} \text{ and } C_3 = \frac{6C_{ox}}{5} \]

\[ \frac{1}{R_1} = XRCRG_1, \frac{1}{R_2} = XRCRG_2, \frac{1}{R_3} = XRCRG_3 \]

\[ C_2 = XRCCG.CGGI \]

\[ R_3 = R_{geltd} \text{ and } C_3 = XGCCG.CGG \]

where, \( XRCRG_1 = 40, XRCRG_2 = \frac{120}{7} \),
\( XRCCG = \frac{49}{20} \text{ and } XGCCG = \frac{6}{5} \)

**NQS: Improved Model**

If we use $XRCRG_1 = 40$, $XRCRG_2 = \frac{120}{7}$, $XRCCG = \frac{49}{20}$ and $XGCCG = \frac{6}{5}$

- Gives the required NQS trend.
- Cannot give a good fitting at high frequency
- For $V_{DS} \neq 0$ channel is tapered from source to drain
- Also have some layout effects in the actual fabricated device
- Fitting parameters can provide more flexibility
NQS: Improved Model

2D TCAD does not consider the impact of gate electrode distributed network on NQS

- Increases the fitting flexibility
- Developed model involves assumptions
Improved Complete Model: TCAD Validation

2D TCAD does not consider the impact of gate electrode distributed network on NQS.

Graphs showing comparisons between TCAD, 1st-order NQS model, 10-segmented model, and this work with and without substrate model.
Improved Complete Model: Validation on Measured Data
Large Signal Analysis

![Graphs showing I_D vs Time and I_D-I_S vs Time curves. The graphs compare different models and datasets, including TCAD simulations and experimental data.](image-url)
Summary of BSIM-BULK

• Charge based physical compact model
  – Physical effects & Parameter names matched to BSIM4 → No new training required for engineers
  – Smooth charge/current/capacitance & derivatives
• Model is symmetric and continuous around $V_{DS}=0$
  – Fulfills Gummel symmetry and AC symmetry
  – Shows accurate slope for harmonic balance simulation
• BSIM4’s extraction methodology can be easily used for BSIM6 → fast deployment & lower cost
• Rapid development
  – From scratch to production level in two years!
High Voltage MOSFET Modeling in BSIM-BULK

High Voltage MOSFET Model

High Voltage Devices: Overview

- Wide application domain: Display, self-driving cars, etc.
- To withstand high voltage:
  - Increase gate oxide thickness
  - Add a drift region between drain/gate: prevents breakdown of gate oxide and breakdown of drain junction.

![Diagram of a high voltage MOSFET model](image-url)
Physics of Drift Region

• Transport in the drift

\[ I_{dr} = Q_{dr} \cdot v_{dr} \]
\[ I_{dr} = I_{ds} \]

• To support higher current, carrier velocity in the drift region increases

\[ V_g \uparrow \rightarrow I_{ds} \uparrow \rightarrow v_{dr} \uparrow \]

• As the carrier velocity reaches the saturation velocity limit, the resistance of the drift region increases
Physics of Drift Region

\[ I_{dr} = W \cdot Q_{dr} \cdot \nu \]
\[ = W \cdot Q_{dr} \cdot \mu \cdot \frac{E}{1 + E/ESAT} \]

On integration,

\[ R_{dr} = \frac{V_{dr}}{I_{dr}} = \frac{R0}{1 - R0 \cdot \frac{I_{drift}}{ESAT \cdot L_{drift}}} = \frac{R0}{1 - \frac{I_{dr}}{I_{dr,max}}} \]

\[ R0 = \frac{L_{dr}}{W \cdot \mu \cdot Q_{drift}} \]
\[ I_{drift,max} = Q_{dr} \cdot W \cdot VSAT \]
Compact Model Adoption

\[ R_{dr,D} = \frac{RDLCW}{1 - \delta_{HV} \left( \frac{I_{ds}}{I_{dr,sat,D}} \right)^{MDRIFT}} \]

\[ I_{dr,sat,D} = q \times NDRIFTD \times W_{eff} \times VDRIFT \]

\[ \delta_{HV} \] introduced for smoothness. Nominal value \( \sim 1 \)

Source side parameters: RSLCW, NDRIFTS

**RDLCW**: Resistance of the Drain side at Low Current

**MDRIFT**: Smoothing parameter for velocity saturation

**VDRIFT**: Saturation Velocity in the drift

**NDRIFTD**: Charge Density in the drift

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Implementation in BSIM-BULK

- **Turn-key feature**: Activates only when switch HVMOD is set to 1.
- **Default value of HVMOD** is 0 (HV feature turned-off)

```plaintext
if (RDSMOD== 1 && HVMOD == 1) begin
    T4 = 1 + PDRWB * Vbsx;
    T0 = ids;
    T11 = NF * Weff * `q * VDRIFT_t;
if (RDLCW!=0) begin
    idrift sat d = T11 * NDRIFTD;
end
rdrift d = rdstemphv * RDLCW * WeffWRFactor/T2D * T4;
Rdrain = Rdrain + rdrift_d;
Rsource = Rsource + rdrift_s;
```
Experimental 35V LDMOS

Symbols: Exp. Data  
Lines: Model

$V_{dd}$: 0.1V to 0.5V  
steps of 0.1V

$R_{on} = V_{ds}/I_{ds}$
Experimental 90V LDMOS

Id-Vg  gm-Vg

\[ V_{DG}: 0.1\text{V} \]

Symbol: Exp. Data
Lines: Model

<table>
<thead>
<tr>
<th>Drain Current (\text{\mu A})</th>
<th>0</th>
<th>20</th>
<th>40</th>
<th>60</th>
<th>80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Voltage (V)</td>
<td>10</td>
<td>8</td>
<td>6</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

Ron

\[ V_{ds}: 0.25\text{V} \]

\[ R_{on} = \frac{V_{ds}}{I_{ds}} \]

Symbol: Exp. Data
Lines: Model

<table>
<thead>
<tr>
<th>On Resistance (k-\text{ohm})</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Voltage (V)</td>
<td>12</td>
<td>10</td>
<td>8</td>
<td>6</td>
<td>4</td>
</tr>
</tbody>
</table>

Id-Vd

\[ V_{G}: 5, 6, 9, 12\text{V} \]

Symbol: Exp. Data
Lines: Model

<table>
<thead>
<tr>
<th>Drain Current (mA)</th>
<th>8</th>
<th>6</th>
<th>4</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage (V)</td>
<td>100</td>
<td>80</td>
<td>60</td>
<td>40</td>
</tr>
</tbody>
</table>

\[ gds \]

\[ V_{G}: 5, 6, 9, 12\text{V} \]

Symbol: Exp. Data
Lines: Model

<table>
<thead>
<tr>
<th>gds (\text{\mu A/V})</th>
<th>\text{10}</th>
<th>\text{100}</th>
<th>\text{1000}</th>
<th>\text{10000}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Voltage (V)</td>
<td>100</td>
<td>80</td>
<td>60</td>
<td>40</td>
</tr>
</tbody>
</table>
Experimental 40V VDMOS

Lines: Model
Symbols: Exp. Data

Id-Vg

Id-Vd
Temperature Dependence

$T = -40 \degree C$

$T = 25 \degree C$

$T = 125 \degree C$

$T = 175 \degree C$
Capacitances in HV Devices

Two important differences as compared to low voltage transistor

- Presence of high series resistance

\[ Q_g = f(V_g, V_{di}, V_s, V_b) \]

\[ \frac{dQ_g}{dV_g} = \frac{\partial Q_g}{\partial V_g} + \frac{\partial Q_g}{\partial V_{di}} \times \frac{dV_{di}}{dV_g} \]

\[ C_{gg} = C_{gg,i} - C_{gd,i} \times \frac{dV_{di}}{dV_g} \]

Presence of overlap region: Contributes bias dependent capacitance
### Charge Model

![Gate Voltage vs Surface Potential](image_url)

- **Inversion**
- **Accumulation**

**Surface Potential in Overlap Region**

\[
V_{gdi} - V_{fb} = \psi_P + \gamma \sqrt{e_P^-} + \psi_P - 1
\]

(Solved analytically)

\[
Q_{I,dr} = W \times L_{dr1} \times 2n_q \times C_{ox} \times V_t \times q_{dr}
\]

\[
Q_{B,dr} = W \times L_{dr1} \times 2n_q \times C_{ox} \times V_t \times (V_{gdi} - V_{fb} - \psi_{s,ov} - 2n_q \times q_{dr})
\]
Model Implementation

- Activate the model: *Set HVCAP=1 along with HVMOD =1*
- Default value of HVCAP is 0

```plaintext
if (HVCAP == 1 && HVMOD == 1) begin

    // CV calculations

    vgbfdrift = -devsign * V(g,di) - VFBOV;
    vgbfdrift = vgbfdrift/Vt;

    gamhv = sqrt(2.0 * `q * epssi * NDR * inv_Vt) / Cox;
    phibHV = lln(NDR / ni);

    `PO_psip(vgbfdrift,gamhv,0,phibHV,psip_k)
    `BSIM_q(psip_k, phibHV, devsign *V(di,b)/Vt, gamhv, q_k)

    QBOV = NF * Wact * LOVER * `EPS0 * EPSROX / BSIMBULKTOXP * Vt *
    QIOV = NF * Wact * LOVERACC * 2 * nq_hv * Vt * T0 * q_k ;

    Qovb = Qovb + QIOV;
    Qovd = Qovd + QBOV;
```

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Model Implementation

Parameters introduced for the charge model:

**VFBOV**: Flat-band voltage of the drift region
**LOVER**: Length of the drift region
**LOVERACC**: Effective length in accumulation
**NDR**: Doping of the drift region
**SLHV**: Parameter and Flag for smoothing the capacitance
**SLHV1**: Parameter for smoothing the capacitance
TCAD Validation

Symbols: TCAD
Lines: Model
TCAD Validation

Ldr1 = 1μm  
Ldr2 = 1μm  
Lch = 2μm
Validation with Experimental Data-1

$C_{gs}$ vs $V_{gs}$

$C_{gd}$ vs $V_{ds}$
Validation with Experimental Data

Experimental data 2

![Graph showing C_{gg} vs Gate Voltage for Model, Measurement, and Model without overlap charge.]

Experimental data 3

![Graph showing C_{gg} vs Gate Voltage for different Vds (0, 1, 2, 3, 4V) with Measurement symbols and Model lines.]

Vds: 0, 1, 2, 3, 4V
Symbols: Measurement
Lines: Model
Speed Test

21 stage Ring Oscillator: 1000 cycles
100 points/cycle

Simulation time per cycle

BSIM-BULK + $R_{\text{drift}}$ + $R_{\text{drift}}$ + Cap.

Simulation Time

1
1.03
1.058
Summary of High Voltage Model

• HV module is turned off-by default in BSIM-BULK model.
  – Default value of model selector HVMOD = 0
  – Activate the HV feature by setting HVMOD=1

• Model captures the physics of high-voltage devices

• Excellent convergence in large circuit simulations
Journal Publications


Conference Publications-2


Thank You