A Highly Scalable High Voltage MOSFET Model

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Outline

• Motivation – why new HV MOSFET Model
• Device Architecture and Modeling Strategy
  • Core – Low Voltage EKV MOSFET Model
  • Analytical bias dependent drift resistance
  • Strategy for charge evaluation based on $V_K$
• Validation and Results
  • Most of the results on VDMOS
  • Some results on LDMOS
• Conclusion
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Motivation

- Robust HV Model for circuit simulators
- Analytical & Physical Compact Model
- Accuracy in DC & AC
- Small number of parameters: EKV!
- Scaling with physical & electrical parameters
- Convergence and Speed
- Open Source

- **General** HV-MOS Model?
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General HV MOSFET Modeling Strategy

- EKV Model
  - Physically based parameters
  - Less parameters than BSIM

EKV MOSFET Model (constant doping)

Intrinsic drain potential

\[ V_G \quad V_S \quad V_B \quad V_K \quad V_D \quad R_{Drift} (V_D, V_G) \]
Device Architectures

- **VDMOS**: $V_{D_{\text{max}}} = 50\,\text{V}$, $V_{G_{\text{max}}} = 3.3\,\text{V}$

- **LDMOS**: $V_{D_{\text{max}}} = 40-100\,\text{V}$, $V_{G_{\text{max}}} = 13\,\text{V}$

Most of the available models use macro-models for HV devices with thick oxide.
## Main EKV Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>Channel Width</td>
<td>m</td>
</tr>
<tr>
<td>L</td>
<td>Channel Length</td>
<td>m</td>
</tr>
<tr>
<td>COX</td>
<td>Oxide Cap. per unit area</td>
<td>F/m²</td>
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<tr>
<td>VT0</td>
<td>Long-channel Threshold Voltage</td>
<td>V</td>
</tr>
<tr>
<td>U₀</td>
<td>Low Field mobility</td>
<td>cm²/Vs</td>
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<tr>
<td>GAMMA</td>
<td>Body Effect Parameter</td>
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<tr>
<td>PHI</td>
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<td>V</td>
</tr>
<tr>
<td>E₀</td>
<td>Mobility Reduction Coefficient</td>
<td>V/m</td>
</tr>
<tr>
<td>UCRIT</td>
<td>Longitudinal Critical Field</td>
<td>V/m</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>Channel Length Modulation</td>
<td>-</td>
</tr>
</tbody>
</table>
Modeling Strategy

- Drift Resistance expression

\[ R_{Drift} = R = \text{constant} \]

\[ R_{Drift} = \frac{R_{Drift0}}{(1 + \theta_{Acc} \cdot V_G)} \]

**Why not?**

- Accumulation in Drift

(Images showing graphs of current vs. voltage for different voltages, with red and blue lines indicating model and measurement, respectively.)

(red - model & blue - measurement)
Modeling Strategy

• Drift part mainly affects the linear region of the output characteristics.

• Delayed transition between linear and saturation regime at high \( V_G \) - velocity saturation in the drift

\[
R_{Drift} = \frac{R_{Drift0}}{(1 + \theta_{Acc} \cdot V_G)}
\]

\[
R_{Drift} = R_{Drift0} \left[ 1 + \left( \frac{V_D - V_K}{V_{SAT}} \right)^{\alpha_{vsat}} \right]
\]

High \( V_D \) but linear region

\[ V_G = 2.8V \] (red - model & blue - measurement)

\[ V_G = 1.2V \]
Scalable Drift Resistance

\[ R_{\text{Drift}} = R_{\text{Drift}0} \left( 1 + \left( \frac{V_D - V_K}{VSAT} \right)^{\alpha_{\text{vsat}}} \right) \left( 1 \pm \left( k_{rd} - 1 \right) \frac{N_F - 1}{N_F + N_{\text{CRIT}}} \right) \left( 1 + \alpha_T \Delta T \right) \]

\[ R_{\text{Drift}0} = \rho_{\text{Drift}0} \left( \frac{L_{\text{DR}}}{N_F (W + \Delta W)} \right) \]

- \( + \): Drain-on-sides
- \( - \): Drain all-around

Effect of Temperature

Drift Length

Number of Fingers

Width and Width Offset
Modeling of Self Heating Effect

$R_{th} \rightarrow \text{Thermal Resistance}$

$C_{th} \rightarrow \text{Thermal Capacitance}$

$P_D = I_{DS} \cdot V_{DS}$

$\mu(T), V_T(T)$

$\Delta T$

• External Temperature Node

AC Modeling

• Charges in MOSFET and Drift region

\[ Q_G = Q_{EKV} + Q_{Drift} = Q_S + Q_K + Q_B + Q_{Drift} \]

\[ Q_{Drift} = (V_G - V_{FB} - \psi_s) \cdot W \cdot L_{DR} \cdot C_{ox} \]

Assumptions

• \( \psi_s \) varies linearly across accumulation charge sheet
AC Modeling

$V_K$ behavior

- As mentioned earlier, Drift does not affect the transistor characteristics in saturation.
- $V_K$ obtained from Spice is valid for linear region. Many models use interpolation function for smooth $V_K$ from linear to saturation.

Normalized reverse Current

$$i_r = [\ln(1 + e^{\frac{v_p - v_k}{2}})]^2$$

Normalized charge density at $V_K$ (EKV)

$$q_k = \sqrt{i_r + 0.25} - 0.5$$

Normalized $v_k$ (EKV)

$$v_k = \frac{V_K}{U_T} = v_p - (2.q_k + \ln(q_k))$$

\( V_K \) vs. \( V_G \) and \( V_D \) for VDMOS

- \( V_K \) – Important parameter for design of HV-MOS


- Trend matches with device simulation and also reported with literature
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Model Validation on 50V VDMOS

Transfer Characteristics ($I_D$-$V_G$)

- Weak inversion to Strong inversion transition
- Subthreshold slope correctly matched
- Good accuracy

(red - model & blue - measurement)
Transconductance for $V_D=0.1-0.5V$

- Subthreshold slope correctly matched
- Descending slope – drift resistance

(red - model & blue - measurement)
Output Characteristics

- Linear region correctly modeled by drift resistance.
- Self Heating Effect
- Peaks on $g_{ds}$

(red - model & blue - measurement)
\( C_{GD} \text{ and } C_{GS}+C_{GB} \text{ vs } V_G \)
\( V_D=0-3V \)

Lateral Doping in the channel

Interpolation function used in drift (to be improved)

- Modeling of Non-uniform doping in intrinsic MOS (Chauhan et al. in *IEDM 2006*)
Temperature Scaling in VDMOS

Self-Heating scales well with temperature

ZTC point
Width Scaling in VDMOS

- Increase in Current and transconductance with Width

(red - model & black - measurement)
$R_{ON}$ Scaling with number of fingers in VDMOS

- $R_{ON} \downarrow - N_F \uparrow$ for drain all-around-device due to current spreading at finger edges

W=5000µm

W=40µm

T=30ºC
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Model Validation on 40V LDMOS

Transfer Characteristics

![Graphs showing transfer characteristics for 40V LDMOS with model and measurement data.](image-url)
Model Validation on 40V LDMOS

Output Characteristics

- Impact-Ionization Effect
- Self-Heating Effect
- Effect of drift resistance

![Graph showing output characteristics with model and measurement lines, and annotations for different effects.](image-url)
Drift Length Scaling : 100V LDMOS

\[ V_G = 12V \]
\[ V_G = 4V \]
Conclusion

• An HV-EKV MOSFET model proposed
• Main number of parameters - 24
• Good performance in DC and AC operations
  – Error ($I_{DS}$) ~ 10%
  – Error ($g_m$) ~ 10%
  – Error (Capacitance) ~ 25%
• Tested for transient operations
• Model validated on industrial devices
• Excellent convergence and scalability
• Self-Heating effect included – No ill convergence
• Implemented in Verilog-A – Platform independent
• Tested on ELDO, SABER, Spectre, UltraSim simulators
• Model has been accepted for evaluation as a candidate for LDMOS standardization by CMC
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