Negative Capacitance MOSFETs for Future Technology Nodes

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Current members – 30

- Postdoc – 5
- Ph.D. – 17
- Three PhD graduated
  - Postdocs in UC Berkeley and U. Bordeaux France

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Device Characterization Lab
- Pulsed IV/RF
- PNA-X 43.5GHz
- High Power IV
Outline

• MOSFET and Scaling
• Negative Capacitance and Transistor
• Modeling of NC-FinFET
• Impact of Material Parameters
• Switching Delay and Energy
• Conclusion
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• MOSFET and Scaling
• Negative Capacitance and Transistor
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MOSFET is a transistor used for **switching** electronic signals.

**Switch vs. MOSFET**

- High $I_{ON}$
- Low $I_{OFF}$

Inverse slope is subthreshold swing, $S$ [mV/dec]
Bulk MOSFET

• Drain current in MOSFET (ON operation)
  \[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

• Drain current in MOSFET (OFF operation)
  \[ I_{OFF} \propto 10^{\left(\frac{V_{GS} - V_{TH}}{S}\right)} \]

- High \( I_{ON} \) (↓L, ↑Cox, ↑\( V_{DD} - V_{TH} \))
- Low \( I_{OFF} \) (↑\( V_{TH} \), ↑S)
Technology Scaling

- Each time the minimum line width is reduced, we say that a new technology node is introduced.

- Example: 90 nm, 65 nm, 45 nm
  - Numbers refer to the minimum metal line width.
  - Poly-Si gate length may be even smaller.
Technology Scaling

• Scaling – At each new node, all geometrical features are reduced in size to 70% of the previous node.

• Reward – Reduction of *circuit size by half*. (~50% reduction in area, i.e., $0.7 \times 0.7 = 0.49$.)
  – Twice number of circuits on each wafer
  – Cost per circuit is reduced significantly.

• Ultimately – *Scaling drives down the cost of ICs.*
Scaling and Moore’s Law

- Number of components per IC function will double every two years – April 19, 1965 (Electronics Magazine)
- Shorthand for rapid technological change!

Source: http://www.intel.com/pressroom/kits/events/moores_law_40th/
Moore’s Law

It’s not technology! → It’s economy.

- Ways to Huge Profits
  - High performance and Low Cost
  - Achieved by making everything SMALLER

The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

In 1978, a commercial flight between New York and Paris cost around $900 and took seven hours. If the principles of Moore’s Law had been applied to the airline industry the way they have to the semiconductor industry since 1978, that flight would now cost about a penny and take less than one second.
Scaling Overview

A. Xj: Shallow junctions

B. Tox: Scale oxide thickness

C. Wdep: Increase doping

1. High scattering

2. Poor Subthreshold Slope

\[ S = \frac{dV_{gs}}{d \log I_{ds}} = 2.3 n v_t \]

3. Large junction capacitance

Limit circuit speed

Other Issues

1. Random Dopant Fluctuation
2. Increased Effective \( T_{ox} \) (Quantum Mechanical Effect)
3. Polysilicon Gate Depletion

Yeo et al., IEEE TED, Vol. 50, 2003


Ohguro, et al., ULSI Science and Technology 1997
Scaling and Innovations

TABLE 7–1 • Scaling from 90 nm to 22 nm and innovations that enable the scaling.

<table>
<thead>
<tr>
<th>Year of Shipment</th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
<th>2010</th>
<th>2013</th>
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<tr>
<td>Technology Node (nm)</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
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<tr>
<td>( L_g ) (nm) (HP/LSTP)</td>
<td>37/65</td>
<td>26/45</td>
<td>22/37</td>
<td>16/25</td>
<td>13/20</td>
</tr>
<tr>
<td>( EOT_e ) (nm) (HP/LSTP)</td>
<td>1.9/2.8</td>
<td>1.8/2.5</td>
<td>1.2/1.9</td>
<td>0.9/1.6</td>
<td>0.9/1.4</td>
</tr>
<tr>
<td>( V_{DD} ) (V) (HP/LSTP)</td>
<td>1.2/1.2</td>
<td>1.1/1.1</td>
<td>1.0/1.1</td>
<td>1.0/1.0</td>
<td>0.9/0.9</td>
</tr>
<tr>
<td>( I_{on, HP} ) (( \mu A/\mu m ))</td>
<td>1100</td>
<td>1210</td>
<td>1500</td>
<td>1820</td>
<td>2200</td>
</tr>
<tr>
<td>( I_{off, HP} ) (( \mu A/\mu m ))</td>
<td>0.15</td>
<td>0.34</td>
<td>0.61</td>
<td>0.84</td>
<td>0.37</td>
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<tr>
<td>( I_{on, LSTP} ) (( \mu A/\mu m ))</td>
<td>440</td>
<td>465</td>
<td>540</td>
<td>540</td>
<td>540</td>
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<tr>
<td>( I_{off, LSTP} ) (( \mu A/\mu m ))</td>
<td>1E-5</td>
<td>1E-5</td>
<td>3E-5</td>
<td>3E-5</td>
<td>2E-5</td>
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<td>Innovations</td>
<td>Strained Silicon</td>
<td>High-k/metal-gate</td>
<td>Wet lithography</td>
<td>New Structure</td>
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</tbody>
</table>

- Scaling For: Cost, Speed and Power
- New technology node every two year
- Channel length reduction ~30%
- Area reduction ~50%

HP: High-Performance technology, LSTP: Low Standby Power technology for portable applications.
EOT: Equivalent electrical Oxide Thickness, i.e., equivalent \( T_{oxe} \)
\( I_{on} \): NFET \( I_{on} \)

Yogesh S. Chauhan, IIT Kanpur 1311/09/2017
Technology Trend

- **2003**: 90 nm
- **2005**: 65 nm
- **2007**: 45 nm
- **2009**: 32 nm
- **2011**: 22 nm

**Product**

- **45 nm** Process Technology
  - Penryn
  - Nehalem
  - Westmere
  - Sandy Bridge
  - Ivy Bridge
- **32 nm** Process Technology
  - Penryn
  - Nehalem
  - Westmere
  - Sandy Bridge
  - Ivy Bridge
- **22 nm** Process Technology
  - Penryn
  - Nehalem
  - Westmere
  - Sandy Bridge
  - Ivy Bridge

**Source**: www.intel.com

Yogesh S. Chauhan, IIT Kanpur

11/09/2017
Scaling Issues/Challenges

- $V_{TH}$ not following scaling
- Current Scaling
  - Mobility is not constant
  - Velocity Saturation
  - Higher $I_{off}$
- Parasitic resistance and capacitance don’t scale linearly
- Process variations
- Affordable Litography
- Heat dissipation and Cooling
IC industry for >40 years

• Closer distance between elements – *Pitch*
  – *Faster* signal transfer and processing rate
• For the same Chip size (or cost), *more functionality*
• Use less energy (or *power*) for same function
• In the last 45 years since 1965
  – *Price* of memory/logic gates has dropped 100 million times.
• Miniaturization is key to the improvements in *speed and power consumption* of ICs.
Why divorce after 40 years?

- $Q_G = Q_i + Q_b$
- Charge sharing

Source

Gate

Drain

Body

11/09/2017

Courtesy: Chenming Hu
Threshold Voltage Roll-Off

Energy band diagram from source to drain when $V_{gs}=0\,V$ and $V_{gs}=V_{t}$.
A-b long channel; c-d short channel.

$V_{t}$ decreases at very small $L_{g}$. It determines the minimum acceptable $L_{g}$ because $I_{off}$ is too large when $V_{t}$ becomes too low or too sensitive to $L_{g}$.

Ref. – Modern Semiconductor Devices for Integrated Circuits by Chenming C. Hu
Short Channel Effects

\[ C_g \quad \text{Oxide} \quad C_d \]

Gate

Source

Drain

Conduction Band Energy (eV)

Position (\(\mu\text{m}\))

Drain Current, \(I_{\text{DS}}\) (A/\(\mu\text{m}\))

Gate Voltage, \(V_{\text{GS}}\) (V)

Smaller size
Making Oxide Thin is Not Enough

Gate cannot control the leakage current paths that are far from the gate.
Leakage current in MOSFET

MOSFET in sub-22nm era

FinFET

FDSOI

New Transistor Grows in the Third Dimension
The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

**TRADITIONAL TRANSISTOR**
Planar conductive area

**NEW INTEL TRANSISTOR**
Conductive area is expanded on three sides of a raised fin

The new transistor with its raised fin requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

New platform enables planar FD technology, the only planar solution to sustain Moore’s law

From the Semicon West trade show, San Francisco, July 12, 2010 – The Soitec Group (Euronext Paris), the world’s leading supplier of engineered substrates for the microelectronics industry, announced today that the company is ready with the Ultra-Thin Buried Oxide (UTBOX) extension to its Ultra-Thin (UT) silicon-on-insulator (SOI) platform, thereby providing a robust substrate solution for chip designers tackling the performance, power and density challenges of mobile consumer devices. Fully Depleted (FD) planar body transistors are now recognized as the right path on the CMOS roadmap for the 22nm generation and beyond. With FD planar transistor technology on UTBOX wafers, chip designers can enhance their usual design flows and techniques. High-volume capacity is available for the 22nm node at Soitec’s manufacturing sites in France and Singapore.

“Soitec is ready with the UTBOX wafers for planar FD architectures: the infrastructure, the process maturity, yield and the capacity are all in place to support demand,” said Soitec president and chairman, André-Jacques Auberton-Hervé. “Industry leaders confirm that FD planar technology is the right choice for mobile consumer products, which need higher performance without compromising power. Our UTBOX offering shows the critical role our materials play as the starting point for energy-efficient, state-of-the-art electronics.”
Eliminate Si Far from Gate

Thin body controlled
By multiple gates.

FinFET body is a thin Fin.

N. Lindert et al., DRC paper II.A.6, 2001
Challenges & Solutions

Power challenge

\[ I_{ON} = \mu \frac{W}{L} C_{ox} (V_{DD} - V_{TH})^2 \]

\[ I_{OFF} \propto 10^{V_{GS}-V_{TH}/S} \]

Scaling both the \( V_{DD} \) and \( V_{T} \) maintains same performance (\( I_{ON} \)) by keeping the overdrive (\( V_{DD} - V_{T} \)) constant.

Adrian Ionescu et al., Nature 2011
Spectrum of Approaches to Analyzing Electronic System

The “Big Picture”

Physics

Device

Quantum mechanical

Semiclassical

Monte Carlo

Hydrodynamic

Drift-diffusion

Circuit

Device

Circuit

MC

HD

DD

Behavioral

Electrical

Timing

Switch

Gate

RTL

System

Functional

Structural

Behavioral

Engineering
Compact Modeling or SPICE Modeling

- Good model should be
  - **Accurate:** Trustworthy simulations.
  - **Simple:** Easy Parameter extraction.
- Balance between accuracy and simplicity depends on end application

- Excellent Convergence
- Simulation Time – ~µsec
- Accuracy requirements
  - ~ 1% RMS error after fitting
- Example: BSIM6, BSIM-CMG
Compact Model is Art Based on Science

Output Conductance
Current Saturation
Quantization
Gate Current
GIDL Current
Impact Ionization Current
Noise models
S/D Resistance
Gate Resistance

Mobility and Transport
Short Channel Effects
Inversion Layer Thickness
Non-Quasi-Static Effects
Substrate RC Network
Parasitic Diode, BJT
Self Heating
Temperature Effects
Proximity Effects
Random Variations

BSIM Family of Compact Device Models


BSIM1,2 BSIM3


BSIM4

BSIM5 BSIM6

BSIMSOI

BSIM-CMG BSIM-IMG

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model
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• MOSFET and Scaling

• **Negative Capacitance and Transistor**

• Modeling of NC-FinFET

• Impact of Material Parameters

• Switching Delay and Energy

• Conclusion
Subthreshold Swing

Amount of gate voltage required to change the current by 1-decade.

\[ S = \frac{dV_{GS}}{d(\log I_{ds})} = \frac{1}{SS} \]

\[ \Delta V_G = 80 \text{ mV} \]

\[ 1/\text{slope} = SS \]

\[ S = \left( 1 + \frac{C_S}{C_{ins}} \right) \cdot 60 \text{ mV/decade} \]

As \( 1 + \frac{C_S}{C_{ins}} \geq 1 \), \( S \geq 60 \text{ mV/decade} \)
Capacitance Definition

- In general, insulator can be a non-linear dielectric whose capacitance density (per unit volume) can be defined as

- **Definition 1:** \( C_{ins} = \left( \frac{\partial^2 G}{\partial P^2} \right)^{-1} = \) inverse curvature of free energy density

- **Definition 2:** \( C_{ins} = \frac{\partial P}{\partial E} = \) slope of the polarization vs electric field curve

  where \( P = \) Polarization in dielectric, \( G = \) Free energy density and \( E = \) Externally applied electric field

- Two types of non-linear dielectrics:
  - **Paraelectric:** No polarization when electric field is removed.
  - **Ferroelectric:** Two possible states of polarization when electric field is removed.
Negative Capacitance Transistor

- What if insulator has a Negative Capacitance!

  \[ C_{ins} < 0 \text{ and } \frac{C_S}{C_{ins}} < 0, \text{ then } \left(1 + \frac{C_S}{C_{ins}}\right) < 1 \Rightarrow S < 60\text{mV/decade} \]

- For a linear capacitor
  - Energy \( G = \frac{Q^2}{2C} \) \( \Rightarrow \) Capacitance \( C = \frac{1}{\frac{d^2G}{dQ^2}} = \frac{1}{\text{Curvature}} \)
  - The same holds also for a non-linear capacitor.

\[ Q = \varepsilon E + P \approx P \]

Landau-Khalatnikov Theory of Non-Linear Dielectrics

• Free energy of a non-linear dielectric is given as
  \[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]

• In general, \( \alpha \) and \( \beta \) can be +ve or –ve but \( \gamma \) is always +ve for stability reasons.

• Dynamics of \( G \) is given by
  \[ \delta \frac{dP}{dt} = -\frac{\partial G}{\partial P} \quad \delta = \text{Polarization damping factor} \]

• In the steady state, \( \frac{dP}{dt} = 0 \Rightarrow E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \)

For \( \alpha > 0 \) and at \( E = 0 \), there exit only one real root

\[ P = 0 \]

A Paraelectric Material

For \( \alpha < 0 \) and at \( E = 0 \), there exit three real roots

\[ P = 0, \pm P_r \; \text{where} \; P_r = \sqrt[3]{\frac{\beta^2 - 3\alpha\gamma - \beta}{3\gamma}} \]

A Ferroelectric Material has a non-zero \( P \) at zero \( E \).
Positive and Negative Capacitances

Only one solution at $E = 0$

Three possible solutions at $E = 0$

$P = 0$ is not possible in an isolated Ferroelectric due to maxima of energy or a negative capacitance

\[ C_{ins} = \left( \frac{\partial^2 G}{\partial P^2} \right)^{-1} = \frac{\partial P}{\partial E} < 0 \]
Negative Capacitance in Ferroelectric

\[ C_{\text{ins}} = C_{fe} \]

-ve slope region can be stabilized if

\[ C_{GG} = \left( \frac{1}{-|C_{fe}|} + \frac{1}{C_S} \right)^{-1} > 0 \]

or,

\[ |C_{fe}| > C_S \]

How to stabilize a Negative Capacitance?

• Add a positive dielectric capacitance in series such that total free energy of system has a minima in the negative capacitance regime of ferroelectric.

\[ \frac{1}{C_{tot}} = \frac{1}{C_{FE}} + \frac{1}{C_{DE}} > 0 \]

• \( C_{DE} < |C_{FE}| \) and \( C_{FE} < 0 \)

• \( C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0 \)

A. I. Khan et al., APL, vol. 99, no. 11, p. 113501, 2011
Ferroelectric-Dielectric Systems


Total Capacitance of Ferroelectric-dielectric hetero-structure becomes greater than the dielectric capacitance.

\[ C_{tot} = \frac{C_{DE} \cdot |C_{FE}|}{|C_{FE}| - C_{DE}} > 0 \]
Negative Capacitance FETs

PbZr$_{0.52}$Ti$_{0.48}$O$_3$ FE with HfO$_2$ buffer interlayer

P(VDF$_{0.75}$-TrFE$_{0.25}$) Organic Polymer FE

HfZrO FE CMOS compatible FE


J. Jo et al., Nano Letters, 2015

K.-S. Li et al., in IEEE IEDM, 2015.
Outline

• MOSFET and Scaling
• Negative Capacitance and Transistor
• **Modeling of NC-FinFET**
• Impact of Material Parameters
• Switching Delay and Energy
• Conclusion
Device Structure

Metal-ferroelectric-Metal-Insulator-Semiconductor (MFMIS)

- Metal internal gate provides an equipotential surface with a spatially constant $V_{\text{int}}$.
- Simplifies modeling as ferroelectric and baseline MOSFET can be considered as two separate circuit entities connected by a wire.
Experimental Calibration of L-K Model

Gibb’s Energy,

\[ G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \]

Dynamics of G is given by

\[ \delta \frac{dP}{dt} = -\frac{\partial G}{\partial P} \]

In the steady state, \( \frac{dP}{dt} = 0 \)

\[ E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

\[ P = Q - \varepsilon E \approx Q \text{ (Gate Charge)} \]

Calibration of L-K with P-V\textsubscript{fe} curve for Y-HfO\textsubscript{2} with 3.6 mol% content of YO\textsubscript{1.5}\textsuperscript{3}

\[ \alpha = -1.23 \times 10^9 \text{ m/F} \]

\[ \beta = 3.28 \times 10^{10} \text{ m/F} \]

\[ \gamma = 0 \text{ (2nd order phase transition)} \]


Calibration of Baseline FinFET

Calibration of baseline FinFET with 22 nm node FinFET.

BSIM-CMG model is used to model baseline FinFET.

Gate length (L) = 30nm,
Fin height (Hfin) = 34nm
Fin thickness (Tfin) = 8nm

Complete Modeling Flowchart

\[ V_{int} = V_G - V_{fe} \]

\[ E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

\[ P = Q - \varepsilon E \approx Q \text{ (Gate Charge)} \]

Landau-Khalatnikov Model of ferroelectric
Verilog-A Code

BSIM-CMG Model of FinFET
Verilog-A Code

\[ I_D \]
Outline

• MOSFET and Scaling

• Negative Capacitance and Transistor

• Modeling of NC-FinFET

• Impact of Material Parameters
  – Impact of ferroelectric thickness
  – Ferroelectric Parameters Variation

• Switching Delay and Energy

• Conclusion
**Capacitances and Voltage Amplification**

\[ E = \frac{V_{fe}}{t_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 \]

\[ V_{fe} = t_{fe}(2\alpha P + 4\beta P^3 + 6\gamma P^5) \]

\[ C_{fe} = \frac{\partial Q}{\partial V_{fe}} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)} \]

\[ \frac{1}{C_{int}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{Drain} + C_{Source}} \]

Internal Voltage Gain,

\[ A_V = \frac{\partial V_{int}}{\partial V_G} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}} \]

Capacitance matching between \(|C_{fe}|\) and \(C_{int}\) increases the gain.
Capacitance Matching

- Capacitance matching increases with $t_{fe}$ which increases the gain.
- Hysteresis appears for $|C_{fe}| < C_{int}$ which is region of instability.

- Increase in $V_D$ reduces the capacitance matching
  - Reduces gain.
  - Reduces width of hysteresis window.
**$I_D-V_G$ Characteristics – SS region**

- As $t_{fe}$ increases
  - Capacitance matching is better
  - $C_S$ and $C_{ins}$ are better matched

\[ S = \left(1 - \frac{C_S}{|C_{ins}|}\right) . 60 \text{mV/dec} \]

- As $t_{fe} \uparrow \Rightarrow SS \downarrow
**I_D-V_G Characteristics – ON region**

- As $t_{fe}$ increases
  - Capacitance matching is better

$$A_{V} = \frac{\partial V_{int}}{\partial V_{G}} = \frac{|C_{fe}|}{|C_{fe}| - C_{int}}$$

- As gain increases, $I_{ON}$ increases.

> Note the significant improvement in $I_{ON}$ compared to SS.
• NCFET is biased in negative capacitance region.
  – $Q_G$ or $P$ is positive $\rightarrow$ $V_{fe}$ is negative.

• $V_{DS} \uparrow$ $\rightarrow$ $Q_G$ or $P \downarrow$ $\rightarrow$ $|V_{fe}| \downarrow$ $\rightarrow$ $V_{int} = V_G + |V_{fe}| \downarrow$ $\rightarrow$ $A_V \downarrow$ $\rightarrow$ Current reduces

$I_D-V_G$ Characteristics – High $V_{DS}$

- Hysteresis appears for $|C_{fe}| < C_{int}$ which is the region of instability.
- As $t_{fe}$ increases
  - SS reduces, $I_{ON}$ increases.
  - $I_{OFF}$ reduces for high $V_D$.
- Width of hysteresis at larger thicknesses can be controlled with $V_D$. 
Negative DIBL

- $V_D$ reduces $Q_G$ which, in turn reduces $V_{int} = V_G - V_{fe}$ in the negative capacitance region.
  - Negative DIBL increases with $t_{fe}$ due to increased $V_{fe}$ drop.
- $V_{th}$ increases with $V_D$ instead of decreasing.
  - Higher $I_{ON}$ still lower $I_{OFF}$!
Optimum NC-FinFET

- Same $I_{ON}$ as 22 nm node FinFET.
- Steeper SS of 58.2 mV/decade.
- $V_{DD}$ reduction by 0.4 V.
- $I_{OFF}$ reduction by 83%.
If $\gamma = 0$, 

$$\alpha = -\frac{3\sqrt{3}E_c}{P_r} \quad \beta = \frac{3\sqrt{3}E_c}{P_r^3}$$

$P_r = \text{Remnant Polarization}$

$E_c = \text{Coercive Field}$

$C_{fe} = \frac{1}{t_{fe}(2\alpha + 12\beta Q^2)}$

- **Low $P_r$ and high $E_c$**
  - reduce $|C_{fe}|$ which leads to improved capacitance matching and hence, a high gain.
  - **Low SS**
  - increase $I_{ON}$ but reduce $I_{OFF}$ due to a more negative DIBL $\Rightarrow$ high $I_{ON}/I_{OFF}$.

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Intrinsic Delay

\[ \tau = \frac{\Delta Q_G}{I_{ON}} \]
\[ \Delta Q_G = Q_G(V_G = V_D = V_{DD}) - Q_G(V_G = 0, V_D = V_{DD}) \]

- NC-FinFET driving NC-FinFET
  - For high \( V_{DD} \), high \( I_{ON} \) advantage is limited by large amount of \( \Delta Q_G \) to be driven.
  - Outperforms FinFET at low \( V_{DD} \).
  - Minimum at \( V_{DD} \approx 0.28 \) V corresponds to a sharp transition in \( Q_G \).

NC-FinFET driving FinFET load provides full advantage of NC-FinFET.
Power and Energy Delay Products

\[ PDP = \Delta Q_G \cdot V_{DD} \]

\[ EDP = \frac{(\Delta Q_G)^2 V_{DD}}{I_{ON}} \]

- NC-FinFET driving NC-FinFET shows advantage only for low \( V_{DD} \).
- NC-FinFET driving FinFET load is the optimum choice.
Modeling of MFIS NCFET

Contrast with MFIMS structure:

• $P$ and $V_{\text{int}}$ vary spatially in longitudinal direction
• Better stability w.r.t. Leaky ferroelectric and domain formation

Issues with Existing Models[1,2]:
Implicit equations – tedious iterative numerical solutions

Explicit Modeling of Charge

\[ V_{fe} = E_{t_{fe}} = aQ_G + bQ_G^3 \]

Voltage Balance:
\[ V_G - V_{FB} = V_{fe} + \frac{Q_G}{C_{ox}} + \psi_S = a_{eff}Q_G + bQ_G^3 + \psi_S \]

\[ Q_G - \psi_S \text{ relation}^{[1]} \]
\[ Q_G = \text{sign}(\psi_S)\gamma C_{ox} \left[ \psi_S + V_t(e^{-\psi_S/V_t} - 1) \right.\]
\[ + \left. e^{-(2\phi_F + V_C)/V_t} \left(V_t e^{\psi_S/V_t} - \psi_S - V_t \right) \right]^{1/2} \]

→ Implicit equation in \( Q_G \)
→ Goal: Explicit Model with good initial guesses for each region of NCFET operation

Both the \( Q_G \) and its derivatives match well with implicit model

Drain Current Model Validation

Against Full Implicit Calculations

![Graphs showing comparison between Drain Current Model and experimental data.](image)

Against Experimental Data

![Graphs showing comparison between Drain Current Model and experimental data.](image)


MFIS Vs MFMIS

- MFIS excels MFMIS for low $P_r$ ferroelectrics only.
- A smooth hysteresis behavior in MFIS compared to MFMIS.
- MFIS is more prone to hysteresis → exhibits hysteresis at lower thicknesses compared to MFMIS.

NC-FinFET based inverters

- Although the transistor characteristics show no Hysteresis, the VTCs of NC-FinFET inverters can still exhibit it due to the NDR region in the output characteristics.

NC-FinFET based SRAM

- Read time: reduced due to the increased drive current
- Write time: slower due to the gate capacitance enhancement
- $P_{\text{avg}}$: NC-SRAM performs better with lower standby leakage only at small $t_{fe}$, taking advantage of the lower subthreshold currents

Impact of Process Variations

- Variability in $I_{ON}$, $I_{OFF}$, and $V_t$ due to combined impact of variability in $L_g$, $T_{fin}$, $H_{fin}$, EOT, $t_{fe}$, $E_c$, and $P_r$
- $I_{ON}$: Improvement is non-monotonic with $t_{fe}$
- $I_{OFF}$: Decreases monotonically with $t_{fe}$
- $V_t$: Decreases monotonically with $t_{fe}$

Process Variation in Ring Oscillator

- The overall average delay variability in NC-FinFET based RO is lesser compared to the reference RO.
- The improvement is non-monotonic with nominal FE thickness scaling.

Conclusion

• Maintaining $I_{ON}/I_{OFF}$ is the biggest challenge in new technology nodes

• Negative capacitance FET is one of the best choice
  – Need to find sweet material (HfZrO$_2$)
  – Integration in conventional CMOS process remains a challenge (lot of progress)
  – Speed/Switching need more research
Relevant Publications


Thank You