EE210: Analog Electronics

Question Set 7

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1) Consider the circuit in Fig 1. $\mu_n C_{ox} = 0.2mA/V^2$, $I_0 = 1mA$, $V_{DD} = 6V$, $R_1 = R_2 = 2k\Omega$, $V_{tn} = 1V$.

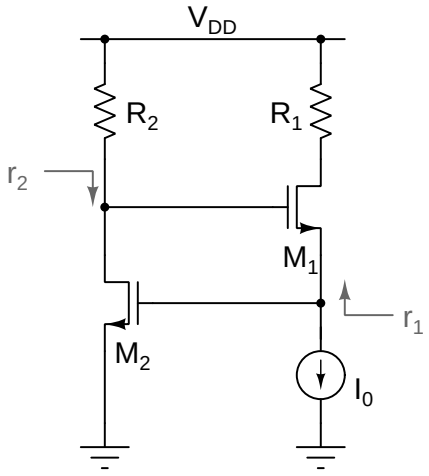

Figure 1: Question 1.

a) Size $M1$ and $M2$ such that $M1$ is in saturation with a margin of 500 mV, and g_{M1} =1 mS.

b) Find the incremental resistances r_1 and r_2.

c) Use the configuration to implement a common source amplifier.

d) If you want to implement a CCCS, where and how will you apply the i/p and take the o/p?

e) How is this config. different from a standard common gate config.?

f) If you want to implement a VCVS having gain ≈ 1 while driving a load $R_L \approx$ 1kΩ to 2kΩ, what will you do?

2) The circuit shown in Fig. 2 is used to generate a bias voltage V_B=V_{tn}+V_{ov}. If we want to generate a bias voltage of V_B=V_{tn}+2V_{ov}, how will you change the circuit without changing the I_0?

3) $I_0 = 1mA$, $(W/L)_1 = 10$, $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 100\mu A/V^2$ $(W/L)_2 = 20$, $V_{DD} = 5\,V$

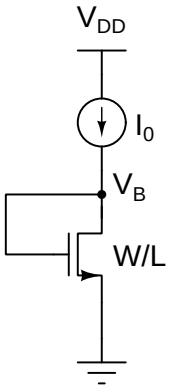

Figure 2: Question 2.

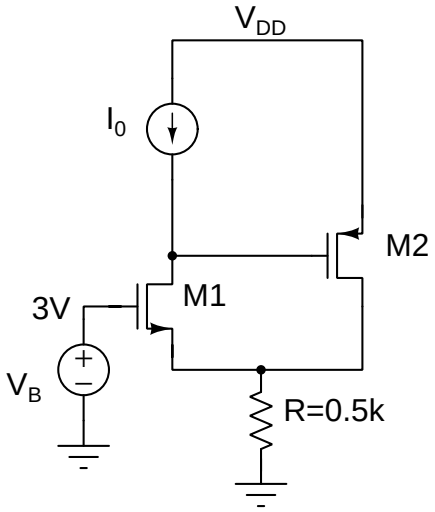

Figure 3: Question 3

a) Find the quiescent current through M1 and M2.

b) Between M1 and M2 ,what will you change to bias M1 at the edge of saturation region ?

c) Among the four types of biasing schemes that you have learnt, which one is being used here to bias M1?

- Observe the drain, feedback at source.
- Observe the drain, feedback at gate.
- Observe the source, feedback at source.
- Observe the drain, feedback at gate.

d) Find the maximum and minimum V_B required to keep both the transistors in saturation while maintaining the constraint of a minimum overdrive voltage of 100 mV?