Partially and Fully Depleted SOI MOSFET’s

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Abstract—A physics based analytical model for partially and fully depleted MOSFET’s is presented. Various non-idealities like short channel effects, floating body effect etc. present in a MOSFET are also discussed. Several devices based on PDSOI or FDSOI are contrasted qualitatively.

Index Terms—Modelling, short channel effects, electrostatic control, scaling, SOI substrate.

I. INTRODUCTION

The quest for scaling down MOSFET size has been going on since its advent due to obvious advantages like speed enhancement, reduction in power consumption and cost [22]. The conventional bulk Si MOSFET has already reached its limit and can’t be scaled down any more without compromising any performance metric. Many novel device structures [2,15] like FinFET, multiple gate (MuGate), gate all around (GAA), ultra thin body (UTB) etc. have been proposed to continue the scaling down to sub-micron range [13,14]. Fully depleted substrate is at the heart of all of the above mentioned devices. Fabricating a device on SOI substrate improves performance by reducing parasitic capacitances and various leakage currents [17]. A SOI MOSFET is also suitable for uses in harsher environment. This motivates one to undertake a study of SOI based devices.

Si body thickness varies for different SOI devices and is tailored based on specific application. A SOI MOSFET with thick Si body is similar to a bulk MOSFET (except for floating body effects). For such devices the depletion region depth below the gate is smaller than the body thickness and hence the name Partially Depleted SOI MOSFET. SOI devices with very thin Si body (which is fully depleted) have better control of gate over channel and thus reduced short channel and floating body effects. This enables scaling down of channel lengths up to nm range. Generally the body in such a device is either undoped or very lightly doped reducing the random dopant effects [6,10]. Also the subthreshold swing in FDSOI is close to unity (ideal).

This paper is organized as follows. In section II a model for PDSOI MOSFET is presented. Floating body and associated kink effects present in a PDSOI device are also discussed. In section III a surface potential based model is derived for FDSOI under different modes of operation. In section IV novel devices – FinFETs, MuGate and GAA and their corresponding scaling is presented. Some non-idealities associated with these devices are also introduced. Conclusion is presented along with a short discussion of future prospects in the final section V.

II. PDSOI MOSFET MODEL

A PDSOI MOSFET is similar to a bulk MOSFET and hence the I-V characteristics are also similar. Following model [25] is presented for an n channel MOSFET working in strong inversion region ($V_{GS} > V_{T}$).

$$I_{DS} = \begin{cases} \frac{W}{L} \mu N C_{OX}' (V_{GS} - V_{T})^2 - \frac{1}{2} V_{DS}^2 & ; V_{DS} < V_{DSAT} \\ \frac{1}{2} W \mu N C_{OX}' (V_{GS} - V_{T})^2 (1 + \lambda_{N} V_{DS}); V_{DS} > V_{DSAT} \end{cases}$$

Similarly the current in weak inversion region varies exponentially with the gate voltage. The above model is the Level 1 NMOS model and only an approximation. A surface potential based all region model is succinctly given below (2).

$$V_{GB} = \Psi_{OX} + \Psi_{S} + V_{FB}$$

$$Q'_G + Q'_D + Q'_C = 0$$

$$Q'_G = C_{OX}' \Psi_{OX}$$

$$Q'_C = -\text{sgn}(\Psi_{S}) \sqrt{2q \epsilon_s N_A} * \sqrt{\phi_{S} e^{-\psi_{S}/\psi_{t}} + \psi_{S} - \phi_{t} + \frac{2 \phi_{F} + V_{CB}}{\phi_{t}} (\psi_{S} - \phi_{t})}$$

$$Q'_G = Q'_D + Q'_C$$

$$Q'_h = -\sqrt{2q \epsilon_s N_A C_{OX}' \Psi_{S}}$$

The above equations are non-linear and can be solved numerically or using suitable approximations for different modes of operation. Also note that $\Psi_{S}$, $Q'_{G}$, $Q'_{C}$ etc. are functions of position when a drain to source bias is applied. The problem becomes 2-D and can be solved using only numerical techniques. To simplify the situation “gradual channel approximation” is made which is justified for long channel devices and small horizontal electric fields. The error made by such simplification is modelled as various short channel effects. In steady state current is same at all points and consists of drift and diffusion components which can be position dependent.

$$I_{DS} = I_{drif}(x) + I_{diff}(x)$$

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$$I_{DS} = I_{drif}(x) + I_{diff}(x)$$
\[ I_{\text{drift}}(x) = \mu W (-Q') \frac{d\Psi_S}{dx} \]
\[ I_{\text{diff}}(x) = \mu W \phi_t \frac{dQ'}{dx} \]
\[ I_D = \mu W \left[ \int_{\Psi_S}^{\Psi_{SL}} (-Q')d\Psi_S + \phi_t \int_{Q_{l0}}^{Q_{l1}} dQ' \right] \]

Again the above expression can be only evaluated numerically because \( Q' \) is a complex function of \( \Psi_S \). In strong inversion using some approximation an explicit expression for \( I_D \) is obtained as given in (equ.1). This model can be further modified to incorporate short channel effects considering one effect at a time. Thus a semi-empirical model is obtained whose parameters can be adjusted suitably to model different devices. Note that
\[ I_D = \frac{W}{L} F(\Psi_{SL}, \Psi_{S0}) \]
\[ I_D = \frac{W}{x} F(\Psi_S(x), \Psi_{S0}) \]
\[ x = \frac{F(\Psi_S(x), \Psi_{S0})}{F(\Psi_{SL}, \Psi_{S0})} \]

\( \Psi_S \) and \( \Psi_{SL} \) can be computed from equation set (2) by substituting \( V_{CB} = V_{SB} \) and \( V_{DB} \) respectively. So the above equation gives the relationship between \( x \) and \( \Psi_S(x) \).

III. EFFECTS OF FLOATING SUBSTRATE POTENTIAL

In this section we analyze the non-idealities arising from the floating body in a PDSOI device [3,9].

A. Threshold voltage change

In saturation the electrons gain very high kinetic energy near the drain because of large electric fields present and thus may cause avalanche generation of electron hole pairs (EHPs). The electrons flow towards the drain whereas the holes are swept by the field in the body. This increases the substrate potential and results in lowering of threshold voltage leading to further rise in the drain current. This is observed as the first kink in Fig.2.

B. Parasitic Bipolar Transistor

If the body current and substrate resistance is significant, the substrate voltage can rise to an extent where the source-body junction gets forward biased. If the drain voltage is increased further the hole current would also rise, but this doesn’t change the substrate voltage appreciably because of the forward biased diode action. A MOSFET inherently has a npn structure but normally the neutral base width is too large for any transistor action to occur. With sufficiently high \( V_{DS} \) the body nearby the drain can get completely depleted decreasing the neutral base width. The length of undepleted substrate is also a strong function of surface potential. When the MOSFET is on the substrate can get completely depleted if the surface potential \( V_{CB}(x) \) is larger than \( V_{De} \) which is given by
\[ V_{De} = qN_A \frac{E_{Si}^2}{2\varepsilon_S} \]
In such a case the neutral base width can reduce to the extent of allowing the BJT action. The neutral base width (\( W_B \)) can be determined as follows. For this analysis it has been assumed that \( V_{DS} \) has been fixed at \( V_{DSat} \).
\[ x = \frac{2V_{GS}V_{CS}(x) - V^2_{GS}(x)}{V^2_{GS}} \]
\[ \frac{W_B}{L} = \frac{2V_{GS}V_{DE} - V^2_{DE}}{V^2_{GS}} < 1 \]

Fig. 4 shows the variation of normalized base width with \( V_{GS} \) and substrate doping. The variation of effective \( \beta \) of the parasitic BJT with \( V_{GS} \), channel length and lifetime is shown in Fig. 5.

IV. FDSOI MOSFET MODEL

In a FDSOI MOSFET the Si substrate being very thin is fully depleted eliminating any floating body effect. The front and back gates (bulk Si below the insulator can be viewed as the second gate) are electrostatically coupled. Unlike PDSOI, \( \Psi_{SF} \) is a function of \( \Psi_{SB} \). This is shown in the figure below. Only the valence and conduction band edges are shown for simplicity.

![Fig.6 – Band diagram of PDSOI and FDSOI](image)

So, a based on front and back gate biasing FDSOI device can operate in 9 different modes as shown below for an n type MOSFET [12].

![Fig.7 – Various modes of operation of FDSOI MOSFET](image)

The surface potential based analysis for FDSOI is fundamentally similar to that for a bulk Si MOSFET and is presented below [5,12,21,23,24]. All relevant parameters are shown in Fig. 8. First let’s consider FDSOI electrostatics without any drain or source biasing. As in conventional MOSFET it’s assumed that all the mobile charges are present at Si surface (delta-depletion approximation).

Applying Gauss’ law to FD bulk:

\[ E(t_{Si}) - E(0^+) = -\frac{qN_A\epsilon_{Si}}{\epsilon_{Si}} = \frac{Q_B}{\epsilon_{Si}} \]
\[ \Delta \Psi = \Psi_{SF} - \Psi_{SB} = \frac{1}{2} (E(t_{Si}^-) + E(0^+)) t_{Si} \]

From these equations we get expressions for \( E(t_{Si}^-) \) and \( E(0^+) \)

\[
E(0^+) = \frac{\Psi_{SF} - \Psi_{SB}}{t_{Si}} + \frac{qN_{A}t_{Si}}{2\varepsilon_{Si}}
\]

\[
E(t_{Si}^-) = \frac{\Psi_{SF} - \Psi_{SB}}{t_{Si}} - \frac{qN_{A}t_{Si}}{2\varepsilon_{Si}}
\]

\[
E_{OF} = \frac{V_{GF} - \Psi_{SF}}{t_{OF}} \text{ where } V_{GF}' = V_{GF} - V_{FBF}
\]

\[
\epsilon_{ox}E_{OF} = \epsilon_{Si}E(0^+) - Q_{IF}'
\]

\[
E(0^+) = \frac{\epsilon_{ox}V_{GF}' - \Psi_{SF}}{\epsilon_{Si}} + \frac{Q_{IF}'}{\epsilon_{Si}}
\]

Doing a similar analysis for back gate -

\[
E(t_{Si}^-) = \frac{\epsilon_{ox} \Psi_{SB} - V_{GB}'}{\epsilon_{Si}} - \frac{Q_{IB}'}{\epsilon_{Si}}
\]

Eliminating the field terms from these equations –

\[
V_{GF} = V_{FBF} + \Psi_{SF} - \frac{q_{IF}' + \epsilon_{ox}t_{OF}}{\epsilon_{OF}}(\Psi_{SF} - \Psi_{SB}) \quad (3)
\]

\[
V_{GB} = V_{FBF} + \Psi_{SB} - \frac{q_{IB}' + \epsilon_{ox}t_{OF}}{\epsilon_{OF}}(\Psi_{SF} - \Psi_{SB}) \quad (4)
\]

From equation (3) \( V_{TF} \) is obtained by setting \( \Psi_{SF} = 2\phi_{B} \)

\[
V_{TF} = V_{FBF} + 2\phi_{B} - \frac{q_{IF}'}{2\epsilon_{OF}} + \frac{\epsilon_{Si}}{\epsilon_{OF}} (2\phi_{B} - \Psi_{SB})
\]

From the equations (3) and (4) it can be seen that for a given \( V_{GF} \) increasing \( V_{GB} \) increases \( \Psi_{SF} \), thus effectively reducing \( V_{TF} \). So the back gate (substrate) biasing can be used to tune the threshold voltage. This is shown in fig.9 and is modelled below for different regions [8].

Fig.9 – Threshold voltage control using back gate in FDSOI

A. Back Inverted ( \( \Psi_{SB} = 2\phi_{B} \) )

\[ V_{TF} = V_{FBF} + 2\phi_{B} - \frac{q_{IF}'}{2\epsilon_{OF}} \]

Even when \( V_{GF} < V_{TF} \) current flows because the back side remains inverted and the device does not turn off. So this mode of operation is not useful.

B. Back Accumulated ( \( \Psi_{SB} \approx 0 \) )

\[ V_{TF} = V_{FBF} + 2\phi_{B} - \frac{Q_{IB}'}{2\epsilon_{OF}} + \frac{\epsilon_{Si}}{\epsilon_{OF}} 2\phi_{B} \]

For the aforementioned regions, this mode of operation is also not useful. Now the total shift \( \Delta V_{TF} \) can be obtained.

\[ \Delta V_{TF} = V_{TF}(\text{back acc}) - V_{TF}(\text{back inv}) \]

\[ \Delta V_{TF} = \frac{\epsilon_{Si}}{\epsilon_{OF}} t_{OF} 2\phi_{B} \]

C. Back Depleted ( \( Q_{IB}' \approx 0 \) )

We need to relate \( \Psi_{SB} \) to \( V_{GB} \). This can be done in a similar manner as in bulk Si MOSFET [25]. But exact analysis is complex and gives only an implicit equation. For our purpose, we assume that \( V_{TF} \) varies linearly with \( V_{GB} \). Thus the task is to find the corresponding slope or rate of change. Note that this approximation is very good as seen from fig.9.

At front threshold (or beyond) \( \Psi_{SF} = 2\phi_{B} \)
\[ V_{GB} = V_{FBB} + \Psi_{SB} - \frac{q}{2C_{GB}} - \frac{C_{SI}'}{C_{OB}'} (2\phi_B - \Psi_{SB}) \] (5)

At the start of back accumulation (\( \Psi_{SB} = 0 \))

\[ V_{GB}(acc) = V_{FBB} - \frac{q}{2C_{GB}} - \frac{C_{SI}'}{C_{OB}'} 2\phi_B \] (6)

The back surface is depleted when \( V_{GB} > V_{GB}(acc) \).

From equations (5) and (6) –

\[ \Psi_{SB} = \frac{C_{GB}'}{C_{OB}'+ C_{SI}'} (V_{GB} - V_{GB}(acc)) \]

Using this in equation and then differentiating –

\[ \frac{dV_{TF}}{dV_{GB}} = -\frac{t_{OF}}{t_{OB}} \times \frac{1}{1 + C_{OB}' / C_{SI}'} \]

Similarly subthreshold swing (\( m \)) can be computed.

\[ m = \frac{dV_{GF}}{d\Psi_{SF}} = 1 + \frac{C_{SI}' C_{OB}'}{C_{OB}' (C_{OB}'} + C_{SI}') \]

If the bottom oxide is thick \( C_{OB}' < C_{SI}' \), \( m \rightarrow 1 \)

So an ideal subthreshold swing is obtained.

V. MOSFET ARCHITECTURES BASED ON THIN (FD) SUBSTRATE

Having thin body, increases the control of gate over the drain current as the conduction occurs quite close to the gate. This mitigates the short channel effects present in conventional MOSFETs and thus helps in further scaling down of device sizes[4,6,18,19]. Similarly increasing the number of gates adds further control on channel. Gate all around (GAA) device is the ultimate device using this approach. This is shown in the figure below [1].

VI. CONCLUSION

In this paper we discussed the scaling bottlenecks for conventional MOSFET’s and motivated the need for PDSOI and FDSOI based devices. SOI devices offer less parasitics but suffer from self heating effects. We then presented a physics based model for PDSOI device and analyzed floating body effects namely threshold voltage lowering and parasitic BJT effects. A FDSOI device has no such problems and allows for a tighter gate control over channel because of better electrostatics. We also derived a surface potential based model for FDSOI devices. The threshold voltage can be tuned using back gate bias. A simple model was presented showing this dependence for

Fig. 6. Architectures which reduce source–drain interaction.

Fig. 8. Maximum allowed silicon film thickness and device width vs. gate length to avoid short-channel effects in single-, double- and quadruple-gate SOI MOSFETs.
various modes of operation. An ideal subthreshold swing is yet another benefit of FDSOI devices. We also derived an expression for the same and discussed the design criteria required for improving this factor. Various devices architectures exist today based on FD body. A brief introduction to such devices was given along with their scaling issues. These devices can be analyzed in a similar manner as adopted in this paper. Improved short channel effects in such devices was also discussed using 2-D simulation results. All these device structures are promising and it’s difficult to predict which one would be adopted for nanometer size devices. Fabrication issues (cost, compatibility with present technology etc.) are likely to play a deciding role in this regard [1,6,11,15,16,22].

REFERENCES
[14] FDSOI - http://www.youtube.com/watch?v=uvV7jcPQ7UY.