Design and Development of 5G massive MIMO Testbed

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Need and mandate of the testbed

- India imports most of the telecom hardware
- Design and build 5G wireless systems in India
  - Should lead to new deep-technology start-ups
- Train students and engineers on 5G systems
- Testbed also helps in evaluating the system performance

5G testbed project partners

- IIT Kanpur
- IIT Madras
- IIT Bombay
- IIT Delhi
- IIT Hyderabad
- IISc
- CEWiT
- SaMMER

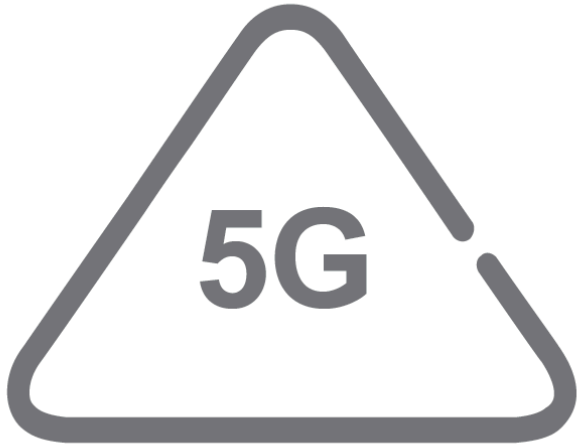
Team at IITK

- Eleven people
  - 2 B.Tech students
  - 2 B.Tech+M.Tech students
  - 1 M.Tech student
  - 1 PhD student
  - 3 Research Associates
  - 2 Management staff
- Currently collaborating with a board fabrication company
- Work closely with IIT Madras

5G use cases

eMBB

High data rates, high traffic volumes



mMTC

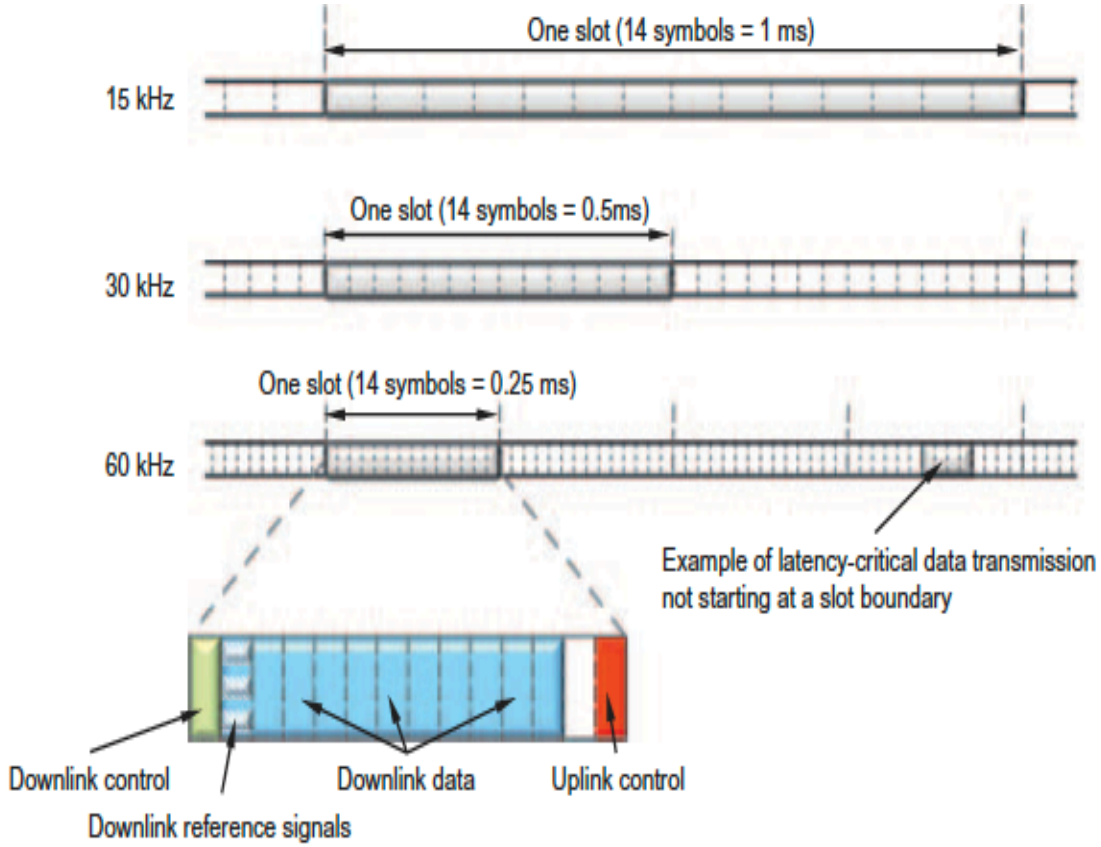
Massive number of devices,
low cost, low energy consumption

URLLC

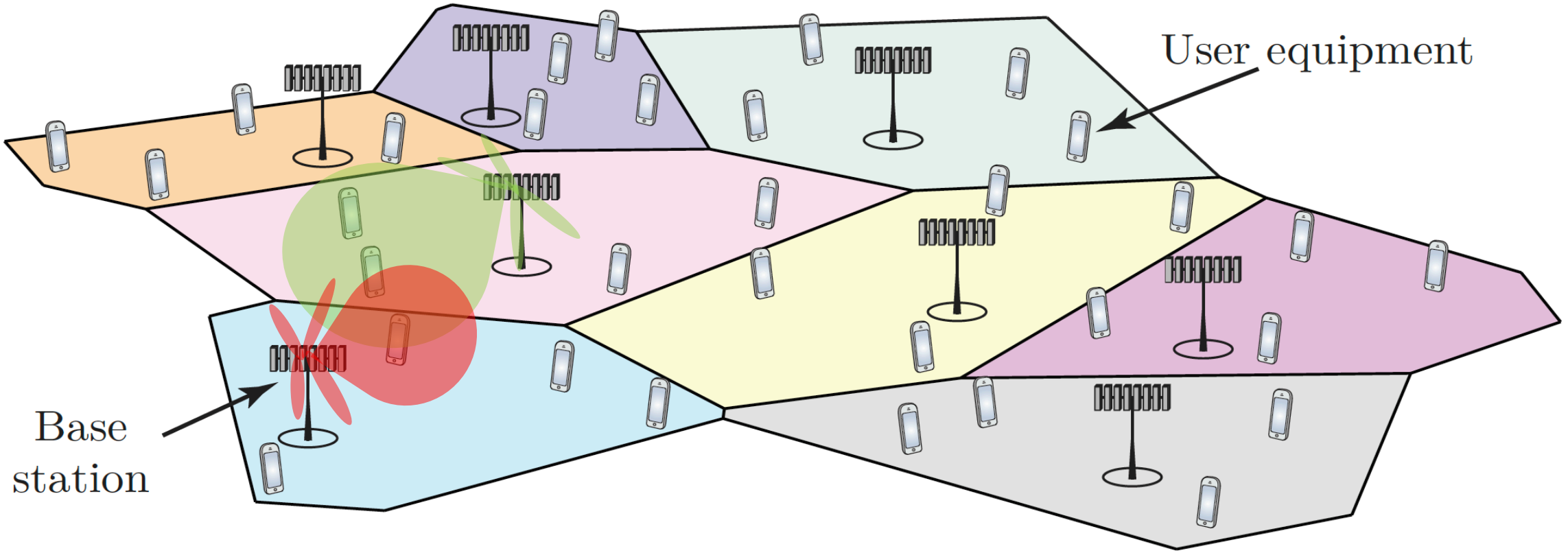
Very low latency,
very high reliability and availability

5G design philosophy

- High data rate
  - Bandwidth : 100 MHz-400 MHz (4G: 20 MHz)
  - Number of antennas : 64 to 128 (4G: 8 antennas)
- Low latency: 1ms (4G: 10 ms)

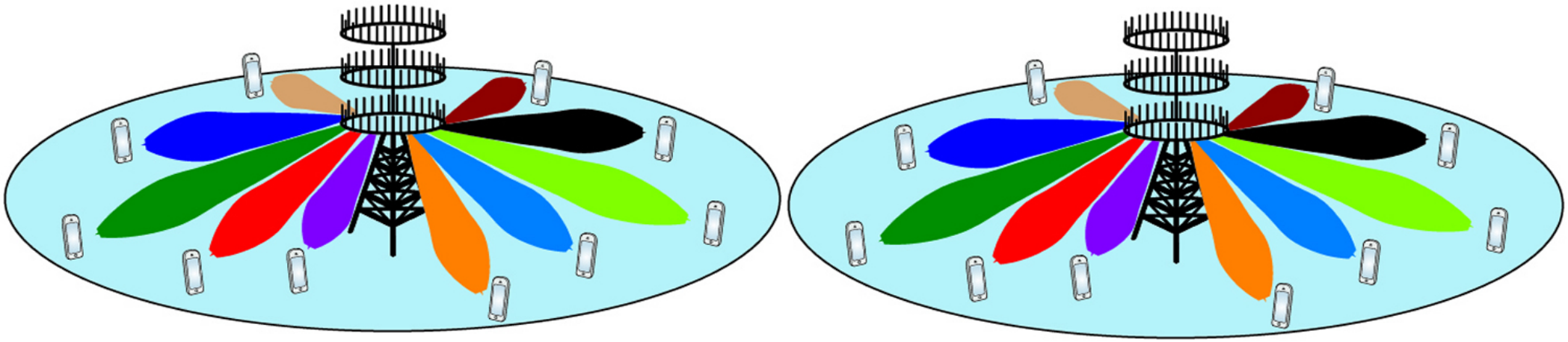


Cellular system layout



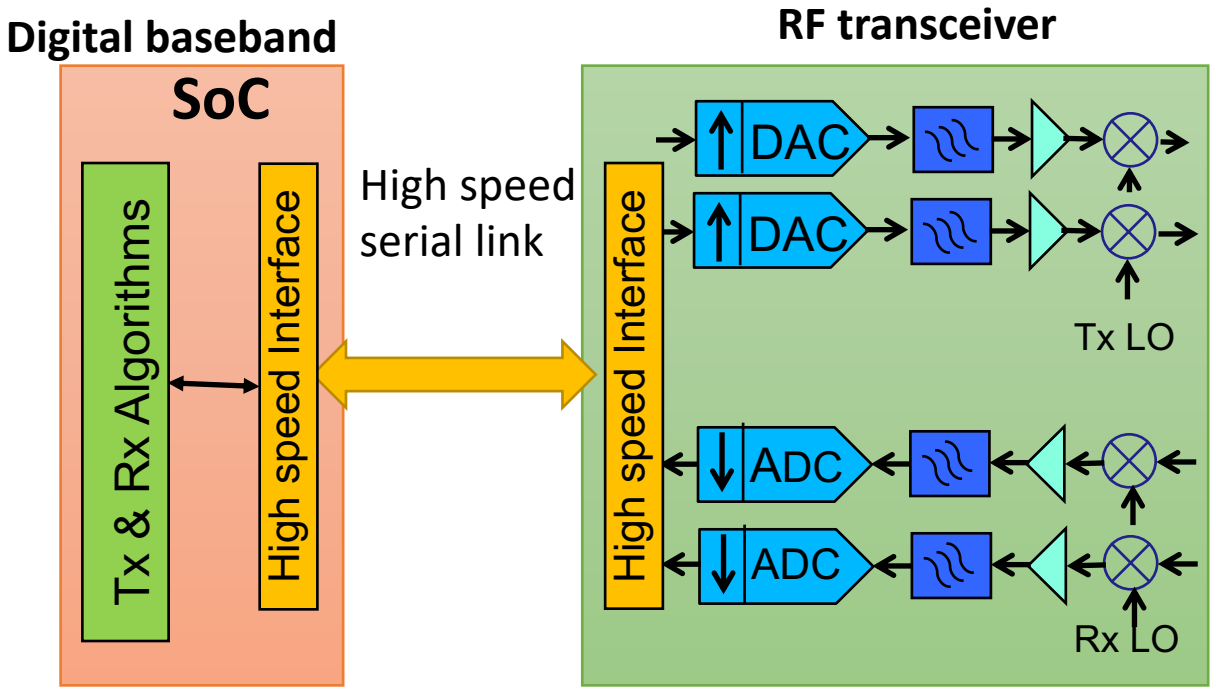
- **4G cellular systems reuse spectrum in each cell – leads to inter-cell interference**

Massive antennas at the BS



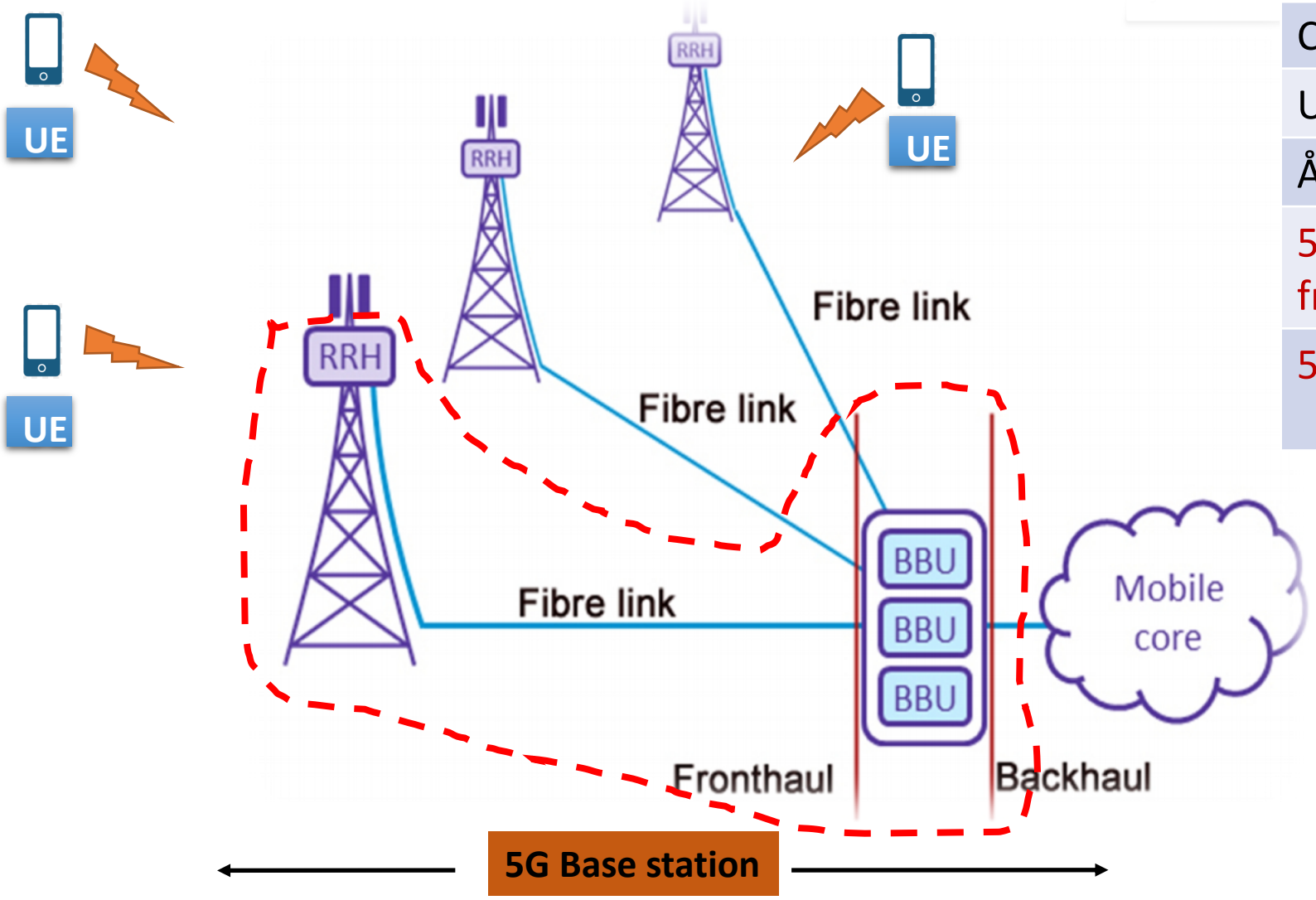
- **Large number of antennas help in forming pointed beams towards the users**
  - **Reduces inter-cell interference**

Wireless transceiver chip architecture



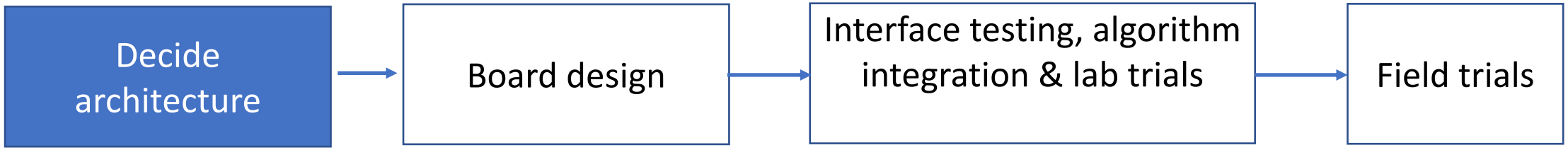
- **Tx & Rx algorithms e.g., Channel estimation, MIMO transmit and receiver**
- **Processing of algorithms can be split across different unit**

Architecture of 5G networks –cloud radio

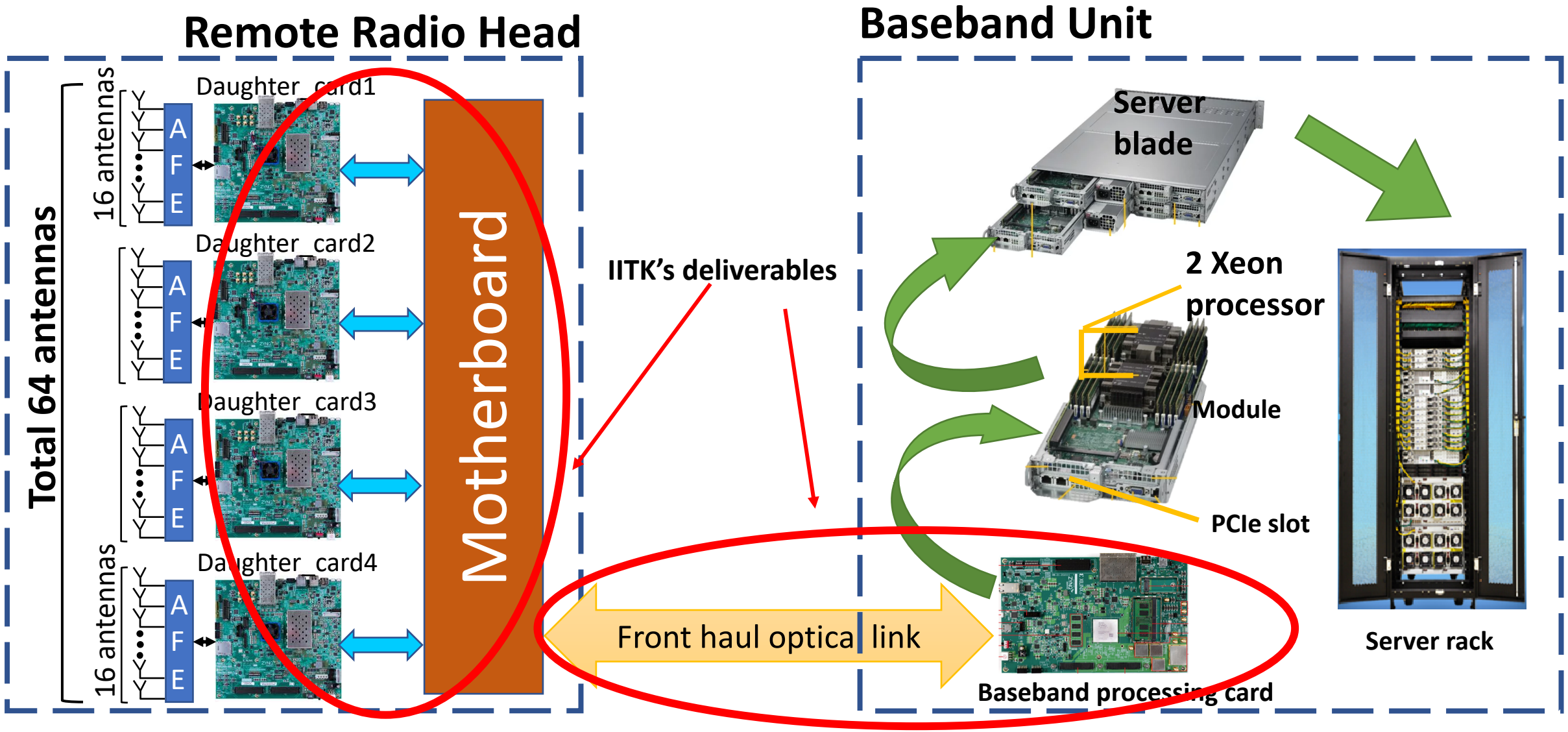


Work	Responsibility
Core N/W	IITB , CEWiT
UE	IITH
Åntenna array	SAMEER
5G Base station H/W, fronthaul/backhaul	IITK, IITM
5G Algorithms	IITK, IITM, IISc, IITD,CEWiT

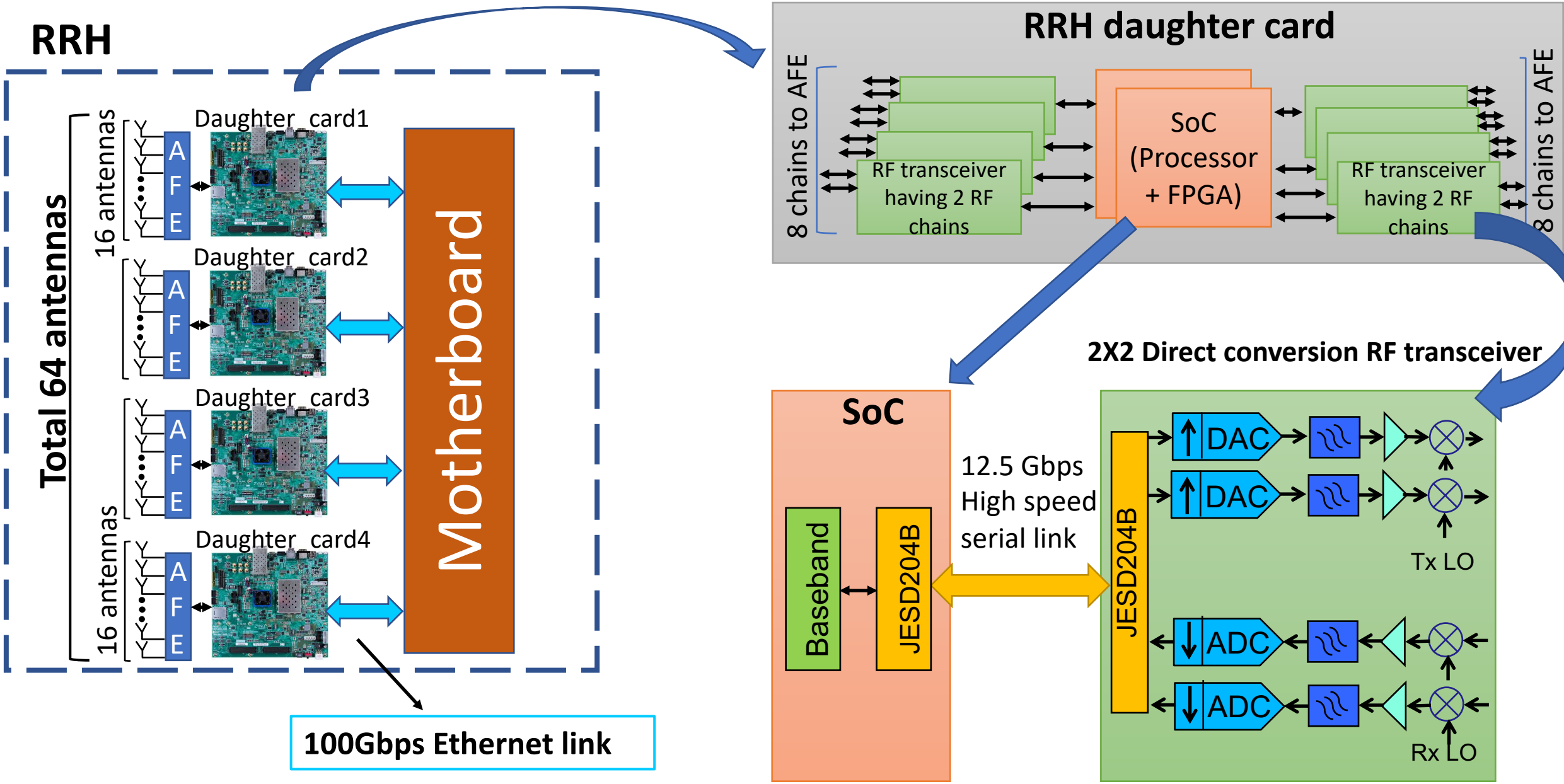
System development process



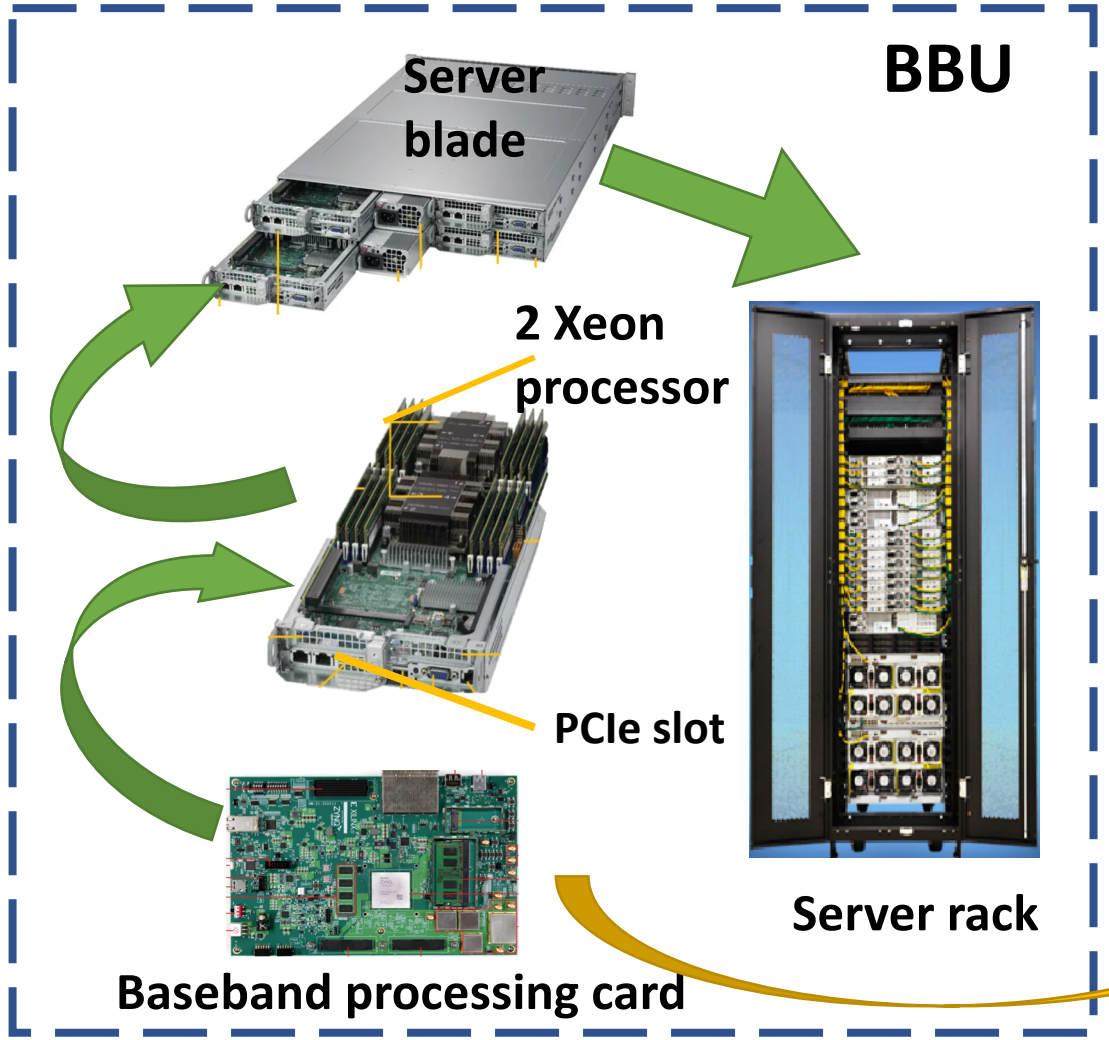
5G base station: Cloud radio

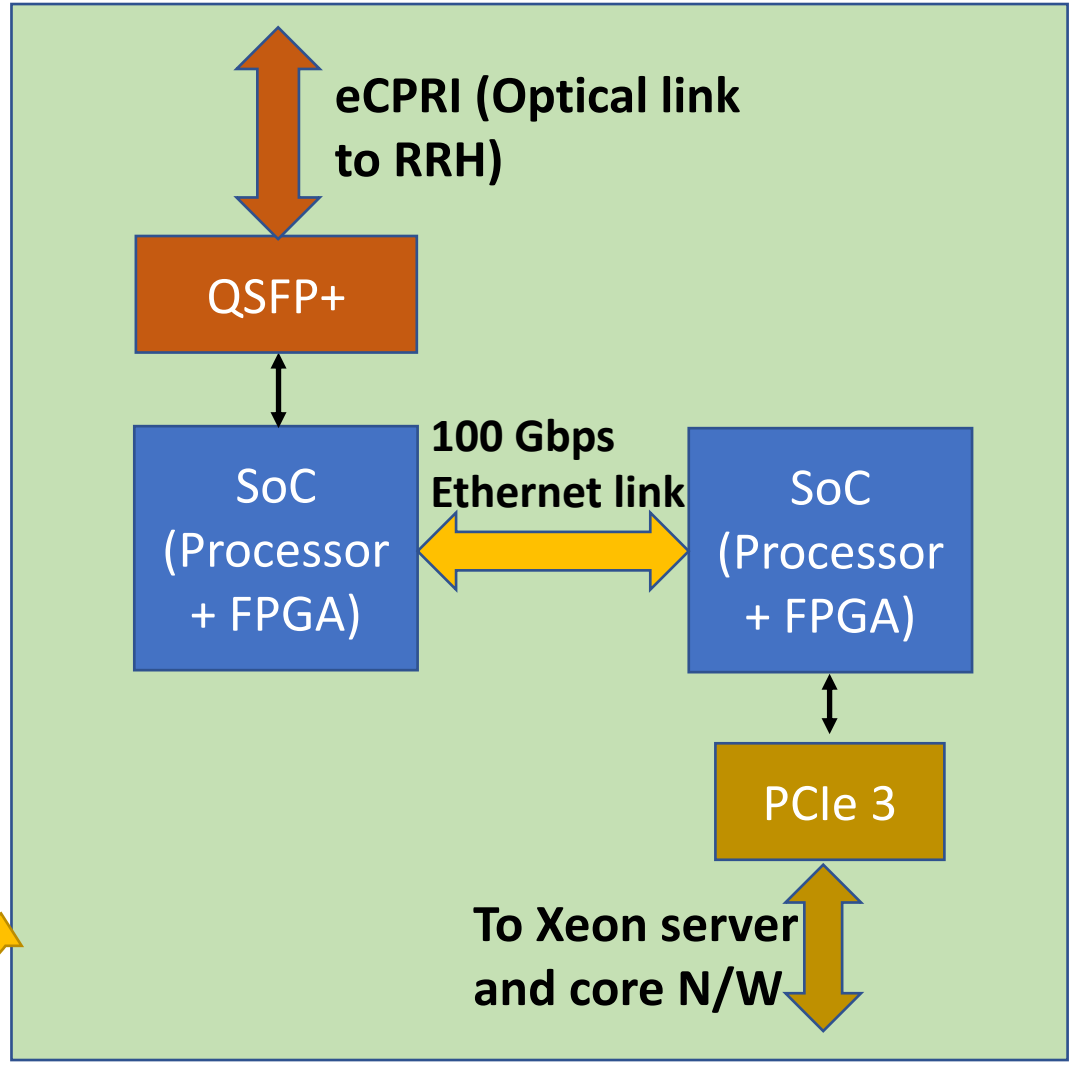


Remote radio head (RRH) architecture

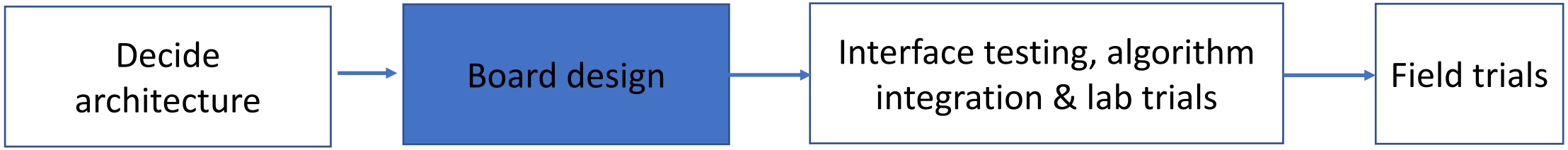


Architecture of baseband unit (BBU)





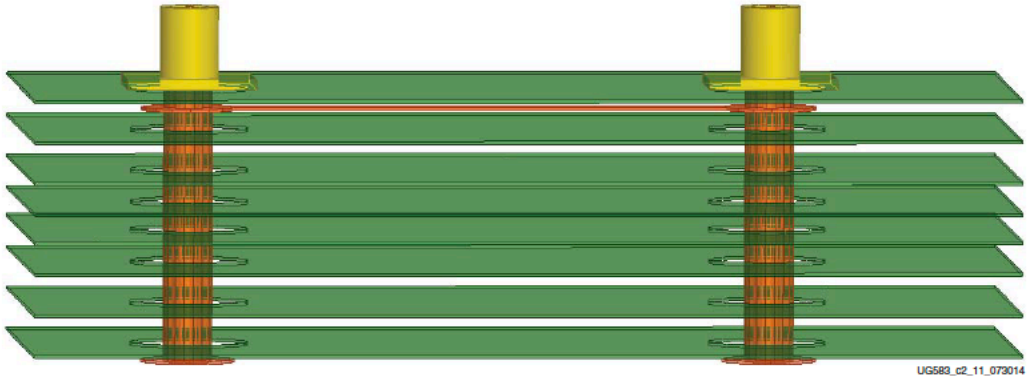
System development process (recap)



Board design

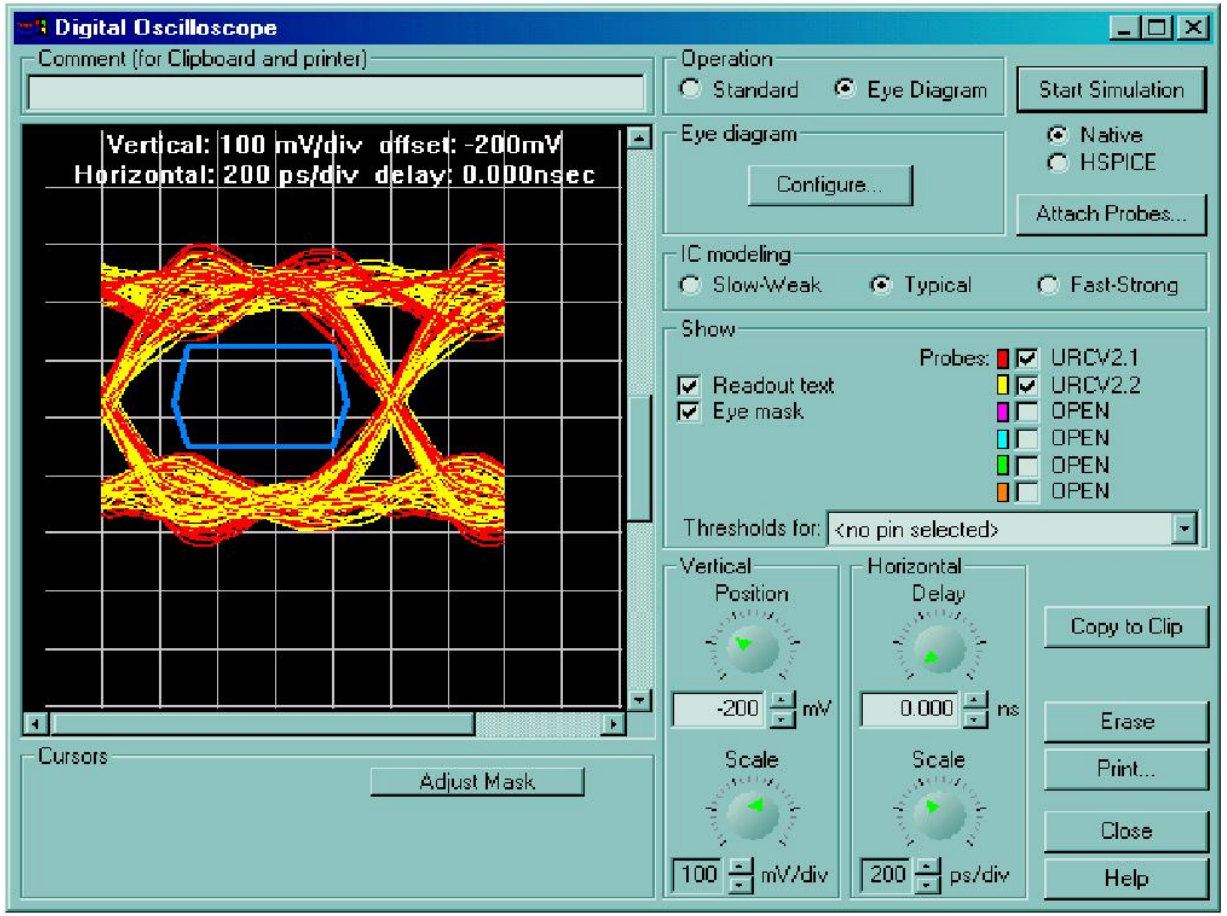
- Collate requirements of different ICs
  - Power supplies, interfaces to inter-connect
- High speed interconnects like 100G Ethernet are a challenge
- Performance of RF chains depend on placement & routing
- Signal integrity analysis of interconnects is done before fabrication

Interconnect design and signal integrity analysis



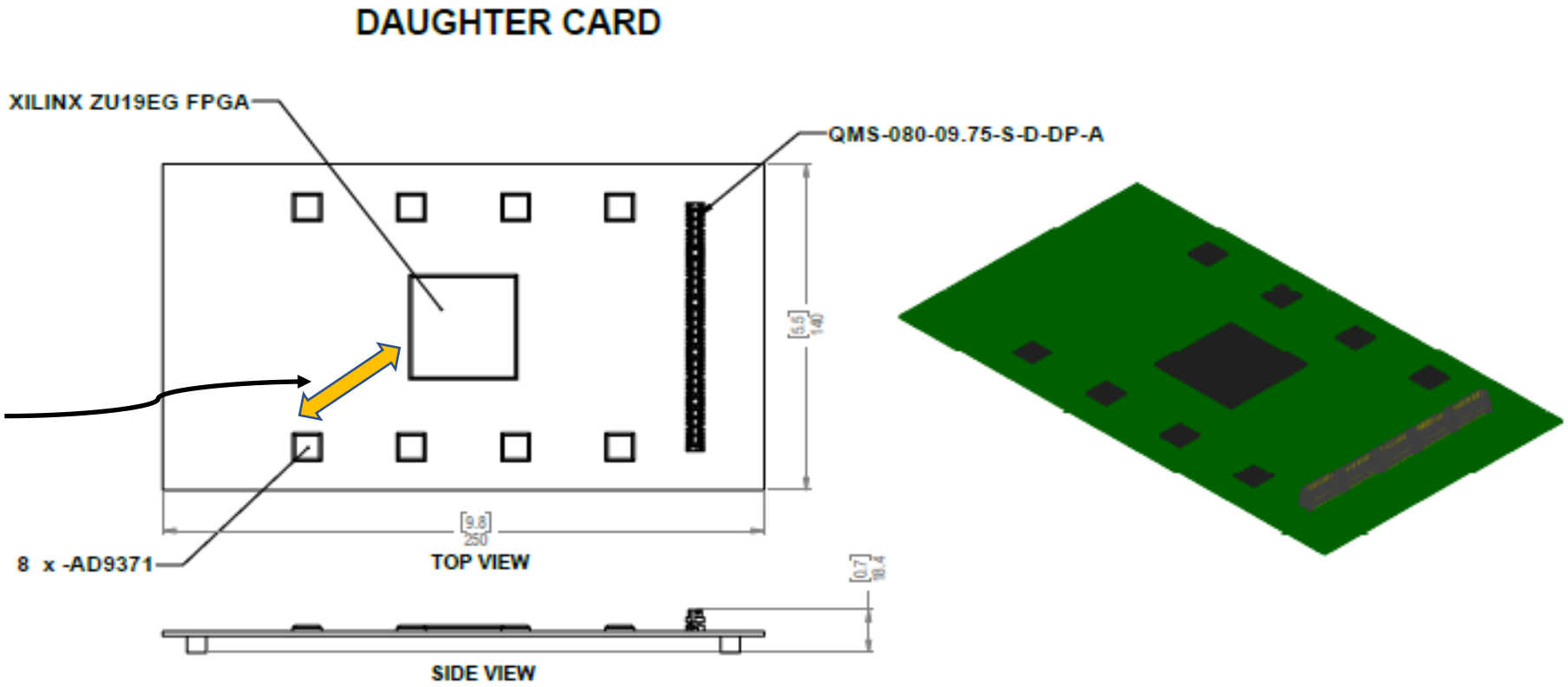
PCB Stack-up -1

PCB Stack-up -2

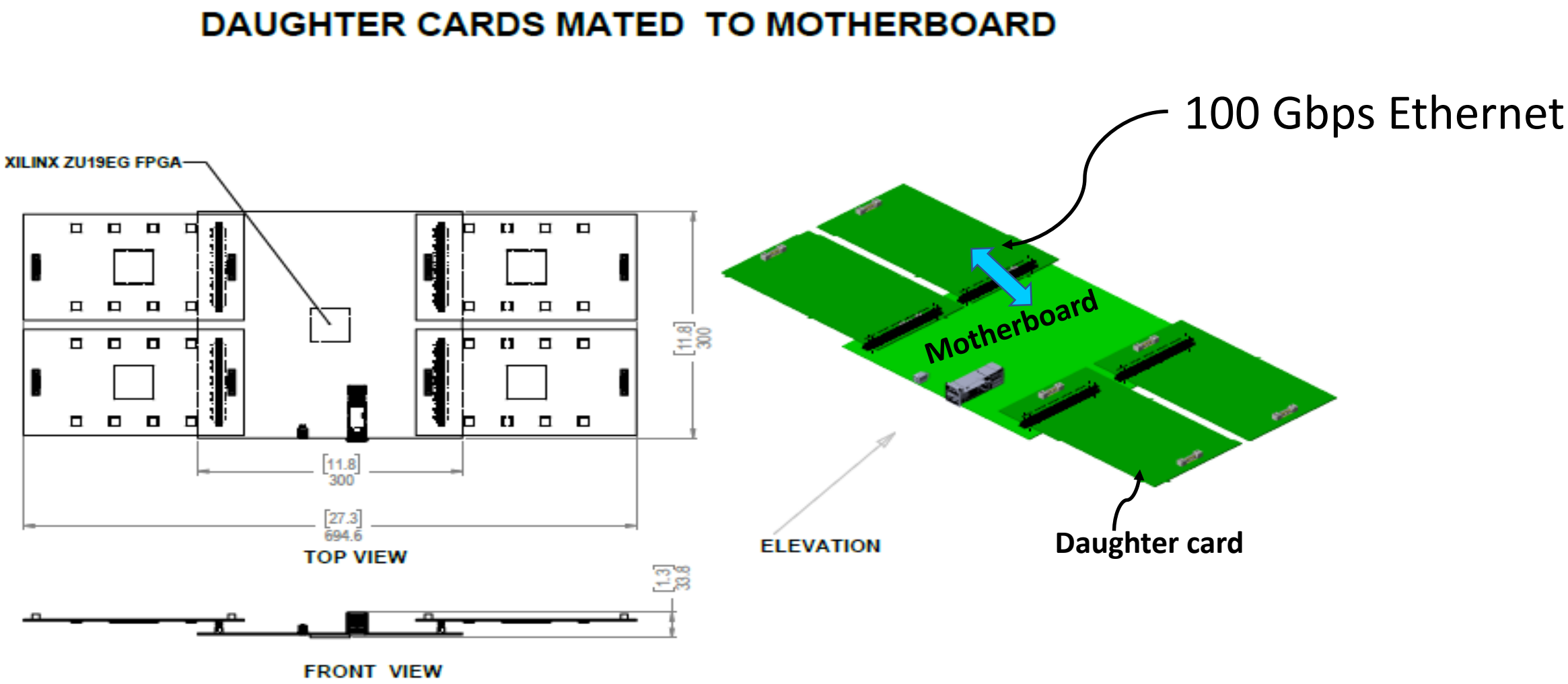


Remote radio head hardware (1)

12.5 Gbps serial link

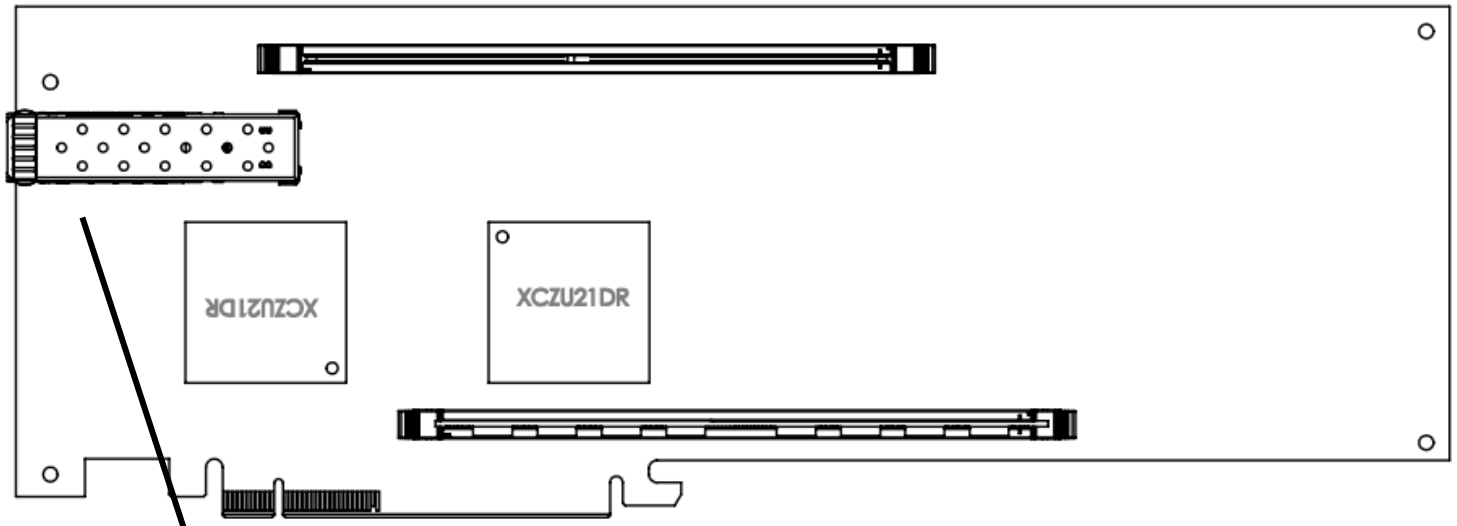


Remote radio head hardware (2)



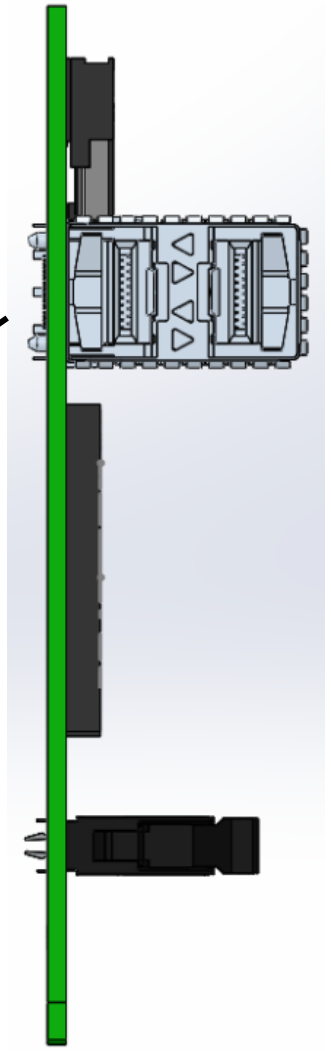
Remote radio head: An isometric view

Baseband unit hardware



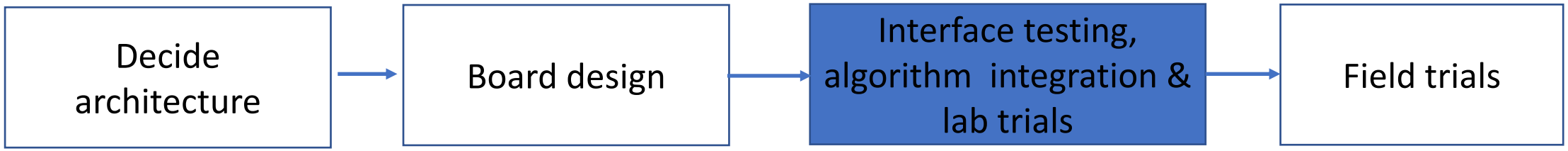
PCIe golden fingers

Stacked optical connecter



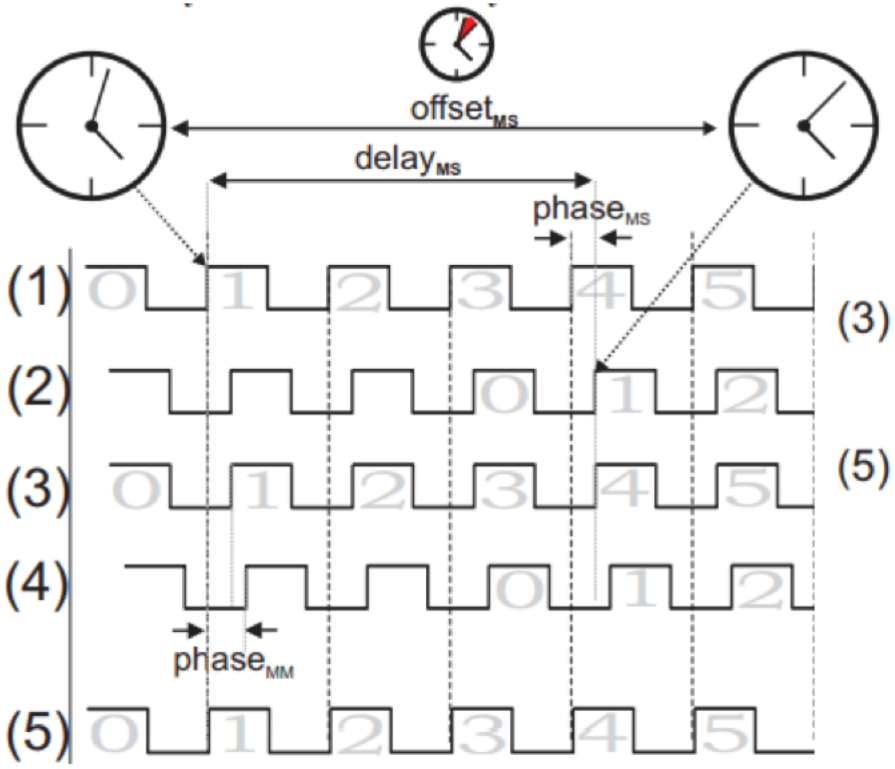
Side view

System development process (recap)



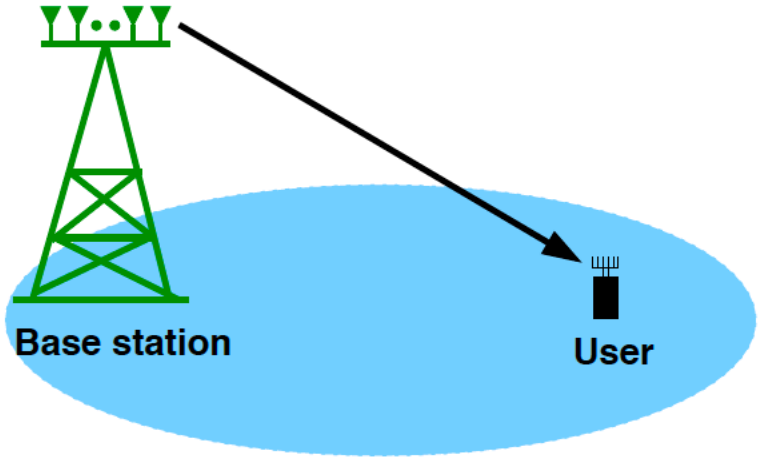
Algorithm to synchronize RRH and BBU

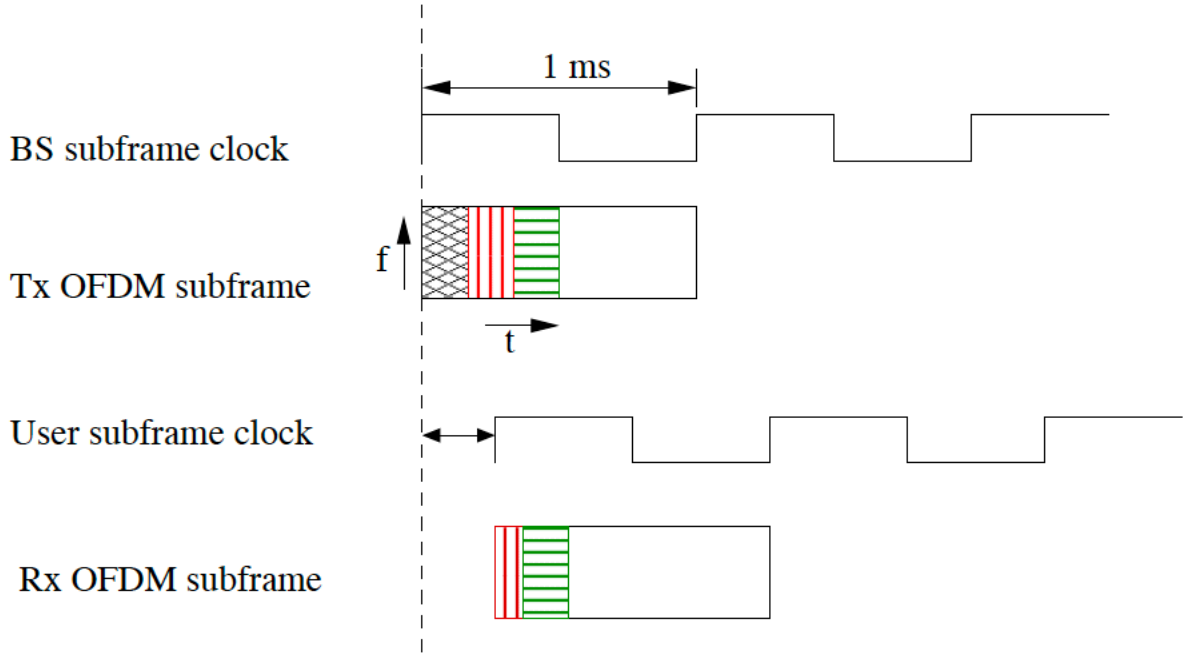
- Remote radio head and baseband unit are connected using optical fiber - unsynchronized



- Synchronization between them is achieved over Ethernet
  - We use White-Rabbit protocol - provides sub nano-second timing accuracy

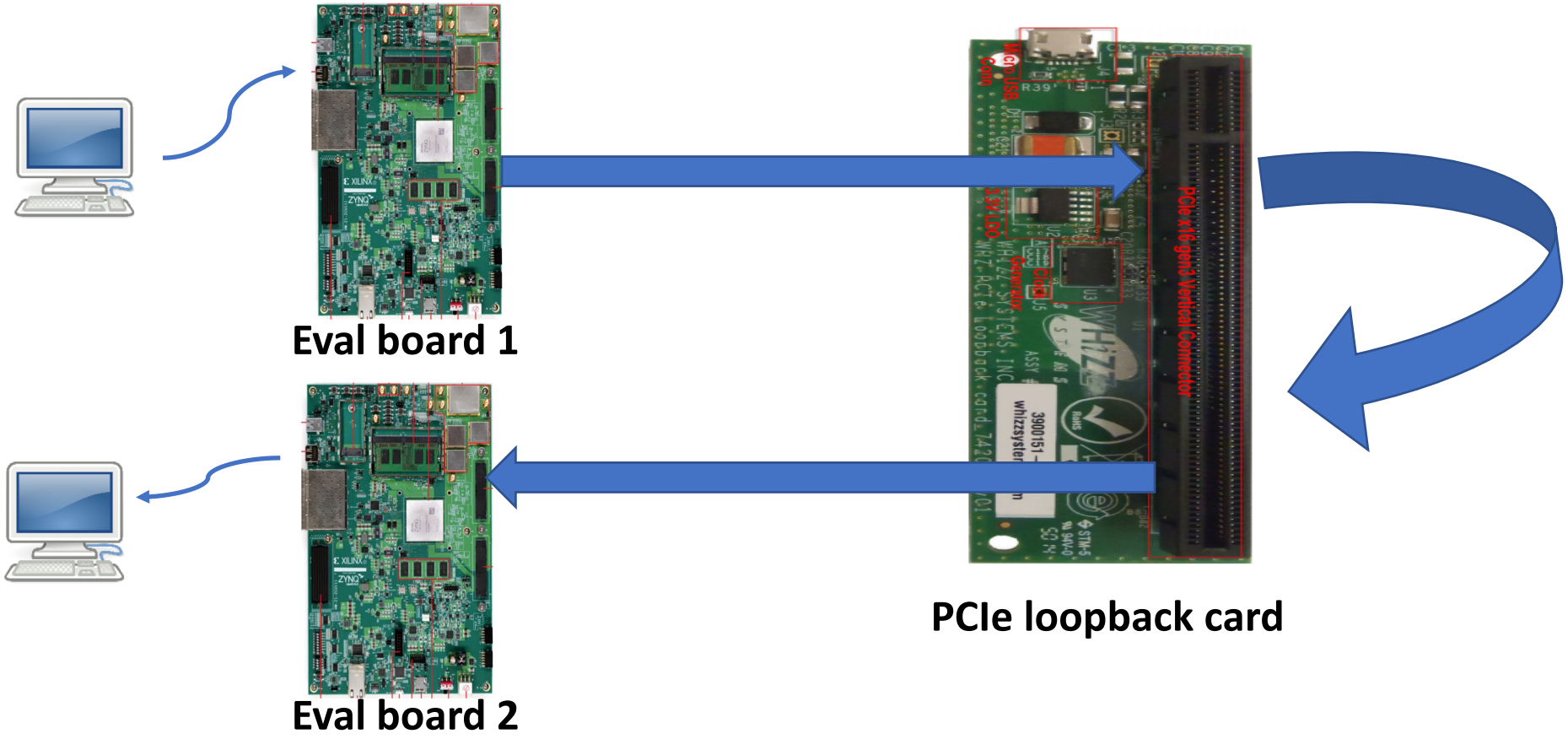
Downlink synchronization





Interface development, integration & lab trials

- Different interfaces e.g.,100G Ethernet, PCI express, eCPRI
- Interface driver development is done with off-the-shelf eval-boards



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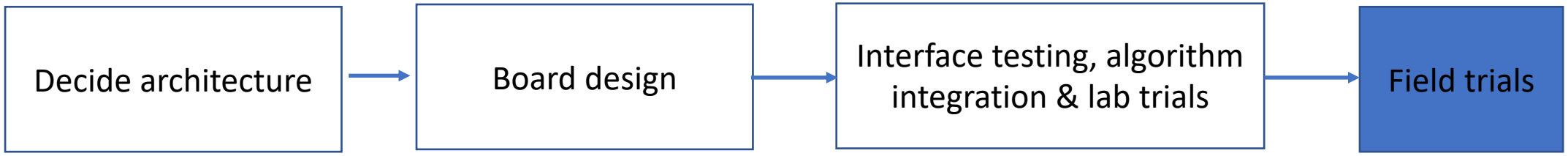
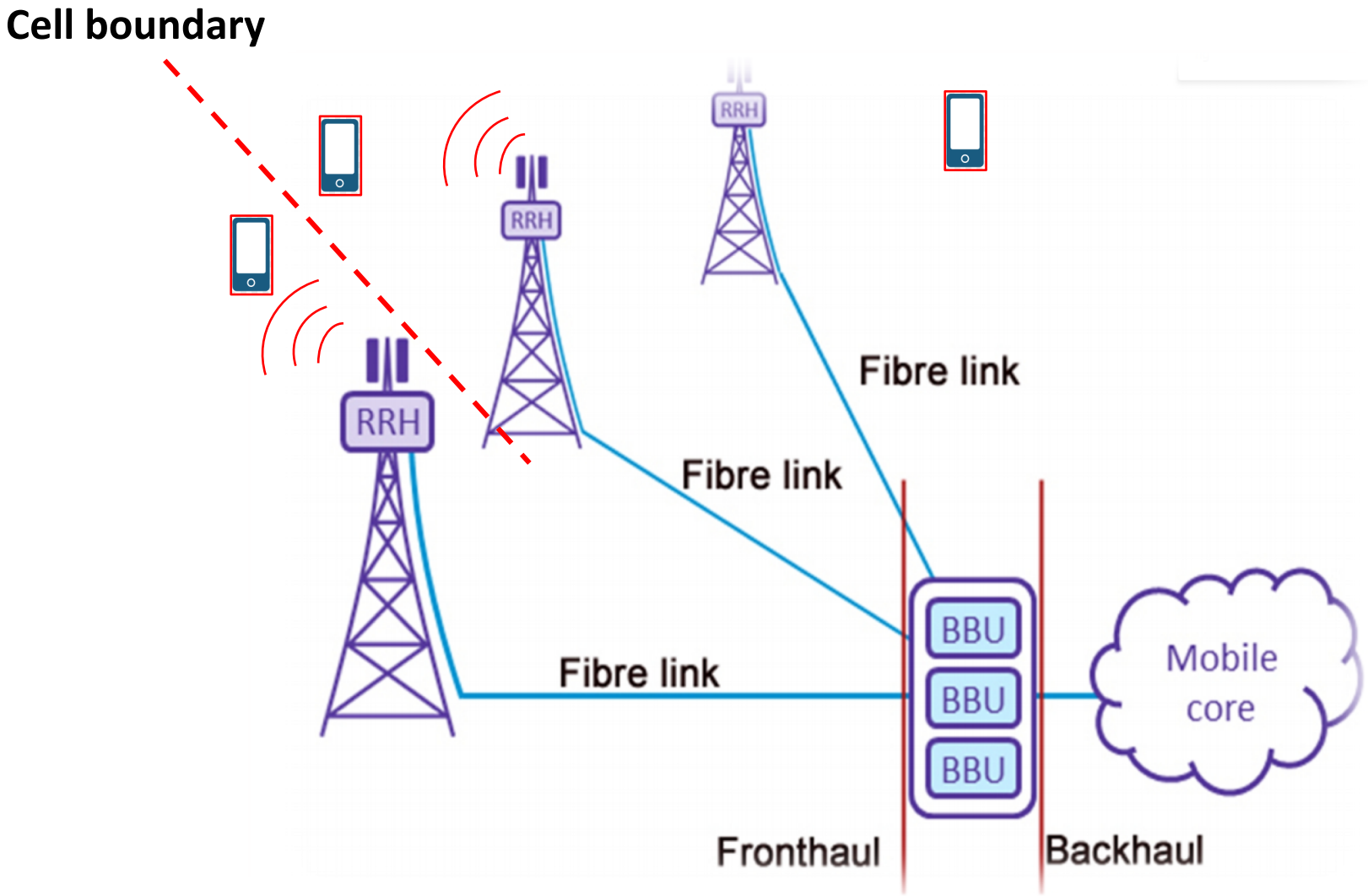


Planned field trials in IIT campus



Conclusions

- State-of-the-art 5G hardware and algorithms being built in IIT Kanpur
- Extreme engineering
  - Design of 20+ layers of printed circuit boards with 100 Gbps interfaces
  - Protocol development for 100 G/40G Ethernet, SERDES
- Algorithm design to process 100 MHz of bandwidth in < 1 ms
- Ericsson, Nokia, Huawei have this kind of hardware - can lead to start-ups

Thanks