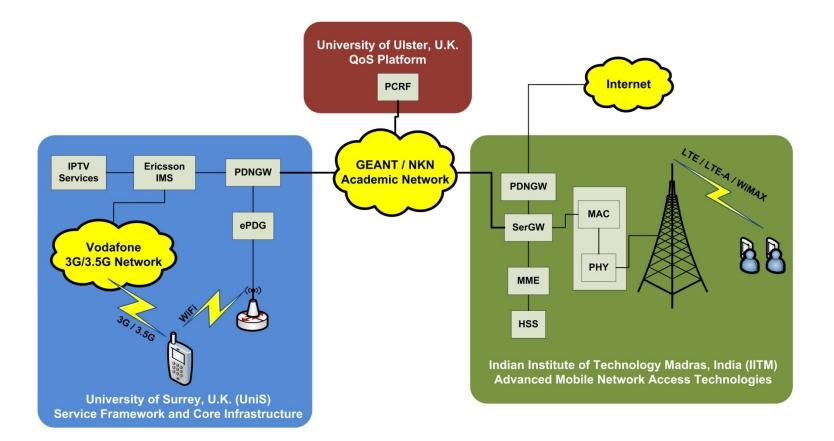


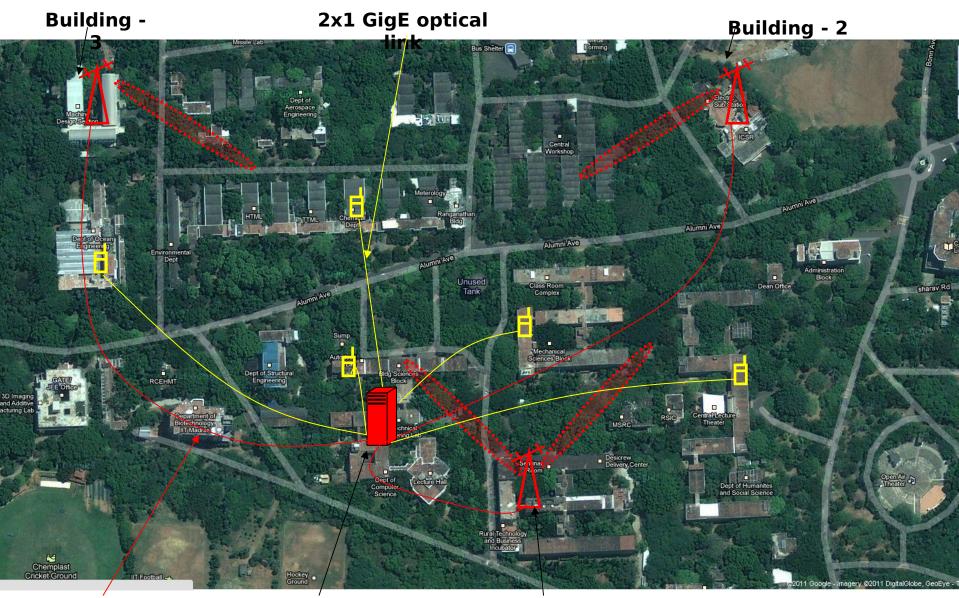
Overview of the Testbed



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Footprint of the IITM Access N/W Testbed



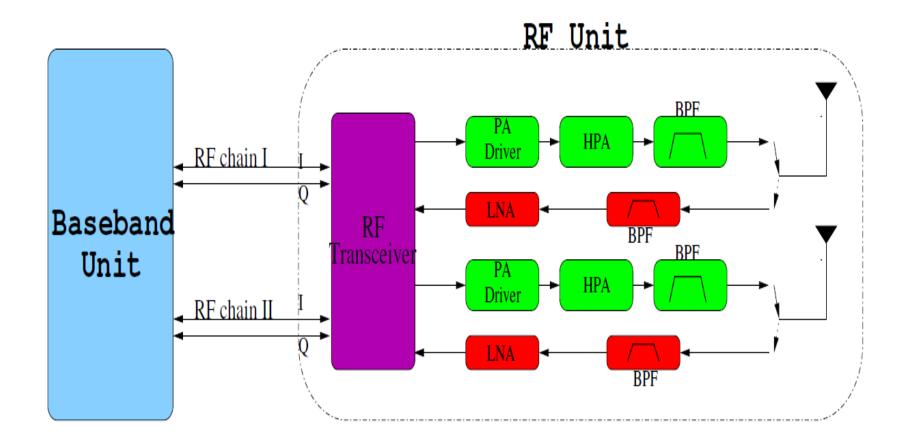


4x1 GigE optical link Computer Center

Building - 1

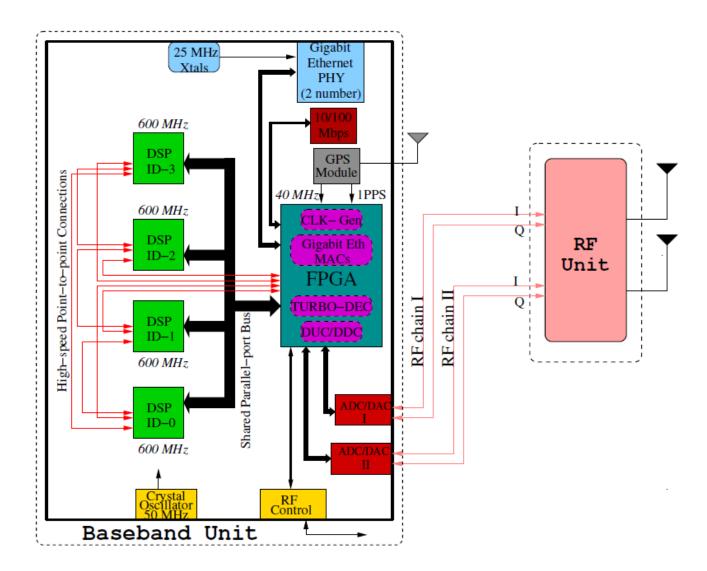


Testbed hardware architecture



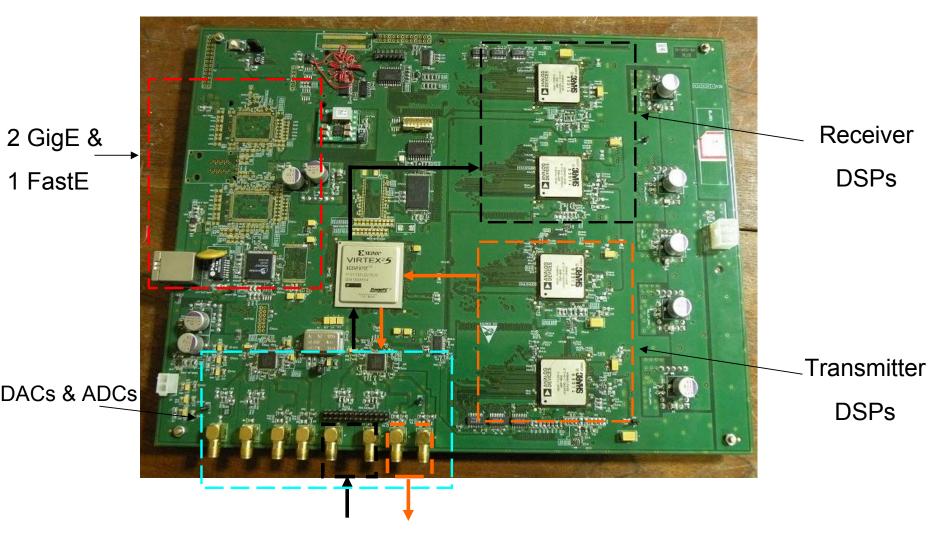


Testbed hardware architecture (contd)





Snapshot of the Baseband Platform



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Features of the Baseband platform

- Supports 20 MHz bandwidth
- Capable of operating in both FDD & TDD mode
- One board supports 2x2 MIMO
 - Board design is such that 2 boards can be used for 4x4 MIMO
- DSP bank for embedded processing
 - 4DSPs: TigerSharc TS201
 - 32-bit floating-point processor; 24 Mb on-chip memory
- FPGA: Xilinx Virtex-5
 - One embedded RISC processor: PowerPC 440x5 32-bit from IBM
- On-board 16Mbit x 16 DDR SDRAM interfaced to PowerPC
- Two GigE & one Fast Ethernet interface
- GPS connectivity
- Multi-Gigabit intra-DSP & DSP-FPGA interfaces

System parameters of the Access N/W Testbed



Parameters

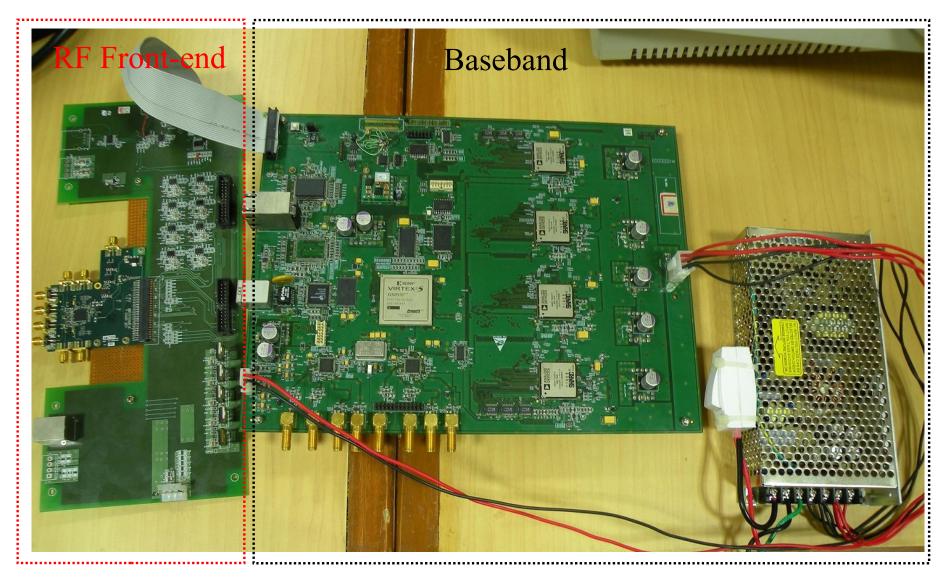
Number of BSs Number of UEs Number of sectors Transmission bandwidth BS transmit power UE transmit power

BS antenna radiation pattern MS antenna radiation pattern BS antenna configuration UE antenna configuration Antenna polarization DAG/ADC resolution

Value 4 12 4 20 MHz 5 W 250 mW Sector (90° beamwidth) Omni 4x42x2 Cross 12 bits

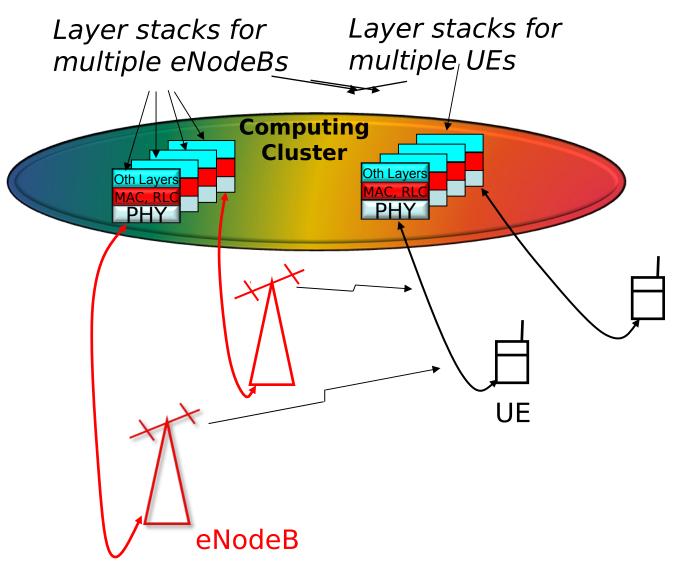


Snapshot of Baseband with RF



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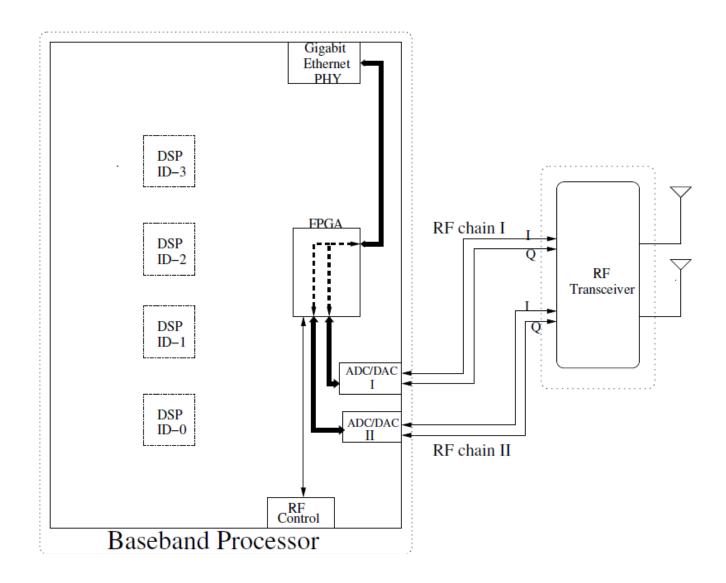
Software flow-diagram for SDR mode





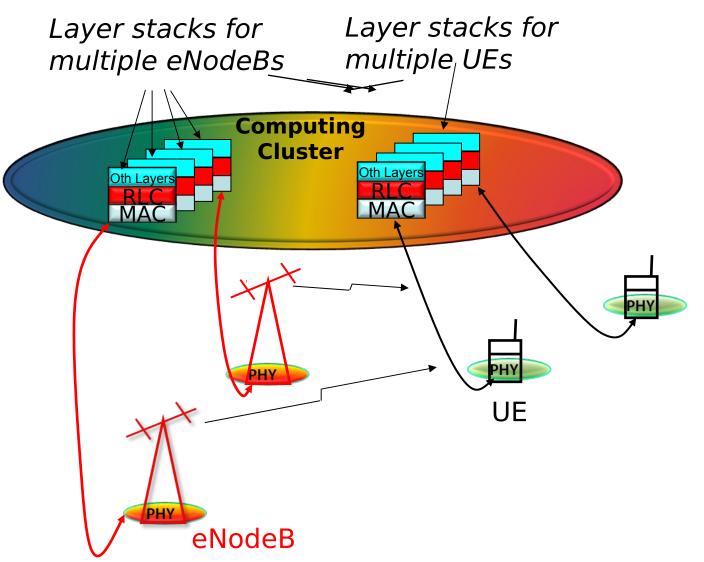


Data flow for SDR mode



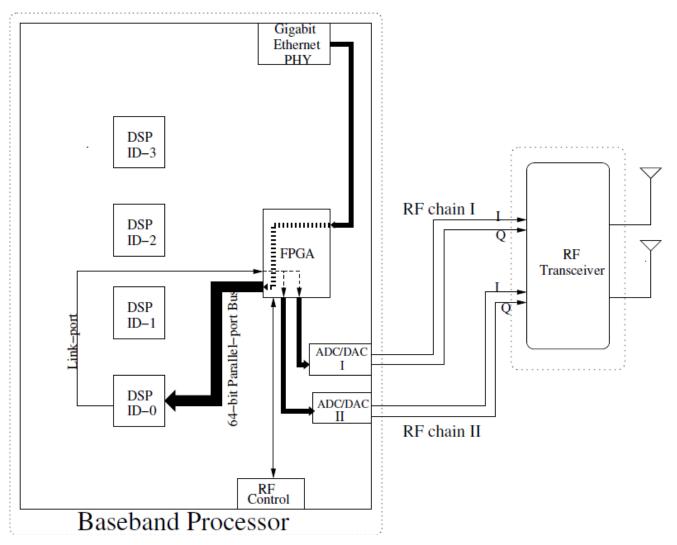
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Software flow-diagram for real-time mode



CEWiT/

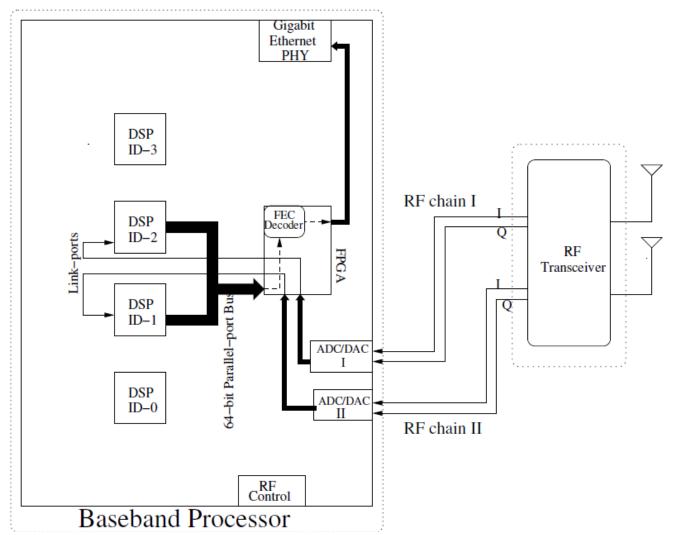
Transmit data flow for real-time mode



CEWIT

INDIA

Receiver data flow for real-time mode

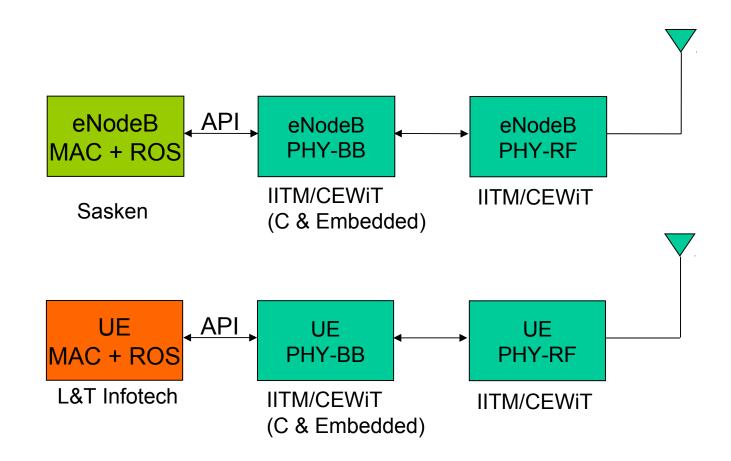


CEWIT

INDIA



Testbed software schematics

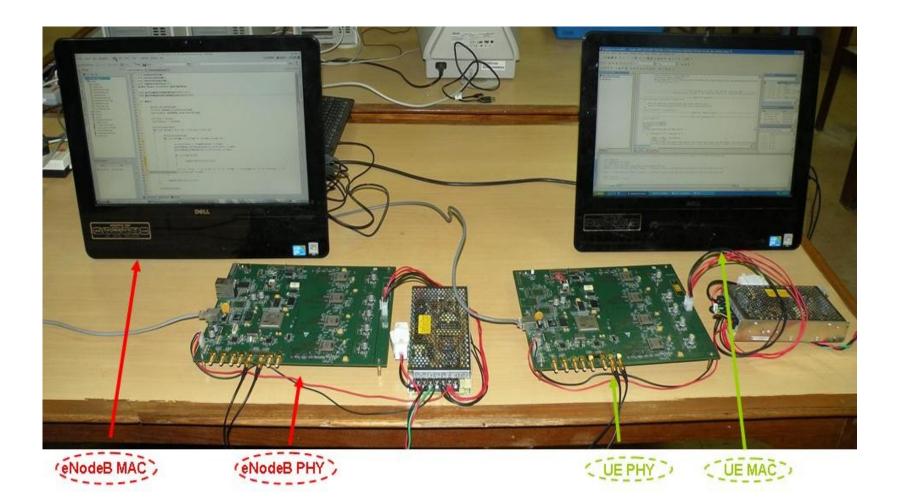


ROS: Rest Of the Stack

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MAC-PHY Integration set-up of the Testbed





Physical Layer design

- 3GPP Release 8 compliant
- PHY functionality of eNodeB and UE
- Support for TDD and FDD mode
- Support for various MIMO modes
- Scalable bandwidth up to 20 MHz
- PHY functions developed in C/C++, MATLAB and Assembly
- APIs defined to interface with higher layers
- PHY layer being integrated with higher layers from other organizations

Project Partners









