

Design of LTE radio access network testbed

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Brief profile

Practical system design experience – Jan. 2004 - Jul. 2011

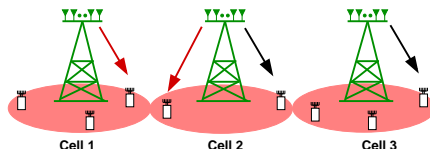
- ▶ WiMAX system design (MIDAS).
 - ★ [Hardware and physical layer algorithm design](#) for base station and user.
- ▶ Design of LTE radio access network testbed (CEWiT).
 - ★ [Hardware design and physical layer algorithm](#) development.

Academic research experience

- ▶ Aug. 2011 - Jul. 2015 – PhD.
 - ★ Transceiver design for MIMO asymmetric two-way relaying.
- ▶ Jul. 2000 - Dec. 2003 – MS.
 - ★ Design of Transceiver for 3G DECT Physical Layer.

Motivation

Cellular design requires system-level evaluation.



Reason: link-level techniques do not perform well at system level

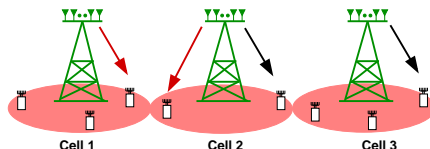
- ▶ **Spatial multiplexing MIMO** – loses effectiveness in multi-cell environment.¹
- ▶ **Interference alignment** – blanket use is altogether detrimental.²

¹ Andrews *et al.* "Overcoming interference in spatial multiplexing MIMO cellular networks", IEEE Wireless Commun. Mag., Dec. 2007.

² Mungara *et al.* "System-Level Performance of Interference Alignment", IEEE Trans. Wireless Commun., Feb. 2015.

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System simulators are usually built to analyse performance.

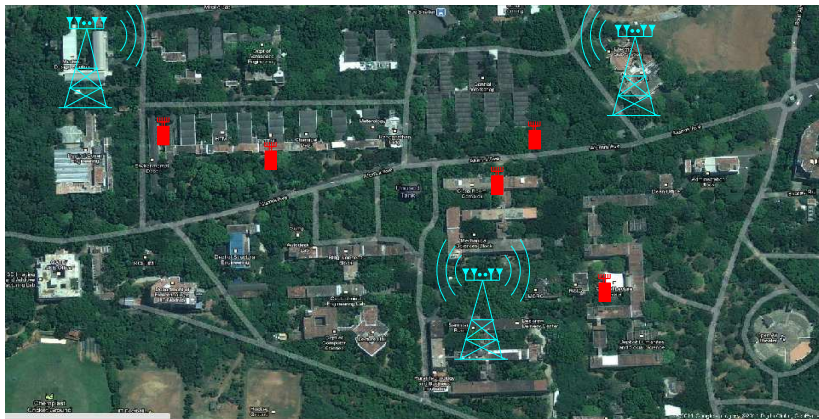
- ▶ Much depends on the choice of channel models.

A testbed provides realistic fading and interference settings.

¹ Andrews *et al.* "Overcoming interference in spatial multiplexing MIMO cellular networks", IEEE Wireless Commun. Mag., Dec. 2007.

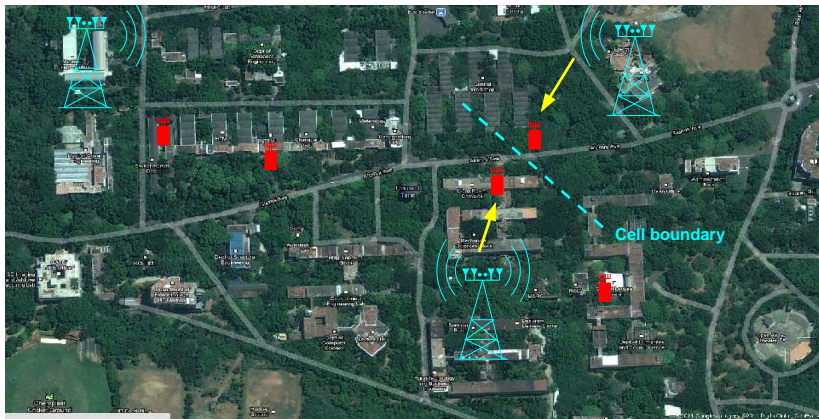
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Testbed at IIT Madras



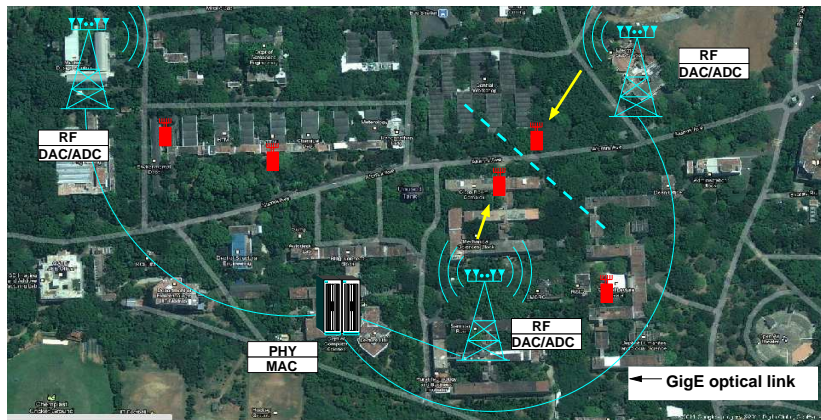
Four base stations and twelve users.

Testbed at IIT Madras



Can emulate realistic interference scenarios.

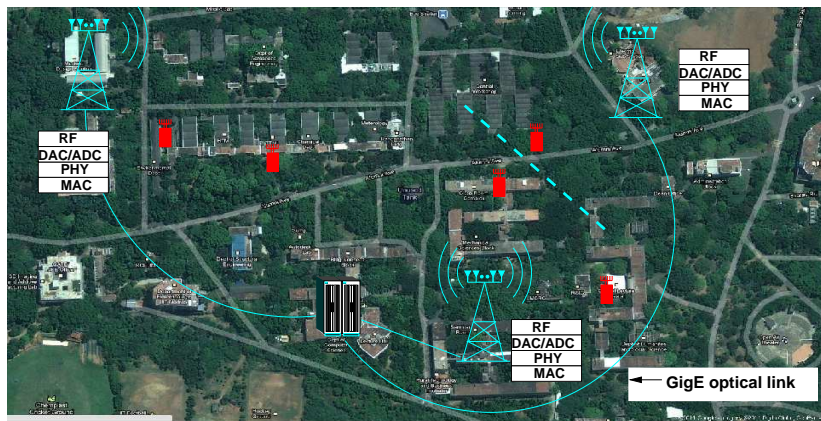
Testbed – cloud radio mode



Base stations can easily coordinate to mitigate interference.

- Possible due to channel and data availability in cloud.

Testbed – conventional distributed mode



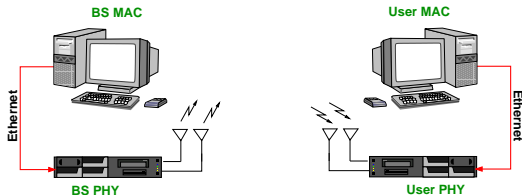
Each base station performs MAC, PHY, mixed-signal and RF processing.

Requirements history

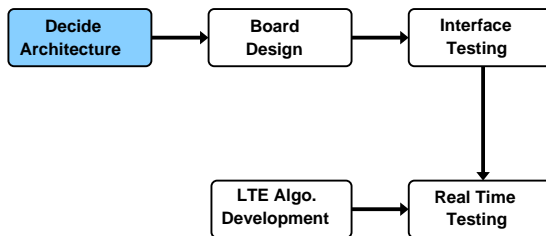
Implement cloud radio or distributed mode first?

Sasken – LTE base station MAC; L&T Infotech – LTE user MAC.

My deliverable – physical layer hardware and algorithms.



System development process



Decide hardware architecture – type/number of IC and IC interconnections

- ▶ Based on system specifications.

Board design

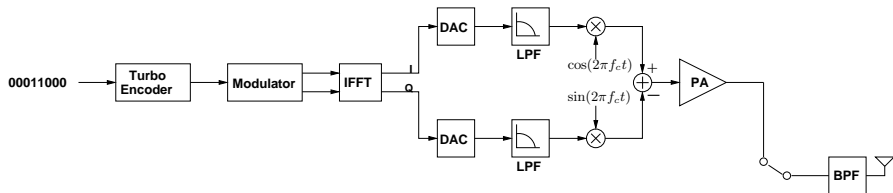
- ▶ Ensure ICs and IC interconnections work reliably.

Hardware architecture development

System specifications – based on LTE:

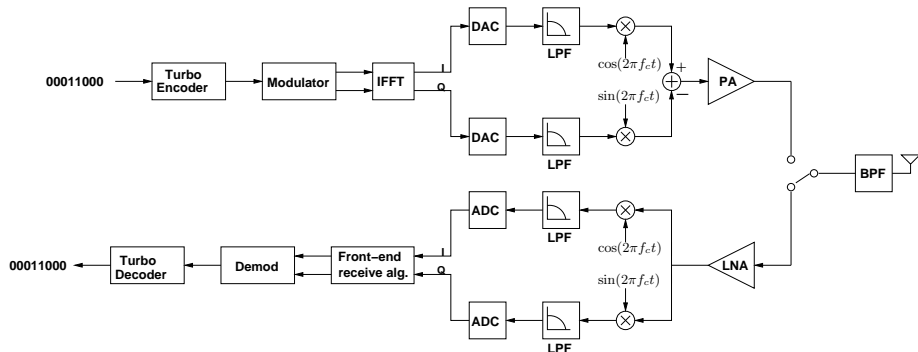
- ▶ OFDMA, 20 MHz bandwidth and 2×2 MIMO.
- ▶ Transmit power – base station: 5 W and user: 250 mW.
- ▶ Baseband hardware should work in
 - ★ Frequency division duplex mode - required by the partners.
 - ★ Time division duplex mode - experimental spectrum availability.
 - ★ Cloud radio/distributed mode.
- ▶ Turbo coding for data.

Architecture of generic OFDM transceiver hardware



Two digital-to-analog converters (DAC) per transmit chain.

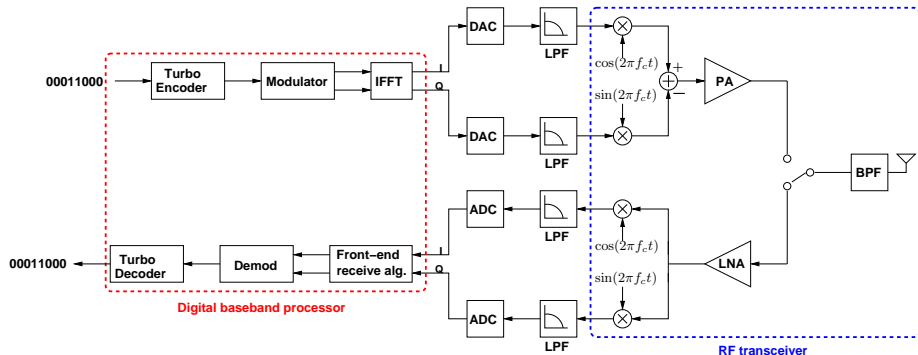
Architecture of generic OFDM transceiver hardware



Front-end receive algorithms

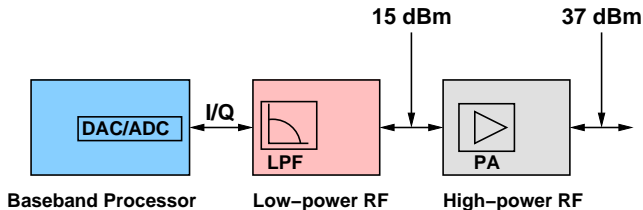
- Synchronization, channel estimation/equalization, MIMO receiver.

Architecture of generic OFDM transceiver hardware

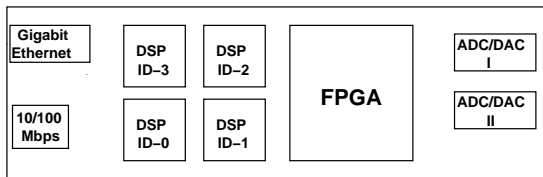


DAC/ADC, LPF can be part of either **baseband processor** or **RF transceiver**.

Our architecture



Architecture of baseband processor



Task partitioning

- ▶ DSPs – most of signal processing except **turbo decoding (FPGA)**.

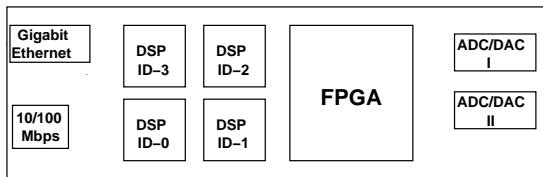
First design decision – number of DSPs, FPGAs, ADCs/DACs

- ▶ System bandwidth – 20 MHz; 2×2 MIMO.
- ▶ Use available processing requirements, cross-compile C code.
- ▶ 4 DSPs and a FPGA; 4 DACs and 4 ADCs.

Second design decision – speed of inter-IC communication links

- ▶ DAC/ADC sampling rates, low-pass filter design.

Architecture of baseband processor



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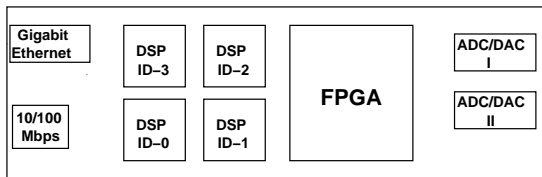
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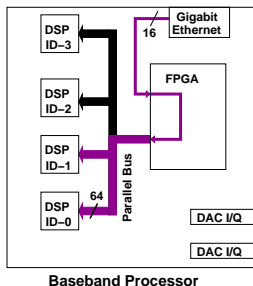
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- ▶ DAC/ADC sampling rates, low-pass filter design.

System dimensioning LTE - 20 MHz

Parameter	Value
Subframe duration	1 ms
OFDM symbols in a subframe	14
FFT size	2048
Cyclic prefix size	144
DAC/ADC sampling rate	$14(2048 + 144)/10^{-3}$ $= 30.72$ MHz.

Speed of inter-IC communication links - transmit



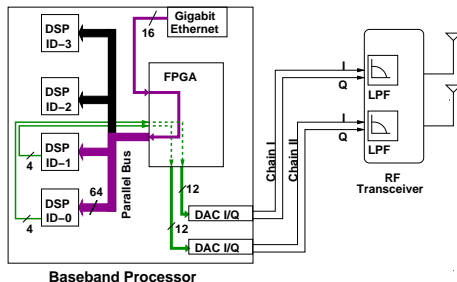
Largest MAC data block size for 1 ms subframe – 75676 bits

- ▶ Peak bit-rate for single antenna – 76 Mbps.
- ▶ Parallel-bus rate – $64 \times 60 = 3.8$ Gbps.

DSPs process transport blocks and compute IFFT samples

- ▶ DSP-0: Tx-chain-I; DSP-1: Tx-chain-II.

Speed of inter-IC communication links - transmit

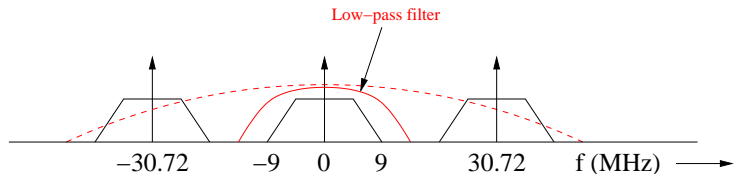


DSPs send IFFT samples to FPGA.

DAC sampling rate 30.72 MHz with I/Q bit-width = 12 bits

- ▶ DSP-FPGA link required bit-rate = $30.72 \times 24 = 737.28$ Mbps.
- ▶ Link works at $F = 150/300/400/600$ MHz with $F \times 8$ throughput.

Transmit low-pass filter and associated rates



Filter design might require interpolating the IFFT output

- ▶ For example, $\uparrow 4$ requires $F=600$ MHz.

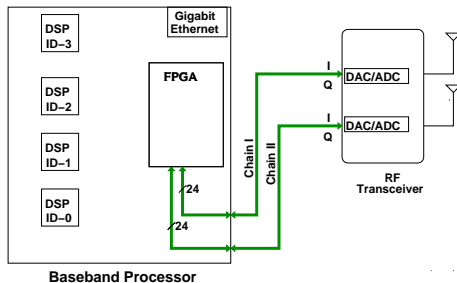
Difficult to design DSP-FPGA link at $F=600$ MHz

- ▶ Timing budget constraints in FPGA.

Two options

- ▶ Perform interpolation in FPGA.
- ▶ DAC which can perform on-chip interpolation.

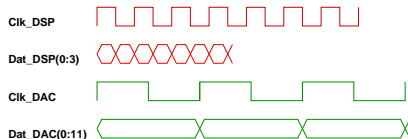
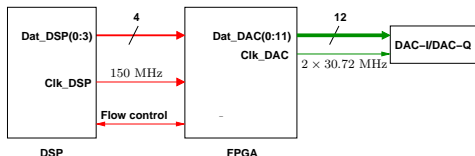
Analog I/Q versus Digital I/Q



Engineering decision – ease of testing vs cost

- ▶ Can validate the entire baseband chain with DAC/ADC on baseband board.
- ▶ RF can be evaluated standalone.
- ▶ Difficult to carry 48 signals.

Role of FPGA – glue logic

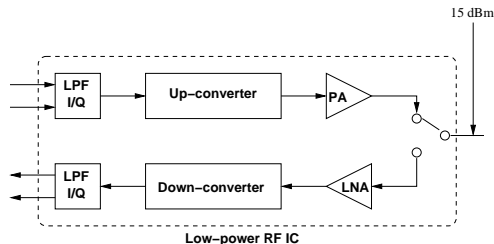


Facts about DSP-FPGA-DAC link

- ▶ DSP-FPGA link – 4 bit, throughput $150 \times 8 = 1.2$ Gbps.
- ▶ FPGA-DAC link – 12 bit, throughput $30.72 \times 2 \times 12 = 737.28$ Mbps.
- ▶ Leads to mismatch in data format and throughput.

▶ GlueDetail

Architecture of RF transceiver

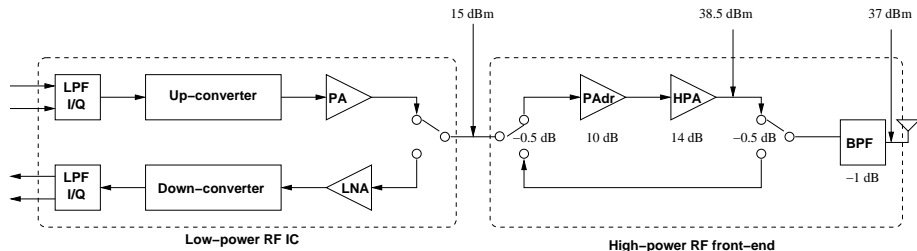


Desired transmit power for base station – 37 dBm.

Direct conversion receiver

- ▶ DC offset not a problem as zeroth subcarrier is not used in LTE.

Architecture of RF transceiver



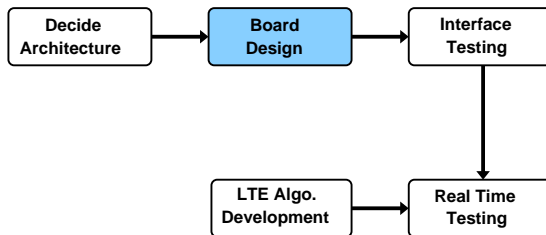
PA driver (PA_{dr}) – 10% efficiency

- ▶ Peak power 33 dBm; back-off by 8.5 dB.

High Power Amplifier (HPA) – 28% efficiency

- ▶ Peak power 45 dBm; back-off by 6.5 dB.

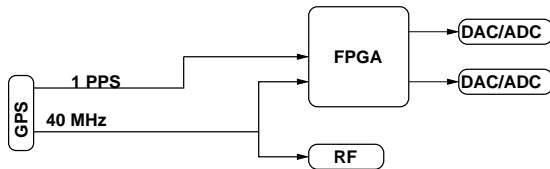
System development process – recap



Board design

- ▶ Collate requirements of different ICs.
- ▶ Design interconnections between different ICs.
- ▶ Route signal interconnections and fabricate the board.

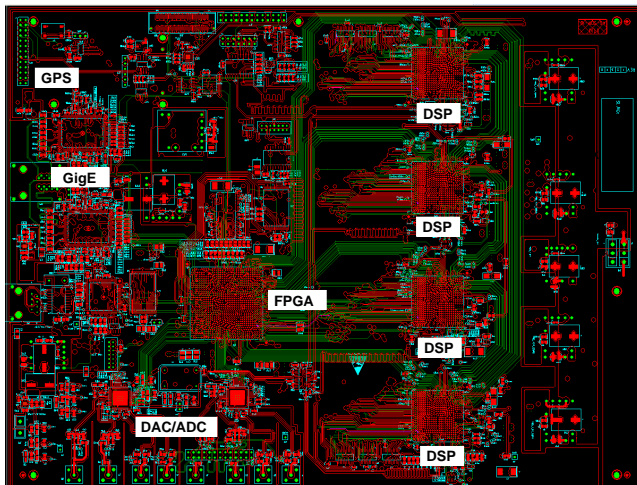
Clocks on the baseband board



GPS clocks – synchronizes frame and frequency for base station and user

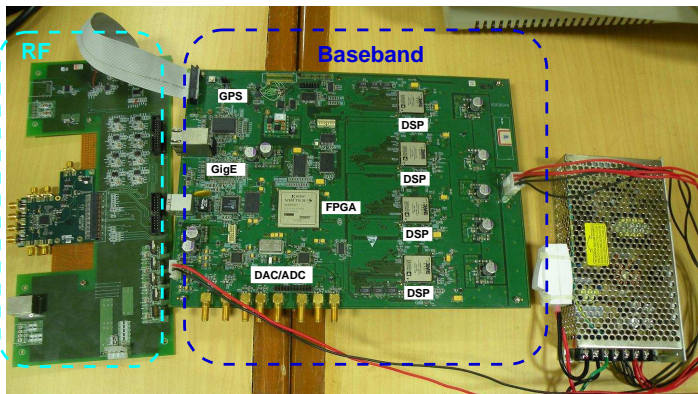
- ▶ To study inter-BS cooperative schemes.
- ▶ Frequency accuracy of ± 0.1 Hz at 2 GHz.

Layout design



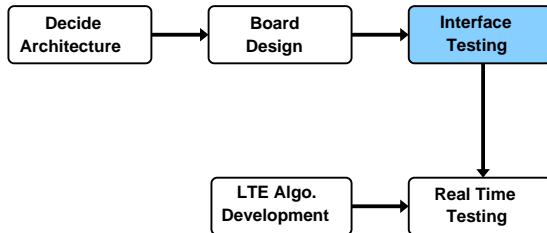
One layer of board layout

Snapshot of base station

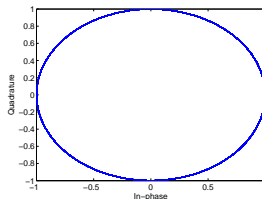
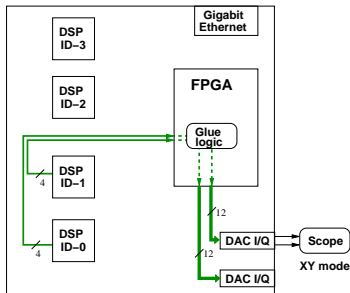


Board design also requires working with multiple vendors/companies.

System development process – recap



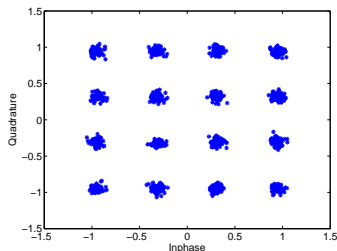
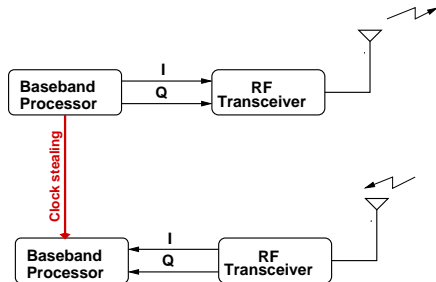
Evaluation of transmit links



Pre-computed sin/cos samples stored in DSP memory.

Validates DSP-FPGA, FPGA-DAC, DAC-connector links and glue logic.

Testing of baseband + RF

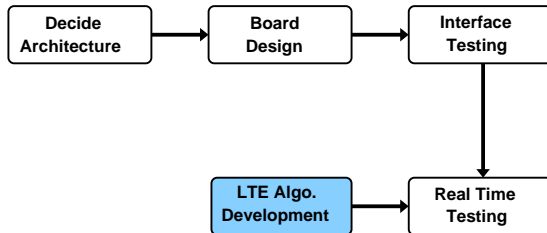


Captive testing with stolen frame and RF reference clocks

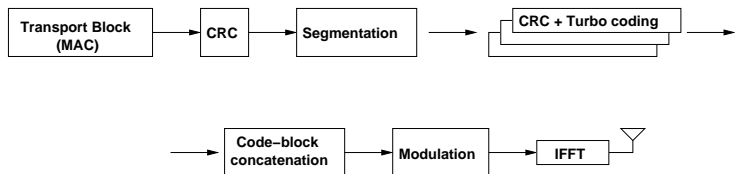
- ▶ Useful for standalone RF evaluation, without synchronization algorithms.
- ▶ **Hardware should be designed for clock stealing!**

EVM for 16-QAM 7% (LTE: 12.5%).

System development process – recap



LTE transmit chain – data



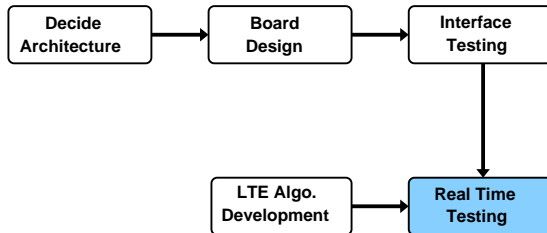
Largest transport (**turbo code**) block size – 75676 (**6144**) bits

- ▶ Multiple turbo decoders work in parallel – reduced delay.
- ▶ For 6144 code block size, our turbo decoder required 0.8668 ms.
- ▶ MAC transport block should be segmented.

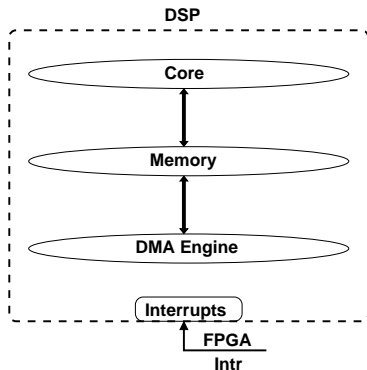
Developed MATLAB code also for other front-end receiver algorithms

- ▶ Used by students to develop embedded code.

System development process – recap



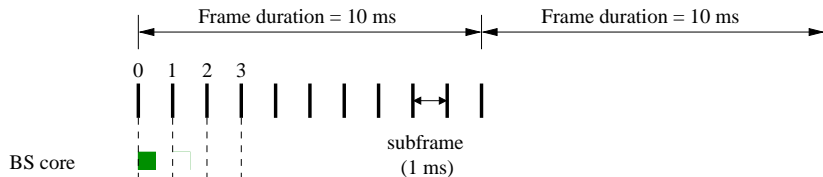
Short primer on DSP architecture



Core executes PHY transceiver functions and alerts DMA engine.

DMA engine sends data to FPGA.

PHY processing and transmission



FPGA is the time-keeper and generates all on-board clocks.

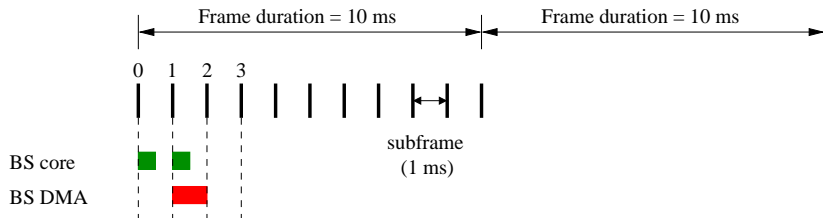
- ▶ Generated using a counter running at 30.72 MHz.

Every 1 ms, FPGA interrupts the DSP to indicate subframe start.

DSP starts PHY processing at $t = 0$ ms and finishes at $t < 1$ ms.

- ▶ DSP copies processed subframe into its DMA buffer.

PHY processing and transmission



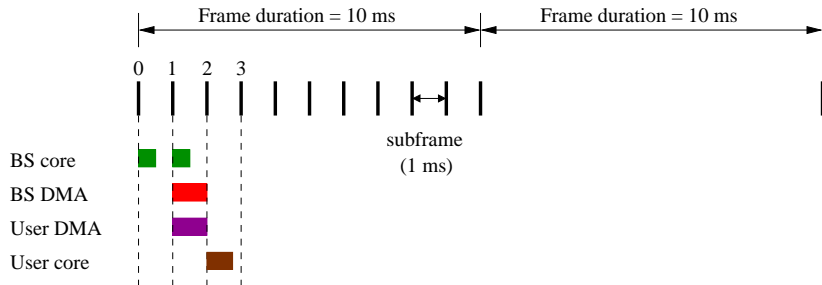
At $t = 1 - \delta_1$ ms, DMA engine starts sending data to FPGA which buffers it.

- Core concurrently starts processing new subframe at $t = 1$ ms.

At $t = 1 - \delta_2$ ms with $\delta_2 < \delta_1$, FPGA starts sending data to DAC.

At $t = 1$ ms, first subframe transmission starts and gets over at $t = 2$ ms.

PHY processing and transmission



User starts receiving data at $t = 1$ ms and finishes at $t = 2$ ms.

User starts processing data at $t = 2$ ms and finishes at $t < 3$ ms.

► MacPhyInt

Snapshot of integrated MAC-PHY setup



Demonstrated FTP link that validated

- Inter-working of Sasken, L&T MAC, IITM PHY hardware, algorithms.

Concluding remarks

Led a team of 15 students, project associates and CEWiT engineers.

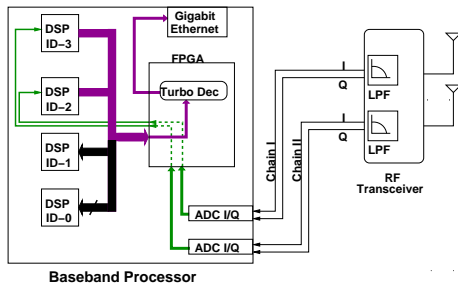
Worked with RF designer, OS engineers from Sasken and L&T.

Testbed provided a framework where students tested advanced algorithms.

Ten MTechs, DD and MS thesis – highly trained LTE engineers.

Extra slides

Receive data flow



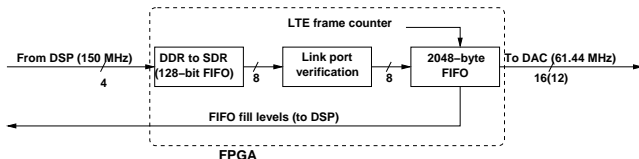
Receive baseband filters select exact 20 MHz channel

- ▶ Otherwise adjacent channel interference aliases into desired channel.
- ▶ ADC samples the receive signal at 30.72 MHz.

DSP-2 and DSP-3 perform complete receive processing except turbo decoder.

▶ Back

Role of FPGA – glue logic

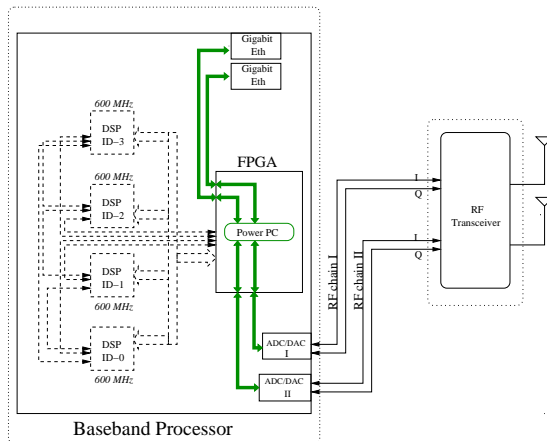


FPGA glues DSP and DAC together by performing following tasks

- ▶ Flow control using FIFO buffer to match data rates.
- ▶ Validate CRC.

▶ Back

Data flow for cloud radio

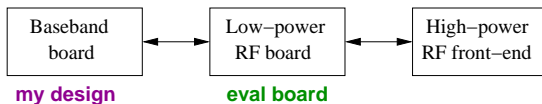


Here IFFT output is send from the computing cloud

- ▶ Required link throughput from cloud to board = $30.72 \times 24 = 737.28$ Mbps.

Require 2 GigE links for 2×2 spatial multiplexing MIMO.

Board design



High-power RF – architected by me with help from a consultant

- ▶ Developed by the consultant.

Power supply requirements

DSP

- ▶ Digital - 1.2 V, 1.6 V, 2.5 V.

FPGA

- ▶ Digital - 1 V, 2.5 V, 3.3 V

Gigabit Ethernet

- ▶ Digital - 1.8 V, 2.5 V, Analog - 1.8 V, 2.5 V

ADC/DAC

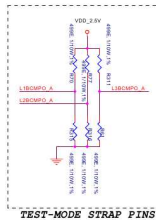
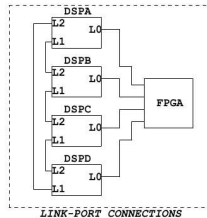
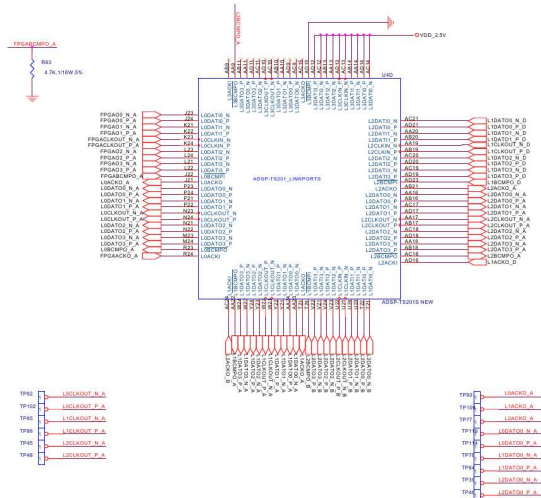
- ▶ Digital 3.3 V, Analog 3.3 V

Different supply rails

- ▶ Digital 1.2 V, 1.6 V, 1.8 V, 2.5 V, 3.3 V
- ▶ Analog - 1.8 V, 2.5 V, 3.3 V

Design the power supplies

Schematics entry – snapshot



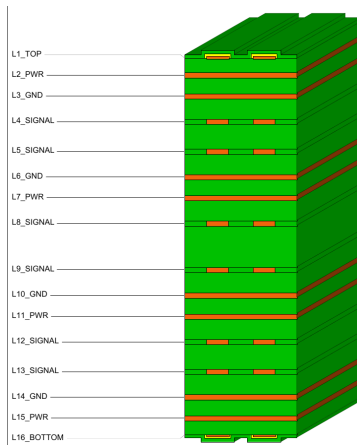
Baseband-SDR-4G-Wireless		Drawn By: Rohit Budhiraja	
File			
DSPA: LINK PORTS			
Size	Document Number		Rev

Stackup design

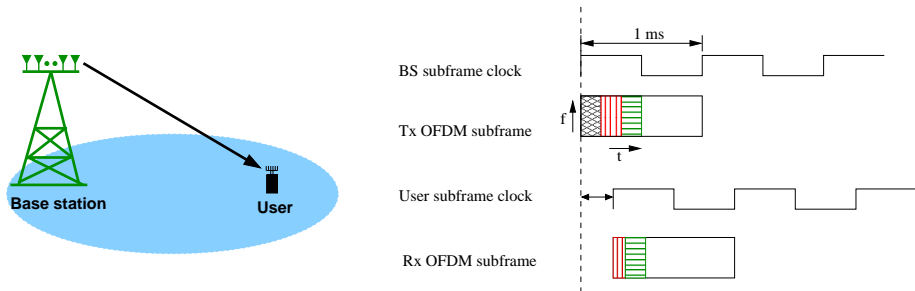
Number/distribution of layers.

Crucial for signal integrity and impedance design.

Each inter-IC link is simulated to evaluate signal integrity.



Downlink synchronization by user

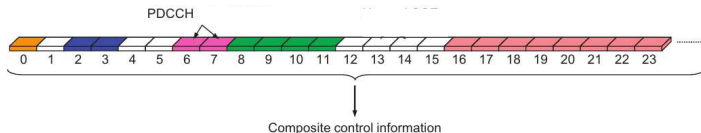


User first acquires symbol and subframe boundaries

- ▶ Symbol boundary and fractional frequency offset using CP correlation.
- ▶ Subframe boundary and integer frequency offset using synch. signals

▶ Back

Blind decoding of control information

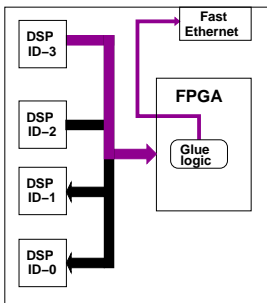


Blind control information decoding by user

- ▶ User need not be necessarily scheduled in a subframe.
- ▶ Needs to blindly scan control region for its control channel (PDCCH).

▶ Back

Evaluation of DSP-Ethernet link



No.	Time	Source	Destination	Protocol	Length
1	0.000000	192.168.0.1	192.168.0.2	TCP	60
2	0.000000	192.168.0.1	192.168.0.2	TCP	60
3	0.000000	192.168.0.1	192.168.0.2	TCP	60
4	0.000000	192.168.0.1	192.168.0.2	TCP	60
5	0.000000	192.168.0.1	192.168.0.2	TCP	60
6	0.000000	192.168.0.1	192.168.0.2	TCP	60
7	0.000000	192.168.0.1	192.168.0.2	TCP	60
8	0.000000	192.168.0.1	192.168.0.2	TCP	60
9	0.000000	192.168.0.1	192.168.0.2	TCP	60
10	0.000000	192.168.0.1	192.168.0.2	TCP	60

Wireshark

Packet stored in DSP memory is sent fixed number of times to PC.

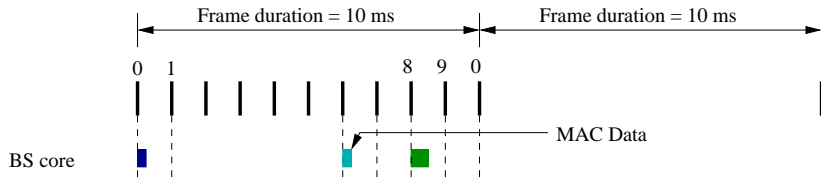
- ▶ Wireshark used to capture packets in PC.

Bit-twist used to send packets from PC to board.

Problem of spurious interrupt generation by Ethernet IC.

Testing starts with writing driver code for accessing Ethernet.

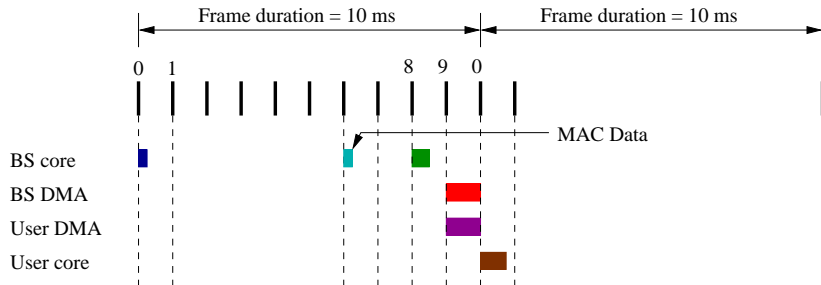
LTE timings and integrated MAC-PHY processing



$t = 0$ ms: transmit PHY TICK to MAC.

$t = 1$ to 8 ms: wait for data from MAC layer.

LTE timings and integrated MAC-PHY processing



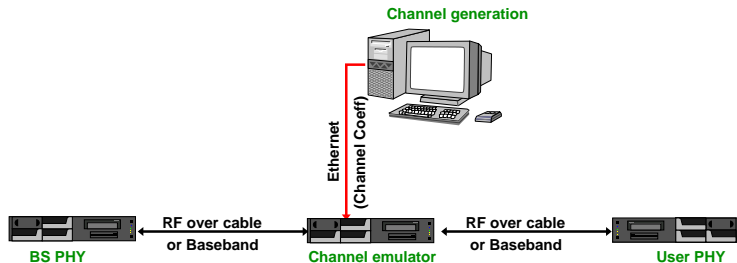
$t = 8$ ms: start processing the MAC data.

$t = 9$ ms: transmit the PHY subframe.

APIs need to be developed for MAC-PHY interaction.

▶ Back

Channel emulator



Latency of $2.4\mu\text{secs}$, which is less than normal cyclic prefix of $4.7\mu\text{secs}$.

Supports 2×2 , 2×1 , 1×2 and 1×1 MIMO modes.

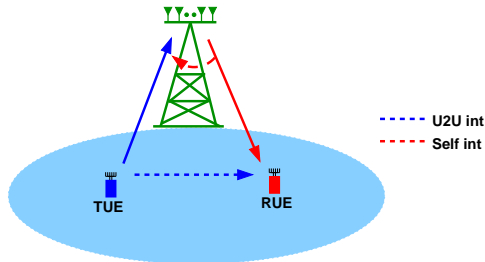
Can emulate any channel up to 72 taps.

Hardware was also used to build WiMAX base station, multi-user emulator.

Future research

In-band full-duplex cellular networks.

- ▶ Network analysis with new sources of interference.
- ▶ Use of multiple antennas.



Verification of network analysis by building testbeds.

Future research

Cross layer design between digital baseband and analog RF.

- ▶ Hardware impairments for mm-wave and massive MIMO systems.
- ▶ Examine effect of low precision ADC on mm-wave systems.
- ▶ Transceiver chain calibration for TDD massive MIMO.
- ▶ Design hybrid digital-analog beamforming.

Build prototypes and technology demonstrators.