CHAPTER III POWER BIPOLAR JUNCTION TRANSISTOR (BJT)

3.1 INTRODUCTION

Switching time and switching losses are primary concerns in high power applications. These two factors can significantly influence the frequency of operation and the efficiency of the circuit. Ideally, a high power switch should be able to turn-on and turn-off controllably and with minimum switching loss. The Bipolar junction transistor is an important power semiconductor device used as a switch in a wide variety of applications. The switching speed of a BJT is often limited by the excess minority charge storage in the base and collector regions of the transistor during the saturation state. The conventional methods for improving the switching frequency by reducing the lifetime of the lightly doped collector region through incorporation of impurities such as Au, Pt or by introducing radiation-induced defects have been found unsuitable for high voltage devices due to increased leakage, soft breakdown and high 'ON' state voltage [27]. Among the techniques proposed to overcome these problems, use of universal contact (UC) [2, 14] is particularly promising. The present work looks in detail at the various aspects arising out of incorporation of UC in BJTs. The UC is incorporated in the transistor by creating additional diffused regions in an otherwise conventional transistor. These diffused regions influence the minority carrier distribution, nature of minority current flow and also some other parameter such as V_{CE(sat)}. To study these phenomena, an analytical model is developed and is utilized to understand the effect of universal contact on reverse recovery, $V_{CE(sat)}$ and other related issues.

3.2 REVERSE RECOVERY OF POWER BJT

Fig. 3.1 shows a schematic of a conventional bipolar junction transistor (BJT), henceforth referred as structure S-I. In the ON state, large storage of minority electrons and holes takes place in base and collector regions respectively. These minority charges must be removed during the turn-off process to restore the device to its blocking state. To speed up the reverse recovery, a reverse bias to the base-emitter junction is generally applied to enhance the turn-off process.



Fig. 3.1 Conventional bipolar junction transistor (S-I) showing single emitter finger between two base fingers

Fig 3.2 shows a typical base and collector current reverse recovery waveform of the transistor. These were obtained using the Silvaco simulation package [15]. The 2D simulations are based on drift-diffusion formalism and take into account the concentration dependent SRH recombination, concentration and field dependent mobility,

band gap narrowing and Auger effects. To put off the transistor, reverse bias is applied at the instant t_0 . The base current immediately changes to reverse current, J_{BR} with a magnitude depending upon the supply voltage and series resistance. The constant collector current continues flowing in the same direction till the time t_1 . After t_1 , collector current starts decreasing. The constant collector current phase and the 90% of the fall time are defined as the total reverse recovery time (τ_{rr}).



The excess electron and hole concentration profiles at 2 μ s, 4 μ s and at 6 μ s in the different phases of the reverse recovery waveform are shown in Fig. 3.3 [28]. As seen



Fig. 3.3 Carrier concentration during reverse recovery in hard switching

The potentials at these different phases of reverse recovery time are also shown in Fig. 3.4. As seen from the Fig. 3.4, the voltage drop at 2 μ s is constant through out the device and is less than 0.5V. At 4 μ s, the voltage has risen to 1V after the depletion

region has formed near the base-collector region. At 6 μ s the voltage has risen to 10V and there is still excess charge left out inside the device. This remaining charge give rise to long fall time tail observed in high voltage devices.



Fig. 3.4 Potential drop in reverse recovery during hard switching

The reverse recovery time (τ_{rr}) of the transistor is intimately related to the effective minority carrier lifetime (τ_{eff}) in the device defined as

$$\boldsymbol{t}_{eff} = \frac{Q}{I_B} \tag{3.1}$$

Where Q is the total minority charge stored in emitter, base and collector regions and I_B is the base terminal current. As an example Fig. 3.5 shows a comparison of reverse recovery time for a BJT of breakdown voltage >1000 Volts with the effective minority carrier lifetime obtained using 2D numerical simulations of the transistor.



Fig. 3.5 A comparison of effective lifetime with reverse recovery time of BJT of >1000 V

It can be seen from Fig. 3.5 that the effective lifetime tracks the reverse recovery time quite well so that it can be used as a simple and easy to model parameter for study.

3.3 ANALYTICAL MODEL - EFFECTIVE LIFETIME

The effective lifetime can be related to other device parameters by noting that in the ON state, the transistor is in saturation so that both the base-emitter and base-collector junctions are forward biased. As a result, minority charges are stored in the emitter (Q_{hE}), base (Q_{eB}) and collector (Q_{hC}) regions so that Eq. (3.1) can be re-written as

$$\boldsymbol{t}_{eff} = \frac{Q_{hC}}{I_B} \left(1 + \frac{Q_{hE}}{Q_{hC}} + \frac{Q_{eB}}{Q_{hC}} \right)$$
(3.2)

Since the doping in the emitter region is much higher as compared to doping in the collector region, $Q_{hE} \ll Q_{hC}$, so that Eq. (3.2) may be simplified to

$$\boldsymbol{t}_{eff} = \frac{Q_{hC}}{I_B} (1 + \frac{Q_{eB}}{Q_{hC}}) \tag{3.3}$$

If I_{hC} is the hole current injected into the collector, then

$$Q_{hc} = \mathbf{t}_0 \times I_{hC} \tag{3.4}$$

Where τ_0 is the hole lifetime in the collector region. This allows Eq. (3.3) to be expressed as

$$t_{eff} = t_0 \frac{I_{hC}}{I_B} (1 + \frac{Q_{eB}}{Q_{hC}})$$
 (3.5)

Since the doping in the base is often much higher than that in the collector and base width is also much smaller than collector thickness, it can be assumed that $Q_{eB} \ll Q_{hC}$, so that

$$\boldsymbol{t}_{eff} = \boldsymbol{t}_0 \frac{\boldsymbol{I}_{hC}}{\boldsymbol{I}_B} \tag{3.6}$$

Equation (3.6) indicates that there are two ways of decreasing the effective lifetime. One is by reducing the bulk lifetime τ_0 , by introducing the life killing elements Au, Pt etc and the other is by reducing the fraction $(\frac{I_{hC}}{I_B})$ of current that results from recombination in the collector region to base terminal current. Eq. (3.6) can be cast into an alternative form by noting that the total base current I_B can be expressed as sum of three components; hole current injected into the emitter, hole recombination current in base region and hole current injected into the collector. For transistors with moderate or high current gain, the component of current due to injection of holes into the emitter is much smaller than the other two components in saturation state so that, $I_B \approx I_{hB} + I_{hC}$.

This allows Eq. (3.6) to be re-written as

$$\boldsymbol{t}_{eff} \cong \boldsymbol{t}_{0} \frac{1}{\left(1 + \frac{I_{hB}}{I_{hC}}\right)}$$
(3.7)

Eq. (3.7) can be re-written in a more instructive form as

$$\frac{1}{\boldsymbol{t}_{eff}} \cong \frac{1}{\boldsymbol{t}_0} + \frac{1}{\boldsymbol{t}_{hB}}$$
(3.8)

Where $t_{hB} = t_0 \left(\frac{I_{hC}}{I_{hB}} \right)$. Eq. (3.8) shows that effective lifetime can also be decreased

by reducing the time constant τ_{hB} by increasing the hole recombination current into the base relative to hole current injected into the collector. The hole current in the base can be viewed as consisting of two components; one due to recombination in the intrinsic base region (I_{hBi}) and the other due to recombination with electrons injected by the collector into the extrinsic base region (I_{hBx}). This allows the time constant τ_{hB} to be decomposed into two components:

$$\frac{1}{t_{hB}} \cong \frac{1}{t_{hBi}} + \frac{1}{t_{hBx}}$$
(3.9)

Where $\tau_{hBi} = t_0 \frac{I_{hC}}{I_{hBi}}$ is the lifetime in the intrinsic base and $\tau_{hBx} = t_0 \frac{I_{hC}}{I_{hBx}}$ is the

lifetime in the extrinsic base region.

The base current component I_{hBx} is normally small because of the small electron recombination velocity of the p⁺p base ohmic contact so that time constant τ_{hBx} is large. However, if the p⁺p base contact is replaced by the n⁺p⁺ universal contact as shown inside the base of the BJT of Fig. 3.6, henceforth called structure S-II, the electron current injected into the extrinsic base is expected to increase considerably resulting in sharp decrease in τ_{hBx} and the overall effective recombination lifetime.



Fig. 3.6 Bipolar junction transistor (S-II) including single emitter finger and two base fingers with universal contact

This method of reduction in effective lifetime is similar to the improvement in reverse recovery obtained by connecting a Schottky diode externally between base and collector. The use of Schottky diode with lower turn-on voltage allows base current to be diverted from collector region of the transistor where recombination lifetime is high to the Schottky diode which has zero effective minority carrier lifetime. In the present approach also, the base current is diverted from collector region to extrinsic base region where effective recombination lifetime is low due to presence of universal contact. Although the principle is essentially same, the present approach has the benefit of being applicable to high voltages also and also promises to have lower silicon area. The discussion so far has brought about the importance of low value of the time

constant τ_{hBx} or equivalently the ratio $\frac{I_{hC}}{I_{hBx}}$ for improving the effective lifetime. We

next discuss the important factors that impact the ratio of hole current injected into the collector and the electron current injected into the extrinsic base region.

3.4 ANALYTICAL MODEL - DEPENDENCE OF EFFECTIVE LIFETIME ON DEVICE PARAMETERS

Fig. 3.7 shows a 1D view of the device in the extrinsic base in the region where n^+ diffusion in p-diffused base as part of universal contact has been made.



Fig. 3.7 A one-dimensional view of the transistor incorporating universal contact at A-A' of Fig. 3.6.

The x_{j1} , x_{j2} and x_{j3} are the metallurgical junctions in front n^+p "universal contact", pv junction and back vn^+ contact. The x_1 and x_2 are the depletion edges of n^+p and pv junctions inside the p diffused region. Analogous to PIN [29] diode, the collector voltage (V_{BC}) in saturation can be expressed as the sum of three components as follows:

$$V_{BC} = V_{BC1} + V_{BC2} + V_{BC3}$$
(3.10)

Where V_{BC1} is the voltage drop at x_{j2} , V_{BC2} is the voltage drop in the collector region in saturation and V_{BC3} is the voltage drop at x_{j3} .

The hole current, I_{hBx} , which is identical to the electron current injected by the collector into the base, can be expressed

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC1}}{kT}\right)}{Q_p} V(A_{BC} - A_E)$$
(3.11)

Where A_{BC} is the base-collector area, and A_E is the emitter area, $V = \frac{A_{N^+}}{(A_{BC} - A_E)}$,

is the fraction of extrinsic base area occupied by n^+ part of the universal contact and A_N^+ , is the area of n^+ in the universal contact.

Defining a factor $\eta_{\rm B} = \frac{V_{BC}}{V_{BC1}}$, equation (3.11) may be written as

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC}}{\mathbf{h}_B kT}\right)}{Q_p} \mathbf{V}(A_{BC} - A_E)$$
(3.12)

For simplicity, we assume that when junction is forward biased $x_2 = x_{j2}$ and low level injection conditions prevail so that $Q_p = q \int_{x_1}^{x_{j2}} N_a(x) dx$. To avoid reach-through prior to onset of breakdown, we require that at breakdown $(x_{j2} - x_1) > 0$. Taking E_C as the

critical field, we obtain the condition

$$\frac{q}{\mathbf{e}_{s}}\int_{x_{1}}^{x_{p}}N_{a}dx > E_{c}$$
or $Q_{p} > \mathbf{e}_{s}E_{c}$
(3.13)

Defining $f_B = \frac{Q_p}{\boldsymbol{e}_S E_C}$, allows Eq. (3.12) to be re-written as

$$I_{hBx} = \frac{q^2 n_i^2 D_n \exp\left(\frac{qV_{BC}}{\mathbf{h}_B kT}\right)}{f_B \mathbf{e}_s E_C} \mathbf{V}(A_{BC} - A_E)$$
(3.14)

The factor f_B represents a safety factor in the sense that for $f_B > 1$, the charge, Q_p under the universal contact is large enough to prevent onset of reach-through prior to onset of avalanche breakdown. On the other hand if $f_B < 1$, then the reverse blocking voltage would be determined primarily by the occurrence of reach-through.

The minority carrier current $I_{hC}\xspace$ can be modeled as recombination current in the collector region and written as

$$I_{hC} = qn_i \; \frac{W_C}{t_0} \exp\left(\frac{qV_{BC}}{h_C kT}\right) \; A_{BC}$$
(3.15)

Where $\eta_{\rm C} = \frac{V_{BC2}}{V_{BC}}$ is the ideality factor of the recombination current in the

collector region. The ratio I_{hBx}/I_{hC} can now be obtained using Eq. (3.14) and Eq. (3.15) as

$$\frac{I_{hBx}}{I_{hC}} = q n_i D_n \frac{\boldsymbol{t}_0}{W_C} \frac{\exp\left(\frac{q V_{BC}}{kT} \left(\frac{1}{\boldsymbol{h}_B} - \frac{1}{\boldsymbol{h}_C}\right)\right)}{f_B \boldsymbol{e}_s E_C} \boldsymbol{V} \frac{(A_{BC} - A_E)}{A_{BC}}$$
(3.16)

The total base current J_B may be written in terms of its ideality factor n as

$$J_{B} = J_{O} \exp\left(\frac{qV_{BC}}{nkT}\right)$$
(3.17)

Equation (3.17) can be used to re-write Eq (3.16) as

$$\frac{I_{hBx}}{I_{hC}} = C_B \frac{t_0}{W_C} \frac{J_B^{a_{BC}}}{f_B}$$
(3.18)

Where $\boldsymbol{a}_{BC} = n \times \frac{\boldsymbol{h}_{C} - \boldsymbol{h}_{B}}{\boldsymbol{h}_{C} \boldsymbol{h}_{B}}$ and $C_{B} = \frac{q n_{i} D_{n}}{\boldsymbol{e}_{s} E_{C} J_{0}^{\boldsymbol{a}_{BC}}} V \frac{(A_{BC} - A_{E})}{A_{BC}}$

Substitution of Eq. (3.18) and corresponding value of $\frac{I_{hC}}{I_{hBi}}$ in Eq. (3.7), we obtain

$$\frac{1}{\boldsymbol{t}_{eff}} \cong \frac{1}{\boldsymbol{t}_o} + \frac{1}{\boldsymbol{t}_{hBi}} + \frac{1}{\boldsymbol{t}_{hBx}}$$
(3.19)

Where
$$\boldsymbol{t}_{hBx}^{-1} = C_B \frac{J_B^{a_{BC}}}{f_B W_C}$$

Eq. (3.19) can be used to explain several important features regarding the effective minority carrier lifetime and therefore the switching speed of the transistors with universal contact. For example Eq. (3.19) shows that the effective lifetime will decrease with increase in base or collector current density. The reason for this is due to the different ideality factors of the current injected into the collector and extrinsic base region. The minority hole current in the collector region increases as $exp(qV_{BC}/2kT)$ due to high level injection in the collector region, while the current injected into the base increases $exp(qV_{BC}/kT)$ due to low level injection condition, causing the ratio I_{hBx}/I_{hC} to increase with increase in bias or with increase in current density. Eq. (3.19) also indicates that the effective lifetime will increase as breakdown voltage increases. The reason for this is that increase in the breakdown requires increase of the thickness W_C of the collector region, which decreases the ratio of I_{hBx}/I_{hC} . Eq. (3.19) also shows that a decrease in safety factor f_B will improve I_{hBx}/I_{hC} . In fact, f_B may be made less than unity indicating onset of reach-through prior to avalanche breakdown. This illustrates a new mechanism whereby the reverse blocking characteristics can be traded with the switching characteristics.

Along with reverse recovery time and breakdown voltage, the collector-emitter voltage in ON state is another very important transistor characteristics. The insertion of universal contact in the extrinsic base region is expected to have influence on this parameter. A simple analytical model is described in the next section.

3.5 ANALYSIS OF 'ON' STATE-VOLTAGE

The collector-emitter voltage in the ON state can be expressed as

$$V_{CE(sat)} = V_{CE(sat)}^{\text{intrinsic}} + I_C \left(R_C + R_E \right)$$
(3.20)

Where the first term represents the intrinsic collector-emitter voltage and the second term represents the voltage drop in the parasitic collector resistance R_C and the emitter resistance R_E . A model for the first term is developed first, followed by a model for the second term.

An expression for intrinsic collector-emitter voltage can be easily obtained from Ebers-Moll [8] model:

$$V_{CE(sat)}^{\text{int}} = V_T \ln \frac{\frac{1}{\boldsymbol{a}_R} + \frac{I_C}{I_B} \left(\frac{1}{\boldsymbol{b}_R}\right)}{1 - \frac{I_C}{I_B} \left(\frac{1}{\boldsymbol{b}_F}\right)}$$
(3.21)

Where β_F and β_R are current gains in forward and reverse active modes respectively. I_C/I_B is the forced β in saturation. The insertion of universal contact in the

extrinsic base region leaves the forward current gain, β_F unchanged but reduces the reverse current gain, β_R . The change in reverse current gain β_R can be explained by noting that

$$\boldsymbol{b}_{R} = \frac{I_{E}}{I_{B}} = \frac{I_{E}}{I_{hC}} \frac{I_{hC}}{I_{B}}$$
(3.22)

Defining injection efficiency (γ_C) of the collector-base junction as

$$g_{c} = \frac{J_{E}}{J_{hC} + J_{E}}$$
(3.23)

allows Eq. (3.22) to be re-written as

$$\boldsymbol{b}_{R} = \frac{A_{E}}{A_{BC}} \frac{1}{\boldsymbol{g}_{C}^{-1} - 1} \frac{I_{hC}}{I_{B}}$$
(3.24)

Since the first two factors are the same in the normal and modified transistor, Eq. (3.24) shows that the change in β_R is directly related to the ratio $\frac{I_{hC}}{I_B}$. This means that

as the ratio $\frac{I_{hC}}{I_B}$ decreases due to the incorporation of "universal contact", β_R will also be

reduced leading to an increase in collector-emitter voltage in saturation. However, due to the logarithmic dependence of the voltage on current gain, the increase in voltage is expected to be small.

In the second term of Eq. (3.20), the contribution of the emitter resistance on the ON state voltage would remain unchanged as a result of insertion of universal contact

because the emitter resistance is unaffected. Similarly, in the absence of conductivity modulation in the collector region, the collector resistance would also remain unchanged. This would be true for transistors designed for low voltage operation where high-level injection condition in the collector may not occur. However, for high voltage transistors, high level injection does occur and insertion of universal contact by altering current distribution is expected to result in a modification of collector resistance.

As long as high-level injection conditions prevail in the entire collector region, the collector resistance and the voltage drop across it remain small due to conductivity modulation. However, as collector current density (and therefore base current density for a constant I_C / I_B ratio) increases, the region where conductivity modulation occurs begins to shrink leaving behind a portion of high resistance collector layer [30]. The voltage drop across this neutral collector region result in a sharp increase in collector-emitter voltage. The voltage drop in un-modulated part of the collector region is given by

$$V_U = \frac{J_C \left(W_C - W_M\right)}{q \mathbf{m}_I N_D} \tag{3.25}$$

The modulated portion of the collector region W_M, can be expressed as

$$W_M = \frac{2qD_n p(0)}{J_C}$$
(3.26)

Since the hole density, p (0), at the collector-base junction is directly proportional to recombination current in collector region, J_{hC} , Eq. (26) can be written as

$$W_M = a \frac{I_{hC}}{I_C} \tag{3.27}$$

Where 'a' is a constant. Use of Eq. (3.26) allows Eq. (3.25) to be expressed as

$$V_U \propto \frac{J_C}{N_D} \left[W_C - a \frac{I_B}{I_C} \times \frac{I_{hC}}{I_B} \right]$$
 (3.28)

Eq. (3.28) is valid only after the un-modulated region of collector begins to form. This would occur when

$$\frac{I_{hC}}{I_B} < \frac{W_C}{a I_B / I_C} \tag{3.29}$$

Since the incorporation of universal contact results in a decrease in fraction of hole current injected into the collector, the sharp increase in collector-emitter voltage is expected to occur at lesser collector current density as compared to the conventional transistor.

The analytical models developed in this section provide insight into important factors affecting different characteristics of the transistor. The next section describes an elaboration of these results obtained using 2D numerical simulation of the transistors.

3.6 SIMULATION RESULTS

To study the effect of incorporation of "universal contact" on transistor's characteristics, 2D numerical simulation were carried out. The simulations are based on

drift-diffusion formalism and take into account concentration dependent SRH recombination, concentration and field dependent mobility, band gap narrowing and Auger effect. A transistor with inter-digitated base–emitter geometry was chosen for simulations. This configuration has large extrinsic base region where the universal contact could easily be incorporated. For simulation purpose, only half of an emitter finger and a single base finger as shown in Fig. 3.8 were taken. The structure of conventional transistor S-I is same as structure of transistor S-II shown in Fig. 3.8 except that in the former, there is no universal contact in the extrinsic base region. Two different kinds of BJT devices, one with relatively low BV_{CBO} of ~150 Volts and another with BV_{CBO} exceeding 1000 Volts were chosen for study.



Fig. 3.8 Transistor structure (S-II) consisting of half of emitter finger and single base finger

The description of the low voltage transistor including surface and bulk concentration, junction depths etc is given in Table 3.1. Transistor geometry with half emitter finger width of 50 mm and a base finger width of 80 mm was taken.

Table 3.1- Details of parameters of simulated low voltage transistor

Device	Base Resistivity/ Doping and Epi- thickness	p diffusion	p ⁺ diffusion	n ⁺ diffusion in emitter & in "universal contact"	Material Lifetime τ_{n0} and τ_{p0}
Low Voltage (100-155 V)	$3.4 - 4.6 \Omega$ -cm, $1.15e15 / \text{cm}^3$, 15 mm nn ⁺ Epitaxial Substrate thickness 280 mm	Xj=5.7 mm, Surface Conc. 2e18, gaussian profile	Xj=1.6 mm, Surface Con 2.0e19	Xj=3.0 mm, Surface Con. 4.0e20, gaussian profile, $n^+:p^+:: 40$ mm:, 40 mm.	2.6 ms

In structure S-II, universal contact was incorporated with a n+/p+ ratio of 1:1. The Gummel plots obtained from simulations were found to be identical for both the transistor structures with a current gain of 80 at a collector current density of 100 A/cm². This is expected because the universal contact in the extrinsic base region will make a difference only when the collector-base junction is forward biased. The switching characteristics of the two structures were simulated by abruptly switching the base voltage in such a way that the forward and initial values of reverse base currents were identical. Reverse recovery time, defined as the sum of storage and 90% of fall times were extracted from the waveforms of the collector/base currents and studied as a

function of collector current density. In these simulations, the ratio of collector to base currents in the ON state was kept at a fixed value of 10. Fig. 3.9 shows a comparison of reverse recovery time for the two structures.



Fig. 3.9 Reverse recovery vs Jc of low voltage transistors S-I and S-II

The reverse recovery time decreases with increase in collector current density in accordance with the predictions of the model developed earlier. The reverse recovery time of BJT S-II is significantly shorter than that of the conventional BJT S-I with an improvement of 62.2% at a collector current density of 1 A/cm² and 47% at about 100 A/cm². Effective minority carrier lifetime was also extracted from the simulations using the definition given in Eq. 3.1. A plot of τ_{eff} versus J_C for the two structures is shown in Fig. 3.10. τ_{eff} for BJT S-II is lower by 73.8% at about 1 A/cm² and 56% at about 100 A/cm².



Fig. 3.10 t_{eff} vs J_C of low voltage transistors S-I and S-II

These results are in general agreement with those of the reverse recovery time. The improvement in effective minority carrier lifetime as a result of introduction of universal contact is due to reduction in time constant τ_{hB} in structure S-II. A plot of current ratio I_{hC}/I_B is shown in Fig. 3.11. It is clear from the figure that the hole current injected into the collector is significantly reduced in structure S-II, thereby implying less minority charge storage and improved reverse recovery.



Fig. 3.11 I_{hC}/I_B ratio vs J_C for low voltage transistors S-I and S-II

As discussed earlier, the improvement in reverse recovery as a result incorporation of universal contact is accompanied with an increase in collector-emitter voltage in the ON state.



Fig. 3.12 $V_{CE(sat)}$ vs J_C at $\frac{I_C}{I_B} = 10$ of low voltage transistors S-I and S-II

Fig. 3.12 shows a comparison of ON state voltage for the two transistor structures for an over drive current ratio of $\frac{I_c}{I_B} = 10$. The ON state voltage of BJT S-II increases by 30-50 mV in comparison to BJT S-I. As discussed earlier, the increase in ON state voltage is due to reduced value of current gain in the reverse active mode. The current gain in the reverse active mode, for the two BJT structures are shown in Fig. 3.13.



Emitter Current Density (A/cm²)



As can be seen, the current gain reduces from approximately 6 to 1.5 as a result of insertion of universal contact. Substitution of these values in Eq. (3.21) predicts a difference of 28mV in the ON state voltage of the two transistors in general agreement with the simulated values.

In order to estimate the impact of insertion of universal contact in transistors with high breakdown voltage, BJT with doping and other parameters suitable for operation of BV_{CB0} larger than 1000 Volts was studied. Transistor structures S-I and S-II with description given in Table 3.2 and geometry with half emitter finger width of 100 µm and base finger width of 150 µm were simulated.

Device	Bulk	p diffusion in	p^+	n ⁺	n ⁺ Back	Material
	Resistivity/	base	diffusion in	Diffusion	diffusion	lifetime
	Doping and		base for p ⁺	in emitter		paramet
	Collector			and for		er τ_{n0} &
	width			"universal		τ_{p0}
				contact"		I.
	100 Ω-cm,	Xj=23 mm,	Xj =1.0	Xj=7.0	Xj=35.0	20 ms
High	$4e13 / cm^3$,	Surface	m m,	m m,	mm	
Voltage	$W_{C} = 150$	Conc.6.7e17	Surface	Surface	Surface	
Transistor	m m,	gaussian	Con. Erfc	Con.	Concentrati	
Structure		profile	4.0e19	4.0e20,	on 6.0e19	
				width 80		
				mm		

 Table 3.2
 Details of parameters of simulated high voltage transistor

Unlike their low voltage counterparts, the I_C - V_{CE} curves for S-I and S-II high voltage transistor show some differences. Fig. 3.14 shows that there are no difference at large values of collector-emitter voltage but the collector currents for the two transistors begin to differ as the voltage gets smaller. The structure S-II is characterized by an early onset of quasi-saturation effect.



Fig. 3.14 $I_C - V_{CE}$ characteristics of high voltage transistor S-I and S-II

This, as explained earlier, is due to reduced hole injection into the collector. Fig. 3.15 shows a comparison of reverse recovery time for the two structures. The current ratio I_C/I_B was maintained at 2 for all the collector current densities.



Fig. 3.15 Reverse recovery (τ_{rr}) vs J_C of high voltage transistors S-I and S-II

The improvement in reverse recovery for S-II is again noticeable though the magnitude is less being about 23.6% at 2 A/cm² and 20 % at 40 A/cm². The improvements in effective minority carrier lifetimes are also similar. Fig. 3.16 shows that τ_{eff} decreases by 30% at about 2 A/cm² and 28% at about 40 A/cm².



Fig. 3.16 **t**_{eff} vs J_C of high voltage transistors S-I and S-II

As for the low voltage transistors, these results can be explained in terms of current ratio I_{hC}/I_B shown in Fig. 3.17.



Fig. 3.17 I_{hC}/I_B ratio vs J_C for high voltage transistors

The ON state voltage at a current ratio of I_C/I_B equal to 2 for transistors S-I and S-II are shown in Fig. 3.18.



Fig. 3.18 Vce(sat) vs Jc for high voltage transistors, S-I and S-II

At low collector current densities, the ON state voltage for S-II is only marginally higher due to reduced reverse current gain. However, as collector current density increases, the ON state voltage begins to increase rapidly at a lower collector current for structure S-II. This result is in agreement with the predictions of the model Eq.(28-29) developed earlier. The reduction in hole injection into the collector results in formation of high resistance collector region at a lower collector current density in structure S-II. Although Eq. (28) is a highly simplified description of the transistor in saturation mode of operation, it fits the simulated data quite well for both the transistor structures. A plot of the ratio V_U/J_C with respect to I_{hC}/I_C in the region where collector-emitter voltage varies rapidly with collector current is shown in Fig. 3.19. The curves for both the transistors are almost identical indicating that as the I_{hC}/I_C ratio decreases, the ratio V_U/J_C also increases.



Fig. 3.19 $V_U/J_C \text{ vs } I_{hC}/I_C$

To summarize, the results of 2D numerical simulations are in general agreement with the predictions of the analytical model and indicate that significant improvement in reverse recovery is possible through incorporation of universal contact in the extrinsic base region. However, this improvement is obtained at the expense of increased ON state voltage especially for transistors designed for high voltage operation at relatively higher collector current densities. Apart from incorporating universal contact in the base, there is also a possibility of fabricating a structure in which a separate diode having universal contact, called Low Loss Diode (LLD), is integrated monolithically [2] along with the transistor in a manner similar to Schottky clamped transistor. This structure (Fig. 3.20), henceforth called S-III, is less efficient in reducing the effective minority carrier lifetime as compared to the structure S-II.





For both the structures, the effective minority carrier lifetime can be described by Eq.(3.8), which is reproduced again as:

$$\frac{1}{t_{eff}} = \frac{1}{t_o} + \frac{1}{t_{hBi}} + \frac{1}{t_{hBx}}$$
(3.30)

To use Eq. 3.30 with transistor structure S-III, the externally connected low loss diode is viewed as an extension of the collector base area since it is electrically connected to it. A comparison of τ_{hBx} for the two structures gives an estimate of the relative efficiencies of the two structures. For structure S-III shown in Fig. 3.20, t_{hBx}^{S-III} can be expressed using Eq. (3.7) as

$$\mathbf{t}_{hBx}^{S-III} = \mathbf{t}_0 \frac{A_{BC} + A_{LLD}}{A_{N^+}} \frac{J_{hC}^{S-III}}{J_{hBx}^{S-III}}$$
(3.31)

Where A_N^+ is the area of n^+ region of the universal contact, which is taken to be the same in both S-II and S-III, A_{BC} , is collector-base area of S-III, also assumed to be the same as that for structures S-I and S-II and A_{LLD} is the area of LLD.

Similarly, for structure S-II

$$\mathbf{t}_{hBx}^{S-II} = \mathbf{t}_0 \frac{A_{BC} J_{hC}}{A_{N^+} J_{hBx}}$$
(3.32)

Using the assumption that the injection efficiency of collector - base junction is the same for both structures, dividing Eq.3. 31 by Eq.3.32 give

$$\frac{t_{hBx}^{S-III}}{t_{hBx}^{S-II}} = \frac{A_{BC} + A_{LLD}}{A_{BC}}$$
(3.33)

Eq. (3.33) shows that $t_{hBx}^{S-III} > t_{hBx}^{S-III}$ because when universal contact is introduced separately as in LLD, an additional region of area A_{LLD} has to be introduced which

besides increasing the electron injection in the external base region increases the hole injection into the collector also. This increases the effective lifetime in S-III.

Fig. 3.21 shows a comparison of reverse recovery waveforms obtained for structures S-II and S-III. The collector-base area of both the transistors was kept identical at 250 μ m x 1 μ m. In S-II, an N⁺ region of area 80 μ m x 1 μ m was introduced in the extrinsic base region.



Fig. 3.21 Collector waveforms for structure S-II and S-III

In S-III, the area of LLD was taken as 190 μ m x 1 μ m with an n⁺ region of area 80 μ m x 1 μ m, which is identical to that in S-II. To verify the above, two structures have been simulated for reverse recovery. The reverse recovery time of S-II is determined to be 33% lower than that of structure S-III. Substitution of area values in Eq. (3.32) shows that the effective lifetime of S-II is about 30.5% smaller than that for the structure S-III.

These results clearly show it is much more advantageous to introduce the universal contact inside the base of a transistor as in S-II rather than in the form of a low loss diode externally connected to it.

3.7 Experimental Results

Transistor structures S-I and S-II with two different breakdown voltages were fabricated and experimentally characterized. Table. 3.1 gives the doping and thickness of low voltage transistors that were fabricated using a four-mask process. The area of collector is $1.6 \times 1.6 \text{ mm}^2$ and base area is $1.4 \times 1.4 \text{ mm}^2$. The emitter has been diffused in finger like structure with area of 0.5606 mm². BJT S-II was also fabricated on the same chip by carrying out n⁺ emitter diffusion in parts of the extrinsic base as well. In structure S-II, n⁺ for making universal contact has been introduced in fine strips with total area of 0.33264 mm² and it covered approximately ¹/₄ fraction of extrinsic base. The I_C-V_{CE} characteristics of both S-I and S-II were identical and are shown in Fig. 3.22.



 $V_{CE}(V)$

Fig.3. 22 I_C -V_{CE} characteristics of experimental low voltage (BV_{CBO} ~ 150 V) transistor

A current gain of 70 and identical breakdown voltages ranging between 100-155V were measured for both S-I and S-II. The reverse recovery measurements were carried out using a resistive load and abrupt switching of the base voltage. The reverse recovery waveforms for S-I and S-II are shown Fig. 3.23(a) & (b) respectively.





(b)

Fig. 3.23 Photograph of measured reverse recovery of low voltage transistors (a) S-I (b) S-II (Hor. Scale 0.2 mJ/Div, Ver. Scale 5 V/Div)

A reverse recovery time of 1 μ s for S-I and 0.44 μ s for S-II were obtained at a collector current of 20 mA. The 56% improvement in reverse recovery time is in fair agreement with simulation results considering the uncertainties due to factors such as collector recombination lifetime, Gummel charge under the extrinsic base etc used in simulation. The reverse recovery time for both S-I and S-II also improved with increase in collector current density. For example, values of reverse recovery of 0.5 μ s at 10 mA and 0.38 μ s at 40 mA were measured for S-II. The reverse recovery for few other collector current values are shown in Table 3.3.

Device I.D	BV _{CBO} & leakage	Lifetime of collector	β	I _C (mA)	Storage Time (µs)		Fall time (µs)		Total Recovery (µs)	
		with emitter open			S-I	S-II	S-I	S-II	S-I	S-II
W—12 (3x4)	BV 100- 150 V, 0.1 μA at 50 V	2.6 µs	70	10 20 30 40	0.84 0.8 0.76 0.72	0.2 0.22 0.2 0.18	0.3 0.2 0.2 0.2	0.3 0.2 0.2 0.2	1.17 1.0 0.96 0.92	0.5 0.44 0.4 0.38

Table 3.3 Measured dc & dynamic characteristics of experimental low voltage transistor

Measurement of V_{CE(sat)} were carried out for different collector currents at a constant $\frac{I_c}{I_B}$ =10. As can be seen from Fig. 3.24, the ON state voltage for S-II is higher

as compared to S-I. As discussed earlier, at low currents, this is due to reduction in reverse current gain in S-II. The gain in reverse active mode was measured to be 8.8 and 1.8 for S-I and S-II respectively. Substitution of these numbers in Eq.(3.21) gives a difference of 28.6 mV in the ON state voltage of the two transistors.



Fig. 3.24 V_{CE}(sat) vs collector current at $\frac{I_c}{I_B} = 10$ of low voltage transistor

In order to measure the impact of universal contact in transistors of high breakdown voltages, devices with the description given in Table 3.2 were fabricated using a five-mask process details of which are given in Chapter IV. The area of collector is 3.4 x 3.4 mm² and that of base is 2.7 x 2.7 mm². The emitter has been diffused in finger like structure with area of 3.14 mm². BJT S-II was also fabricated along side by carrying out n⁺ emitter diffusion in parts of the extrinsic base as well. In structure S-II, n⁺ for making universal contact has been introduced in fine strips with total area of 1.1232 mm² and it covered approximately ¹/₄ fraction of extrinsic base. The I_C-V_{CE} characteristics of structure are shown in Fig.3.25. A current gain ranging between 15-25 and identical breakdown voltages > 1000 were measured for S-I and S-II.





Fig. 3.25I_C-V_{CE} Characteristics of experimental high voltage (BV_{CBO} > 1000 V) transistor

The reverse recovery measurements were carried out using a resistive load and abrupt switching of the base voltage. The reverse recovery waveforms for S-I and S-II are shown Fig.3.26 (a) & (b) respectively.



Fig. 3.26 Photograph of measured reverse recovery of high voltage transistor (a) S-I (b) S-II (Hour. Scale 2 ms/Div, Ver. Scale 5 V/Div)

A reverse recovery time of 10.4 μ s for S-I and 8.4 μ s for S-II were obtained at a forward collector current of 200 mA. The 23% improvement in reverse recovery time is in fair agreement with simulation results. The reverse recovery time for both S-I and S-II also improved with increase in collector current density. The reverse recoveries for few collector current values are shown in Table 3.4.

Table 3.4	Measured dc & dynamic characteristics of experimental hi	<u>gh</u>
	voltage transistor	

Wa fer I.D	BV _{CBO} , Leakage	Life time in Collect	β	I _C ma	Storage Time (µs)		Fall time (µs)		Total Recovery (µs)	
		or			S-I	S-II	S-I	S-II	S-I	S-II
A3 (2x 3)	> 1000 V, 10 µA at 1000 V	20 µs	15-25	100 200 300	12 8.4 6.2	8 6.4 5.2	3 2.0 1.6	4.0 2.0 1.6	15.0 10.4 7.8	12.0 8.4 6.8

Measurement of $V_{CE(sat)}$ were carried out for different collector currents at a constant $\frac{I_C}{I_B}$ = 2. As can be seen from Fig. 3.27, the on-state voltage for S-II is higher as compared to S-I. As discussed earlier, at low currents, this is due to reduction in reverse

current gain in S-II. At high currents, it is due to the quasi-saturation as explained earlier.



Fig. 3.27 V_{CE}(sat) vs collector current at $\frac{I_c}{I_B} = 2$ of high voltage transistor

No measurable difference in breakdown voltage and leakage current was observed in low and high voltage transistors S-I and S-II.

3.8 SUMMARY OF BJT RESULTS

The use of "universal contact" for improving the reverse recovery of power bipolar transistor (BJT) was studied in detail using a combination of analytical model, numerical simulation and experimental work. It is shown that use of universal contact allows redistribution of base current in saturation from collector region where recombination lifetime is high to extrinsic base region where effective recombination lifetime is low. The analytic model also predicts that the effective lifetime is inversely proportional to the current density. It is also shown through analysis that the efficacy of the universal contact in reducing the effective lifetime becomes less as the breakdown voltage of the transistor increases. The improvement in reverse recovery is accompanied by degradation of the ON state voltage. For low voltage, the degradation is solely due to reduction in current gain in reverse active mode while for high voltage transistor, the degradation is characterized by an early onset of quasi-saturation effect.