CHAPTER IV
DEVICE TECHNOLOGY

In this work, we fabricated diodes and transistors, conventional and the ones having universal contact adopting identical processes. The voltage rating of these devices is approximately same as the devices, which have been simulated in previous sections. The material, technology and process flow of the fabricated diodes and transistors is described in following sections.

4.1 RAW MATERIAL

The reverse voltage capability of the diode and transistor is the sole factor for deciding the resistivity and width of the raw material. The current rating depends upon the length of the emitter periphery and can be increased by proper design of fingers, cells or area of the device. To study the universal contact in low (~150) and high voltage (~1000V) devices, the following materials were obtained:

For a 150V devices	nn^+ Epitaxial
	Resistivity 3.4 – 4.6 Ω-cm
	Phosphorous doped Epi thickness 15 μ m
	Substrate (Sb doped), Resistivity 0.015 Ω-cm
	Substrate thickness 310 ± 20 μ m
Supplier	Wacker-Chemitronic GmbH, German

For > 1000V devices	Phosphorous doped bulk FZ grown silicon
	Resistivity 100 Ω-cm
	Initial thickness 350 ± 10 μm
Supplier	Wacker-Chemitronic GmbH, German

4.2 DIODE FABRICATION

The four-mask process was developed for planar low voltage diode. First mask for p^+ window open, second mask for n^+ UC, third mask for contact open and fourth one for aluminum metal patterning. An additional mask for moat etching was required for high voltage diode. All masks were locally designed and developed. The base area is 1.4 x 1.4 mm^2 for planar structure. The actual base area of mesa etched devices is reduced to 1.1 x 1.1 mm^2. The conventional diode (S-I) and diode incorporating universal contact (S-III) has been made in the same wafer as to reduce the material and process variations. The p^+ diffusion was done using boron doped oxide by Chemical Vapor Deposition (CVD)[31] using tri-propyle-borate and tetra-ethyle-orthosilicate (TEOS) by pyrolytic decomposition at 660^oC. It was followed by soak-in, removal of doped oxide and drive-in to obtain the required surface concentration and junction depth. In last step, the n^+ diffusion was done using $POCl_3$ from back and front. This last high temperature step getters the metallic impurities besides introducing the n^+ doping required for universal contact. In high voltage devices, the curved portion of the p diffusion gives rise to high

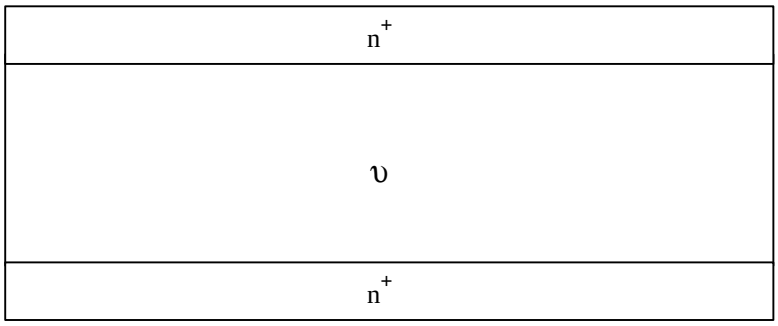
electric field near the surface, which may cause ionic drift. This affects the reliability of the device. To overcome this, the curved portion producing the high surface field is chemically etched. Out of the different technique [32] for lowering the surface electric field, the mesa etching, which is compatible with batch process has been used. To passivate the junction, the mesa has been filled with a special glass, GP-601 from Nippon Electric Glass (NEG). A paste of the glass with Ethyl Cellulose and Butyl Carbitol is made which is then filled in mesa grooves by doctor blading. The glass was fired in oxygen in a suitable glass firing cycle. Al evaporation was done in 3-4 x 10^{-6} mbar range on the front side, patterned and sintered at 450-500^{o}C. The Ti-Au was done on the backside of the wafer. The four-probe setup was used for sheet resistivity measurement. The junction depth was measured using lapping and staining with copper nitrate. The process flow is given as under:

Pre-processing of Epitaxial wafers (3.4 –4.6 Ω-cm) using TCA oxidation, 4 hrs, 1170°C, O_2 1 lpm, TCA 75 ml/m

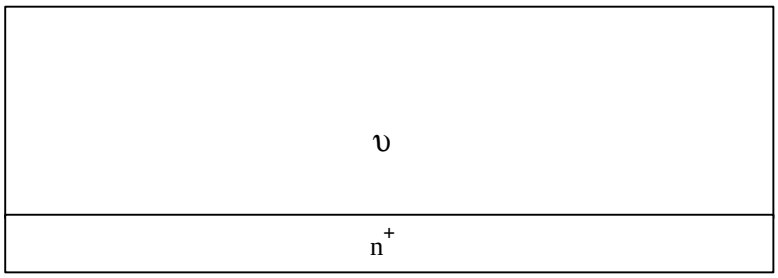
Pre-processing of bulk wafers (100 Ω-cm) to remove point defects and metallic impurities using , $POCl_3$ gettering at 1050°C, 1 hr, Rs. 1.4 -1.6 Ω/sq,
Etching of few μm silicon from both sides and
TCA oxidation, 6hrs 1170°C, O_2 1 lpm, TCA 75 ml/m

↓

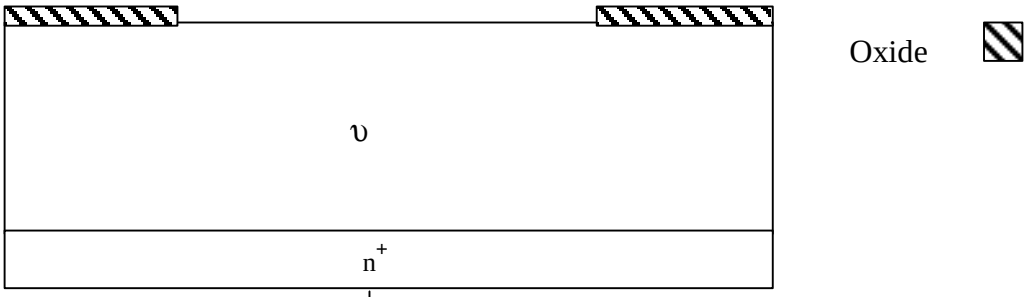
n^+ deposition on both sides of bulk wafer of 100 Ω-cm and 30 hrs drive-in at 1225°C in oxygen and TCA ambient. Rs 5.6 – 18.8 Ω/sq, xj 30-35 μm.



Removal of n^+ from one side, using lapping and polishing

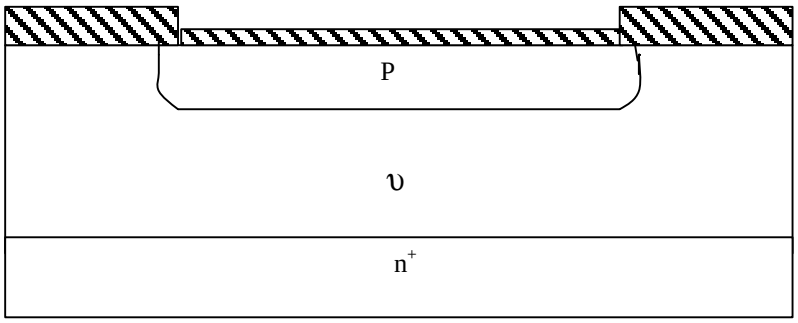


Oxidation, Photolithography for Ist mask for p^+ window open.



Boron deposition and drive-in 1200°C 4 hrs in oxygen & TCA ambient, Rs = 98.0 Ω/sq, xj = 5.44 μm for low voltage diode/transistor.

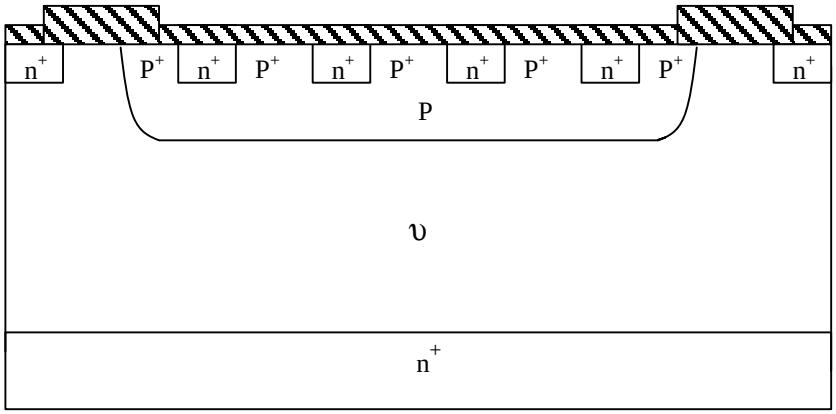
Boron deposition, soak-in and drive-in at 1240°C 28 hrs in oxygen & TCA ambient, Rs = 100 Ω/sq., xj = 23 μm for high voltage diode/transistor



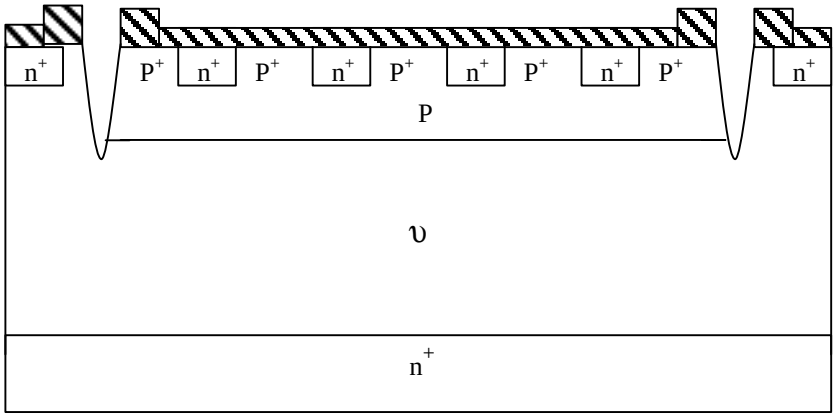
Oxid

Photolithography for IInd mask for n^+ & $POCl_3$ deposition at 1000°C, 25 min, Drive-in at 1100°C, 1 hrs, Rs=1.8 Ω/sq, xj= 3.2 μm in oxygen ambient for Low Voltage diode/transistor

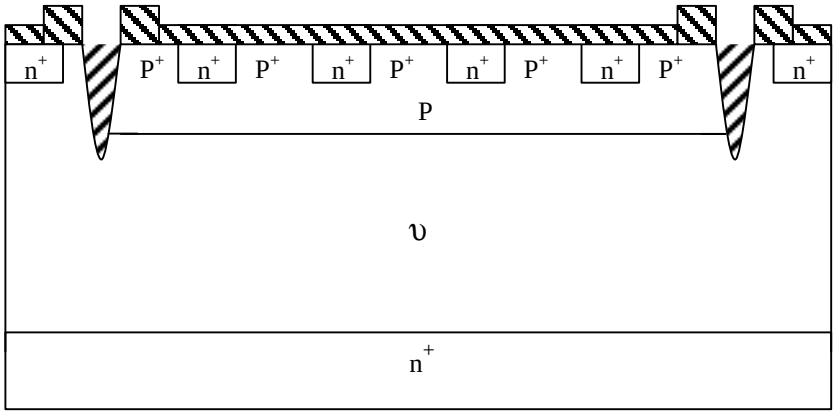
Photolithography for IInd mask for n^+ & $POCl_3$ deposition at 1050°C, ½ hrs. Drive-in at 1100°C, 6 hrs, in oxygen ambient, Rs=5.6 Ω/sq, xj= 7 μm for high voltage diode/ transistor



Moat etching 40-50 μm using 5:3:3::HnO_3:HF:Acetic Acid
Using IIIrd mask



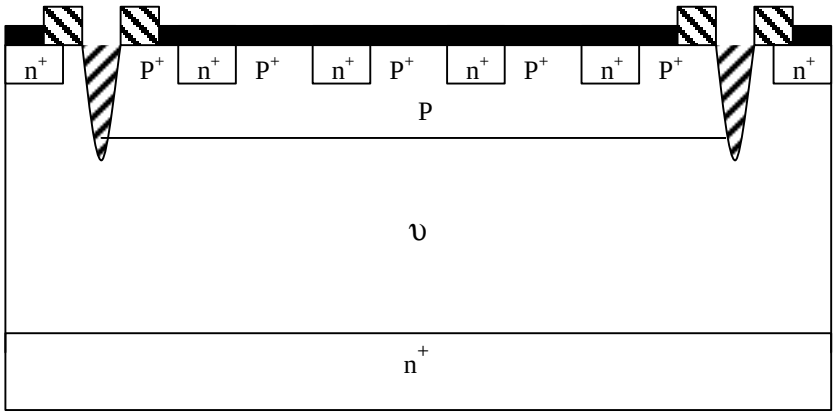
Glass (NEG GP-601) filling using doctor blading and firing the glass according to specified cycle



Oxide

Glass

Front Al metallization and patterning using Vth mask

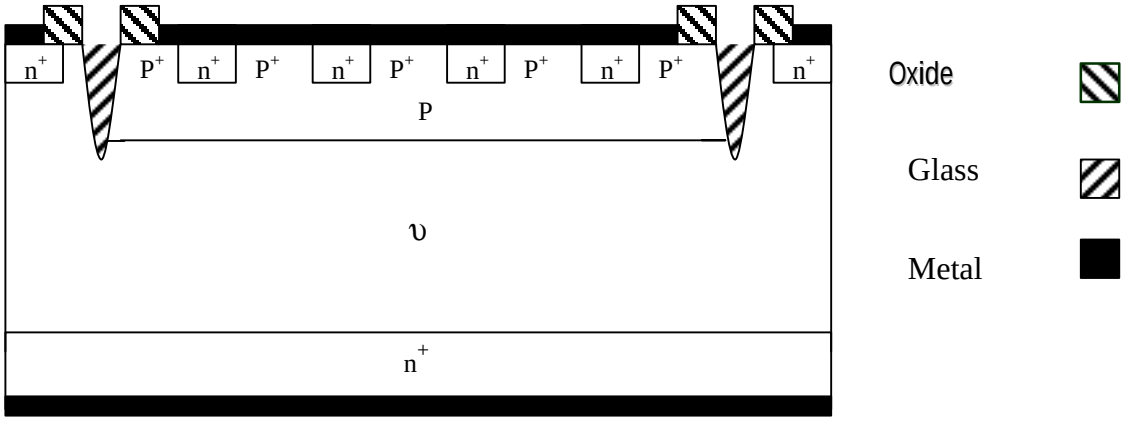


Oxide

Glass

Metal

Back Ti-Au Metallization



The photographs of the finished die of conventional diode and the one having n^+ and p^+ ratio of 1:1, 2:1 and 4:1 for making the universal contact are shown in Fig. 4.1.

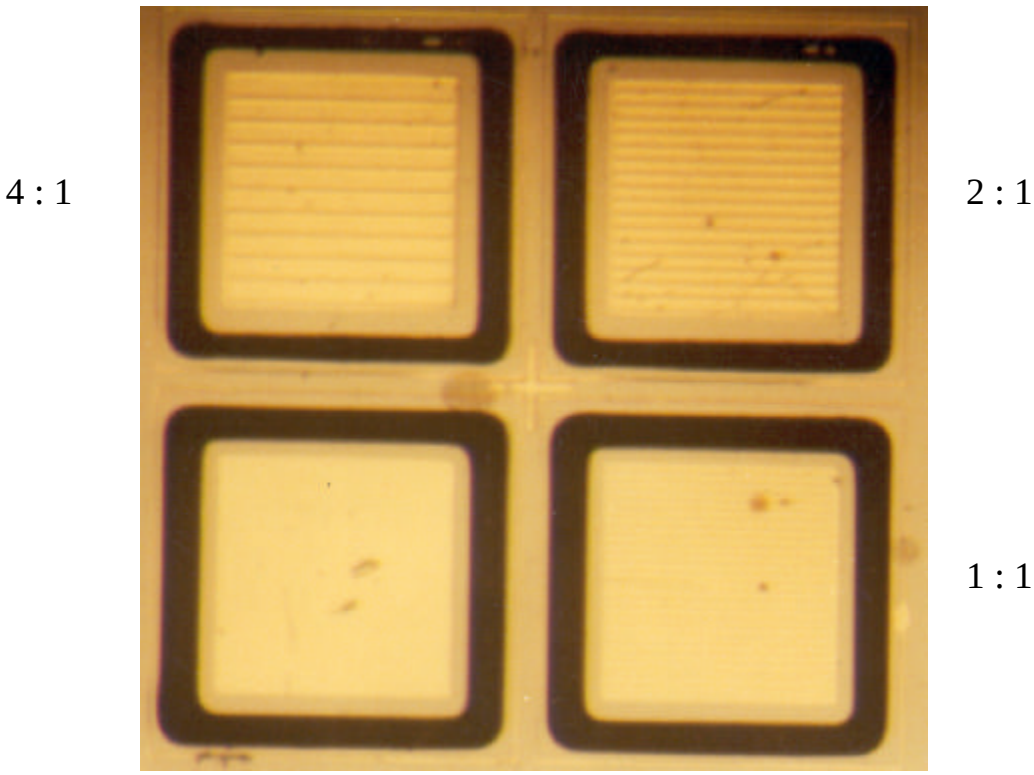


Fig. 4.1 Photograph of conventional (S-I) and modified (S-III) diodes

The high voltage diode structure incorporating universal contact at the end of high resistivity region has also been fabricated. There is about 35 μm n^+ diffused region on right side of a power diode made in bulk silicon. This n^+ diffused region has been etched away and n^+ p^+ contact has been made in its place. This structure in essence becomes equal to the diode structure S-II shown in Fig. 2.3.

4.3 TRANSISTOR FABRICATION

4.3.1 LOW VOLTAGE TRANSISTOR

Similar to diodes, the fabrication of low voltage planar transistor required four masks process. First mask for p^+ window open, second mask for emitter and n^+ UC, third mask for contact open and fourth one for aluminum metal patterning. All masks were locally designed and developed. The base area is 1.4 x 1.4 mm^2 for planar low voltage transistors. The conventional low voltage transistor (S-I) and the transistor incorporating universal contact (S-II) has been made in the same wafer as to reduce the material and process variations. The emitter layout has been designed using inter-digitated emitter-base finger geometry. The emitter finger width is 100 μm and that of base finger is 80 μm. The n^+ p^+ universal contact has been applied with 1:1 ratio in base fingers. However, the device has additional extrinsic base area for metal pad. In this area too, universal contact has been applied. The n^+ diffusion for making the universal contact has been made at the time of emitter diffusion.

The enlarged photograph of the fully processed low voltage planar transistor is shown in Fig. 4.2.

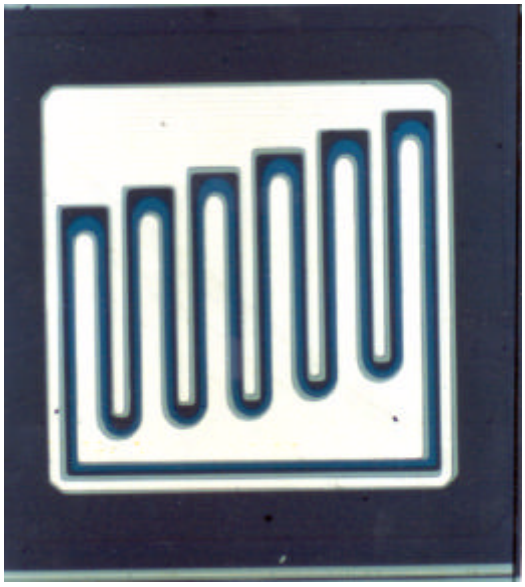


Fig. 4.2 Photograph of the low voltage conventional planar transistor

4.3.2 High Voltage Transistor

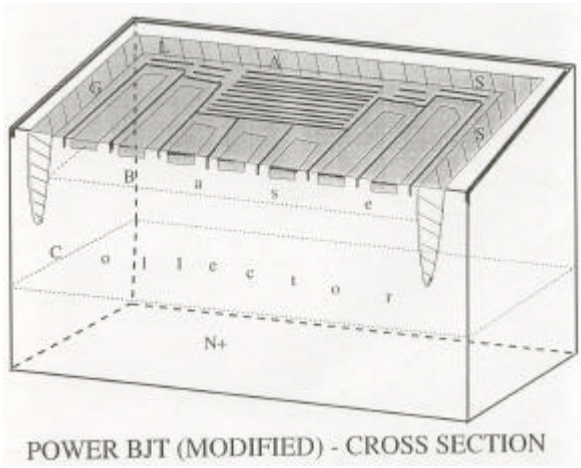
The fabrication of high voltage transistor required five-mask process. First mask for p^+ window open, second mask for emitter and n^+ "universal contact", third mask for contact open, fourth mask for moat etching and fifth mask for aluminum metal patterning. All masks were locally designed and developed. The high voltage transistor is different from its low voltage counterpart. The main concern in high voltage transistor is to reduce the ON state voltage. To operate device at high currents and low ON forward voltage, recourse is usually made to increase the device area. The high voltage transistor

have been fabricated in chip size 3.5 X 3.5 mm^2 die of BV_{CBO} ~ 1500 V and current rating of ~ 5 A. The emitter finger width is 200 μm and base finger width is 150 μm.

The process flow for low and high transistor is similar to the one adopted for low and high voltage diodes respectively. The top views of high voltage transistors S-I and S-II are shown in Fig. 4.3 (a) and (b). 3-D view of S-II is shown in Fig.4.3(c).

(a)

(b)



POWER BJT (MODIFIED) - CROSS SECTION

(c)

Fig. 4.3 (a) Top view of conventional (S-I) transistor, (b) Top view of modified (S-II) transistor, (c) 3-D view of S-II

A photograph of fully processed die of conventional high voltage BJT is shown in Fig. 4.4. The modified transistor S-II has also been made in the same batch. The n^+p^+ universal contact has been introduced in extrinsic base similar to the top view shown in Fig.4.3(b).

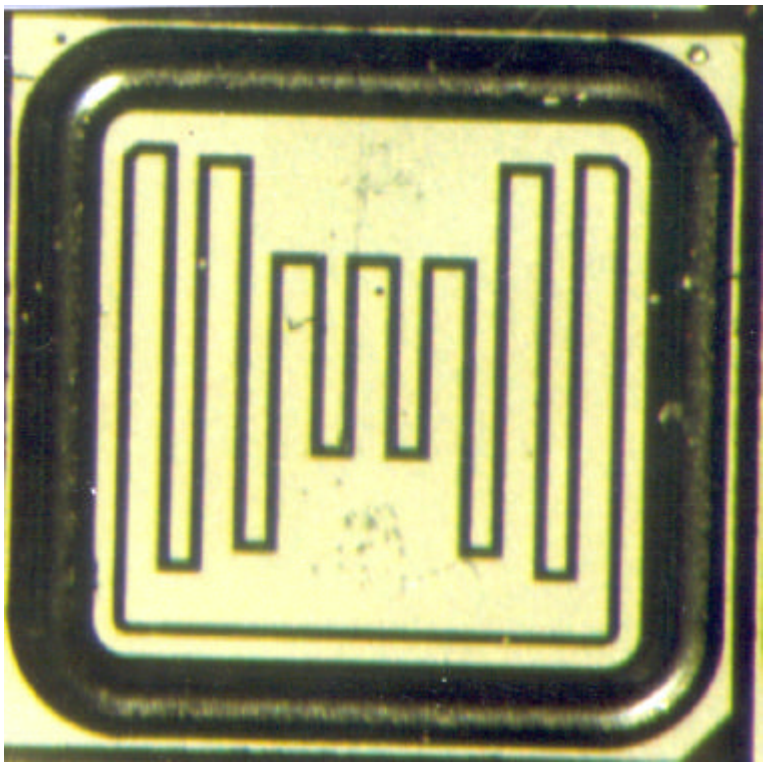


Fig. 4.4 Photograph of the high voltage conventional transistor

4.4 GROWN IN DEFECTS AND YIELD PROBLEMS

The main difficulty faced in the development of these devices was the quality of the raw material. For low voltage diodes and transistors, epitaxial wafers have been used.

The FZ silicon bulk wafers have been used for high voltage devices. The hyper pure quality wafers were procured from a world-renowned manufacturer. The devices made in the raw wafers in the first few runs had large leakage current. There was almost no visible sharp breakdown voltage. The $POCl_3$ gettering [33, 34] was not enough to remove these defects. To find the cause of the low breakdown and large leakage, an investigation of raw and processed wafers was carried out. During preferential etching, large number of tiny defects distributed in swirl pattern were observed in raw wafers. These defects pointed to the presence of silicon point defects either excess self-interstitial or vacancies. The excess interstitial may nucleate at defect sites and act as recombination centers, causing large leakage. The Electron Probe Microanalysis (EPMA) revealed that there were trace amounts of metallic impurities present in the bulk of the wafer.

To remove these metallic impurities, gettering at higher concentration of $POCl_3$ and longer time was carried out. No improvement was observed in leakage current and breakdown. It was found during these gettering experiments that the excessive $POCl_3$ gettering rather spoiled the wafers further. The $POCl_3$ treatment though helpful in removing the metallic impurities, introduces excess silicon interstitial. The CZ or FZ methods of pulling the crystal invariably introduce some impurities and grown-in point defects [35, 36]. The kind and concentration of point defects in silicon wafer depends on its growth conditions. The parameter s defined as growth rate (v) / temperature gradient (G) [37] during crystal growth decides whether it will have excess interstitial or vacancies.

The excess interstitial in the wafer can be removed by treating them at high temperature in chlorine containing ambient. The chlorine introduces excess vacancies at the surface of the wafer [38], which induces diffusion towards the surface of the silicon atoms sitting in silicon precipitates. The silicon precipitates are thus dissolved and removed from the bulk of the wafer by chlorine treatment. Keeping the effects of the chlorine containing ambient and that of the $POCl_3$ in view, a wafer cleaning process was optimized. For creating chlorine ambient, 1-1-1 trichloroethan (TCA) was bubbled through by passing N_2 in it. The process details for 100 Ω-cm bulk wafers are given in the flow chart. The epitaxial wafers were also subjected to mild TCA treatment. The devices with low leakage and high breakdown were ultimately obtained.