

# CHAPTER V

## CONCLUSIONS

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The objectives of this thesis has been to study the reduction of reverse recovery in low and high voltage diodes and bipolar transistors by the incorporation of universal contact and its effects on other device characteristics. The conclusions drawn from the present work are summarized below.

### 5.1 DIODE

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1. The use of  $n^+p^+$  “universal contact” for improving the switching performance of power diodes was examined in detail through modeling of effective minority carrier lifetime ( $\tau_{eff}$ ). It was shown that  $\tau_{eff}$  depends not only on the lifetime in the lightly doped  $v$  region but also on other time constants determined by the fraction of total current that results from the injection of minority currents into  $p^+$  and  $n^+$  region. Using this viewpoint, it is shown that effective minority carrier lifetime and therefore reverse recovery time which is closely related to it, can be reduced by redistributing current away from lightly doped  $v$ -region to  $n^+$  and  $p^+$  regions where effective minority carrier lifetime can be reduced by incorporating universal contact. It was found that the incorporation of

this modification in  $p^+$  improved the effective lifetime of low voltage diodes (100 —200 V) by 68% at  $100 \text{ A/cm}^2$  and for high voltage (1000 V) diode by 39% at about  $50 \text{ A/cm}^2$ . The corresponding improvement in effective lifetime in high voltage diode structure as proposed by Amemiya et al is 43% but this structure compromised the breakdown voltage which is reduced to less than half of the conventional high voltage diode

2. The analytical model developed in this work shows that the effective lifetime decreases with increase in current density and that the advantages of incorporating a universal contact decrease as the breakdown voltage of the diode increases. Due to the large middle region thickness in high voltage diodes, the fraction of current injected into  $p^+$  region is relatively less and the improvement of reverse recovery is also less as compared to low voltage diodes. The reverse recovery time for both low and high voltage diodes was found to decrease with current density. This is due to the difference in voltage dependence of current injected into the  $p^+$  region (ideality factor  $\sim 1$ ) and the middle  $v$  region (ideality factor  $\sim 2$ ). It is also shown that the incorporation of universal contact allows a new tradeoff between the switching speed and the reverse blocking voltage determined by the proximity of universal contact to the lightly doped region of the diode. The predictions of the model were verified through extensive 2-D [4] numerical simulation and fabrication and characterization of low ( $\sim 150 \text{ V}$ ) and high ( $>1000 \text{ V}$ ) voltage diodes.

3. A new diode structure incorporating universal contacts inside both  $n^+$  and  $p^+$  diffused regions has been proposed. It was shown through analytical calculations and 2D numerical simulations that this diode structure results in large reduction in reverse recovery. The improvements in reverse recovery are 60% and 66% at  $0.3 \text{ A/cm}^2$  and  $50 \text{ A/cm}^2$  respectively with respect to the conventional diode structure. It is further shown that the ON state voltage of the proposed structure is smaller than that of the conventional diode structure by 145 mV at about  $50 \text{ A/cm}^2$ . [39]

## 5.2 TRANSISTOR

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4. The use of “universal contact” for improving the reverse recovery of power bipolar transistor (BJT) was studied in detail using a combination of analytical model, numerical simulation and experimental work. The analytical model developed for PIN diodes was extended to model the effects of incorporating universal contact within the extrinsic base of BJTs. It is shown that use of universal contact allows redistribution of base current in saturation from collector region where recombination lifetime is high to extrinsic base region where effective recombination lifetime is low. The analytic model also predicts that the effective lifetime is inversely proportional to the current density. The numerical simulation results show that effective lifetime decreases from 849 ns at  $1 \text{ A/cm}^2$  to

88 ns at about  $110 \text{ A/cm}^2$ . It is also shown through analysis that the efficacy of the universal contact in reducing the effective lifetime becomes less as the breakdown voltage of the transistor increases. There is about 50-70% improvement in reverse recovery in low voltage transistor by incorporating the universal contact. This improvement is only 20-35% in high voltage transistor.

5. The improvement in switching characteristics as a result of incorporation of universal contact is accompanied with an increase in the ON state voltage,  $V_{CE(sat)}$  of transistors. For low voltage device, there is about 30-50 mV increase in  $V_{CE(sat)}$  due to reduction in current gain in reverse active mode in transistors incorporating UC. In high voltage transistor, the increase in  $V_{CE(sat)}$  in transistors with universal contact at high current density is in the order of few volts due to early onset of quasi-saturation effect. These results are verified through 2-D numerical simulation and fabrication and characterization of low voltage ( $BV_{CBO} \sim 150 \text{ V}$ ) and high voltage ( $BV_{CBO} > 1000 \text{ V}$ ) transistors.
6. The usefulness of the universal contact at high voltage ( $BV_{CBO} > 1000 \text{ V}$ ) transistors has been experimentally demonstrated for the first time. An improvement of 23% in reverse recovery was experimentally measured in high voltage BJT [40].

7. It is much more advantageous to introduce the “universal contact” inside the base of a transistor rather than in the form of a low loss diode (LLD) externally connected to it [2,14].

## APPENDIX 'A'

**TABLE 'A'      OPTIMUM DRIFT REGION WIDTH AND DOPING FOR DESIRED BREAKDOWN VOLTAGE**

| Width (mm) | Back Ground Concentration ( $/\text{cm}^3$ ) | Desired Breakdown (V) |              |                   |
|------------|----------------------------------------------|-----------------------|--------------|-------------------|
|            |                                              | Parallel Plane        | Planar (50%) | Mesa Etched (80%) |
| 5          | 9.5e14                                       | 131                   | 65.5         | -                 |
| 10         | 5e14                                         | 237                   | 118.5        | -                 |
| 18         | 2.5e14                                       | 393                   | 196.5        | -                 |
| 20         | 2e14                                         | 430                   | 215.0        | -                 |
| 30         | 1.3e14                                       | 609                   | 304.5        | -                 |
| 40         | 9.0e13                                       | 780                   | 390.0        | 623               |
| 50         | 7.0e13                                       | 944                   | 472.0        | 755               |
| 60         | 5.5e13                                       | 1104                  | 502.0        | 882               |
| 70         | 5.0e13                                       | 1260                  | 630.0        | 1008              |
| 80         | 4.0e13                                       | 1413                  | 706.5        | 1130              |
| 100        | 3.0e13                                       | 1710                  | -            | 1368              |
| 110        | 2.9e13                                       | 1856                  | -            | 1485              |
| 120        | 2.6e13                                       | 2000                  | -            | 1600              |
| 130        | 2.4e13                                       | 2142                  | -            | 1713              |
| 140        | 2.2e13                                       | 2282                  | -            | 1826              |
| 150        | 2.0e13                                       | 2421                  | -            | 1937              |
| 160        | 1.9e13                                       | 2559                  | -            | 2047              |
| 170        | 1.7e13                                       | 2696                  | -            | 2156              |
| 180        | 1.6e13                                       | 2830                  | -            | 2264              |
| 190        | 1.5e13                                       | 2965                  | -            | 2372              |
| 200        | 1.4e13                                       | 3098                  | -            | 2478              |

## APPENDIX 'B'

### DEVICE SIMULATION SOFTWARE TOOLS

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Many software packages like MEDICI[41], ATLAS[15] and BIPOLE [42] are commercially utilized for the simulation and optimization of the various device parameters before manufacturing them. The simulation package [15] has been utilized for the 2-D simulation done in the present work. It consists of the following modules.

#### DevEdit

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It is an interactive tool for specifying and modifying device structure. It includes a meshing module that supports mesh generation, refinement, and un-refinement. It uses triangular mesh. Base material, doping profile types their type, doping etc. may be defined and modified using analytical functions. It can be used as a stand-alone tool or it can be invoked by DeckBuild. Large devices with many grids points may be specified completely using DevEdit making this tool valuable as a preprocessor for 2D Device simulations. DevEdit3 supports the definition and meshing of 3D structures. We have license for 2D simulation for the present.

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## ATLAS

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ATLAS is a physically based two and three-dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation. Semiconductor device operation is modeled in ATLAS by a set of anywhere from one to six coupled, non-linear, partial differential equations (PDEs). ATLAS produces numerical solutions of these equations by calculating the values of unknowns on a mesh of points within the device. An internal discretization procedure converts the original, continuous model to a discrete non-linear algebraic system that has approximately the same behavior. The set of PDEs, the mesh and the discretization procedure determine the non-linear algebraic problem that must be solved. The non-linear algebraic system is solved using an iterative, Newton, Gummel or Block or any combination of it, procedure that refines successive estimates of the solution. Iteration continues until the corrections are small enough to satisfy convergence criteria, or until it is clear that the procedure is not going to converge. The non-linear iteration procedure starts from an initial guess. The corrections are calculated by solving linearized versions of the problem. The linear sub-problems are solved by using direct techniques or iteratively.

In transient simulation, the carrier continuity equations are integrated in the time domain. Time integration schemes differ in their accuracy, in the number of previous time levels they employ, and in their stability properties. For drift-diffusion calculations, ATLAS uses a composite of trapezoidal rule (TR) - Backward Difference Formula-2 (BDF2) scheme that was developed by Bank et.al [43]. This method is one-step, second

order and both A-stable and L-stable. An estimate of local truncation error (LTE) is obtained at each time step, and this estimate is used to automatically adapt the time step.

The order in which statements occur in an ATLAS input file is important. There are five groups of statements, and these must occur in the correct order. The failure to do so usually causes an error message and termination of the program.

- |    |                               |                                                        |
|----|-------------------------------|--------------------------------------------------------|
| 1. | Structure Specification       | MESH<br><br>REGION<br><br>ELECTRODE<br><br>DOPING      |
| 2. | Material Models Specification | MATERIAL<br><br>MODELS<br><br>CONTACT<br><br>INTERFACE |
| 3. | Numerical Method              | METHOD                                                 |
| 4. | Solution Specification        | LOG<br><br>SOLVE<br><br>LOAD<br><br>SAVE               |

## 5. Results

## EXTRACT

## TONYPLOT

**DeckBuild**

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ATLAS is normally used through the DeckBuild run-time environment that supports both interactive and batch-mode operation. The input files can be directly entered once the Deckbuild is started. DeckBuild Command Menu can help to create input files. It can be configured for different default modules. The Command Menu gives access to pop-up windows in which desired information is typed. When “Write” button is selected, syntactically correct statements are written to the DeckBuild text edit region. It covers most of the possible ATLAS syntax. The run-time output shows the execution of each ATLAS command and includes error messages, warning, extracted parameters and other important output for evaluating each ATLAS run.

**Tonyplot**

It is a Visualization Tool, which provides comprehensive interactive scientific visualization capabilities. All of the usual ways of displaying scientific data are supported by it and we can get hard copy of plots.

The above modules provide the general framework of the simulator. There are different modules, which supports different material and analysis capabilities. For silicon, S-PISCES is used. GIGA provides the non-isothermal calculations. Mixedmode provides

the device based circuit simulation capabilities. BLAZE for III-V compounds, TFT for poly-silicon based devices, LUMINOUS for opto-electronic devices, LASER for hetero-structures, DEVICE3D for three dimensional device simulation. Besides, the general framework of the simulator as described above; we have license only for S-PISCES and GIGA.

We have carried out different static I-V experiments and reverse recovery experiments using the above. The input files have been written in the Deckbuild editor window.

## APPENDIX 'C'

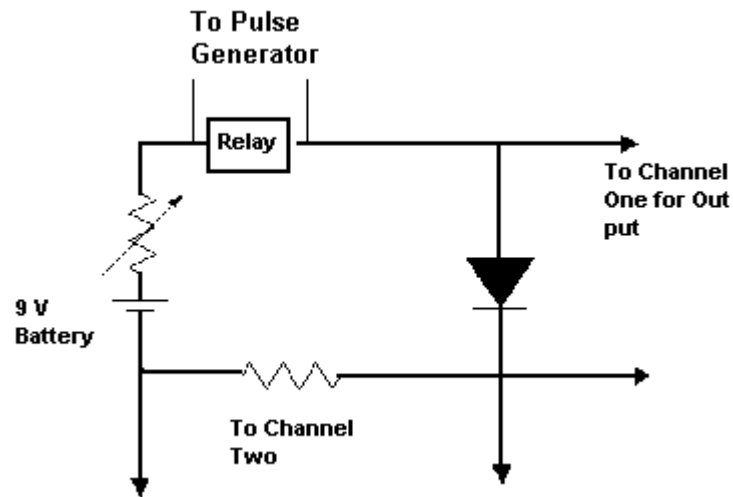
## LIFETIME MEASUREMENT USING OPEN CIRCUIT VOLTAGE DECAY (OCVD)

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The operating principle and circuit are given in [43]. To the first order, the effective recombination lifetime is given by

$$t_{eff} = \frac{n \frac{kT}{q}}{\frac{dV}{dt}}$$

Where n varies 1 to 2 from low to high injection conditions. The  $\tau_{eff}$  is an effective lifetime influenced by emitter recombination, back surface recombination for short-base diodes, edge effects and process conditions. The following circuit was rigged to measure the lifetime using Open Circuit Voltage Decay (OCVD).



**Fig. (C.1) Experimental setup for measuring Lifetime using Open Circuit Voltage Decay (OCVD)**

**Table C – Change of Lifetime of PIN Diode with Current**

| Current (mA) | Small Area (1 mm <sup>2</sup> )      |               | Large Area (25 mm <sup>2</sup> )     |               |
|--------------|--------------------------------------|---------------|--------------------------------------|---------------|
|              | Current Density (A/cm <sup>2</sup> ) | Lifetime (ms) | Current Density (A/cm <sup>2</sup> ) | Lifetime (ms) |
| 1            | 0.1                                  | 26            | 0.004                                | 115           |
| 10           | 1.0                                  | 17.3          | 0.04                                 | 104           |
| 70           | 7.0                                  | 14.8          | 0.28                                 | 86            |

The above result show that lifetime depends on area. Also as seen from above Table ‘C’ and shown by [44], the effective lifetime also depends upon current levels. The lifetime of the experimental diode and transistor were therefore measured at low current density using the above circuit.

## APPENDIX 'D'

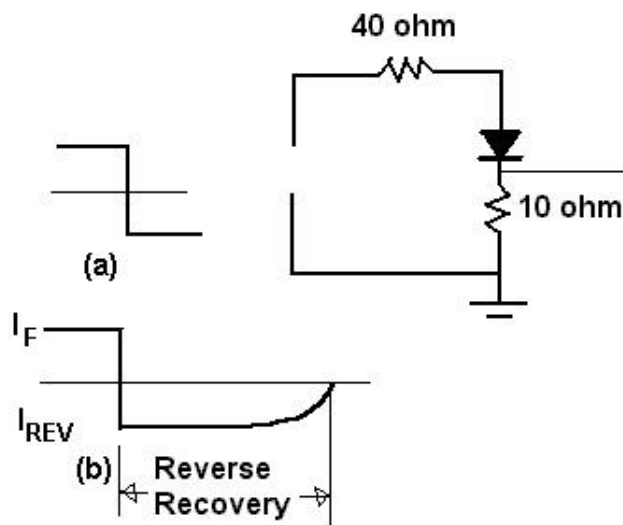
### EXPERIMENTAL MEASUREMENTS

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Numbers of measurements were made in diodes and transistors. Static characteristics like leakage current, breakdown voltage,  $V_{CE}$  and  $\beta$  were measured using curve tracer. Reverse recovery including the storage and fall time effects were measured using reverse recovery method. These values are given in chapters II and III under subsection of Experimental Results.

#### EXPERIMENTAL SETUP TO MEASURE THE REVERSE RECOVERY OF DIODES

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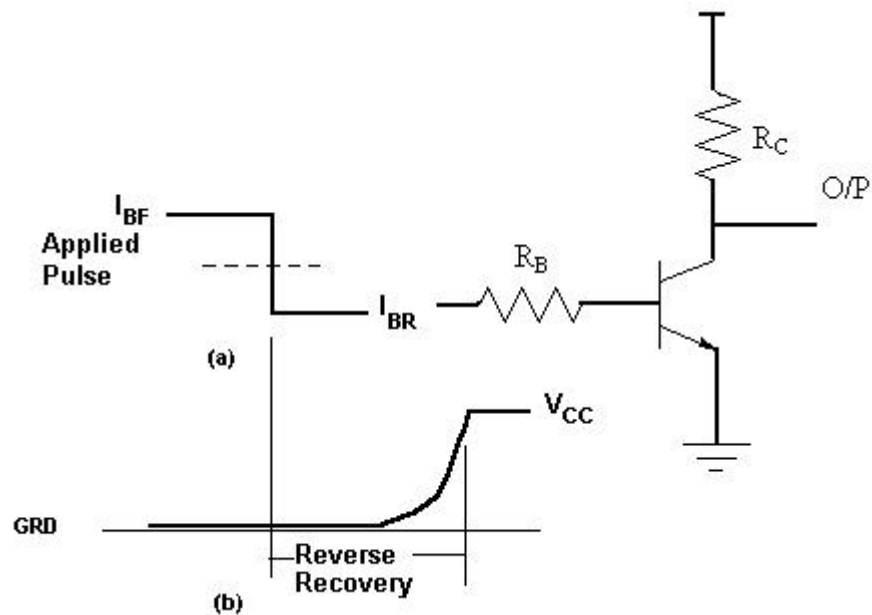
**Fig. D.1** Experimental circuit for reverse recovery measurement of diodes

The circuit as shown in Fig (D.1) was rigged-up. Forward and reverse drive currents were kept same. The applied pulse and response of the diode are shown in Fig. D.1.

## EXPERIMENTAL SETUP - TRANSISTORS

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The circuit as shown in Fig. D.2 was rigged-up. A base drive pulse wide enough to saturate the device was applied



**Fig. D.2** Experimental circuit for reverse recovery measurement of transistors.

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