Unified Power Quality Conditioner (UPQC) for Power Distribution Systems

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Introduction

Motivation

Design, Simulation and Hardware Implementation of Unified Power Quality conditioner (UPQC)
(Single phase and Three phase)

Optimum UPQC

Conclusion and Scope of future research
**Introduction**

**Power Quality**: Measure of proper utilization of power by customers

“Electrical Pollutant” vs “Clean Utility”

- Advent of wide spread use of high power high frequency switching devices
- Additional System required to maintain quality
- Deregulation, tariff

![Diagram](image)

**Responsibility of Both!**

- Power Supply Authority
- Consumer
- Clean Power Supply/Correction Measure
- No Electrical Pollution
Power Quality Affected by Polluting Load

Other loads connected at the Point of Common Coupling (PCC) suffer!

Two Main PQ Problems

- Harmonic and reactive current drawn by the loads.

- Voltage sag/ Distortion.
Harmonic Polluting Loads

- Computers
- Computer controlled machine tools
- Photo-copying machines
- Various digital controllers
- Adjustable speed drives
- PLCs
- Uncontrolled or phase controlled rectifiers

Some Important Observations of Power Quality (PQ) Surveys

- More low r.m.s. voltage sag occur at the PCC
- Majority of voltage sag are 10-20%
- More disturbances occur above 70% of nominal line voltage
- The occurrence of most severe sag events are least frequent.
POWER QUALITY STANDARDS

IEEE 519 Voltage Limits

<table>
<thead>
<tr>
<th>Bus Voltage (PCC Voltage)</th>
<th>Maximum Individual Harmonic components (%)</th>
<th>Maximum THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>69 kV and below</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>115 - 161 kV</td>
<td>1.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Above 161 kV</td>
<td>1</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Power Quality Solution Strategies
Power Quality (PQ) Solution Strategies

**Local Solution**

(a) Providing ‘ride-through’ capability to the equipment so that they can be protected against certain amount of voltage sag and swell

(b) Equipment are provided with an arrangement so that they draw low reactive power and harmonics

(c) Disadvantage of this approach is that it cannot take care of existing polluting installations and further it is not always economical to provide the above arrangement for each and every equipment

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**Global Solution**

(a) Here independent compensating devices are installed at PCC so that overall PQ improves at PCC.

(b) Advantages of this approach are

- Individual equipment need not be designed according to PQ standards
- Existing Polluting installations can be taken care of.
Modern Solutions

a) Shunt (parallel) Active Filter (STATCOM)

b) Series Active Filter (DVR)

STATCOM

Static Synchronous Compensator

Compensates For
- Reactive Current
- Harmonic Current
STATCOM acting as Capacitor

\[ V_{\text{stat}} = jlwL + V_{\text{pcc}} \]

\[ \frac{V_{\text{stat}} - V_{\text{pcc}}}{jwL} = 1 \]

\[ \pm j(k) = 1 \]
STATCOM acting as a Capacitor

STATCOM acting as an Inductor
STATCOM Control Strategy

i_s is at Unity Power Factor

DVR (Dynamic Voltage Restorer)

Corrects For
- Voltage sag
- Voltage harmonics
Reactive Power Transfer

\[ V_s^2 = V_L^2 - 2V_L V_{dvr} \sin \Phi + V_{dvr}^2 \]

In-Phase Compensation
Phase cum Magnitude Compensation

Motivation

Development of Multipurpose Custom Power Equipment

- Load harmonic and VAR compensation
- Voltage sag mitigation and unbalanced voltage correction
- Fast dynamic response, and steady state accuracy

Unified Power Quality Conditioner (UPQC)
Unified Power Quality Conditioner (UPQC)

Inverter-I compensates for sag through a tuned filter and voltage transformer

Inverter-II (SLCVC) Synchronous Link Converter VAR Compensator provides VAR to the load, isolates load current harmonics, makes input power factor unity

SLCVC maintains the charge of the dc link capacitor
**Phasor diagram of UPQC-Q for fundamental power frequency, when \( \theta < \Phi \)**

\[
V_{inj} = \sqrt{V_{s1}}^2 - V_{s2}^2
\]
\[
\sqrt{2}V_{inj} = mV_{dc} / 2
\]
\[
m = 2\sqrt{2} \cdot \sqrt{x(2 - x)} \cdot V_{s1}
\]

From power balance
\[
I_{s2} = I_{s3} \left( \frac{\cos \phi}{\cos \theta} \right)
\]

Where, \( x \) is p.u. sag
\( m \) = Modulation Index (max MI=1)
and transformer ratio 1:1
Series VA Loading of **UPQC-Q**

![Graph showing Series VA loading of UPQC-Q](image)

Shunt VA Loading of **UPQC-Q**

![Graph showing Shunt VA loading of UPQC-Q](image)
Combined VA Loading of UPQC-Q

Control Block Diagram
Control Strategy

Four Modules

- Controller for maintaining DC link Voltage
  - PC based software control
- Current Controller for Shunt Inverter
  - Analog control, instantaneous response
- Dynamic sag Controller
  - Feed forward and feedback control combined
- PWM Voltage Controller for Series Inverter
  - Analog Control

Fig. 3.15 Block diagram of hardware implementation
Fig. 3.22 Simulation result of supply and load current corresponding to Fig. 3.21
X axis = 5 ms/div Y axis = 5 A/div

Fig. 3.21 Experimental result of supply current and load current
X axis : 5 ms/div Y axis : 5 A/div

Fig. 3.23 Load current (i_{load}) spectra (Experimental)

Fig. 3.24 Supply current (i_s) spectra (Experimental)
Fig. 3.25 Experimental results of supply current \( (i_s) \) and supply current reference \( (i_s^*) \)
- X axis: 5 ms/div
- Y axis: 10 A/div

Fig. 3.26 Simulation results of supply current \( (i_s) \) and supply current reference \( (i_s^*) \)
- X axis: 5 ms/div
- Y axis: 10 A/div

Fig. 3.27 Experimental result of \( v_L, v_s \) and \( v_{sec} \)
- Trace-1: Load voltage \( (v_L) \)
  - Y axis: 50 v/div
- Trace-2: Supply voltage \( (v_s) \)
  - Y axis: 50 v/div
- Trace-3: Series injected voltage \( (v_{sec}) \)/38
  - Y axis: 1 v/div
- X axis: 20ms/div

Fig. 3.28 Simulation result of \( v_L, v_s \) and \( v_{sec} \)
- Trace-1: Load voltage \( (v_L) \)
  - Y axis: 50 v/div
- Trace-2: Supply voltage \( (v_s) \)
  - Y axis: 50 v/div
- Trace-3: Series injected voltage \( (v_{sec}) \)/38
  - Y axis: 1 v/div
Fig. 3.29 Load voltage ($v_L$) spectra

THD = 3.6%

Fig. 3.30 Steady state experimental results of DC link voltage ($V_{dc}$), supply ($i_s$) and load current ($i_L$)

X axis: 50ms/div Y axis: $V_{dc}$ 20V/div, $i_s$, $i_L$ 5A/div

Fig. 3.31 Steady state simulation results of DC link voltage ($V_{dc}/1000$), supply ($i_s$) and load current ($i_L$)

X axis: 50ms/div Y axis: $V_{dc}$ 1V/div, $i_s$, $i_L$ 2A/div
Fig. 4.20a Experimental results of supply current and load current of phase-A
X axis: 50 ms/div, Y axis: 5 A/div for $i_{sa}$, 2 A/div for $i_{loada}$

Fig. 4.20b Simulated results of supply current and load current of phase-A

Fig. 4.21a Experimental results of supply current and supply voltage of phase-A
X axis: 50 ms/div, Y axis: 5 A/div for $i_{sa}$, 20 V/div for $v_{sa}$

Fig. 4.21b Simulated results of supply current and supply voltage of phase-A
<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>Load Current (A-phase)</th>
<th>Supply current (A-phase)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Magnitude</td>
<td>% fundamental</td>
</tr>
<tr>
<td>1st</td>
<td>1.645 A</td>
<td>100</td>
</tr>
<tr>
<td>5th</td>
<td>313.47 mA</td>
<td>19</td>
</tr>
<tr>
<td>7th</td>
<td>204.86 mA</td>
<td>12.45</td>
</tr>
<tr>
<td>11th</td>
<td>113.09 mA</td>
<td>6.87</td>
</tr>
<tr>
<td>13th</td>
<td>80.05 mA</td>
<td>4.86</td>
</tr>
<tr>
<td>15th</td>
<td>31.43 mA</td>
<td>1.91</td>
</tr>
<tr>
<td>17th</td>
<td>26.13 mA</td>
<td>1.71</td>
</tr>
<tr>
<td>23rd</td>
<td>13.67 mA</td>
<td>0.83</td>
</tr>
<tr>
<td>25th</td>
<td>9.159 mA</td>
<td>0.5</td>
</tr>
<tr>
<td>THD</td>
<td>23.28%</td>
<td>2.957%</td>
</tr>
<tr>
<td>Displacement Factor</td>
<td>0.768</td>
<td>0.992</td>
</tr>
</tbody>
</table>

Fig. 4.23a Experimental result of peak of supply voltage and load voltage of phase-A
X axis: 100 ms/div, Y axis: 50 V/div for v_loada, 10.48 V/div for Vsa_peak.

Fig. 4.23b Simulated result of peak of supply voltage and load voltage of phase-A
Fig. 4.24a Experimental result of peak of supply voltage and supply current of phase-A
X axis: 100 ms/div, Y axis: 20.96 V/div for Vsa_peak, 2 A/div for i_loada

Fig. 4.24b Simulated result of peak of supply voltage and supply current phase-A

Fig. 4.25a Experimental result of peak of supply voltage and injected voltage and supply voltage of phase A, X axis: 10 ms/div, Y axis: 10 V/div for secv_a, 50 V/div for vsa, 52.4 V/div for Vsa_peak

Fig. 4.25b Simulated result of injected voltage and supply voltage of phase-A
Conventional UPQC-P

- $V_{\text{inj}}$ by DVR in phase with the supply voltage
- DVR consumes active power
- No sharing of Load VAR between STATCOM and DVR
- Can compensate for both voltage sag and swell
Operation under Sag (UPQC-P)

Series VA Loading of UPQC-P
Shunt VA Loading of UPQC-P

Combined VA Loading of UPQC-P
Limitations of UPQC-Q/P

- **UPQC-Q**
  - Unable to mitigate voltage unbalance in magnitude
  - Unable to mitigate voltage unbalance in phase shift
  - Does not compensate for voltage swell

- **UPQC-P**
  - Capable of compensating both voltage sag and swell
  - Capable of mitigating voltage magnitude unbalance
  - Unable to mitigate voltage phase unbalance

VA Minimization by Injecting Voltage at an Optimum Angle
Unbalanced Sag Mitigation

DVR control is done to inject voltage at an optimized phase angle.

DVR Control Strategy
Source voltages during normal and sag condition

Load voltages during normal and sag condition
Case Study (Optimized UPQC)

Load p.f. angle (Φ) = 30° lag, PU voltage sag (x) = 20%

optimum angle (θ) = 24°

Effectiveness of the scheme through comparison

- VA (UPQC-Q) = 0.7 p.u., (θ = 36.7°)
- VA (UPQC-P) = 0.6 p.u., (θ = 0°)
- VA (UPQC-proposed) = 0.48 p.u., (θ = 24°)

Conclusions on UPQC

1. UPQC can mitigate voltage sag.
2. Hybrid (combined analog and digital) control implemented, the control scheme is applicable for both single phase and three phase.
3. No additional energy storage device required for sag compensation, long duration sags and under voltages can also be compensated.
4. Dynamic response is fast.
5. UPQC can supply VAR to the load.
6. It isolates the load current harmonics from flowing to the utility.
7. It maintains input unity power factor at all conditions.
8. Optimized UPQC leads to minimum VA loading of the converters.

Future Scope of Research

- UPQC for three phase four wire system
- Voltage swell compensation
Thank you