Department of Electrical Engineering,
Indian Institute of Technology, Kanpur

EE 370A Digital Electronics 2021-22-I

Instructor: Dr. Shubham Sahay (ssahay@iitk.ac.in)

Tutors: **Section I** (Roll no. ≤ **190125**) Dr. Shubham Sahay (sashay@iitk.ac.in)
Section II (**190126** ≤ Roll no. ≤ **190364**) Prof. Aloke Dutta (aloke@iitk.ac.in)
Section III (**190365** ≤ Roll no. ≤ **190597**) Dr. Imon Mondal (imon@iitk.ac.in)
Section IV (**190598** ≤ Roll no. ≤ **190775**) Dr. Rik Dey (rikdey@iitk.ac.in)
Section V (Roll no. ≥ **190795**) Ravi Goel (gravi@iitk.ac.in)

Tutorial Schedule: Tuesdays, Timing: 5:10 p.m. to 6:00 p.m.
(Zoom meeting link for the tutorial sessions of the individual sections to be sent by the tutors separately as an announcement over mooKIT)

TAs: **Section I** Anmol Anand (anmolanand20@iitk.ac.in)
Section II Souvik Ghosh (souvikecin20@iitk.ac.in)
Section III Kumari Anjali Sinha (kumarianju20@iitk.ac.in)
Section IV Anupam Jaiswal (anuwal20@iitk.ac.in)
Section V Jitendra Singh (jitsingh20@iitk.ac.in)

Course Schedule: The course would run in an asynchronous mode, and the lectures would be uploaded on mooKIT before the stipulated classroom lecture time (Mondays, Wednesdays, and Fridays: 11:00 a.m. to 11:50 a.m.)

Discussion Session: Fridays, Timing: 11:00 a.m. to 11:50 a.m.

Zoom link for the Discussion Session:

https://iitk-ac-in.zoom.us/j/94333021982?pwd=ZVV2Y3p4Um5DRUxJYXcwem9BR0VVQT09

Meeting ID: 943 3302 1982

Passcode: 233338

Course Objective:
This course intends to provide a deep insight into the world of digital electronics from a design perspective. At the end of the course, the student should be able to:

(a) Develop an understanding of the digital circuit design techniques and the trade-offs associated with the design methodologies for digital circuits and memories.
(b) Develop an appreciation for the hierarchical design translating the elementary combinational and sequential circuits to complex systems.

Grading Scheme: To be discussed in the first lecture.

Course content:

S. No.	Tentative topics to be covered
1.	Introduction: historical perspective, state-of-the-art and a peek into the future.
2.	Issues with fully automated digital design, quality metrics: cost (real estate), function and robustness, power and energy, speed.
3.	Inverters in isolation: different inverter implementations, MOSFET as a switch, CMOS inverter, static and dynamic behavior of CMOS inverters, performance metrics, A design perspective: analysis of chain of inverters and impact of scaling.
4.	Combinational circuits: design guidelines and trade-offs involved with static CMOS design, ratioed logic design, pass-transistor design, and dynamic logic design.
5.	Sequential circuit design: static timing analysis (STA), Bi-stable circuits: static and dynamic latch and registers, pipelining, and non-bistable sequential circuits.
6.	Array based logic designs: field-programmable gate array (FPGA).
7.	CMOS memory design: memory hierarchy and organization, peripheral circuitry, static random-access memory (SRAM) design, dynamic RAM (DRAM) design.
8.	Moving up the hierarchy: system level design, Datapath and register transfer operation.
9.	Introduction to hardware description language (HDL).
10.	Register-transfer level (RTL) to GDSII flow (lecture by an industry expert).

Recommended texts

- Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, "Digital Integrated Circuits – a design perspective", *Prentice-Hall India.* (We will borrow material freely from this book during this course.)
- M. Morris Mano and Charles R. Kime, "Logic and Computer Design Fundamentals", *Pearson Education* (We will follow chapter 7 of this book for discussions on Datapath and register transfer.)
- Adel S. Sedra and Kenneth C. Smith, "Microelectronics Circuits", *Oxford University Press* (We will follow chapter 10 and 11 of this book.)
- Morris Mano, "Digital Design", *Pearson Education* (For revising fundamentals of digital electronics taught in ESC201)