

Analytical Modeling for Performance Studies of an FLBM-Based All-Optical Packet Switch

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Abstract—This letter analyzes an all-optical packet switch based on fiber loop buffer memory (FLBM). The number of recirculations of a packet in the fiber loop is limited by noise constraints whereas the total number of packets stored in the fiber loop is constrained by the number of available wavelengths. The switch operates as an output-queued switch with these constraints. We analyze this switch for its blocking performance for incoming packets.

Index Terms—Optical fiber applications, optical fiber switches, packet switching, queueing analysis.

I. INTRODUCTION

OPTICAL FIBERS are replacing cables as the transmission media in most long and short-haul communication networks. Switching and routing in these networks may either be done through lightpath switching through optical cross-connects as in WDM systems [1], [2] or by using a high speed packet switch [3][4]. We consider an all-optical implementation of such a packet switch in this paper and present its analysis. This proposed switch is based on the multi-wavelength fiber loop buffer memory (FLBM) of the RACE-ATMOS project [3] and assumes packets (or cells) of a fixed length as in an ATM network

II. SWITCH ARCHITECTURE AND MODEL

The basic switch architecture is given in Fig. 1. At each of the inputs, a packet destined for one of the outputs may arrive on a single wavelength in each time slot. The header of the packet is analyzed (not shown in Fig. 1) for making the required routing decisions. The packet then goes through a tunable wavelength converter and its carrier wavelength is changed as decided by a switch controller (not shown in Fig. 1). The decision on what wavelength the packet will be transformed to is taken depending on the free wavelengths available in the FLBM buffer.

The FLBM consists of a fiber loop with wavelength multiplexer/demultiplexer and semiconductor optical amplifiers (SOA). The SOA's can switch specific wavelengths ON/OFF as required. The FLBM stores packets by keeping the corresponding optical signal re-circulating in the loop. The length of the FLBM fiber is exactly equal to the packet duration at the given speed of transmission. Packets from the FLBM may then either continue in the FLBM or may be directed to a output port—in that case, the corresponding SOA is turned off erasing

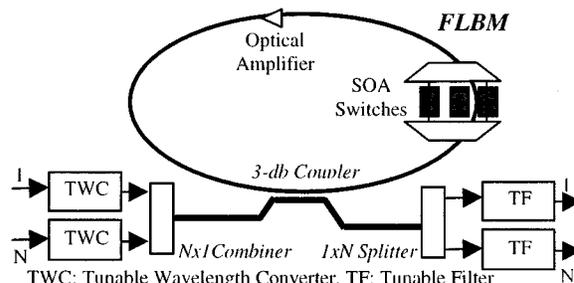


Fig. 1. All-optical FLBM packet switch.

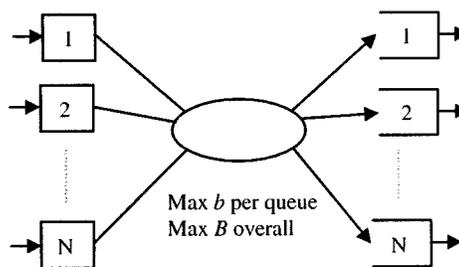


Fig. 2. Queueing structure for all-optical packet switch.

the packet from the loop. Simultaneous read/write in the same FLBM wavelength will not be allowed from the viewpoint of practical implementation.

The optical amplifier and the SOA will add noise for each recirculation of the optical signal corresponding to a packet stored in the FLBM. We model this by assuming that at most b recirculations may be allowed for a packet stored for a particular output. This would then also be the limit on the number of packets that may be buffered for a particular output. Packet loss would occur whenever this limit is exceeded. If there are $b - k$ packets for a particular output presently buffered in the FLBM, and if $K (K > k)$ inputs have packets for this output, then the controller will drop $(K - k - 1)$ of these. (The “-1” term accounts for the packet passed on to the output during this slot.) We assume that B is the total number of wavelengths available for packet storage in the FLBM. This would then also be the total number of buffers available for sharing between all the N outputs of the switch. Fig. 2 shows the equivalent discrete queueing model for this $N \times N$ all-optical FLBM packet switch.

III. MODELING OF THE SWITCH

We consider a $N \times N$ switch for switching fixed length packets of unit length. The inputs are assumed to be synchronous with slots also of unit length. For each of the N inputs, let p be the probability that a packet is generated in a slot

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and that the packet may be routed to any of the N outputs with equal probability. For the buffer constraints b and B mentioned earlier, the routing rules followed by the switch controller are as follows.

- 1) If there are $i(1 \leq i \leq b)$ packets in buffer for output j , then one of them will be sent to the output. If in that slot, there are one or more packets also present at the inputs for output j , then these will be buffered in the FLBM, to the extent allowed by rules 3)–5).
- 2) Consider the case, where there are no packets in the buffer for output j , but K input lines have packets for that output. Then one of these K packets is directly sent to output j . The other $K - 1$ packets will be buffered in the FLBM to the extent allowed by rules 3)–5).
- 3) Number of packets x_j in buffer for output j should never be greater than b , i.e., $x_j \leq b$ for $j = 1, \dots, N$.
- 4) The total number of packets in all the buffers should never be greater than B , i.e., $\sum x_j \leq B$.
- 5) The buffers are such that simultaneous read and write is not allowed in the same slot for the same wavelength in the FLBM.
- 6) Depending on the current buffer state and the offered input pattern, one or more of the input packets may be lost. The switch controller adopts the rule of dropping packets for the lower indexed output lines first (from the input pattern), whenever this is needed. [Other approaches such as dropping packets of the highest indexed output first or random dropping may also be proposed for this.]
- 7) In addition, the controller is expected to maintain FCFS flow between inputs and corresponding outputs for all packets that are not dropped. This is important from the viewpoint of virtual circuit based transport.

It may be noted that for this switch to be *fully output queued*, B should be greater than or equal to $[(N - 1)b + N]$ for any given value of b . Moreover, the FLBM buffer will only be able to store up to $(N - 1)b$ packets overall under this condition. The following theorem may also be shown

Theorem: For this switch, if $B \leq (N - 1)b + N$ and $B > N$, then for $y = \lfloor (B - N)/b \rfloor$, the maximum number of packets that can be stored in the FLBM buffer would be

- (a) $(B - y - 1)$, if $[(B - N) \bmod b] + N - y - 1 \leq b$
or
- (b) $(B - y - 2)$, if $[(B - N) \bmod b] + N - y - 1 > b$.

IV. ANALYTICAL MODEL OF THE SWITCH

In any given time slot, we define $\mathbf{I} = (I_1, I_2 \dots I_N)$ to be the input pattern and $\mathbf{O} = (O_1, O_2, \dots, O_N)$ as the buffer state of the $N \times N$ switch. Here, I_i = total number of packets arriving at all the input lines in that slot which are destined for output i and O_j = number of packets destined for output j presently in the FLBM buffer.

Let p be the probability of a packet arrival in a slot at one of the inputs where we assume that the packet is equally likely to be destined for any one of the N outputs. (Note that this

offers a net load of Np packets per slot to the switch.) For this binary arrival model, we can calculate the probability $P(\mathbf{I})$ for any input pattern \mathbf{I} which would be feasible. For example, for a 2×2 switch, we get $P\{\mathbf{I}(0, 0)\} = (1 - p)^2$, $P\{\mathbf{I}(1, 0)\} = P\{\mathbf{I}(0, 1)\} = (1 - p)p$, $P\{\mathbf{I}(1, 1)\} = p^2/2$, and $P\{\mathbf{I}(2, 0)\} = P\{\mathbf{I}(0, 2)\} = p^2/4$. For an $N \times N$ switch, similar expressions for $P(\mathbf{I})$ may be derived for any \mathbf{I} .

We obtain the set of feasible buffer states \mathbf{O} by applying the routing rules given in Section III to the switch for all possible input patterns \mathbf{I} applied to all possible initial buffer states. We did this by using a computer program to build up an exhaustive table of all possible buffer states as follows

Step 1: Let the all-zero buffer state be the current state.

Step 2: Apply all possible input patterns to the current buffer state to generate new buffer states. Add any new buffer state generated to the buffer state table.

Step 3: For each of the new buffer states generated above, repeat the procedure of *Step 2* until all possible output states have been generated.

This procedure also allows us to build a table for the number of packets lost $n_{\text{lost}}(\mathbf{I}, \mathbf{O})$ for input pattern \mathbf{I} and buffer state \mathbf{O} for all combinations of \mathbf{I} and \mathbf{O} . Using this, the probability P_L of packet loss for the $N \times N$ switch with parameters b and B and input probability p will be found from

$$P_L = \sum_{\forall \mathbf{O}} \sum_{\forall \mathbf{I}} n_{\text{lost}}(\mathbf{I}, \mathbf{O}) P(\mathbf{I}) P(\mathbf{O}) / (Np).$$

In the above equation, $P(\mathbf{O})$ will be found by solving the appropriate balance equations for the state. We have automated this process (because of the large number of state variables involved) by writing a computer program which generates all the global balance equations using the routing rules given in Section III. These balance equations may then be directly solved using MATLAB or any other similar package. As an example, we give a sample equation next; this is the *global balance equation* for the buffer state (1,1) in a 2×2 switch for $b = 2$, $B = 3$

$$\begin{aligned} P\{\mathbf{I} = (2, 0)\}P\{\mathbf{O} = (0, 2)\} + P\{\mathbf{I} = (0, 2)\}P\{\mathbf{O} = (2, 0)\} \\ = P\{\mathbf{O} = (1, 1)\} [P\{\mathbf{I} = (0, 0)\} \\ + P\{\mathbf{I} = (0, 1)\} + P\{\mathbf{I} = (1, 0)\} \\ + P\{\mathbf{I} = (1, 1)\} + P\{\mathbf{I} = (0, 2)\} + P\{\mathbf{I} = (2, 0)\}]. \end{aligned}$$

Note that some of the above transitions will involve packet loss. For example, if the input pattern (0, 2) is applied to the buffer state (1, 1) in this switch, then one packet will be lost and the buffer state reached will be (0, 1). Note that this happens because simultaneous read/write on a FLBM wavelength will not be allowed.

V. RESULTS

The approach described above can be used to study the performance of the $N \times N$ FLBM-based, all-optical packet switch as described in Sections II and III. Apart from the size of the switch (i.e., N), the other parameters that will affect its performance are as follows.

- 1) The noise in the optical amplifier and the SOA's of the FLBM which will effectively decide the recirculation

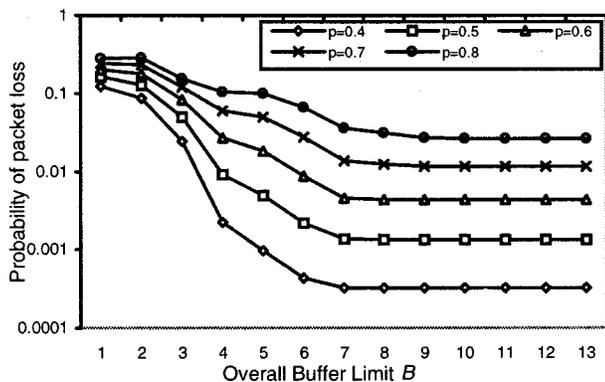


Fig. 3. Probability of packet loss vs. B for $b = 3$ and different values of the traffic intensity p .

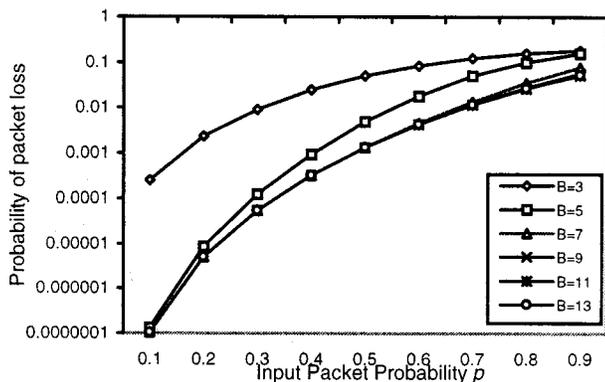


Fig. 4. Probability of packet loss vs. the input packet probability p for $b = 3$ and different values of B .

limit and hence the buffer limit b for each of the switch outputs.

- 2) The hardware investment in terms of the number of SOA's and wavelengths supported in the FLBM.
- 3) The input packet probability p of a packet arrival in a slot in any one of the input lines. Note that this will lead to an offered traffic of Np packets per slot.

The basic performance result that is needed to characterize the switch is the probability P_L of packet loss. Its dependence on various parameters for a 4×4 switch has been shown in Figs. 3–5.

We note from Fig. 3 that even when the total number of wavelengths B (required in the FLBM) is much smaller than the *fully output queued* limit of $[N + (N-1)b]$ (13 in this case), the switch still performs as well as the latter. Using fewer wavelengths will make the fabrication of the FLBM easier. As shown in Fig. 3,

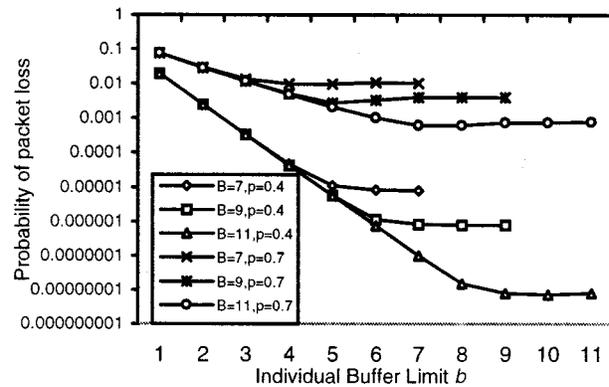


Fig. 5. Probability of packet loss vs. the individual buffer limit b for different values of B and p .

this can be done to a large extent without compromising the overall performance of the switch. As expected, we also find that loss increases with increasing traffic, i.e., increasing values of p . This is evident from the results of Figs. 3 and 4.

Saturation behavior similar to that in Fig. 3 is also seen in Fig. 5 where P_L is shown as a function of the individual buffer limit b . The FLBM amplifiers etc., should be low noise ones so that b will be as high as possible. Fig. 5 however indicates that for a given value of B (and p), increasing b beyond a threshold value may not provide any further improvement.

VI. CONCLUSIONS

We have presented an all-optical FLBM-based packet switch and have analyzed its performance with respect to various input and design parameters. Important design conclusions can be drawn from this analysis as indicated in this letter. We subsequently plan to approximate this by a simpler queuing model which may be more convenient to analyze large all-optical switches of this kind.

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