Novel Design Modification Proposal for All-Optical Fiber Loop Buffer Switch

Nikhil Verma, Rajiv Srivastava and Yatindra Nath Singh
Center for Laser Technology
Indian Institute of Technology, Kanpur, 208016, INDIA
Email: nverma@iitk.ac.in

1. INTRODUCTION

Current optical switching technologies allow us to rapidly deliver the enormous bandwidth of wavelength division multiplexed (WDM) networks. Broad acceptance of fiber optic and photonic technology in transmission systems has led to potential opportunities for using all-optical switching to utilise high bandwidth of the fiber and to cater the ever increasing demand of higher bandwidths. The major advantage has been all-optical data transmission without any electronic processing of the data in path. A number of configurations and classifications of optical packet switches have been found in literature, [1-4], depending on the buffer position and switch architecture. The switching and routing in these designs have been in optical domain however the control in electronic domain to capitalise the enormous optical bandwidth, functionality and processing power of electronic control. This paper gives an overview of a photonic packet switch, its operation, some application limitations in the existing design of loop-buffer, single stage, feed back delay, switch architecture and proposes modifications for them. The issues aimed in the modifications include the number cell periods required for read/write operation on a particular wavelength, complexity of control unit and dynamic re-allocation of packet wavelength.

2. PHOTONIC PACKET SWITCH

Large photonic packet switches will rely on optical means for data transmission, packet routing and buffering, with electronics for operational control. Key functions of a photonic switch, [3] , are packet routing, buffering and packet header replacement. A general structure of all-optical packet switch is shown in fig. (1), [3], [15]. It consists of an input interface, for header recognition, adapting to packet format and synchronisation. The switching and buffering block performs the routing and buffering of wavelengths for contention resolution and output block

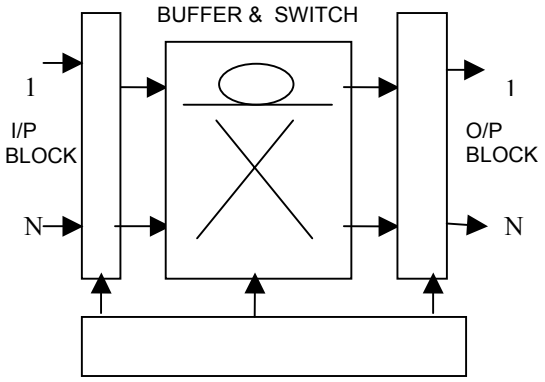


Fig.1. A Photonic packet switch

for header re-insertion. Header is converted from optical-to-electrical (O/E) domain for detection and processing and before re-insertion it is converted back to optical domain (E/O). Routing and buffering is done in all-optical domain. As shown in fig.(1), buffering of photonic packets is essential for contention resolution. The difficulty in implementing optical random access memory (O-RAM) makes optical buffering and synchronisation difficult. Electronic RAMs have speed and capacity limitations for all-optical packet switching systems. Also, electronic RAMs will require optical-to-electronic-to-optical (O/E/O) data conversion. Photonic packet buffer designs include travelling delay lines and re-circulating delay lines. When incorporated in switch architecture the different schemes are wavelength routing, broadcast and select routing and space switch,[3], [4]. The switch design under study is broadcast and select, multi-wavelength, loop-buffer with feed back delay, [4-7]. As shown in fig. (2). It consists of an all-optical tuneable wavelength converter (TWC), for each input, a WDM loop buffer having SOA gate switches for specified number of wavelengths, which may also be equal to the number of input port. The number of buffer wavelengths depend on the switch design, traffic throughput and data rate, [5], [11]. The packet allocation to the loop buffer depends on the routing and priority algorithm for the switch. The packets to be buffered are converted to the wavelengths available in the buffer, if buffer is full then packets are dropped. The TWCs are tuned at every cell slot to place a packet in the loop buffer to avoid contention. For reading or removing a packet from the buffer, the loop SOA gate is switched 'off', and tuneable filter (TF) at output is tuned to the packet wavelength, packet is broadcast to all the output ports but is selected by the desired port only.

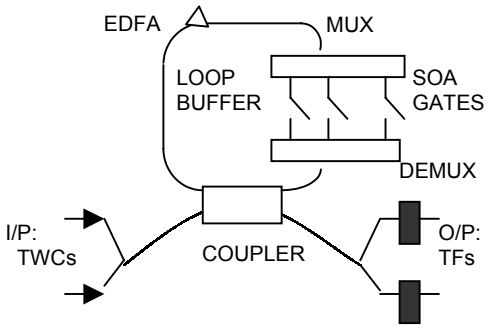


Fig.2. Existing switch architecture

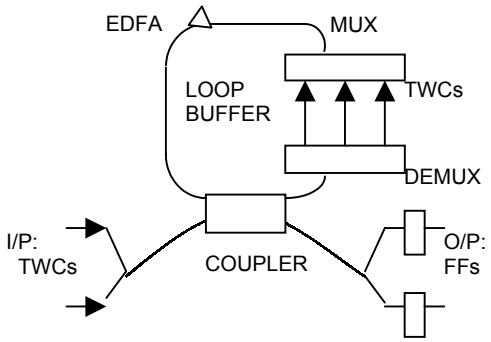


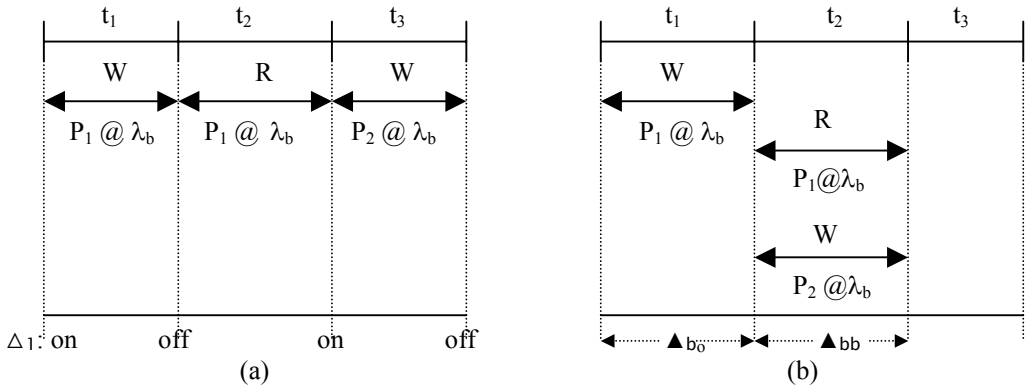
Fig.3. Switch design with proposed modifications

3. PROPOSED MODIFICATIONS

Two modifications are proposed in the existing design of all-optical loop-buffer switch. It is proposed to replace the buffer SOA gates with TWCs and in the output section TFs with fixed filters (FFs). The switch design after modifications is shown in fig. (3). The TWCs should be wavelength independent i.e. capable of conversion to any wavelength within the operational bandwidth of the switch design. When a packet is selected for buffering the respective TWC in the buffer is tuned to the buffer wavelength to accept the packet. As long as a packet is in buffer the selected TWC will remain transparent i.e. no conversion, till it is desired read out the packet or to have dynamic wavelength re-allocation, as explained in section 3.2. For reading a packet, when output contention is resolved, buffer TWC is tuned to the wavelength of appropriate output port FF, the packet is broadcast to all output ports, as in past, but is accepted only by the desired port. Switch design optimisation is one of the criteria for optical packet switching, considering this fact, the proposed modifications may obviate following limitations in the existing switch design.

3.1. Buffering and Read/Write Operation

The buffer memory has a word size equal to one cell period. Its capacity corresponds to pre-determined memory positions or number of buffer wavelengths. A packet is assigned a wavelength not being used by the packets within the buffer by the input TWC, as in fig. (2), the SOA is selected 'on' to accept the packet in the buffer. The packets from buffer are broadcast to the output by switching 'off' the appropriate SOA gate and simultaneously tuning the output filter to the packet wavelength. The read/write operation is explained in fig.(4a). It is clear that writing to same buffer wavelength as being read from cannot be done simultaneously, it is possible only after two cell periods.



Legends: t_{1-3}: Cell periods; **$P_{1,2}$:** Data Packets; **Δ_1:** SOA gate; **$\blacktriangle_{bb}$, $\blacktriangle_{bo}$:** TWC tuning time to λ_b, λ_{output} ; **λ_b:** Buffer wavelength **; λ_{output} :**Output wavelength.; **W**:Write operation; **R**: Read operation

Fig. 4. Comparision of read/write cycles in (a) Existing switch design, and (b) After proposed modifications

In the proposed modification, the loop SOA gates are replaced by TWC. The buffer TWCs can be tuned to any of the input or output wavelengths. As shown in fig.4(b), a packet at λ_b is written into buffer, by tuning the TWC to buffer wavelength λ_b. It takes one cell period for writing a packet. Assuming that contention is removed while a packet is being buffered, this will be the minimum time a packet can be buffered, the buffer TWC is tuned to λ_{out} for outputting the packet. Packet is read out from the buffer after getting converted to λ_{out}. After conversion as complete packet crosses the TWC, in process of being buffered out, the TWC is tuned back to same buffer wavelength λ_b as before. Hence the writing of a new packet on this wavelength can take place simultaneously as a packet from buffer is being read out. There will be no interference in two wavelengths as the inputting/ outputting device is a WDM 3dB coupler. Thus, the possibility of tuning a TWC soon after a packet is written-in and before it's read-out will result in only two cell periods for reading and writing on the same wavelength as compared to three in earlier switch design having SOA gates.

3.2. Dynamic Wavelength Re-allocation

A minimum channel spacing of 6 times the maximum data rate has been proposed and examined, [8],[9], for minimising cross talk in DWDM networks. The switch architecture with SOA gates is designed for fixed interchannel spacing. The design parameters cannot be scaled any further without modifying the switch component parameters. However, with a TWC as a buffer gate, it will be possible to dynamically modify the channel spacing while a packet is circulating. This will give a flexibility of operation by tuning a packet wavelength to any other available wavelength in the buffer. There is a limit to the maximum number of circulation, [10], [11], and thus on the maximum time for which a packet can remain in the buffer to resolve an output contention. One of the limiting factors is the inter and intra channel cross talk. Consider, for example, two packets in buffer at adjacent wavelengths, λ_1 and λ_2, with rest of the buffer wavelengths being free. The packet interchannel spacing, $\Delta\lambda$, can be increased to the extremes of the buffer capacity by tuning one of the TWCs to that wavelength. The dynamic wavelength re-allocation will reduce the noise due to cross talk and may in turn result in an increase in buffer time.

However there will be certain considerations in replacing SOA gates with TWCs. The TWC technology is not yet as developed as SOA, and as of now the tuning time of commercially available TWCs is of the order of msec, however for the packet switched network a tuning time of nsec is desired. Noise, tuning speed, and data rate dependency are major restrictive factors in TWC application, [12], [13], the same needs to be studied for the proposed modifications. Reliability studies have been carried out on fiber loop-buffer switch design,[14], similar studies can be undertaken once sufficient statistics on failure rate of TWCs is available to determine a reliability structure with proposed modifications. The development and test of different TWC technologies is still in progress, so final conclusion can not be made.

3.3. Control Unit Complexities

Typically, the control operation of routing, scheduling, data forwarding etc. is implemented electronically and the actual data transmission takes place optically. The tasks assigned to the control unit can be generally listed as header recognition, routing control, including buffer status, input/output port status, synchronised operation of switch components, synchronisation with master clock, communication with other switching nodes, packet scheduling algorithm etc. The complexities in a control unit increase with DWDM application, where the number of input channels and data rates are very high and with number of photonic components requiring synchronised control. Fig. (5) shows a schematic of electronic control unit with typical signals to and from it. The modification of introducing TWC gates in place of SOA will also result in one less

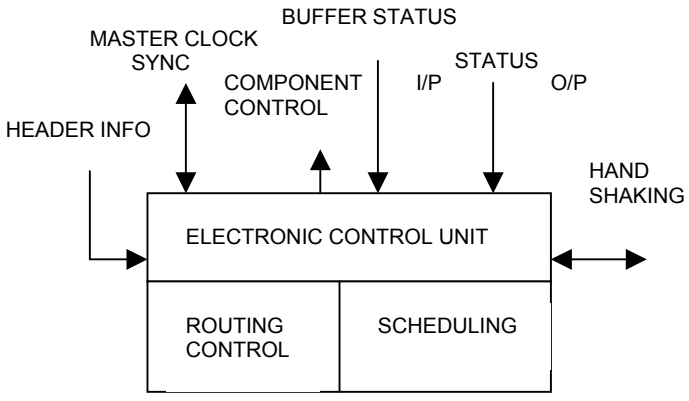


Fig.5. A general layout of signal flow and control information in an electronic control unit

dynamic component, TF, at the output block of the switch.. The attempt of introducing passive photonic component, FF, in the existing switch architecture, yet maintaining the same switching operational characteristics may ease the complexities of the control unit as there will be less active component to control and synchronise.

4. CONCLUSION

Photonic all-optical switch is widely considered as one of the techniques to utilise the enormous optical bandwidth. This paper briefly discussed photonic switching and multi-wavelength loop-buffer switch design. The application of DWDM in all-optical data transmission and packet switching may introduce the discussed limitations in existing loop-buffer switch design. Novel design modifications are proposed for these limitations. Reducing the time for read/write on same wavelength in buffer, limiting the number of active photonic components in the switch fabric to reduce the electronic control unit complexity and dynamic wavelength re-allocation may enhance the efficacy of the switch design. In our opinion, as the technology for tuneable wavelength converter is still developing, there will be tremendous improvements in its operational specifications hence further studies can be undertaken on proposed modifications.

References

1. Wen De Zhong, *IEEE Journal of Lightwave Technology,* **vol 19, No. 8**, pp 1085, (Aug 2001)
2. Shun Yao et.al., *IEEE Comm. Magazine*, pp 84, (Feb 2002),
3 David Hunter, *IEEE Journal of Lightwave Technology*, **Vol 16, No. 12**, pp 2081, (Dec 1998)
4 Rodney S. Tucker and Wen De Zhong, *IEICE Trans. Communication*, **Vol E82-B, No.2**, pp 254, (Feb 1999)
5. G Bendelli, *Proc. of ECOC'94*, pp 821, (Sep 1994),
6. G Bendelli, *OFC'94 Technical Digest*, pp 141, (Mar 1994)
7. Y N Singh, Mandar Niak, *Proc. of NCC 2002*, IIT Mumbai, pp 50, (Jan 2002)
8. Charles A. Brackett, *IEEE Journal on Selected Areas in Communications*, **Vol.8, No. 6,** pp 948, (Aug. 1990)
9. Michael S. Borella, *et.al*, *Proc. of IEEE*, **Vol. 85, No. 8**, pp 1274, (Aug 1997)
10. Mandar Naik, *Masters Thesis, Center for Laser Technology*, IIT, Kanpur, India, (Jan2002)
11. Dhawal Deshmukh, *Masters Thesis, Deptt. of Electrical Engineering*, IIT, Kanpur, India, (Jan 2000)
12. Terji Durhuus, *et.al*, *IEEE Journal of Light Wave Technology*, **Vol 14, No. 6**, pp 942, (Jun 1996)
13 Kristian E. Stubkjaer *et.al*., *IEICE Trans. Communication*, **Vol. 82-B, No.2**, pp 390, (Feb 1999)
14. Lena Wosinska and Lars Thylén, *IEEE Trans. on Communications*, **Vol.47, No.3**, pp 472, (Mar 1999)
15. Mike J. O'Mahony, *IEEE Communications Magazine*, pp 128, (Mar 2001)