Abstract—In this paper we have proposed design modifications in fiber optic loop buffer switch. This paper discusses an automatic gain controlling (AGC) scheme for the loop buffer. We have shown that by changing the position of EDFA automatic gain controlling scheme will not be required. We have utilized the availability of filter in Tunable Wavelength Converter (TWC) to reduce number of components in the buffer. Finally we replaced the combination of splitter and filter as in existing architecture by array waveguide grating (AWG) demultiplexer, which reduces the loss in the architecture. The performance evaluation of the switch is done in terms of packet loss probability and delay.

Index Terms—optical fiber, fiber loop buffer, WDM, TWC, packet switch.

I. INTRODUCTION

The demands for the higher bandwidth is ever increasing due to continuous evolution in the services. Broad acceptance of fiber-optic and photonic technology in transmission systems has led to potential opportunities for using all-optical switching. All optical switching will require optical implementation of all the switch functionalities. The control and processing logic implementations are not technically feasible. Therefore most of the optical switch architectures are hybrid in nature, that only buffering and switching of information packet is optical, while control is electronic. The important aspects of photonic packet switching [1] are control, packet routing, packet synchronization, clock recovery, contention resolution, packet buffering and packet header replacement. This paper emphasizes on the aspects of buffering. In the optical packet switching this buffering will be required when two or more packets arrives for the same destination in any time slot, i.e. WDM is not used in the input and output channels. The number of buffer wavelengths (size of memory) depends on the desired traffic throughput, packet loss probability and various component parameters [3], [4]. The packets to be buffered are converted to the wavelengths available in the buffer; if memory is full then packet cannot be stored and are lost.

II. DESCRIPTION OF THE EXISTING ARCHITECTURES

This architecture (Fig. 1) [2] consists of N tunable wavelength converters (TWC) one at each input, a recirculating loop buffer and N fixed filters, one at each output. Packets from all the inputs use WDM technology to share the loop buffer [1]. At each input only one packet can arrive in any time slot, i.e. WDM is not used in the input and output channels. The number of buffer wavelengths (size of memory) depends on the desired traffic throughput, packet loss probability and various component parameters [3], [4]. The packets to be buffered are converted to the wavelengths available in the buffer; if memory is full then packet cannot be stored and are lost.

Fig. 1. Schematic of loop buffer architecture

A. Drawbacks of the architecture

1) Absence of Gain Control

The main drawback of the existing architecture is the absence of automatic gain control (AGC). This controlling is necessary to compensate the gain variation, which arises due to the number of channels present in the loop buffer in any
time slot. This gain variation violate the condition \((\text{loss} \times \text{gain}) = 1\), which is the optimal condition to maximization \(\text{SNR}\) for the loop buffer switch [5]. Thus this variation in the gain of the amplifier reduces the maximum number of allowed circulations \((K)\) of the data at different power levels in the loop buffer. This reduction in the circulations degrades the switch performance.

2) Large Loop Losses

The total loss of the switch is very large. This large loss degrades the signal quality very quickly.

III. PROPOSED MODIFICATIONS

A. AGC Scheme

In this automatic gain control scheme (Fig. 2), a small amount of power is tapped at the both input and output end of the EDFA and by comparing them gain of the EDFA is evaluated. Gain of the EDFA is designed in such a way, when all the channels are present the loss of the loop is fully compensated by the gain of the EDFA. As the number of channels passing through the EDFA decreases, the gain of the EDFA increases and degrades the switch performance. To combat this variable attenuator is placed after EDFA, which attenuate the extra gain of the EDFA to maintain constant gain irrespective of number of channels present in the buffer. By the induction of AGC a dynamic component has been introduced. This will increase the complexities of the electronic control unit as there is a new active component to be controlled and synchronized.

![Fig. 2. Schematic of gain controlling scheme](image)

B. Shifting the position of EDFA

This AGC scheme will not be required if we shift the position of the EDFA in the loop buffer. The new position of the EDFA is shown in Fig. 3. In this scheme each channel is controlled by a separate EDFA, thus each channel will always get the gain which is equal to the loss of the loop. Other advantage is that no extra filter will be required at the output of the amplifier, because TWC is placed after EDFA which consist of tunable filter that will allow only in-band noise components to pass through it.

![Fig. 3. Schematic of loop section in the modified architecture.](image)

Hence, there is a tradeoff between the two architectures, in the first architecture (Fig. 2) control unit complexity is high as compared to second architecture (Fig. 3), but required number of EDFAs is large in second architecture as compared to first one.

C. Replacing Splitter and Filter by AWG Demultiplexer

The total loss of the loop buffer can be reduced by replacing the combination of splitter and fixed filter (Fig. 4) by the one AWG demultiplexer (Fig. 5). Because splitter divides the total power in equal parts and fixed filter select the particular wavelength. Same operation can also be obtained from AWG demultiplexer with much less insertion loss. The routing pattern of the AWG is given as \(k = (i - j) \mod N + 1\).

![Fig. 4. Output unit (Splitter with fixed filter) in the existing architecture](image)

![Fig. 5. Schematic of AWG as a demultiplexer in modified architecture](image)

If a signal arrives at wavelength \(i\), at input fiber \(j\), then signal will reach at output fiber \(k\) at the same wavelength. In the Table I, numbers indexed 1 to 4 are the inputs and 1' to 4' are the outputs. The electronic controller will tune the wavelength of the buffer TWC by using the routing pattern, given in Table I for a particular output. As we are using AWG as a demux, so all the wavelengths from 3db coupler will come at one input, of the AWG, and will appear at different output, at
different wavelength by following the routing pattern of AWG shown in Table I.

### Table I

<table>
<thead>
<tr>
<th>N</th>
<th>( \lambda_1 )</th>
<th>( \lambda_2 )</th>
<th>( \lambda_3 )</th>
<th>( \lambda_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( \lambda_1 )</td>
<td>( \lambda_2 )</td>
<td>( \lambda_3 )</td>
<td>( \lambda_4 )</td>
</tr>
<tr>
<td>2</td>
<td>( \lambda_2 )</td>
<td>( \lambda_3 )</td>
<td>( \lambda_4 )</td>
<td>( \lambda_1 )</td>
</tr>
<tr>
<td>3</td>
<td>( \lambda_3 )</td>
<td>( \lambda_4 )</td>
<td>( \lambda_1 )</td>
<td>( \lambda_2 )</td>
</tr>
<tr>
<td>4</td>
<td>( \lambda_4 )</td>
<td>( \lambda_1 )</td>
<td>( \lambda_2 )</td>
<td>( \lambda_3 )</td>
</tr>
</tbody>
</table>

### IV. Modified Architecture

The modified architecture for the loop buffer is shown in Fig. 6. In the proposed architecture loss of the output unit has been decreased significantly (Table II). The modified architecture acts as a wavelength routed switch, as compared to existing architecture, which is a broadcast and select switch.

The main advantages of the modified architecture over the existing architecture are

i. No Automatic Gain Control Scheme will be required.
ii. One component (Band Pass Filter) in the loop has been reduced.
iii. Loss of the output module is reduced significantly.

### Table II

<table>
<thead>
<tr>
<th>N</th>
<th>SPLITTER AND FILTER LOSS</th>
<th>AWG LOSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>7.8 dB</td>
<td>1.0 dB</td>
</tr>
<tr>
<td>8</td>
<td>11.2 dB</td>
<td>1.5 dB</td>
</tr>
<tr>
<td>16</td>
<td>14.6 dB</td>
<td>3.0 dB</td>
</tr>
<tr>
<td>32</td>
<td>18.0 dB</td>
<td>5.0 dB</td>
</tr>
</tbody>
</table>

V. Algorithm for Switch Operation

The switch uses \((B+N)\) wavelengths, in which \(B\) are buffer wavelengths, and \(N\) are the number of wavelengths used for direct transmission to the output bypassing the fiber loop [6]. The scheduling algorithm for the architecture is as follows:

1. All tunable wavelength converters at the inputs of the switch can be tuned to any of the \((B+N)\) wavelengths simultaneously.
2. If there are \(i\) \((1 \leq i \leq B)\) packets in the buffer for the output \(j\), where \(2 \leq b \leq \min (K, B)\) then one of them will be send to the output. If in that slot, there are one or more packets also present at the inputs for the output \(j\), then these will be buffered in the loop buffer to the extent allowed by the rules 4-5.
3. Considering the case when there is no packet in the buffer for the output \(j\), but \(m\) input lines have packets for that output. Then, one of these \(m\) packets is directly sent to output \(j\). The remaining \(m-1\) packets will be buffered in the buffer to the extent allowed by the rules 4-5.
4. Number of packets \(X_j\) in the buffer for the output \(j\) should never be greater than \(\min (K, B)\), i.e. \(X_j \leq \min (K, B)\) for \(j=1, \ldots, N\). Here \(K\) is the maximum recirculation allowed in the buffer.
5. The total number of buffer used should never be greater than \(B\), i.e. \(\Sigma X_j \leq B\).
6. Simultaneously read and write is allowed in the same slot for the same wavelength in the loop buffer.
7. If there are \(X_j\) packets in the buffer, and \(I_j\) packets at inputs then \(I_j-(K-X_j)-1\) packets will be dropped as at the end of this slot and \(X_j\) will be equal to \(K\).

VI. Simulations and Results

In this section we examine the packet loss probability, and delay performance of the switch under various load condition. This investigation is done through the computer simulation. The simulation assumes random traffic model.

1. The packet can arrive at any of the input with probability \(p\).
2. Each packet is likely to be destined to any of the output with probability \(1/N\).

In the loop buffer optical amplifier is placed to compensate the loss of the loop. This amplifier induces the ASE noise, which limits the maximum number of allowed circulations of the data in the loop buffer. Following the algorithm of the switch, the maximum number of stored packet for a particular output is \(\min (B, K)\). The maximum number of allowed circulations of the data can be calculated using mathematical model presented in [5]. In the Table III, the values of the allowed circulations at different power levels for various switch size and buffer combination are presented for the existing architecture and similar results for the modified architecture are presented in Table IV. It can be seen from the tables that as the size of switch/buffer increases, the maximum number of the allowed circulations of the data decreases. This happens because as the size of the switch increases, the loss of the architecture increases, to compensate this large loss a high gain amplifier is needed, which will introduce more noise and will reduce the SNR, and degrade the switch performance.
For the configuration of $N = 4$, $B = 4$ there will be no circulations limit, (Table III and IV) because $\min(B,K)$ is always equal to $B$. For the switch configuration of $N = 4$ and $B = 8$, the existing architecture is limited by the maximum number of allowed circulations at the power level of 1 and 2 $mW$, but the modified architecture is independent of the circulation limit. The results for packet loss probability are shown in Fig. 7 and delay results are plotted in Fig. 9. At the offered load of 0.6, packet loss probability for the modified architecture is nearly 30 times better than existing architecture at the signal power level of 1 $mW$. For the switch configuration $N = 4$ and $B = 16$, the existing architecture is limited by the maximum number of allowed circulations at all the power levels, but the modified architecture is limited at power level of 1$mW$ and 2 $mW$ only.

The results for packet loss probability are shown in Fig. 8 and delay results are plotted in Fig. 10. At the load of 0.7 packet loss probability for the modified architecture is 1000 times better than existing architecture at the signal power level of 3 $mW$. 

---

**TABLE III**

<table>
<thead>
<tr>
<th>$N$</th>
<th>$B$</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4</td>
<td>9</td>
<td>17</td>
<td>24</td>
<td>32</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>4</td>
<td>6</td>
<td>9</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**TABLE IV**

<table>
<thead>
<tr>
<th>$N$</th>
<th>$B$</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>4</td>
<td>48</td>
<td>94</td>
<td>140</td>
<td>187</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>16</td>
<td>31</td>
<td>46</td>
<td>60</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>6</td>
<td>11</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>7</td>
<td>13</td>
<td>19</td>
<td>25</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>3</td>
<td>5</td>
<td>7</td>
<td>9</td>
</tr>
<tr>
<td>16</td>
<td>16</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

For the configuration of $N = 4$, $B = 4$ there will be no circulations limit, (Table III and IV) because $\min(B,K)$ is always equal to $B$. For the switch configuration of $N = 4$ and $B = 8$, the existing architecture is limited by the maximum number of allowed circulations at the power level of 1 and 2 $mW$, but the modified architecture is independent of the circulation limit. The results for packet loss probability are shown in Fig. 7 and delay results are plotted in Fig. 9. At the offered load of 0.6, packet loss probability for the modified architecture is nearly 30 times better than existing architecture at the signal power level of 1 $mW$. For the switch configuration $N = 4$ and $B = 16$, the existing architecture is limited by the maximum number of allowed circulations at all the power levels, but the modified architecture is limited at power level of 1$mW$ and 2 $mW$ only.
VII. CONCLUSION
In this paper we have proposed a modified architecture for photonic packet switching. The performance evaluation of the switch is done through computer simulation, and it has been found that performance of the switch improves drastically in terms of packet loss probability.

VIII. REFERENCES


IX. BIOGRAPHIES

Rajiv Srivastava was born in Kanpur, (UP) in India, on Feb’ 18, 1976. He received M.Sc. degree in Physics (Solid State) from CSJM University, Kanpur (UP) in 1997 and M.Tech. degree in Laser Technology from Indian Institute of Technology, Kanpur in Dec’ 2003. Currently, he is pursuing his PhD from Indian Institute of Technology, Kanpur. His research interests are in the field of photonic packet switching and Solitons based optical networks.

Vipin Mangal was born in Gwalior (MP) in India, on Oct’ 8, 1978. He received B.E. degree in Electronics & Telecommunication Engineering from Institute of Technology & Management, Gwalior (MP) in 2002 and M.Tech. degree in Information System from Indian Institute of Technology, Kanpur in May 2006. His research interests are in the field of photonic packet switching, optical networks and signal processing.

Rajat Kumar Singh (M’2005) was born in Jaunpur, (UP) in India, on Dec’ 18, 1975. He received B.Tech. degree in Electronics & Instrumentation Engineering from Bundelkhand Institute of Engineering & Technology, Jhansi (UP) in 1999 and M.E. degree in Communication Engineering from Birla Institute of Technology & Science, Pilani (Raj) in Dec’ 2001. Currently, he is pursuing his PhD from Indian Institute of Technology, Kanpur. His research interests are in the field of photonic packet switching, telecom networking and optical networks.

Yatindra Nath Singh (M’1998) was born in Delhi in India, on Aug’ 26, 1969. He obtained B.Tech. in Electrical Engineering with honors from Regional Engineering College, Hamirpur, Himachal Pradesh in July 1991, M.Tech. in Optoelectronics & Optical Communications from Indian Institute of Technology, Delhi in December 1992 and Ph.D. from Department of Electrical Engineering, Indian Institute of Technology, Delhi in 1997. He was with the Department of Electronics and Computer Engineering, IIT Roorkee, India as faculty from Feb’97 to July’97. He is currently working as faculty in the department of electrical engineering, Indian Institute of Technology, Kanpur. He has been given AICTE young teacher award in 2002. He is a fellow of Institution of Electronics and Telecommunication Engineers (IETE), India and senior member of The Institution of Electrical and Electronics Engineers, Inc., (IEEE) USA. His academic interests include Optical Networks, Photonic packet Switching, Optical Communications, telecom networks, Network managements, E-learning systems, Open-source software development. He is actively involved in development of Open Source E-learning platform tools code-named Brihaspati.