Exact and Approximate Analytical Modeling of an FLBM-Based All-Optical Packet Switch

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***Abstract*—This paper develops both exact and approximate models for the analysis of an all-optical packet switch based on a fiber-loop buffer memory (FLBM). The switch structure and operation is based on the fully shared buffer architecture of the Research and Development in Advanced Communications in Europe—ATM Optical Switching (RACE-ATMOS) project [1], which uses individual wavelengths to store fixed-length packets in the fiber-loop buffer. An exact model of the switch has been developed [2], which can be used to determine the blocking performance of the switch and obtain both its throughput and packet loss characteristics. It has been used to study the switch performance under different loading conditions and for different values of the key design parameters of the switch. This model is difficult to use for studying large switches of this kind because of computational complexities. To tackle this problem, an approximate queuing model has also been presented, which may be used to study the performance of large switches of this kind. The results obtained by the two methods are compared to confirm that the approximate model works well under typical loading conditions of the switch.**

***Index Terms*—All-optical switch, fiber-loop buffer memory (FLBM), performance analysis, queuing analysis.**

I. Introduction

THE NEED for a broad-band integrated communication system, capable of accommodating a variety of diverse services with different bandwidths, has resulted in the evolution of Broadband Integrated Services Digital Networks (BISDN) [3]–[5]. The main requirements for these services would be high bandwidth, high speeds, and fast switching at levels that are difficult to meet using only electronic technology. Photonic technology has the capability to fulfill these requirements [6]–[9].

A. Photonic Packet Switching

Electronic packet switching converts signals from optical to electronic form before the switching function is performed. At the output interface, the signal is converted back to the optical form. In these systems, with increasing bit rates, the costs of the optical–electronic (O–E) and electronic–optical (E–O) interfaces become prohibitively high. The clock skew problem also becomes more difficult to handle. The situation is further complicated by the fact that different edge interfaces may use different formats for data transmission.

In such a scenario, one needs to find ways to reduce the cost of switching systems. One way to do this is to use all-optical packet switching with low-bit-rate headers. In this case, high-speed interfaces will only be needed at the edges of the network. Once converted to optical form, the payload will remain as it is. This will make it possible to achieve higher bit rates in the optical fiber, leading to better utilization of fiber capacity. This will also help in resolving the clock skew problem. The term "all-optical" generally implies that the data portion of a packet remains in optical format all the way, from the source to the destination. The capability of photonic switches (when used in conjunction with optical fibers) to maintain data in all-optical format from the source to the destination allows concurrent transport of various data rates (data-rate transparency) and formats (format transparency). Although the data remains optical, both optical and optoelectronic techniques are needed to implement packet routing functions.

The key functions needed for implementation and operation of photonic packet switches are timing recovery and packet synchronization, packet header replacement, packet buffering, and packet routing [11]. A packet will have a header and a payload. The header contains routing and other control information. The header has to be processed at each switch, and hence, it is desirable that the header has a relatively low fixed bit rate suitable for electronic processing (say, less than 10 Gb/s). The payload (data) itself may have a variety of bit rates as per mutual agreement between source and destination. Using packets of fixed length will significantly simplify the implementation of packet contention resolution, packet buffering, packet routing, and packet synchronization [11].

In this paper, we focus on the buffering aspects. We also assume that all packets are synchronized at the inputs of the switch. Buffering of packets somewhere within the switch is needed to prevent packet contention. The difficulty in implementing fully functional photonic equivalents of electronic random access memory (RAM) makes clocked optical buffering and synchronization difficult. One possible approach is to use a fiber delay line either in recirculating or traveling configurations. In these delay elements, once the signal enters the fiber, it will come out of it after a fixed interval of time [12].

In this paper, we have analyzed the performance of a photonic packet switching architecture, which is based on the multiwavelength fiber-loop memory proposed in the Research and Development in Advanced Communication in Europe-ATM Optical switching (RACE-ATMOS) project [2].

In this architecture, optical buffers recirculate packets, instead of holding them statically in memory. Multiple packets are stored in a single fiber loop using the wavelength-division multiplexing (WDM) technique. The fiber loop attenuates the

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signals as it recirculates. Hence, optical amplifiers (OAs) are used in the loop to amplify the signal, which adds amplified spontaneous emission (ASE) noise to the signal. Because of the accumulation of this noise, the depth of the fiber–loop memory cannot exceed a certain number of recirculations. This implies that we cannot save more than a certain number of packets for any particular output. The erbium-doped fiber amplifier (EDFA) commonly used has limited gain-bandwidth product. Hence, use of more wavelengths in the fiber-loop buffer memory (FLBM) leads to increased crosstalk. This would limit the total number of wavelengths that can be used in the fiber loop. Both these considerations imply that photonic switches will need algorithms that use buffers efficiently, in accordance with the inherent limitations of the switch.

The architecture and mode of operation of the switch under consideration are discussed in Section II. The modeling of the switch is done for two conditions. In the first condition, reading and writing on a particular wavelength cannot be done in the same time slot—this is referred to as a *Type I switch*. The other condition is one in which a particular wavelength can be read and written in the same time slot. This is referred to as a *Type II switch*.

An exact computational model has been developed for both types of switches in Section III. These models have been used to determine the packet loss performance of the switches and obtain their throughput. Then, the exact models have been used to study the performance of the switches under different loading conditions and for different values of the key design parameters of the switches. Computational complexities make it difficult to use the exact model to study large switches of this kind.

To tackle this problem, we also present an approximate queuing approach in Section IV that may be used for large switches of this kind. The results obtained by the two methods are compared to confirm that the approximate models work well under typical loading conditions of the switch. The conclusions and some suggestions for future work are presented in Section VI.

II. Switch Architecture

In general, a photonic switch based on a multiwavelength fiber-loop memory switching fabric consists of two main functional blocks: link interfaces and switching fabric [10].

A. Switch Fabric Architecture

The switch fabric architecture is shown in Fig. 1. The multiwavelength fiber-loop memory in the switch fabric operates in WDM mode. The fiber-loop length is equal to one cell period. The fabric shown in Fig. 1 may be considered as a basic matrix, which can be used to build large dimensional multistage switch configurations. This is characterized by N input and N output ports. The switch fabric consists of the following four functional blocks:

1) the cell-encoder block incorporating N fast tunable optical wavelength converters;
2) the buffering block consisting of a multiwavelength fiber loop used in case of contention;
3) the output block consisting of tunable filters;

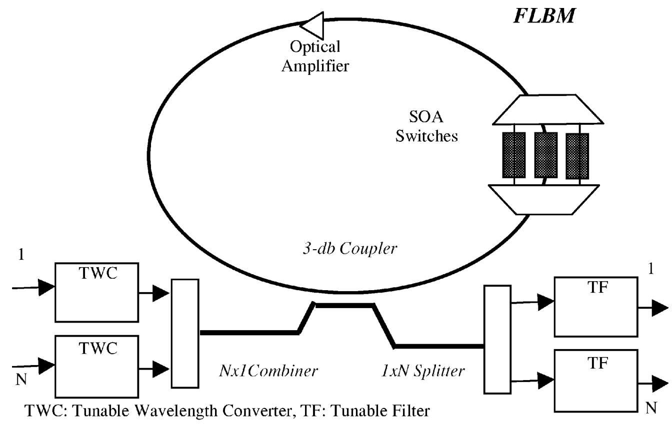

Fig. 1. All-optical FLBM packet switch.

4) the switch control block implementing the switching algorithm by controlling the tunable wavelength converters (TWCs), semiconductor optical amplifier (SOA) switches, and tunable filters.

The main components of the switch are a 3-dB directional coupler, $1 \times N$ splitter and $N \times 1$ combiner, multiplexer/demultiplexer, SOAs, EDFA, TWCs, and tunable filters.

B. Operation of the Switch

The following have been assumed for switch operation.

- Packets coming at the switch inputs are of fixed size.
- The operation of the switch fabric [1], [12] is synchronous on a packet-period basis. (Synchronization of packets are performed by the link processor unit.)
- There are delay elements at the inputs of the switch fabric, which provide delay so that the processing of the headers of incoming packets by the switch controller is complete before the packets enter the encoder block.
- The switch uses $(B + N)$ wavelengths. Here, B is the number of wavelengths corresponding to B SOAs in the fiber loop, and N is the number of wavelengths that are used in case of direct transmission to the output bypassing the fiber loop.
- All-optical wavelength converters at the inputs and tunable filters at the outputs of the switch can be tuned to any of the $(B + N)$ wavelengths instantaneously.

Consider the situation where there are no packets in the buffer for a particular output in a time slot. If more than one packet arrives at the inputs in the same slot and are destined for the same output, then one of the incoming packets is selected for direct transmission using one of the N direct wavelengths. The controller has to make sure that each input–output pair involved in direct transmission uses different wavelengths in the same time slot. The wavelength of each of the remaining packets is tuned to one of the free wavelengths (i.e., using any wavelength that is not currently used to store a packet in this time slot) in the fiber-loop memory, if sufficient free wavelengths are available. Otherwise, the controller will drop the packet. The FLBM stores packets by allowing the corresponding optical signal to recirculate in the loop. Packets from the FLBM may either continue in the FLBM or may be directed to an output port. In the latter case, the corresponding SOA is turned OFF, erasing the packet from the loop. The packets in the fiber-loop memory are kept recirculating (stored) in the WDM loop memory by activating the corresponding SOA, in case they are required to be delayed (i.e., buffered).

At the input of the memory loop, half of the power enters the loop and half goes toward the outputs through the passive coupler. Therefore, when the contention is resolved, the packet is routed to the destination link simply by properly tuning the corresponding output tunable filter to the corresponding wavelength in the fiber loop. In this fabric, one cannot erase and write into the same buffer (i.e., wavelength in the fiber loop) in the same time slot.

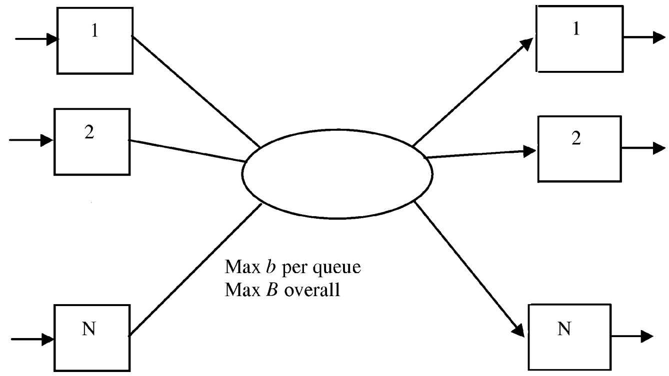

Fig. 2. Queuing structure of the packet switch.

III. Computational Model of the Switch

In this section, a queuing model and a computational approach for calculating the probability of blocking for the photonic switch of Section II has been presented. The modeling of the switch is done for two conditions. The first condition is one in which reading and writing on a particular wavelength cannot be done in same time slot. This is referred as a *Type I switch*. The other condition is one in which a particular wavelength can be read and written into in the same time slot. This is referred to as a *Type II switch* and can be implemented by suitably modifying the architecture.

A. Switching Architecture (Type I Switch)

In a Type I switch, while the packet is being read, it is also erased. Hence, one cannot use the same wavelength for storing a new packet, while a packet is being read. The EDFAs and SOAs in the fiber loop will add noise to the optical signal (corresponding to a packet stored in the FLBM) with every recirculation. Since, ASE noise accumulates with an optical signal, after a certain number of recirculations, the optical signal will become unusable. Consequently, the number of recirculations of a packet in such a loop will be limited. It is assumed that only up to b recirculations are allowed for a packet stored for a particular output. Hence, the number of packets that may possibly be buffered for a particular output is also limited to b. Packet loss would occur whenever this limit is exceeded. In the switch, B is the total number of wavelengths available for packet storage in the FLBM. Hence, this is also the total number of buffers available for sharing between all the N outputs of the switch. Fig. 2 shows the equivalent discrete queuing model for this $N \times N$ all-optical FLBM packet switch.

B. The Traffic Model

Here, we refer to the traffic as seen by the input ports of the switching fabric. Two random processes describe the traffic model. The first governs the arrival of packets in each time slot. The second process describes the distribution by which arriving packets choose their destination ports. Uniform traffic is assumed with packets arriving at each input port of the switch according to independent and identically distributed (iid) Bernoulli processes with parameter p $(0 < p \leq 1)$. Thus, p represents the input load at each input port of the switching fabric. Further, incoming packets choose to go to any of the N output ports with equal probability, independent of all other packets (i.e., it chooses a particular output with probability $1/N$). This assumption is justified because it has been observed that the traffic arriving at the core switching nodes is less bursty than the traffic arriving at access nodes. This is due to the inherent smoothening that takes place when independent bursty packet streams are queued and then released at a given rate (the link service rate) into the network. Furthermore, the subsequent stages cause the traffic to become even less bursty [5].

1) Modeling of a Type I Switch: For an $N \times N$ switch with buffer constraints b and B mentioned previously, the routing rules followed by the switch controller are as follows.

1) If there are i $(1 \leq i \leq b)$ packets in buffer for output j, then one of them will be sent to the output. If, in that slot, there are one or more packets also present at the inputs for output j, then these will be buffered in the FLBM, to the extent allowed by rules 3–5.
2) Consider the case when there are no packets in the buffer for output j, but K input lines have packets for that output. Then, one of these K packets is directly sent to output j. The remaining $K-1$ packets will be buffered in the FLBM to the extent allowed by rules 3–5.
3) Number of packets x_j in buffer for output j should never be greater than b, i.e., $x_j \leq b$ for $j = 1, \ldots, N$.
4) The total number of buffers used should never be greater than B, i.e., $\sum x_j \leq B$.
5) The buffers are such that simultaneous read and write is not allowed in the same slot for the same wavelength in the FLBM.
6) Depending on the current buffer state and the offered input pattern, one or more of the input packets may be lost. The switch controller adopts the rule of dropping packets for the lower indexed output lines first (from the input pattern), whenever needed. (Other approaches, such as dropping packets of the highest indexed output first or dropping randomly, may also be studied.) Dropping lower indexed output lines first may reduce computational load by reducing the number of possible transitions.
7) In addition, the controller is expected to maintain first-come-first-serve (FCFS) flow between inputs and corresponding outputs for all packets that are not dropped.

If $B \geq [(N-1)b+N]$, then the switch is fully output-queued with the output queue length for each output limited to b, the recirculation limit. The FLBM buffer will only be able to store up to $(N-1)b$ packets when equality is satisfied [2].

Theorem 3.1: For a Type I switch, if $B \leq (N-1)b + N$ and $B > N$, then the maximum number of packets that can be stored in the FLBM buffer would be either a) $(B-y-1)$ if $[(B-N) \bmod b] + N - y - 1 \leq b$ or b) $\{B-y-(k+1)\}$, if $(k+1)b \geq [(B-N) \bmod b] + N - y - 1 > kb$, where $y = \lfloor (B-N)/b \rfloor$ and k is an positive integer.

Proof: Let the switch be in a state such that $(B-N)$ buffers have been occupied at the end of the previous slot. This assumption makes sure that all the incoming packets are stored or transmitted directly and that none of them is dropped. This will lead to a buffer state where maximum packets are stored. After reaching the maximum buffer occupancy state, even if N packets arrive, packets that are transmitted in that slot and that are stored in the buffer will be equal, thereby maintaining maximum packets in the buffer. In order to store maximum packets in the buffer and minimize the packets to be transmitted, all the stored packets must be destined for the minimum possible number of outputs. Consequently, the number of outputs that can have all b packets stored in the buffer is $y = \lfloor (B-N)/b \rfloor$. This implies that y packets will be required to keep all those outputs in the same state. Assume that the rest of the packets (i.e., $[(B-N) \bmod b]$ packets) are for the next output. We can then have additional $N-y-1$ packets in the next slot. If $[(B-N) \bmod b] + N - y - 1 \leq b$, then the maximum number of packets that can be stored equals $(B-N)+(N-y-1) = (B-y-1)$. The "-1" term accounts for the packet that will be passed out of the last output in the current time slot.

If $(k+1)b \geq [(B-N) \bmod b] + N - y - 1 > kb$, then the maximum number of packets that can be stored equals $(B-N)+\{N-y-(k+1)\} = (B-y-k-1)$. The "$-(k+1)$" term is due to the $k+1$ packets that would be passed out to the one previous output and k new outputs in that time slot.

2) Analytical Model of the Type I Switch: In any given time slot, we define $\boldsymbol{I} = (I_1, I_2, \ldots, I_N)$ to be the input pattern and $\boldsymbol{O} = (O_1, O_2, \ldots, O_N)$ as the buffer state of the $N \times N$ switch. Here, $I_i =$ the total number of packets arriving at all the input lines in that slot that are destined for output i, and $O_j =$ the number of packets destined for output j presently stored in the FLBM buffer. For this arrival model, as described previously, one can calculate the probability $P(\boldsymbol{I})$ for any feasible input pattern $\boldsymbol{I}$. For example, for a 2×2 switch, we have $P\{I(0,0)\} = (1-p)^2$, $P\{I(1,1)\} = \frac{p^2}{2}$, $P\{I(1,0)\} = P\{I(0,1)\} = (1-p)p$, and $P\{I(0,2)\} = P\{I(2,0)\} = \frac{p^2}{4}$.For an $N \times N$ switch, similar expressions for $P(\boldsymbol{I})$ may be derived for any $\boldsymbol{I}$.

The set of feasible buffer states $\boldsymbol{O}$ are obtained by applying the routing rules given previously, to the switch for all possible input patterns $\boldsymbol{I}$ applied to all possible initial buffer states. This leads to a Markov chain. It is done using a computer program to build up an exhaustive table of all possible buffer states [2].

This procedure also builds a table for the number of packets lost, $n_{\text{lost}}(\boldsymbol{I}, \boldsymbol{O})$, for all combinations of input patterns $\boldsymbol{I}$ and initial buffer states $\boldsymbol{O}$. In dropping the packets, a convention to drop packets for the lower output-index values first is followed. Ideally, in consideration of fairness, the packets should have been dropped at random. However, that would have made the analysis difficult and has not been used here, since a significant effect on performance results is not expected. Using this, the probability of packet loss P_L for the $N \times N$ switch with parameters b and B and input probability p will be given by

$$P_L = \frac{\sum\limits_{\forall \boldsymbol{O}} \sum\limits_{\forall \boldsymbol{I}} n_{\text{lost}}(\boldsymbol{I}, \boldsymbol{O}) P(\boldsymbol{I}) P(\boldsymbol{O})}{Np}. \tag{1}$$

In (1), $P(\boldsymbol{O})$ will be found by solving the appropriate balance equations for the state. The process of writing the balance equations has been automated (because of the large number of state variables involved) by writing a computer program that generates all the global balance equations using the routing rules given previously. These balance equations may then be directly solved using MATLAB or any other similar package. As an example, the *global balance equation* for the buffer state (1,1) in a 2×2 switch for $b = 2$ and $B = 3$ is given by

$$\begin{aligned} &P\{\boldsymbol{I}(2,0)\}P\{\boldsymbol{O}(0,2)\} + P\{\boldsymbol{I}(0,2)\}P\{\boldsymbol{O}(2,0)\} \\ &\quad = P\{\boldsymbol{O}(1,1)\}[P\{\boldsymbol{I}(0,0)\} + P\{\boldsymbol{I}(0,1)\} + P\{\boldsymbol{I}(1,0)\} \\ &\qquad + P\{\boldsymbol{I}(1,1)\} + P\{\boldsymbol{I}(0,2)\} + P\{\boldsymbol{I}(2,0)\}]. \end{aligned} \tag{2}$$

Note that some of these transitions will involve packet loss. For example, if the input pattern (0,2) is applied to the buffer state (1,1) in this switch, then one packet will be lost, and the buffer state reached will be (0,1). Note that this happens because simultaneous read/write on an FLBM wavelength is not allowed.

C. Switching Architecture of a Type II Switch

In order to determine the improvement possible if erasing and writing is feasible in the same slot, a *Type II* Switch is also considered. We assume the same value of recirculation limit b for both the *Type I* Switch and the *Type II* Switch. We assume that B is the total number of wavelengths available for packet storage in the FLBM and are shared between all the N outputs of the switch. Its queuing model may be represented by Fig. 2. The traffic model for this switch is the same as that for a Type I switch.

The recirculation limit is modeled by the maximum number of packets that can be stored for an output, i.e., b. Thus, b slots are the maximum delay that a packet can have. As before, the number of wavelengths in the fiber-loop memory will be limited to B. If $B \geq (N-1)b$, then the switch reduces to a simple output-queued one with the queue length for any output limited to b with B common buffers for storing packets in the case of contention. (In this switch, we have an $(N-1)b$ wavelength, instead of an $[(N-1)b+N]$, because read/write can be done on a wavelength in the same time slot.) For $B < (N-1)b$, the switch will be modeled as a shared buffered switch with constraint b on the maximum logical queue length for any particular output.

1) Modeling of a Type II Switch: The Type II switch is modeled similarly to the Type I switch. For buffer constraints b and B, the routing rules followed by the switch are the same as that for a Type I switch, except that reading and writing in a buffer/wavelength is allowed in the same time slot.

2) Computational Model of "Type II Switch": The computational modeling for a Type II switch is done in exactly the same way as that for a Type I switch, except that the modified routing rules stated previously are used to generate the global balance equations for the switch. The other difference lies in the calculation of blocking probability. The number of packets lost $n_{\text{lost}}(I, O)$ for a specific combination of the input pattern I and the buffer state O is calculated keeping in mind the modified routing rules. Using this, the probability P_L of packet loss for the $N \times N$ switch with parameters b and B and input probability p is found using (1).

IV. Approximate Modeling of the Switch

In Section III, we have described the queuing model for the switch and an exact method for its analysis. This method becomes too complex to solve conveniently, as the size of the switch increases. This is because the number of buffer states increases rapidly with increasing switch size. Consequently, the number of simultaneous equations to be solved to get the probabilities of the buffer states also increases, making this approach difficult to follow for large switches. In this section, we present an approximate queuing model for both the Type I and the Type II switch, which can significantly simplify the analysis for large switches.

A. Approximate Queuing Model for a Fully Output-Queued Switch

To motivate the approximate-queuing-model-based analysis of this switch, consider the fully output-queued switch (such that b packets can be stored at each output). To analyze this, consider a discrete time queue with deterministic service times (equal to the packet duration) and batch arrivals and assume that packet arrivals on the N input lines are governed by independent and identical Bernoulli processes. In any given time slot, the probability that a packet will arrive on a particular input is p. Each packet has an equal probability $1/N$ of going to any given output, and successive packets are stastistically independent.

Considering a particular output queue, we define the random variable A as the number of packets arriving at the tagged queue during a given time slot. It follows that A has a binomial distribution with individual probabilities given by [13]

$$\begin{aligned} a_i =& P_r|_{A=i} = {}^N C_i \left(\frac{p}{N}\right)^i \left(1-\frac{p}{N}\right)^{N-i} \\ i =& 0, 1, 2, \ldots, N. \end{aligned} \tag{3}$$

Its probability generating function $A(z)$ may be expressed as

$$A(Z) = \sum_{i=0}^{N} Z^i a_i = \left(1 - \frac{p}{N} + Z\frac{p}{N}\right)^N. \tag{4}$$

If we now assume that the tagged queue can store, at most, b packets (i.e., the maximum queue length at an output), then the state transition diagram of this queue will contain only $b+1$ buffer states, i.e., $O(0), O(1), \ldots, O(b)$. The probabilities of all the buffer states for any output queue are solved by writing and solving the corresponding balance equations. Let the buffer states have probabilities $P\{O(0)\}, P\{O(1)\}, \ldots, P\{O(b)\}$, where $P\{O(j)\}$ is the probability of j packets in the buffer. Then, the probability generating function of the number of packets in the buffers may be written as

$$P(Z) = \sum_{i=0}^{b} P\{O(i)\}Z^i. \tag{5}$$

Since there are N outputs, we may represent the probability generating function of the number of packets in queue in each of them as $P(Z_1), P(Z_2), \ldots, P(Z_N)$. The probability generating function of the total buffers occupied in the switch can be written as

$$P_{\text{total}}(Z_1, Z_2, \ldots, Z_N) = P(Z_1) \times P(Z_2) \times \cdots \times P(Z_N) \tag{6}$$

assuming the queues to be independent.

Note that (5) represents the probability generating function of the buffer states for a fully output-queued switch such that, at most, b packets can be stored at each output. The powers of $Z_1, Z_2, \ldots, Z_N$ represent the buffer states of the switch, and their coefficients equal the probability of that buffer state.

B. Approximate Queuing Model for Type I Switch

It should be noted that in a Type I switch, no more than B buffers may be occupied in any time slot. The number of packets that may be stored is actually less than B, since reading and writing in the same time slot is not allowed in a Type I switch. To find the $P_B(Z_1, Z_2, \ldots, Z_N)$ considering the limitation on total buffer in a Type I switch, approximations may be done in two heuristic ways, referred to as "Method I" and "Method II."

1) Method I: Renormalization: This procedure of finding $P_B(Z_1, Z_2, \ldots, Z_N)$ may be summarized as follows.

- Step 1) Find $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$ by retaining the terms in (6) that constitute the set of feasible buffer states and omitting the rest from the expression of $P_{\text{total}}(Z_1, Z_2, \ldots, Z_N)$.
- Step 2) Sum up all the coefficients of terms in the expression of $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$.
- Step 3) Divide each of the coefficients of $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$ by the sum obtained in Step 2 and denote the expression obtained as $P_B(Z_1, Z_2, \ldots, Z_N)$.

The probability of any input pattern is found in the same way as explained previously. The number of packets lost $n_{\text{lost}}(I, O)$ for a specific combination of the input pattern I and the buffer state O may be calculated considering the routing rules. Using this, the probability P_L of packet loss for the $N \times N$ switch with parameters b and B and input probability p is then determined from (1).

2) Method II: Adding the Residual Probability Equally to the Buffer States at the Boundaries: The procedure of finding $P_B(Z_1, Z_2, \ldots, Z_N)$ may be summarized as follows.

- Step 1) Find $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$ by retaining the terms that constitute the set of feasible buffer states and omitting the rest from the expression of $P_{\text{total}}(Z_1, Z_2, \ldots, Z_N)$.

Step 2) Sum up all the coefficients of terms in the expression of $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$ and denote the sum by *sum_coefficient*. Find 1-*sum_coefficient* and denote this by diff.

Step 3) Find the number of buffer states in $P_{\text{mod}}(Z_1, Z_2, \ldots, Z_N)$ where the total number of packets is equal to the maximum value given by Theorem 3.1 and denote it as X.

Step 4) Add (diff/X) to the coefficient of each of these buffer states at the boundary and denote the final expression obtained as $P_B(Z_1, Z_2, \ldots, Z_N)$.

C. Approximate Queuing Model for Type II Switch

For the approximate-queuing-model-based analysis of a Type II switch, we proceed in a manner similar to that followed for a Type I switch. This involves calculating $P_{\text{total}}(Z_1, Z_2, \ldots, Z_N)$, i.e., the probability generating function of the buffer states for an $N \times N$ fully output-queued switch, as explained previously. The maximum number of packets that can be stored is equal to B, since reading and writing in a buffer in the same time slot would be allowed in a Type II switch. The approximation may be done using the approach of either Method I or Method II, as given for the Type I switch.

The coefficients of $P_B(Z_1, Z_2, \ldots, Z_N)$ give the probabilities of their respective buffer states O. The main difference lies in the calculation of blocking probability. The number of packets lost $n_{\text{lost}}(I, O)$ for a specific combination of the input pattern I and the buffer state O is calculated following the routing rules for the Type II switch. The probability of packet loss P_L for the $N \times N$ switch with parameters b and B and input probability p may then be found using (1).

V. RESULTS

A. Type I Switch

The approach described previously has been used to study the performance of the $N \times N$ FLBM-based Type I switch. The basic performance result that is needed to characterize the switch is the probability of packet loss P_L. Its dependence on various parameters for a Type I switch has been shown in Figs. 3 and 4. Fig. 3 shows that the performance of the switch is similar to that of a fully output-queued switch with much smaller B (i.e., when $B < N + (N-1)b$). Note that using fewer wavelengths will make the fabrication of FLBM easier. We have observed similar trends for a 2×2 switch with $b = 4$ and a 6×6 switch with $b = 2$. Similar results were reported by us in [2]. As expected, the loss increases with increasing traffic, i.e., increasing values of p. This is evident from the results of Fig. 4. Fig. 5 in [2] shows P_L as a function of the individual buffer limit b. It was observed that P_L reduces with increasing b up to a certain value. Thereafter, P_L does not reduce significantly with an increase in b. For a given value of B and p, this threshold value of b should be used as the value for which P_L reaches a desirably low value. For example, when $p = 0.7$ and $B = 11$, b should be 8.

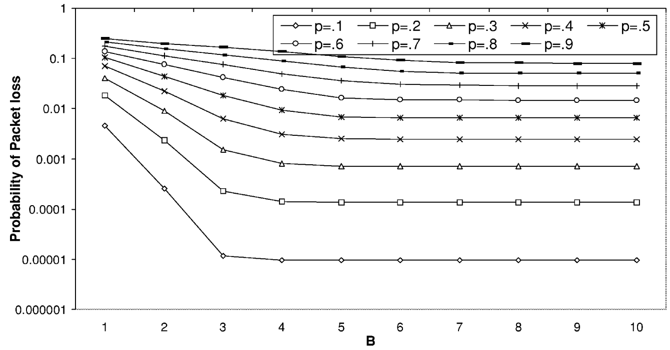

Fig. 3. Probability of packet loss versus $B(b = 2)$ for a 4×4 Type I switch.

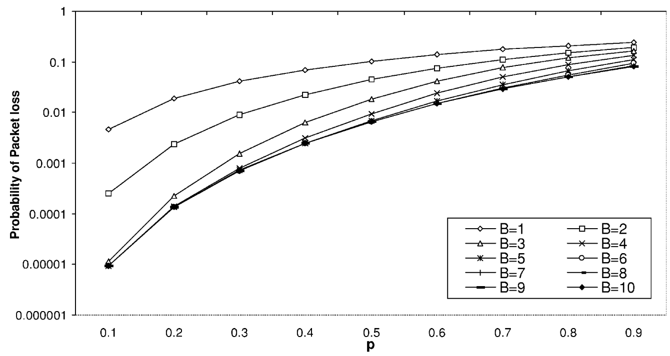

Fig. 4. Probability of packet loss versus $p(b = 2)$ for a 4×4 Type I switch.

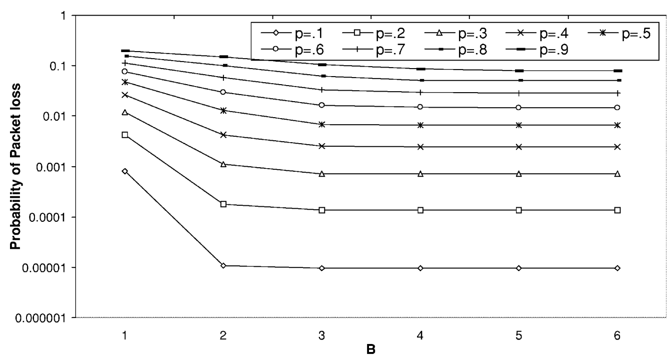

Fig. 5. Probability of packet loss versus $B(b = 2)$ for a 4×4 Type II switch.

B. Type II Switch

The approach described in Section III has been used to study the performance of the $N \times N$ FLBM-based Type II switch. The probability P_L of packet loss and its dependence on various parameters for a Type II switch is shown in Figs. 5–7. It is again observed from Fig. 5 that even when the total number of wavelengths B (required in the FLBM) is much smaller than the *fully output queued* limit of $(N-1)b$ the switch still performs as well as the fully output-queued switch. Consequently, fewer wavelengths are needed for fabrication of the FLBM in the Type II switch with acceptable performance. The P_L increases with increasing values of p. This is evident from the results of Fig. 6.

Fig. 7 indicates that for a given value of B (and p), increasing b improves the performance of the switch. Hence, the FLBM amplifiers, etc., should be low-noise ones so that b will be as high as possible.

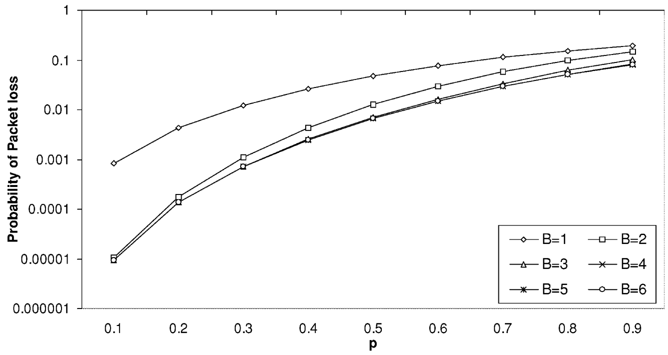

Fig. 6. P_L versus $p(b = 2)$ for a 4 × 4 Type II switch.

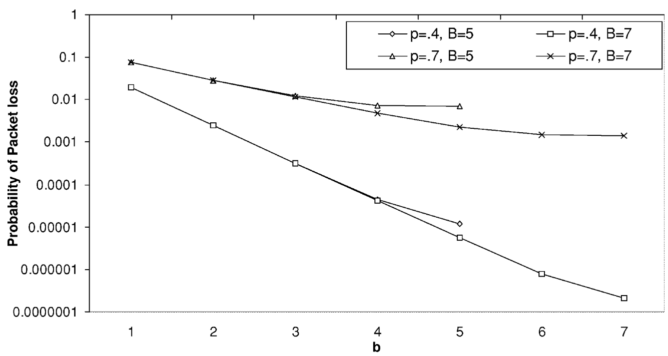

Fig. 7. Probability of packet loss versus b for a 4 × 4 type II switch.

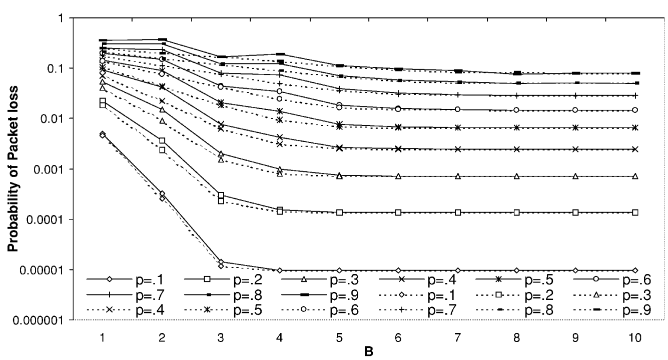

Fig. 8. Probability of packet loss versus $B(b = 2)$ foa 4 × 4 Type I switch. Solid line: Approximate Method 1. Dotted line: Exact analysis.

C. Approximate Models for Type I Switch

The switch is analyzed applying the procedure described in Section IV, and the results are compared with those obtained by our exact analytical procedure. The results obtained by the two approximate models have also been compared with each other.

Fig. 8 compares the results of exact analysis with that of "Method I." In this figure, the dotted lines give the results obtained by exact analysis, while the bold ones are the results obtained using the approximation of "Method I." Fig. 9 compares the results of exact analysis with that of "Method II" for a Type I switch. These results show that for low p and higher values of B, the results of both the approximate models match closely with those obtained by exact analysis. For higher value of p and low values of B, the results tend to deviate somewhat from those obtained by exact analysis. This would be the case if the switch was highly loaded and/ or very few wavelengths are available

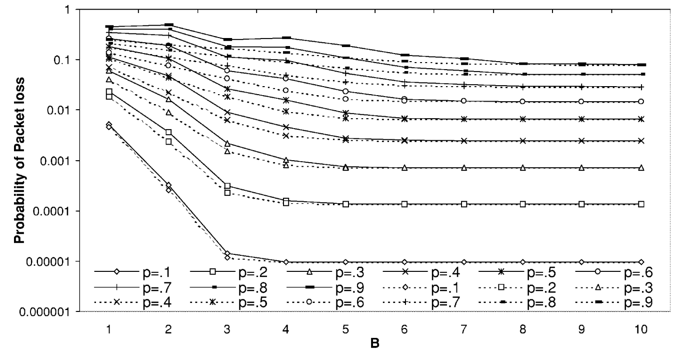

Fig. 9. P_L versus $B(b = 2)$ for a 4 × 4 Type I switch. Solid line: Approximate Method II. Dotted line: Exact analysis.

for buffer storage in the FLBM switch. Note that, either way, this will not be a desirable point of operation for such a switch. We have also observed that when the value of b increases for a fixed size of the switch, the results obtained using the approximate models tend to approach closely to the exact results.

It should also be noted from Figs. 8 and 9 that P_L obtained with the approximation of Method I is less than that using Method II for low values of B and high p. This is expected, since in Method II, it is only the probability of the boundary states that are increased. This will lead to an increase in the probability of packet loss, as the boundary states are the ones that will cause maximum loss of packets. The results for both the models match closely for low probabilities of packet arrivals and high values of B.

Note that, for low values of B and high probabilities of packet arrival, both the approximate models lead to higher probabilities of blocking than the actual values obtained from an exact analysis. Considering this, Method I may be considered a better approximation than Method II for modeling the Type I switch, i.e., Method I will give results that are closer to the actual values.

D. Approximate Models for Type II Switch

Fig. 10 compares the results of exact analysis with that of Method I. Fig. 11 compares the results of exact analysis with that of Method II for a Type II switch. Fig. 10 shows that for low probabilities of arrival and higher values of B, the results of approximate Method I match closely with those obtained by exact analysis. For high p and low values of B, the results tend to deviate somewhat from the values obtained by exact analysis. For the approximation of Method II (Fig. 11), the results tend to match closely with the exact results for all probabilities of packet arrival and B. Similar trends were observed for higher values of b.

It should also be noted from Figs. 10 and 11 that the probability of packet loss for Method I is less as compared with the Method II approximation for low values of B and higher p. This is expected, since in Method II, it is only the probability of boundary states that are increased. This will therefore show an increase in the probability of packet loss, since the boundary states are the ones where packets are more likely to be lost. This implies that, for modeling a Type II switch, the approximation of Method II is a better choice over the whole range of parameters b, B, and p.

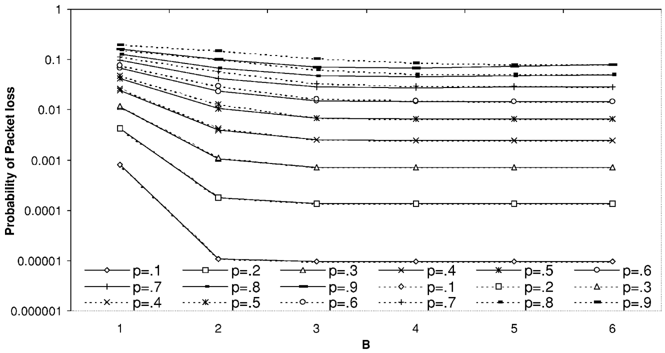

Fig. 10. Probability of packet loss versus $B(b = 2)$ for a 4×4 Type II switch Solid line: Approximate Method 1. Dotted line: Exact analysis.

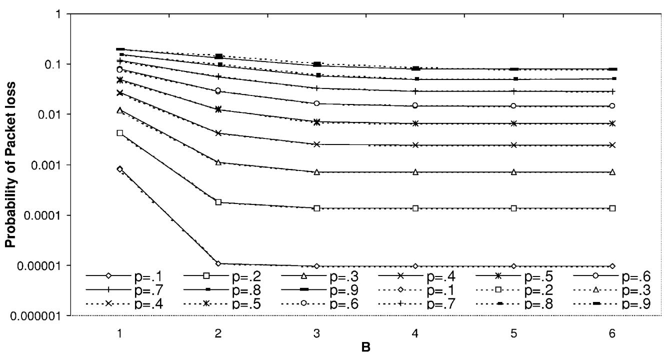

Fig. 11. Probability of packet loss versus $B(b = 2)$ for a 4×4 Type II switch. Solid line: Approximate Method 2. Dotted line: Exact analysis.

VI. Conclusion

This paper analyzes an all-optical packet switch based on multiwavelength fiber-loop memory to study its performance in detail. Based on the switch architecture, an exact analytical model has been developed. This exact model is difficult to use for study of a large switch of this kind because of computational complexities. To tackle this, two simpler approximate queuing models were presented along with the results to confirm their applicability under typical loading conditions.

For a Type I switch, it is observed that, even when the total number of wavelengths B (required in the FLBM) is much smaller than the fully output-queued limit of $[N + (N - 1)b]$, the switch still performs as well as the latter. This can be done, to a large extent, without compromising the overall performance of the switch. Results indicate that, for a given value of B (and p), increasing b beyond a threshold value may not provide any significant further improvement. Still, however, the FLBM amplifiers should be low noise so that b will be as high as possible. Similar performance trends are also observed in a Type II switch.

In a Type I switch, the results show that, for low probability of packet arrival and for higher values of B, the results of both the approximate models match closely with those obtained by exact analysis. For high probability of packet arrivals and for low values of B, the results tend to deviate from those obtained by exact analysis. It should also be noted that the probability of packet loss obtained with the approximate Method I is less than the one obtained using Method II for low values of B and high P. The results for both the models match closely for low P and high values of B.

Note that both approximate models lead to higher probabilities of blocking than the actual values obtained from an exact analysis, for low values of B and high P. Considering this, Method I may be considered a better approximation than Method II for modeling the Type I switch, i.e., Method I will give results that are closer to the actual values. In a Type II switch, the results of the approximate Method I match closely with those obtained by the exact analysis for low p and for higher values of B. For high P and for low values of B, the results tend to deviate somewhat from the values obtained by exact analysis. For the approximation of Method II, the results tend to match closely with the exact results for all p and B. This implies that for modeling a Type II switch, the approximation of Method II is a better choice over the whole range of parameters b, B, and p.

References

[1] F. Masetti *et al.*, "High speed, high capacity ATM optical switches for future telecommunication transport networks," *IEEE J. Select. Areas Commun.*, pp. 979–996, June 1996.

[2] A. Kushwaha, S. K. Bose, and Y. N. Singh, "Analytical modeling for performance studies of an FLBM—Based all-optical apcket switch," *IEEE Commun. Lett.*, vol. 5, pp. 227–229, May 2001.

[3] H. Ahmadi and W. E. Denzel, "A survey of modern high-performance switching techniques," *IEEE J. Select. Areas Commun.*, pp. 1091–1103, Sept. 1989.

[4] M. de Prycker, *Asynchronous Transfer Mode: Solution for Broadband ISDN*. Englewood Cliffs, NJ: Prentice-Hall, 1995.

[5] R. Y. Awdeh and H. T. Mouftah, "Survey of ATM switch architectures," *Communication Networks ISDN Syst.*, vol. 27, pp. 1567–1613, Nov. 1995.

[6] E. Nussbaum, "Communication network needs and technologies—A place for photonic switching?," *IEEE J. Select. Areas Commun.*, pp. 1036–1043, Aug. 1988.

[7] P. E. Green Jr., *Fiber Optic Networks*. Englewood Cliffs, NJ: Prentice-Hall, 1993.

[8] R. Rajiv and K. N. Sivarajan, *Optical Networks: A Practical Perspective*. San Francisco, CA: Morgan Kaufmann, 1998.

[9] D. J. Blumenthal *et al.*, "Photonic packet switches: Architectures and experimental implementations," *Proc. IEEE*, pp. 1650–1667, Nov. 1994.

[10] R. S. Tucker and W. De Zhong, "Photonic packet switching: An overview," *IEICE Trans. Communication*, pp. 254–264, Feb. 1999.

[11] R. F. Kalman, L. G. Kazovsky, and J. W. Goodman, "Space division switches based on semiconductor optical amplifiers," *IEEE Photon. Technol. Lett.*, vol. 4, pp. 1048–1051, Sept. 1992.

[12] D. K. Hunter *et al.*, "Buffering in optical packet switches," *J. Lightwave Technol.*, pp. 2081–2094, Dec. 1998.

[13] M. J. Karol, M. G. Hluchyj, and S. P. Morgan, "Input versus output queueing on a space-division packet switch," *IEEE Trans. Commun.*, vol. COM-35, pp. 1347–1356, Dec. 1987.

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