Amplifier Analysis: A Tradeoff Perspective

B. Mazhari

***Abstract*—Conventional treatment of amplifiers emphasizes relationships between specifications and circuit parameters and gives only marginal importance to relationships among the specification themselves. With a view that an understanding of tradeoffs among specifications is very important from the design perspective, a representation of amplifier results is presented that explicitly highlights these relationships. Results are presented for some commonly used bipolar and metal–oxide–semiconductor field-effect transistor (MOSFET) amplifier topologies.**

***Index Terms*—Amplifiers, bipolar transistor amplifiers, circuit analysis, differential amplifier, metal–oxide–semiconductor field-effect transistor (MOSFET) amplifiers.**

I. Introduction

ANALYSIS and design of amplifiers form an integral part of all electrical engineering curricula. The treatment of analysis commonly begins with dc analysis to obtain the operating point of the active element. Midfrequency small-signal analysis follows to obtain expressions for voltage gain, input resistance, output resistance, voltage swing, etc. The frequency response and noise characteristics are next dealt with, followed by treatment of negative feedback, instability, etc. The analytical expressions obtained from each kind of analysis, such as for voltage gain or upper cutoff frequency, are expressed in terms of different circuit parameters, including the model parameters of the active element [1]–[7]. This representation by making explicit the relationships between amplifier characteristics and circuit variables is very useful for designing an amplifier. However, the strength of this representation is also responsible for its weakness, namely, that it leaves the relationships between important amplifier characteristics implicit and relatively difficult to grasp. However, the relationships among the specifications themselves are equally essential for a better understanding of any given amplifier circuit. Although these relationships are present in an implicit form in the analytical equations that are obtained after the analysis, they are not readily understandable and become evident only after considerable design experience. Based on the concept of design-oriented analysis pioneered by Middlebrook [8], the author presents in this paper a representation of results obtained from amplifier analysis that explicitly highlights the tradeoffs present among the specifications. The amplifier configurations considered in this paper include some common bipolar junction transistor (BJT) and metal–oxide–semiconductor (MOS) amplifier stages.

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The author is with the Department of Electrical Engineering, Indian Institute of Technology, Kanpur 208016, India (e-mail: baquer@iitk.ac.in).

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II. Methodology

The methodology for obtaining relationships among amplifier specifications can be described as follows. Consider a set of specifications $\{S_i\}$, which by using conventional techniques of analysis can be expressed as functions of circuit parameters $\{c_i\}$ and device parameters $\{d_i\}$, as follows:

$$S_i = f_i(c_1, c_2, \ldots\ldots c_n; d_1, d_2, \ldots . d_m). \tag{1}$$

By eliminating all circuit parameters from a suitably chosen subset of equations such as (1), one can obtain an expression of the form

$$g(S_1, S_2, \ldots\ldots S_K) = h(d_1, d_2, \ldots d_m). \tag{2}$$

An expression such as (2) would show explicitly the relationships or tradeoffs among the chosen specifications and also the importance of different device parameters. The task of casting equations in the form of (2) becomes easier if the starting expressions are linear in nature. The methodology for obtaining such expressions is similar to the technique used for casting expressions in the form of dimensionless equations [9]. However, the focus of the present approach is more on eliminating all extraneous variables that obscure comprehension of tradeoffs inherent in the design. In order to illustrate this methodology with concrete examples, analysis of some basic building blocks of BJT and MOS amplifiers is described in the next section.

III. BJT Amplifiers

Analysis of common emitter (CE), common base (CB), and common collector (CC) amplifiers is described first for a small subset of amplifier specifications. This description is followed by a more detailed analysis of an resistor–capacitor (*RC*)-coupled CE amplifier.

A. CE Amplifier

Fig. 1(a) shows a schematic of a BJT CE amplifier. Although the biasing network is not explicitly shown (to keep the treatment simple), the amplifier is implicitly assumed to be biased in a forward active mode. For simplicity, load resistance is also initially assumed to be very high compared with output resistance. An analysis of this circuit using the small-signal BJT model shown in Fig. 1(b) can be used to obtain expressions for midfrequency voltage gain (A_V), input resistance $(R_{\rm IN})$, and output resistance (R_O) [2]

$$A_V = -g_m R_C \tag{3}$$

$$R_{\rm IN} = r_\pi \tag{4}$$

$$R_O = R_C \tag{5}$$

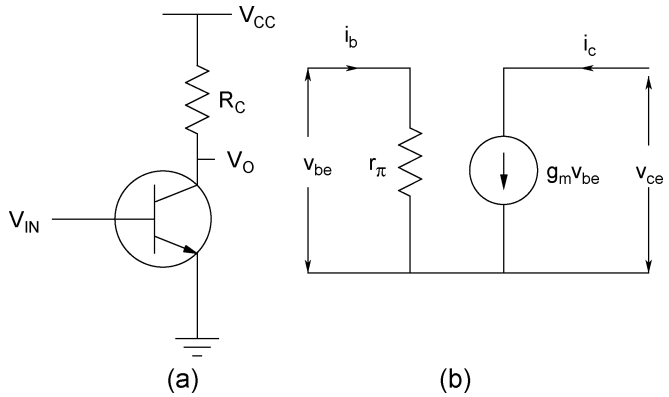

Fig. 1. Schematic of (a) CE amplifier and (b) low-frequency small-signal BJT model.

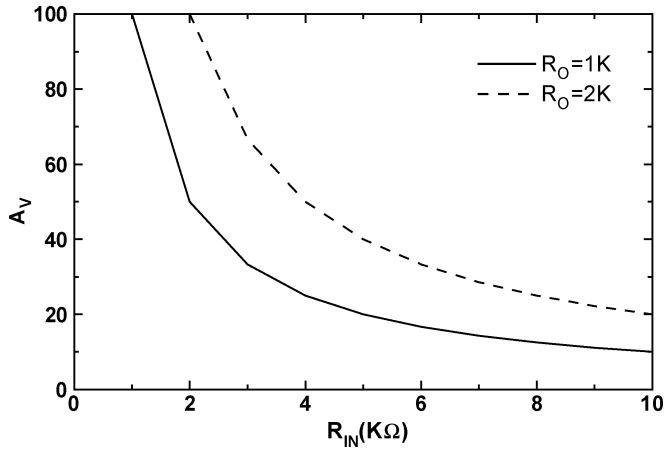

Fig. 2. Tradeoff between voltage gain and input resistance for two different values of output resistance for a CE amplifier with $\beta = 100$.

where $g_m = I_{CQ}/V_T$ and $r_\pi = \beta V_T/I_{CQ}$. I_{CQ} is the dc collector current, $V_T = kT/q$ is the thermal voltage, and β is the current gain of the transistor. In (5), the output resistance of the BJT is neglected. Equations (3)–(5) represent the final form in which results of analysis are commonly presented. This representation by explicitly revealing the dependence of amplifier characteristics on circuit parameters, such as collector resistance and dc biasing current, is essential for carrying out the design. The drawback of this representation is that it obscures the relationships between voltage gain and input and output resistances. However, an understanding of tradeoffs among these three specifications is also equally essential to the design process. Using the methodology outlined in the previous section, all circuit parameters can be eliminated from (3)–(5) to obtain

$$\frac{|A_V| \times R_{\rm IN}}{R_O} = \beta. \tag{6}$$

Equation (6) shows the tradeoffs that exist between voltage gain, input resistance, and output resistance of a CE amplifier because the right-hand side of (6) is a constant. For example, the equation shows that an increase in voltage gain will be obtained at the expense of either a proportionate increase in output resistance or a proportionate decrease in input resistance. The tradeoff described by (6) is shown graphically in Fig. 2. Equation (6) also brings out the importance of the current gain of the BJT by revealing that the ability of a CE voltage amplifier to achieve high voltage gain, low output resistance, and high input resistance is ultimately limited by this gain. This is understandable since BJT is essentially a current-amplifying device. Although the information regarding tradeoffs exists in (3)–(5), the relationship described by (6) is implicit and not readily apparent.

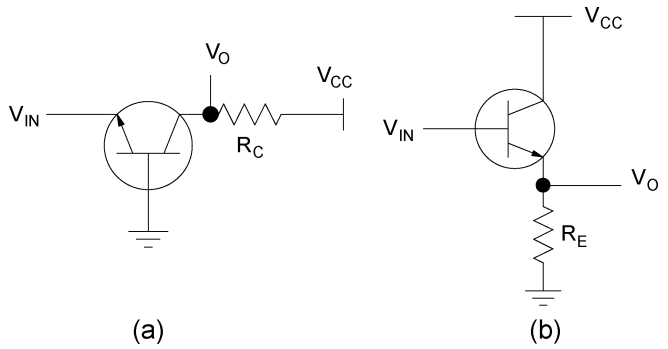

Fig. 3. Schematic of (a) CB amplifier and (b) CC amplifier.

Besides providing valuable insight into the characteristics of a CE amplifier, an expression such as (6) is directly helpful in other design tasks as well. As an example, consider the design of an amplifier for the following set of specifications: $A_V = 100$; $R_{\rm IN} = 2$ k; and $R_O = 1$ k. Suppose one attempts to implement these specifications using a CE amplifier with a transistor having a current gain of 100. An expression such as (6) can serve a useful role in the design process in several ways. First, using this expression, one can determine whether specifications are feasible or not. For the given specifications, one finds that they are not. In this case, (6) can help in modifying specifications so that they can be implemented using a CE amplifier. For example, one can easily obtain the specified values of voltage gain and input resistance, but output resistance is twice the specified value of 1 k. Alternatively, (6) shows that one can obtain the specified values of voltage gain and output resistance, but input resistance is half the specified value of 2 k. Expressions describing relationships among specifications can also help in selection of transistors. In (2), the right-hand side consists largely of device parameters that must have values so that for the given specifications, the expression is satisfied. For the CE amplifier specifications described previously, one found that for a current gain of 100, the specifications were unattainable. However, (6) also shows that a choice of a different transistor with a current gain larger than 200 would make the specifications feasible. Expressions describing relationships among specifications are unique for each distinct class of amplifiers and, as a result, can serve a very useful role in comparing and contrasting them, thereby revealing each one's unique strength and weaknesses. This uniqueness is illustrated through an analysis of a CB and a CC amplifier stage.

B. CB Amplifier

Fig. 3(a) shows a simplified schematic of a CB amplifier. Using conventional techniques of analysis, one can obtain the following sets of expressions [2]:

$$A_V = g_m R_C \tag{7}$$

$$R_{\rm IN} = r_e \tag{8}$$

$$R_O = R_C \tag{9}$$

where $r_e = V_T/I_{CQ}$. Using (7)–(9), one can easily obtain

$$\frac{A_V \times R_{\rm IN}}{R_O} = 1. \tag{10}$$

Equation (10) shows that gain, input resistance, and output resistance can again be traded with each other independent of current gain β. A comparison of (10) with (6) reveals the differences between CE and CB amplifier stages

$$\frac{|A_V(CE)|}{A_V(CB)} \times \frac{R_{\rm IN}(CE)}{R_{\rm IN}(CB)} \times \frac{R_O(CB)}{R_O(CE)} = \beta. \tag{11}$$

While comparing CE with CB amplifiers, a common statement is that while the gain and output resistance in the two are comparable, the latter suffers from a small input resistance [1]. Equation (11) confirms that for same values of voltage gain and output resistance, a CE amplifier offers a much larger input resistance as compared with a CB amplifier. However, (11) is more general in nature. For example, it shows that one can also say that for same values of voltage gain and input resistance, a CE amplifier offers a much smaller output resistance as compared with a CB amplifier. Similarly, for identical values of input and output resistances, a CE amplifier offers a much higher voltage gain. Just as (6) is a signature of CE amplifiers, similarly, (10) represents a signature of CB amplifiers, and their comparison allows one to compare and contrast the two amplifier types. To further illustrate this point, analysis of a CC amplifier is described next.

C. CC Amplifier

Fig. 3(b) shows a simplified schematic of a CC amplifier. Upon analysis, the following expressions can be obtained [2]:

$$A_V = \frac{R_E}{r_e + R_E} \tag{12}$$

$$R_{\rm IN} = \beta(R_E + r_e) \tag{13}$$

$$R_O = r_e \| R_E. \tag{14}$$

Using (12)–(14), the following expression can be obtained:

$$\frac{A_V R_{\rm IN}}{R_O} = \beta\left(1 + \frac{\eta V_{\rm CC}}{V_T}\right) \tag{15}$$

where $\eta = I_{CQ}R_E/V_{\rm CC}$ decides the voltage swing of the amplifier. For maximum voltage swing, one should take $\eta = 0.5$, which corresponds to $V_{CEQ} = V_{\rm CC}/2$. The chief characteristics of a CC amplifier are very high input resistance and very low output resistance at a voltage gain of nearly unity. However, such a statement does not clearly bring out the uniqueness of a CC stage. For example, from (6), one can see that the gain and input resistance in a CE amplifier can be traded with each other, and if a CE amplifier is designed with a voltage gain of unity, then an input resistance as large as 100 k may be obtained along with an output resistance of 1 k for $\beta = 100$. The differences between the CE and CC stages become clearer upon comparison of (15) with (6):

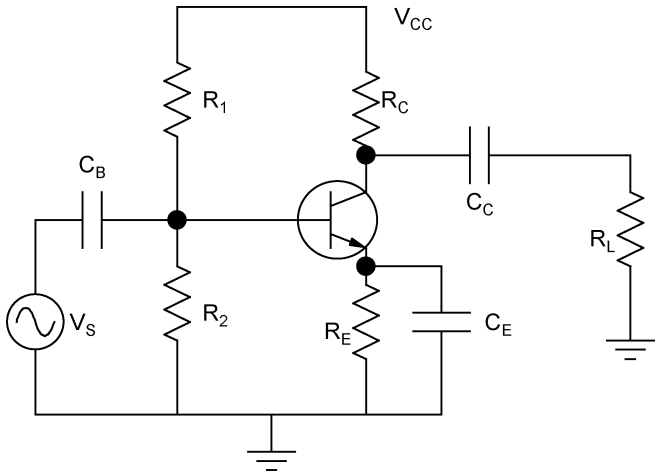

Fig. 4. Schematic of an *RC*-coupled CE amplifier.

$$\frac{A_V(\rm CC)}{|A_V(\rm CE)|} \times \frac{R_{\rm IN}(\rm CC)}{R_{\rm IN}(\rm CE)} \times \frac{R_O(\rm CE)}{R_O(\rm CC)} = \left(1 + \eta\frac{V_{\rm CC}}{V_T}\right) = 101 \tag{16}$$

where $\eta = 0.5$ and $V_{\rm CC} = 5$ V has been assumed. Equation (16) clearly shows the superiority of a CC amplifier in providing high input impedance and low output impedance. Even if a CE amplifier is designed with a voltage gain equal to that of a CC amplifier, one finds from (16) that for the same output impedance, the input resistance of a CC stage is larger by two orders of magnitude. Alternatively, for the same gain and input impedance, a CC stage can provide an output impedance that is two orders of magnitude smaller relative to a CE stage.

D. RC-Coupled CE Amplifier

The authors have so far described the usefulness of the proposed representation of amplifier results using the examples of basic amplifier stages for a small subset of specifications. To illustrate that the proposed methodology is general and applicable to a larger set of specifications, analysis of a *RC*-coupled CE amplifier (Fig. 4) is described for a set of specifications that include voltage gain, input and output resistances, lower and upper cutoff frequencies (f_L, f_H), maximum voltage swing (V_{OM}), and second harmonic distortion (HD_2). The relationships among these specifications are described as follows with the detailed derivation provided in the Appendix:

$$\frac{|A_V| \times R_{\rm IN}}{R_O} = \frac{\beta}{(1 + x_{ro})(1 + x_{ri})} \tag{17}$$

where $x_{ro} = R_O/R_L$; $x_{ri} = R_{in}/R_B$ and $R_B = R_1 \| R_2$

$$f_L \times R_{\rm IN} = \frac{\beta}{2\pi C_E(1 + x_{ri})}. \tag{18}$$

C_E is the emitter bypass capacitor. Equation (18) assumes that the source resistance is much smaller than the input resistance ($R_S \ll R_{\text{in}}$).

$$f_H \times (1 + |A_V|) = \frac{1}{2\pi(R_S + r_{bb})C_{bc}(1 + K_1)} \tag{19}$$

where $K_1 = (C_{be})/(C_{bc}(1+|A_V|))+(\tau_F(1+x_{ro}))/(R_O C_{bc})$. The base spreading resistance is r_{BB}; C_{be}, and C_{bc} are the emitter-base and collector-base junction capacitances, respectively; and τ_F is the forward transit time.

$$\frac{f_H}{R_{\text{IN}}} = \frac{1 + x_{ri}}{2\pi\beta(R_S + r_{bb})\tau_F(1 + K_2)} \tag{20}$$

where $K_2 = (R_O(C_{bc}+(C_{be}/1+|A_V|))/\tau_F(1+x_{ro}))$. Equation (19) is useful when $K_1 < 1$ and (20) when $K_2 < 1$.

$$\frac{HD_2 \times |A_V|}{V_O^{\text{P-P}}} \geq \frac{12.5}{V_T} \tag{21}$$

where HD_2 is the second harmonic distortion (expressed as percentage), and $V_O^{\text{P-P}}$ is the peak-to-peak output voltage. Equation (21) is valid for $HD_2 \leq 25\%$.

$$V_{\text{CC}} \geq |A_V|V_T(1+x_{ro})+V_{OM}+V_{\text{CE}}(\text{sat.})+\frac{\left(S_\beta^{-1}-1\right)V_T}{x_{ri}} \tag{22}$$

where $S_\beta = (\Delta I_{CQ}/I_{CQ})/(\Delta\beta/\beta)$ refers to the stability of collector bias current against variations of current gain. As discussed previously, the strength of the representation described by (17)–(22) lies in the clarity and ease with which the various possible tradeoffs among a CE amplifier's specifications can be understood. Equation (17) is similar to (6) described previously, but it takes into account the impact of biasing and load resistances. The effect of both these parameters can be looked upon as effectively modifying the current gain of the transistor. Since there is a practical limit on the maximum value that can be used for the emitter bypass capacitor, (18) shows that a decrease in lower cutoff frequency can then only be accompanied with an increase in input resistance. Although this increase appears advantageous because a high input resistance is also a desirable feature of a voltage amplifier, (17) shows that an increase in input resistance has to come at the expense of either an increased output resistance or a reduced voltage gain. Therefore, (17) and (18) together show the existence of a tradeoff between lower cutoff frequency on one hand and output resistance and voltage gain on the other hand, as illustrated in Fig. 5. Equation (19) describes the well-known tradeoff between voltage gain and bandwidth, especially true when the upper cutoff frequency is determined dominantly by collector junction capacitance and $K_1 \ll 1$. However, when the forward transit time is the dominant factor determining the upper cutoff frequency, then an increase in f_H will be accompanied with an increase in input resistance according to (20), as discussed previously, resulting in either a decrease in voltage gain or an increase in output resistance. The first case is the usual gain–bandwidth tradeoff, while the second case implies a bandwidth–output resistance tradeoff. Equation (21) highlights that for a constant second harmonic distortion, an increase in voltage swing will be accompanied with an increase in voltage gain. This result along with (17) implies the existence of a tradeoff between output voltage swing on one hand and input and output resistances on the other hand. Equation (22) shows the relationship between supply voltage, voltage gain, maximum voltage swing, and bias point stability. For a fixed supply voltage, an increase in voltage gain can come either at the expense of a reduced voltage swing or a reduced bias stability.

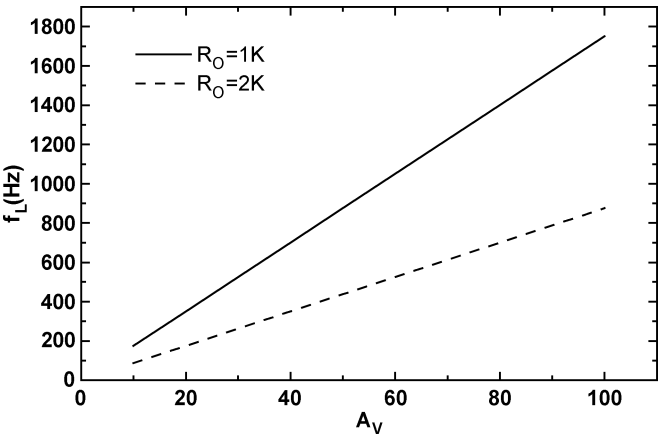

Fig. 5. Tradeoff between lower cutoff frequency (f_L) and voltage gain for an *RC*-coupled amplifier with $\beta = 100$ and $C_E = 10\,\mu$F.

IV. MOSFET Amplifier

Using the approach described previously, a set of expressions describing tradeoffs can be similarly obtained for the basic MOS amplifier stages such as common source, common gate, and common drain amplifiers. In the next section, a detailed analysis of a slightly more complex MOS differential amplifier is presented.

A. Differential Amplifier

Fig. 6(a) shows a schematic of a MOS differential amplifier with P-type MOS current mirror load. The analysis of this amplifier is considered for a set of specifications that include differential mode voltage gain (A_{dm}), output resistance, common-mode rejection ratio (CMRR), unity gain frequency (UGF), Slew rate (SR), input common-mode range voltages (CMR^+, CMR^-), and power dissipation (P_d). By analyzing this amplifier using the small-signal model shown in Fig. 6(b), the following set of expressions relating the specifications to circuit and device parameters can be written [7]:

$$A_{dm} = g_{m1}\, r_{02} || r_{04} \tag{23}$$

$$A_{\text{CM}} = \frac{1}{2g_{m3}r_{05}} \tag{24}$$

$$R_O = r_{02} || r_{04} \tag{25}$$

$$\text{UGF} = \frac{g_{m1}}{2\pi C_L} \tag{26}$$

$$\text{SR} = \frac{I_{SS}}{C_L} \tag{27}$$

$$\text{CMR}^+ = V_{DD} + (V_{T1} - V_{T3}) - \sqrt{\frac{I_{SS}}{\beta_3}} \tag{28}$$

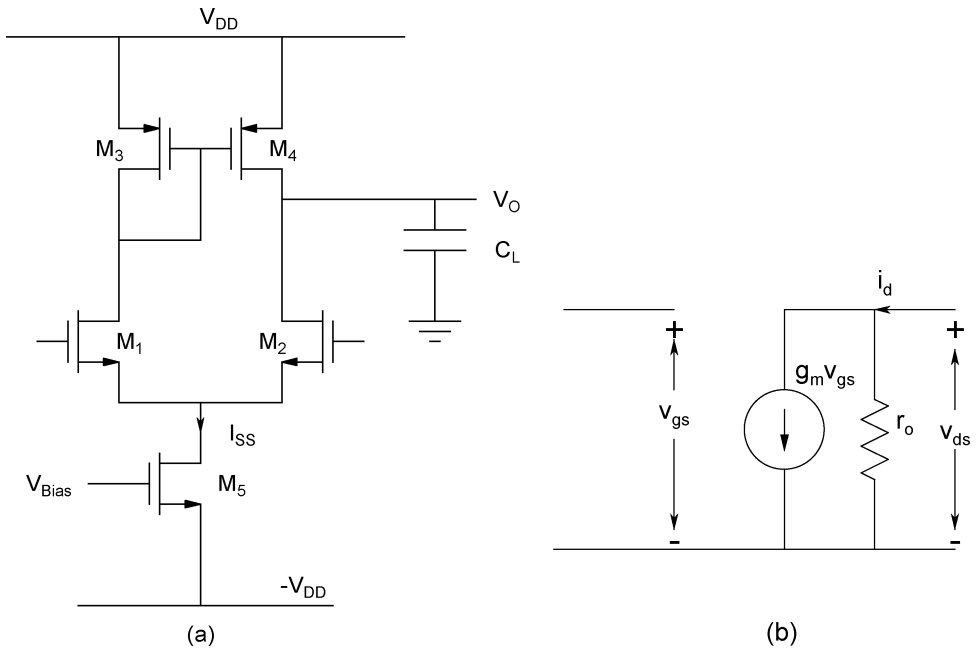

Fig. 6. Schematic of (a) MOS differential amplifier with current mirror load (b) small-signal MOS model.

$$\text{CMR}^{-} = V_{DD} - V_{T1} - 2\sqrt{\frac{I_{SS}}{\beta_1}} \tag{29}$$

$$P_d = 2I_{SS} \times V_{DD} \tag{30}$$

where V_{TK}, $\beta_K = KP(W/L)_K$ and r_{oK} refer to the threshold voltage, transconductance parameter, and output resistance of transistor M_K, respectively. A_{CM} is the common-mode gain. The assumption is that $(W/L)_1 = (W/L)_2 = 0.5(W/L)_5$ and $(W/L)_3 = (W/L)_4$. In the derivation of UGF and SR, the assumption is that load capacitance is much larger than the internal transistor capacitances. Equation (29) gives the magnitude of input CMR in the negative direction. Using (23) and (25), an expression describing the tradeoff among differential voltage gain, output resistance, and area of transistor M_1(or M_2) can be obtained

$$\frac{A_{dm}}{\sqrt{R_O}} = \sqrt{\frac{2KP_N}{L^2} \times \frac{1}{\lambda_P + \lambda_N}} \times \sqrt{\text{Area}(M_1)}. \tag{31}$$

Equation (31) shows that an increase in voltage gain can be obtained at the expense of either an increased output resistance or an increased device size as illustrated in Fig. 7. These results were obtained using the following parameters for N-type MOS and P-type MOS transistors: $KP_N = 100\ \mu\text{A/V}^2$; $KP_P = 40\ \mu\text{A/V}^2$; $\lambda_N = 0.015\ \text{V}^{-1}$; $\lambda_P = 0.065\ \text{V}^{-1}$; $V_{TN} = 0.69\ \text{V}$; and $V_{TP} = -0.86\ \text{V}$, channel length of 1 μm and supply voltage of 3.3 V. Equation (31) also shows that the ability of a differential amplifier to provide a high voltage gain and a low output resistance while keeping the device area small is ultimately limited by the device parameters $(KP_N/(\lambda_N + \lambda_P)L^2)$. Equations (23) and (27) can be used to obtain a relationship between gain and SR

$$A_{dm} \times \sqrt{\text{SR}} = \left(\frac{2}{\lambda_P + \lambda_N}\right) \times \sqrt{\frac{KP_N}{L^2} \times \frac{1}{C_L}} \times \sqrt{\text{Area}(M_1)}. \tag{32}$$

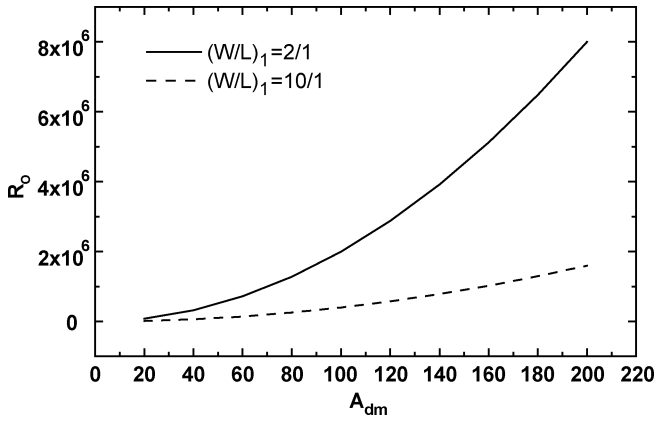

Fig. 7. Tradeoff between differential mode gain (A_{dm}) and output resistance (R_o) for a MOS differential pair for two different sizes of transistor M_1.

This expression shows that an increase in voltage gain must come at the expense of a reduced SR if the area of transistor M_1 is left unchanged. Equations (23) and (26) can be used to obtain a relationship between UGF and differential voltage gain

$$A_{dm} \times \text{UGF} = \frac{KP_N}{\pi L^2 C_L(\lambda_P + \lambda_N)} \times \text{Area}(M_1). \tag{33}$$

Equation (33) shows that an increase in differential mode gain without compromising UGF can only be obtained by increasing the sizes of transistors M_1 and M_2. The tradeoff between differential gain and UGF is illustrated in Fig. 8. Equation (27) and (30) can be used to obtain a relationship between SR and power dissipation

$$\frac{\text{SR}}{P_d} = \frac{1}{2C_L V_{DD}}. \tag{34}$$

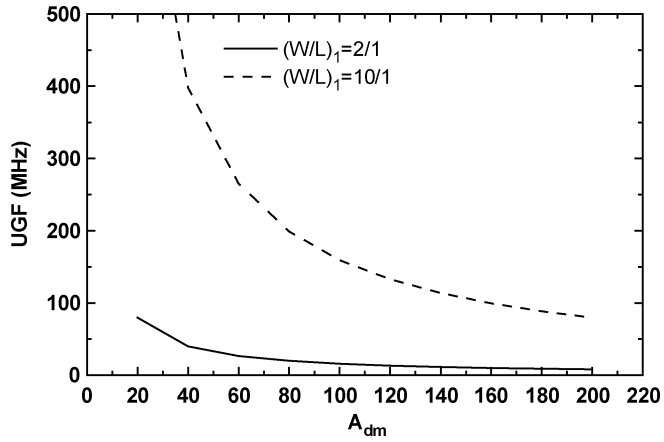

Fig. 8. Tradeoff between UGF and differential mode gain in a MOS differential pair for two different sizes of transistor M_1. A load capacitor of 0.5 pF is assumed.

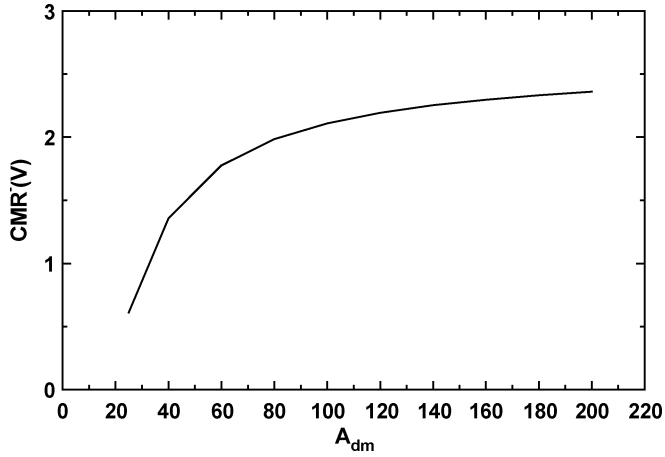

Fig. 9. Relationship between negative input CMR and differential mode gain in a MOS differential pair.

Equations (23) and (29) can be used to derive the relationship between differential gain and negative input common-mode voltage

$$A_{dm} \times \left(1 - \frac{\text{CMR}^-}{V_{DD} - V_{T1}}\right) = \frac{4}{(\lambda_P + \lambda_N)} \times \frac{1}{V_{DD} - V_{T1}}. \tag{35}$$

Equation (35) shows that an increase in CMR^- would require an increase in differential mode gain as well. This relationship between the two is illustrated in Fig. 9. This information along with (31) then implies the existence of a tradeoff between CMR^- on one hand and output resistance on the other hand. Equations (23) and (24) can be used to obtain an expression relating gain with the common-mode rejection ratio (CMRR)

$$\frac{A_{dm}^2}{\text{CMRR}} = \frac{\lambda_N}{\lambda_P + \lambda_N} \times \sqrt{\frac{KP_N}{KP_P}} \times \sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_3}}. \tag{36}$$

Equation (36) shows that for a fixed ratio of sizes of M_1 and M_3, an increase in differential mode gain by a factor K would result in an increase in CMRR by factor K^2, as illustrated in Fig. 10. Equations (35) and (36) along with (28) can be used to obtain the following expression

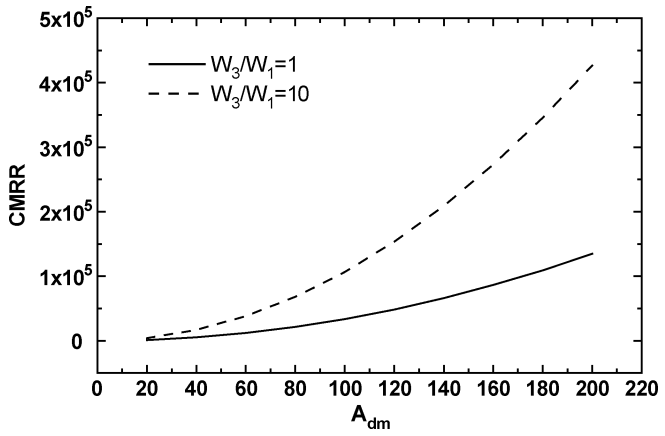

Fig. 10. Relationship between CMRR and differential mode gain in a MOS differential pair.

$$\text{CMRR} \times \left(1 - \frac{\text{CMR}^-}{V_{DD} - V_{T1}}\right) \times \left(1 - \frac{\text{CMR}^+}{V_{DD} + V_{T1} - V_{T3}}\right) = \frac{4}{\lambda_N(\lambda_P + \lambda_N)} \times \frac{1}{(V_{DD} - V_{T1}) \times (V_{DD} + V_{T1} - V_{T3})}. \tag{37}$$

As seen previously, an increase in differential voltage gain by a factor K results in a reduction in $(1 - (\text{CMR}^-)/(V_{DD} - V_{T1}))$ by factor K (35) and an increase in CMRR by a factor K^2. Equation (37) then implies that an increase in differential mode gain would result in an improvement of CMRR and both positive and negative input CMR voltages.

V. Conclusion

To summarize, an alternative representation of the results obtained from conventional methods of analysis of amplifiers is described, which explicitly reveals the relationships among important amplifier specifications. Using the examples of BJT and MOS amplifiers, the new representation is shown not only to facilitate the grasp of tradeoffs inherent in an amplifier but also to help compare and contrast the different amplifier topologies.

Appendix
Analysis of an *RC*-Coupled Common Emitter Amplifier

The expressions for voltage gain, input resistance, and output resistance can be written as

$$A_V = -g_m \times R_C || R_L \tag{A1}$$

$$R_{\text{IN}} = r_\pi || R_1 || R_2 \tag{A2}$$

$$R_O = R_C. \tag{A3}$$

Denoting $x_{ro} = R_O/R_L$, $x_{ri} = r_\pi/R_B \cong R_{\text{IN}}/R_B$, $R_B = R_1||R_2$, and using the relations $g_m = I_{CQ}/V_T$ and $r_\pi = \beta V_T/I_{CQ}$, one can obtain

$$\frac{|A_V| \times R_{\text{IN}}}{R_O} = \frac{\beta}{(1 + x_{ro})(1 + x_{ri})}. \tag{A4}$$

The lower frequency is determined by the coupling and bypass capacitors. Assuming that the effect of capacitor C_E is dominant, the lower cutoff frequency can be written as [5]

$$f_L = \frac{1}{2\pi C_E R_E^{/}} \tag{A5}$$

$$R_E^{/} = R_E \left\| \frac{r_\pi + R_B \| R_S}{\beta + 1} \right. . \tag{A6}$$

In (A6), the effect of base spreading resistance is ignored. Assuming that the source resistance is much smaller than the input resistance ($R_S \ll R_{\rm IN}$) and emitter resistance (R_E) is much larger than r_π/β, one can obtain the following expression by combining (A2), (A5), and (A6):

$$f_L \times R_{\rm IN} = \frac{\beta}{2\pi C_E(1 + x_{ri})}. \tag{A7}$$

The upper cutoff frequency can be expressed as [5]

$$f_H = \frac{1}{2\pi C_T R_S^{/}} \tag{A8}$$

$$C_T = C_\pi + C_\mu \times (1 + g_m R_L \| R_C) \tag{A9}$$

$$R_S^{/} = (R_S \| R_B + r_{bb}) \| r_\pi. \tag{A10}$$

The capacitance C_π can be expressed as

$$C_\pi = C_{be} + g_m \tau_F \tag{A11}$$

where C_{be} is the emitter-base junction capacitance, and τ_F is the forward transit time. C_μ is basically C_{bc}, the collector-base junction capacitance. Using (A1) and (A8)–(A11) and assuming that input resistance ($\sim r_\pi$) is much larger than the resistance $R_S + r_{bb}$, one can obtain

$$f_H \times (1 + |A_V|) = \frac{1}{2\pi(R_S + r_{bb})C_{bc}(1 + K_1)} \tag{A12}$$

where $K_1 = (C_{be})/(C_{bc}(1+|A_V|)) + (\tau_F(1+x_{ro}))/(R_O C_{bc})$. This equation is useful when device and circuit parameters are such that $K_1 < 1$; in other words, collector-base capacitance plays a dominant role. In this case (A12) represents a tradeoff between gain and upper cutoff frequency. In case this constraint is not satisfied, an alternative expression can be derived:

$$\frac{f_H}{R_{\rm IN}} = \frac{1 + x_{ri}}{2\pi\beta(R_S + r_{bb})\tau_F(1 + K_2)} \tag{A13}$$

where $K_2 = (R_O(C_{bc} + (C_{be}/1 + |A_V|)))/(\tau_F(1 + x_{ro}))$. Equation (A13) is useful when $K_2 < 1$; in other words, forward transit time is the dominant factor impacting cutoff frequency. The second harmonic distortion (expressed as a percentage) can be written as [2]

$$HD_2 = \frac{1}{4} \times \frac{v_{\rm IN}}{V_T} \times 100 \tag{A14}$$

where $v_{\rm IN}$ is the magnitude of the applied input voltage. Using the relation $v_{\rm IN} = V_O^{\rm P-P}/2|A_V|$, where $V_O^{\rm P-P}$ is the peak-to-peak output voltage, one can obtain

$$\frac{HD_2 \times |A_V|}{V_O^{\rm P-P}} \geq \frac{12.5}{V_T}. \tag{A15}$$

The supply voltage can be related to gain and other specifications as follows. Application of Kirchoff's voltage law (KVL) to the output loop gives

$$V_{\rm CC} = I_{CQ} R_C + V_{CEQ} + I_{CQ} R_E. \tag{A16}$$

Using (A1), the first term on the right-hand side can be written as

$$I_{CQ} R_C = |A_V| V_T (1 + x_{ro}). \tag{A17}$$

The last term on the right can be expressed in terms of bias point stability against variations in current gain defined as $S_\beta = (\Delta I_{CQ}/I_{CQ})/(\Delta\beta/\beta)$

$$I_{CQ} = \frac{V_{\rm CC} \times \left(\frac{R_2}{R_1 + R_2}\right) - V_{BE}}{R_E + \frac{R_B}{(1+\beta)}} \tag{A18}$$

$$S_\beta \cong \frac{1}{1 + \frac{\beta R_E}{R_B}}. \tag{A19}$$

Using (A19) and (A2), one can obtain

$$I_{CQ} R_E = \frac{\left(S_\beta^{-1} - 1\right) V_T}{x_{ri}}. \tag{A20}$$

The maximum voltage swing (V_{OM}) in an amplifier is determined by the condition that the amplifier does not go into either saturation or cutoff as the input signal voltage is increased. To avoid the transistor's going into saturation, the following condition must hold:

$$V_{CEQ} - V_{OM} \geq V_{\rm CE}({\rm sat}) \tag{A21}$$

where $V_{\rm CE}({\rm sat})$ is the saturation voltage of the transistor. Using (A16)–(A21), one can obtain

$$V_{\rm CC} \geq |A_V| V_T (1 + x_{ro}) + V_{OM} + V_{\rm CE}({\rm sat.}) + \frac{\left(S_\beta^{-1} - 1\right) V_T}{x_{ri}}. \tag{A22}$$

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B. Mazhari received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Khragpur, India, in 1987 and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana Champaign in 1993.

Since 1993, he has been with Department of Electrical Engineering, Indian Institute of Technology, Kanpur, India. His research interests include semiconductor device modeling and analog circuit design.