

# EE210: Analog Electronics

## Question Set 8

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1) Consider the current mirror in Fig. 1.  $I_0 = 100\mu A$ ,  $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 10$  and  $V_{tn} = 1V$ . Neglect body effect. Also, consider  $\mu_n C_{ox} = 0.2mA/V^2$  and  $\lambda = 0.1V^{-1}$ .

a) : Find  $V_{S3}, V_{S4}, V_{G3}$ . Who sets the voltages  $V_{S3}$  and  $V_{S4}$ ? (Neglect CLM for calculating Q-point)

b) : Find the incremental  $R_{out}$ .

c) : Find the minimum  $V_X$  while keeping all transistors in saturation.

d) : If  $V_X$  changes by 100 mV (while keeping  $M4$  is saturation) how much change in current will you observe through  $M2$ ?

e) : If  $V_X$  changes by 100 mV, how much change in  $V_{S4}$  will you observe?

f) : What will you do if you want to reduce  $V_{S3}$  and  $V_{S4}$  by 100 mV without affecting anything else?

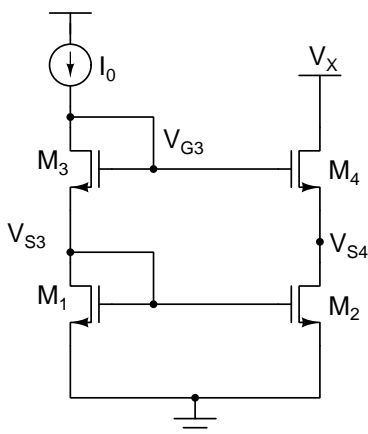


Figure 1: Problem 1.

2) Consider the circuit in Fig. 2. The currents  $I_0$ , and the transistors  $M1 - M4$  are identical to that of Q3.

a) : Is it possible to have  $V_{Xmin} = 2V_{ov|M2, M4}$ ?

b) : What must  $V_{G5}$  be to realize the condition in a)?

c) : How will you size  $M5$  to set this  $V_{G5}$ ?

3) Consider Fig. 3.  $(W/L) = 10$  for all transistors,  $V_{tn} = 1V$ ,  $\mu_n C_{ox} = 200 \mu A/V^2$ . Assume

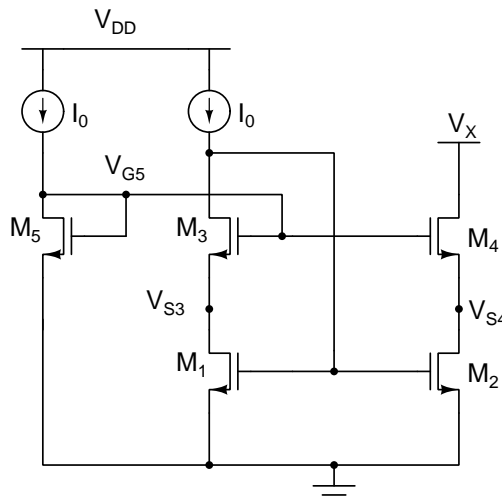


Figure 2: Problem 2.

the amplifier to be a VCVS of gain 100.

a) : Find  $V_B$  such that  $M2$  is biased just at the edge of saturation region.

b) : Assume  $I_{DS2} \approx 1mA$ . Find the incremental  $R_{out}$ .

c) : How does this architecture fare with respect to the previous ones?

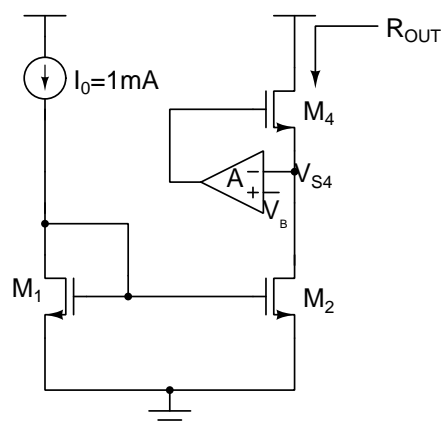


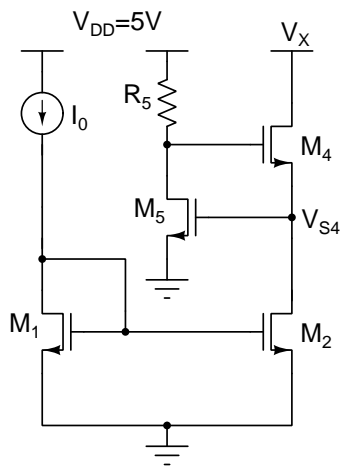
Figure 3: Problem 3.

4) Consider the Fig. 4. The amplifier in Q3. has been replaced by a common source stage. (Neglect channel length modulation for  $M5$ )

a) : Size  $M5$  such that  $V_{DSM2} = V_{DSM1}$ .

b) : What is the gain of the common source stage?

- c) : If you want to move the  $V_{DS_{M2}}$  up or down, what will you change in the circuit?
- d) : If  $I_0$  changes to  $I_0 + \Delta I$ , what will be the total voltage at the drain of  $M_2$ ? (Neglect channel length modulation for this part).



**Figure 4:** Problem 4.