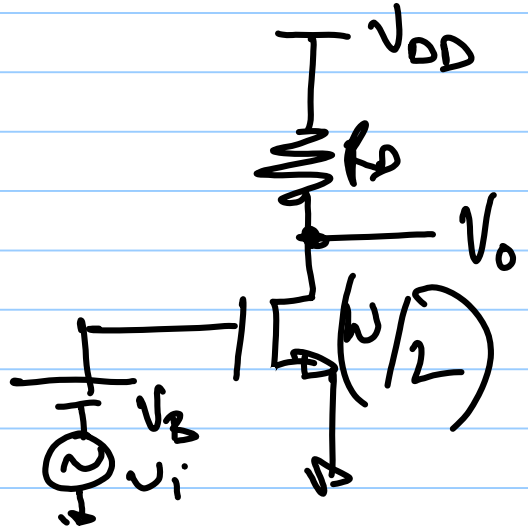
Problem Set # 4

Note Title 03-03-2023

(1) A designer aims to realise a gain of -200 using a common source amplifier. She has a battery of 3V and a MOSFET having $\mu_n C_{ox} = 0.2\ mA/V^2$ and $V_{tn} = 1V$. The only constraint that she needs to follow is that $V_{OV} = V_{GS} - V_{tn}$ must **at least** be 100mV.



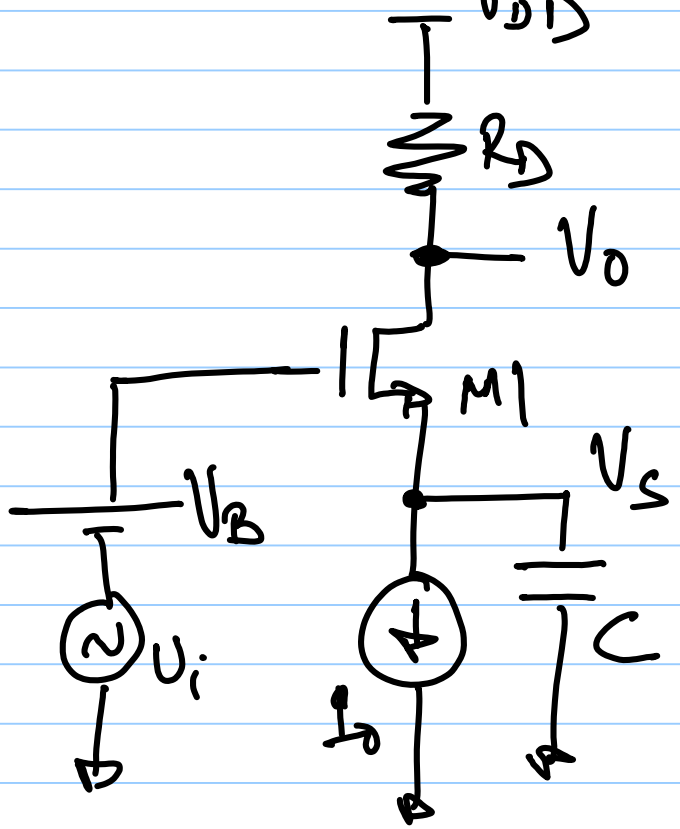
(a) Help her choose the components W/L, R_D, V_B to achieve her goal.

(b) If you are unable to realize a gain of -200, what is the maximum that you can realise?

(c) Can you improve the gain if you are allowed to pick another transistor with a different $\mu_n C_{ox}$?

(d) Can you improve the gain if you are allowed to change V_{DD}?

(2)



$V_{DD} = 5V$, $\mu_n C_{ox} \frac{W}{L} = 200 \mu A/V^2$

$V_B = 3V$, $I_o = 1mA$.

(a) Choose R_D such that M_1 is in saturation with a margin of atleast 100mV.

(b) Find v_o/v_i when $C \to 0$

(c) Find v_o/v_i when $C \to \infty$

(d) What does you of? the result in part (c) remind

(e) Plot $\left|\frac{V_o(j\omega)}{V_i(j\omega)}\right|$ using Bode approximation with the corner frequencies clearly marked. Why does the plot @ $\omega = 0$ and $\omega = \infty$ make sense?

(f) What is the time constant associated with the capacitor?

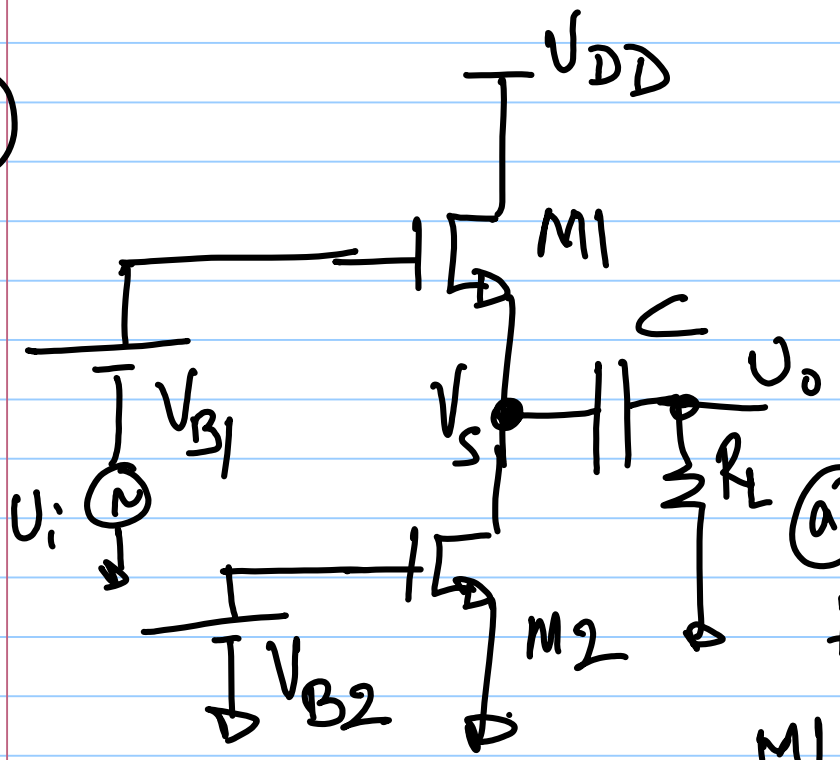
(g) Plot $\left|\frac{V_s(j\omega)}{V_i(j\omega)}\right|$ using Bode approximation.

Why does the values at $\omega = 0$ and $\omega = \infty$ make sense?

(h) If $U_i = 10mV\ u(t)$ (ie. a step input), sketch the total voltage wrt. time @ V_s and V_o.

Also sketch the total current through the transistor wrt. time

(3)



$V_{DD} = 5V$. $\mu_n C_{ox} = 200\mu A/V^2$.

$V_{tn} = 1V$. Assume $V_{ov}|_{M_2} = 100mV$

(a) Size M1, M2 such that the quiescent current through M1, M2 = 1mA, and $V_{B1} = 3V$.

Is the solution unique?

(b) If $(W/L)_{M_1} = 10$, what is $V_{ov}/_{M_1}$?

(c) What is the minimum V_{B_1} that I can set while keeping M1, M2 in saturation?

(d) What changes can I do to M1 so that the minimum V_{B_1} reduces further by 200 mV?

(e) Assume $C \to \infty$, $R_L = 10K\Omega$, $V_{B_1} = 3\ V$, $\left(W/L\right)_{M_1} = 10$ for this part.

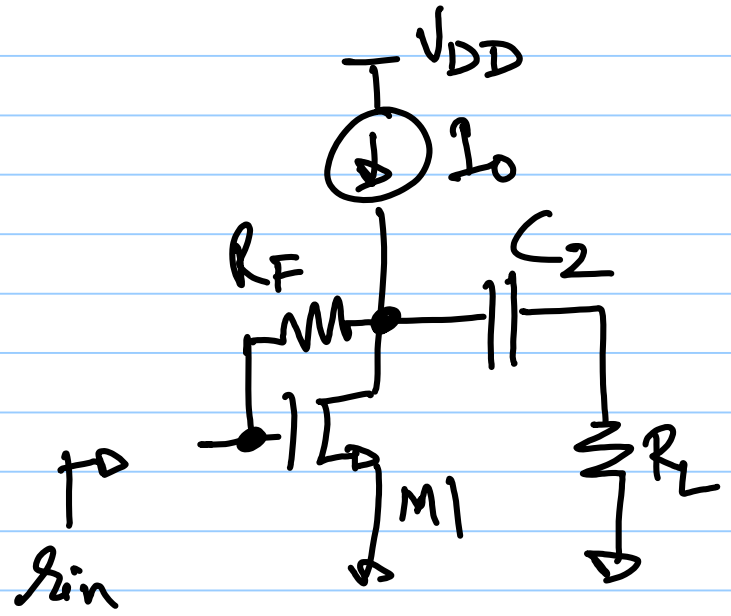
If $v_i(t) = V_p \sin(\omega t)$, find the max (V_p) while keeping both transistors in saturation and away from cut-off.

(f) For this part assume $C = 10pF$, $R_L = 10K\Omega$, $V_B = 3V$, and $\left(W/L\right)_{M_1} = 10$.

$v_i(t) = 10mV\ u(t)$ [where $u(t)$ is an unit step].

Find $v_o(t)$ and sketch it wrt. time.

(4)

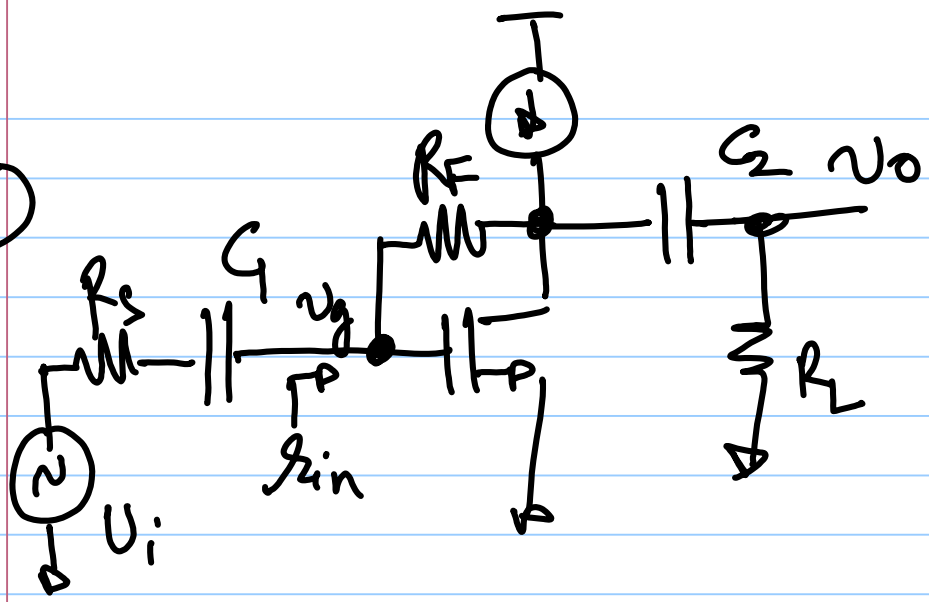


$\mu_n C_{ox} \frac{W}{L} = 2 mA/V^2$, $V_{th} = 1V$

(a) Find the DC operating condition of M1

(b) Find the incremental input impedance R_{in}. Assume $C_2 \to \infty$

(c)



Now we plan to apply an input as shown.

Assume $C_1 \to \infty$ and $R_{in} \gg R_s$. Also assume $g_m R_F \gg 1$.

Find v_o/v_i under these conditions.

Comment on the usefulness of this architecture wrt. the standard common-source amplifier.

(5) Compare the g_m sensitivity of a MOS transistor biased using constant V_{GS} or constant I_{DS} when μ_n changes by $\Delta\mu_n$.