EE210A: Microelectronics I

Problem Set 5

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1): Consider $\mu_n C_{ox} = 200\mu A/V^2$, V_{DD} = 6V, $V_{tn} = 1V$, $(W/L)_1 = 1$, $I_o = 0.1mA$ and $R_D = 2k\Omega$.

a) : Size $M2$, $M3$, $R1$ and $R2$ such that $gm_{M2} = 1mS$, $gm_{M3} = 2mS$, $M3$ is at least 100 mV away from saturation at quiescent.

b) : Find the constraint on C_1 and C_2 such that $v_o/v_i \approx -4$ @ $\omega_o = 100Mrad/s$.

c) : If $v_i = V_p \sin(\omega_0 t)$, find the maximum V_p while keeping all transistors in saturation.

d) : Find v_o/v_i if $C_2 = 0$. What's the intuition behind the result?

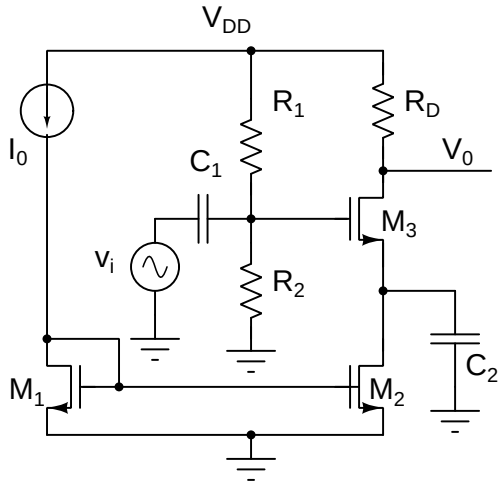

Figure 1: Problem 1.

2) : Consider $\mu_n C_{ox} = 200\mu A/V^2$, $I_0 = 0.1mA$, $V_{tn} = 0.5V$.

a) : Size $M1$, $M2$ and find V_B such that $M2$ is just at the edge of saturation, and $M1$ is 100mV away from the edge of saturation.

Hint: Express $V_{GS_{M1,M2}} = V_{tn} + V_{ov_{M1,M2}}$ for ease of analysis.

b) : Without changing V_B, what will you do to bias $M2$ in saturation with a margin of 100mV?

c) : How much will the voltages at $V1$ and $V2$ change if I_0 changes by $\pm 10\mu A$. (Assume (b) to be the quiescent).

d) : What will be the effect of change of V_{tn} of $M1$ by 10mV?

e) : What will be the effect of change of V_{tn} of $M2$ by 10mV?

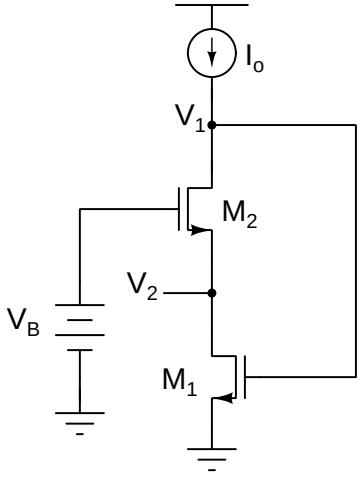

Figure 2: Problem 2.

3) : Consider $\mu_n C_{ox} = 200\mu A/V^2$, $V_tn = 0.5V$, $I_0 = 1mA$, $(W/L)_1 = 2.5$, $(W/L)_2 = 160$, $R_L = 10k\Omega$.

a) : Bias V_B such that M1 is in saturation with a margin of 100mV.

b) : Assume v_i=$V_p$sin(ωt), and C_1 and C_2 are shorted at signal frequencies. Find V_o.

c) : Find the max. allowable V_p while keeping M1,M2 in saturation.

d): Find the time constant associated with C_1 and C_2. While finding the time constant for C_1 assume C_2 is infinitely large, and vice-versa.

e): Assume $C_1 = 0$. Find time-constant associated with C_2.

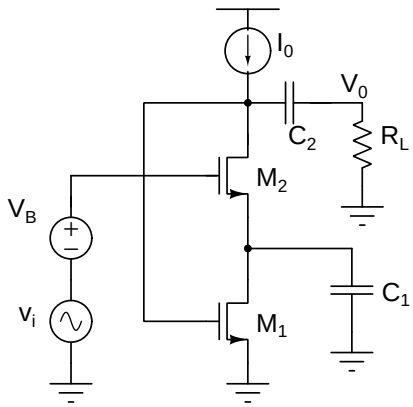

Figure 3: Problem 3.

4a) : Design a common source amplifier for a gain of –20. $V_{DD} = 3V$, $V_{tn} = 1V$, min($V_{GS} - V_{tn}$) = 100 mV. Show the biases and (W/L) of the transistor explicitly.
4b) : Now the user wants to drive an R_L (with one end connected to ground) and achieve a minimum gain of –18 when R_L varies between 100Ω to 200Ω. Without changing your design in part $a)$ what else will you add to the network to realize the specification?