EE210A: Microelectronics I

Problem Set 6

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1) Consider the circuit in Fig 1. $\mu_n C_{ox} = 0.2mA/V^2$, $I_0 = 1mA$, $V_{DD} = 6V$, $R_1 = R_2 = 3k\Omega$, $V_{tn} = 1V$. Assume $g_{mb} = 0.2g_m$. (Neglect channel length modulation)

a) Size $M1$ and $M2$ such that $M1$ is in saturation with a margin of 500 mV, and g_{M1} =1 mS.
b) Find the incremental resistances r_1 and r_2.
c) Use the configuration to implement a common source amplifier.
d) If you want to implement a CCCS, where and how will you apply the i/p and take the o/p?
e) How is this config. different from a standard common gate config.?
f) If you want to implement a VCVS having gain ≈ 0.9 while driving a load $R_L \approx$ 1kΩ to 2kΩ, what will you do?

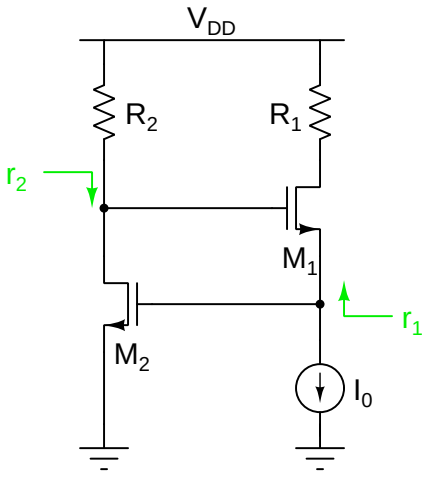

Figure 1: Problem 1.

2) The circuit shown in Fig. 2 is used to generate a bias voltage V_B=V_{tn}+V_{ov}. If we want to generate a bias voltage of V_B=V_{tn}+2V_{ov}, how will you change the circuit?

3) Consider the current mirror in Fig. 3. $I_0 = 100\mu A$, $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4$=10 and V_{tn}=1V. Neglect body effect. Also, consider $\mu_n C_{ox} = 0.2mA/V^2$ and $\lambda = 0.1V^{-1}$.

a) : Find V_{S3},V_{S4},V_{G3}. Who sets the voltages

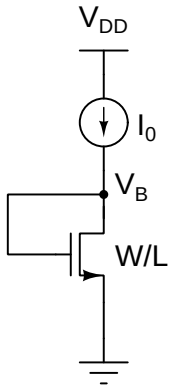

Figure 2: Problem 2.

V_{S3} and V_{S4}? (Neglect CLM for calculating Q-point)
b) : Find the incremental R_{out}.
c) : Find the minimum V_X while keeping all transistors in saturation.
d): If V_X changes by 100 mV (while keeping $M4$ is saturation) how much change in current will you observe through $M2$?
e): If V_X changes by 100 mV, how much change in V_{S4} will you observe?
f): What will you do if you want to reduce V_{S3} and V_{S4} by 100 mV without affecting anything else?

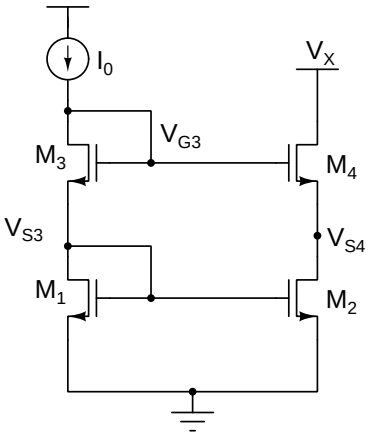

Figure 3: Problem 3.

4) Consider the circuit in Fig. 4. The currents I_0, and the transistors $M1 - M4$ are identical to that of Q3.
a) : Is it possible to have $V_{Xmin} = 2V_{ov|M2,M4}$?
b) : What must V_{G5} be to realize the condition in a)?
c) : How will you size $M5$ to set this V_{G5}?

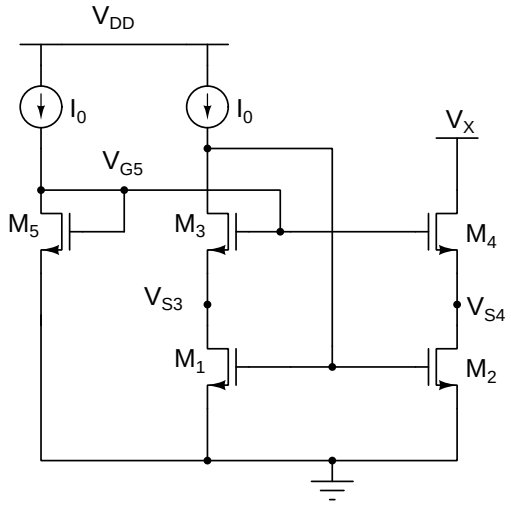

Figure 4: Problem 4.

5) Consider Fig. 5. $(W/L) = 10$ for all transistors, V_{tn}=1V, $\mu_n C_{ox}$=200 $\mu A/V^2$.
a) : Assume $I_{DS2} = 1mA$. Find the incremental R_{out}.
b) : How does this architecture fare with respect to the previous ones?

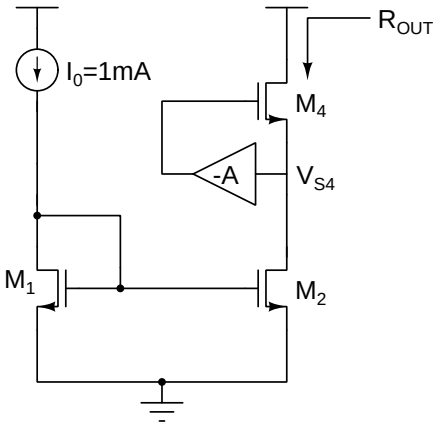

Figure 5: Problem 5.

6) Consider the Fig. 6. The amplifier in $Q5$. has been replaced by a common source stage. (Neglect channel length modulation for $M5$)
a) : Size $M5$ such that $V_{DS_{M2}} = V_{DS_{M1}}$.
b) : What is the gain of the common source stage?
c) : If you want to move the $V_{DS_{M2}}$ up or down, what will you change in the circuit?
d) : If I_0 changes to $I_0 + \Delta I$, what will be the total voltage at the drain of $M2$? (Nelgect channel length modulation for this part).

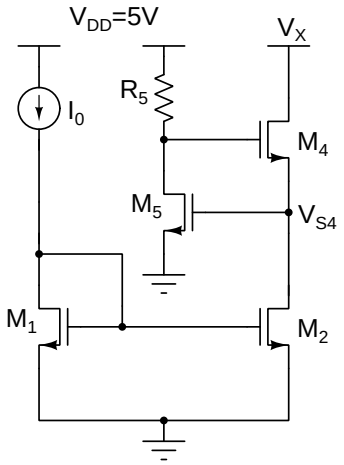

Figure 6: Problem 6.