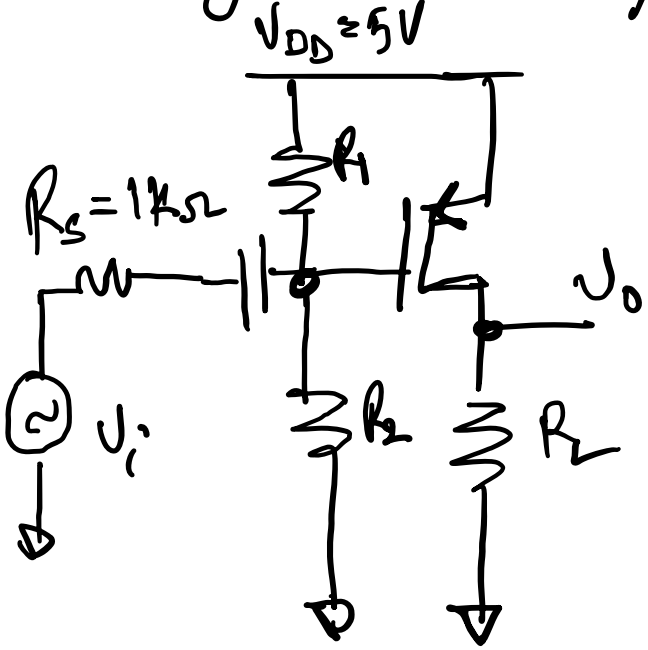
Problem Set 7

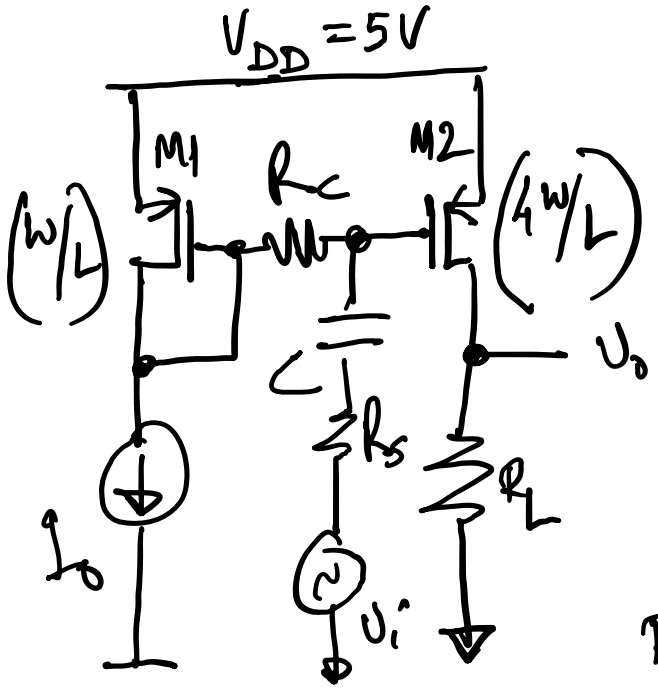
(1) Bias the following common source amplifier by selecting appropriate component values, to achieve a gain of -20. Consider $|V_{tp}| = 1V$, $\mu_p C_{ox} = 100 \mu A/V^2$.



Ensure that $\min(V_{SG} - |V_{tp}|) = 100mV$.

Ignore CLM for your analysis.

(2)



$W/L = 20$

$\mu_p C_{ox} = 100 \mu A/V^2$.

$|V_{tp}| = 1V$.

Ignore CLM.

$R_C = 100K\Omega$, $I_o = 1mA$.

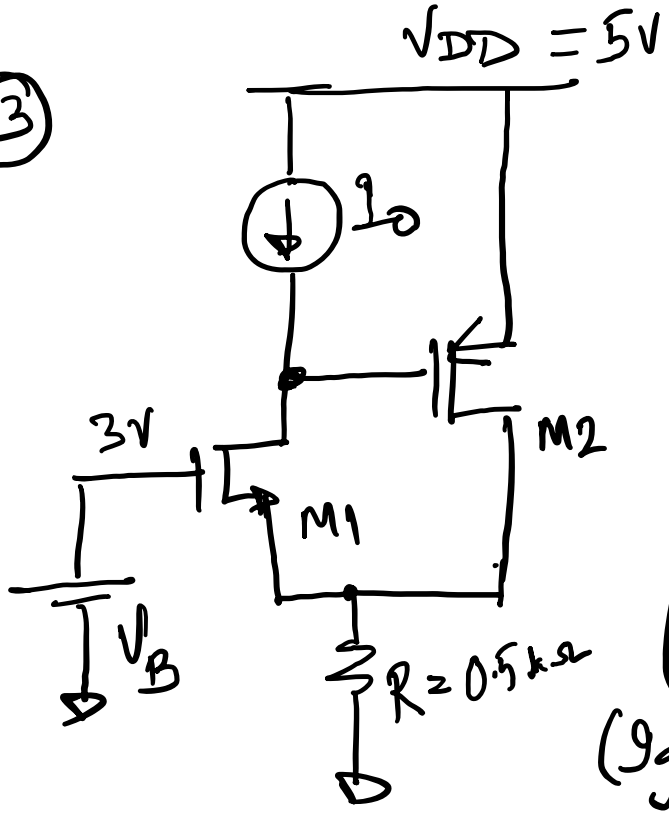
$R_S = 10k\Omega$.

(a) Find R_L such that M2 is biased at the edge of saturation.

(b) Find V_o/V_i.

(c) If $V_i = V_p \sin(\omega_o t)$, find the max V_p while ensuring M1, M2 remain on and within saturation (Assume C is infinitely large).

(3)



$I_o = 1\,mA$.

$\left(\frac{W}{L}\right)_1 = 10$

$\mu_n C_{ox} = 200\,\mu A/V^2$

$\mu_p C_{ox} = 100\,\mu A/V^2$

$\left(\frac{W}{L}\right)_2 = 20$

(Ignore body effect)

(a) find the quiescent currents through M1 and M2.

(b) Between M1, and M2, what will you change to bias M1 at the edge of saturation region?

(c) Among the four types of biasing schemes that you have learnt, which one is being used here to bias M1?

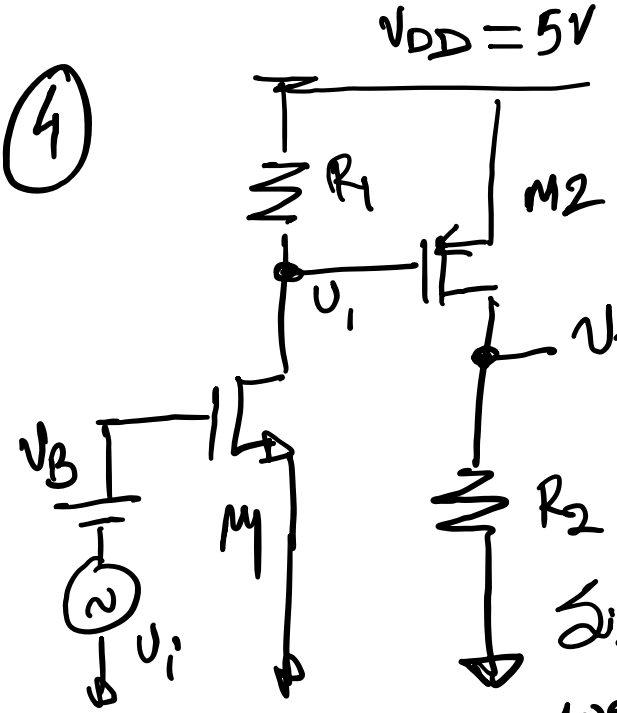
(i) Observe the drain, V_b @ source?

(ii) " " " , " @ gate?

(iii) " " source " @ source?

(iv) " " " " @ gate?

(4)



$\mu_n C_{ox} = 200 \mu A/V^2$

$\mu_p C_{ox} = 100 \mu A/V^2$

$V_B = 2V$, $R_1 = 3K\Omega$.

$\left(W/L\right)_1 = 10.$

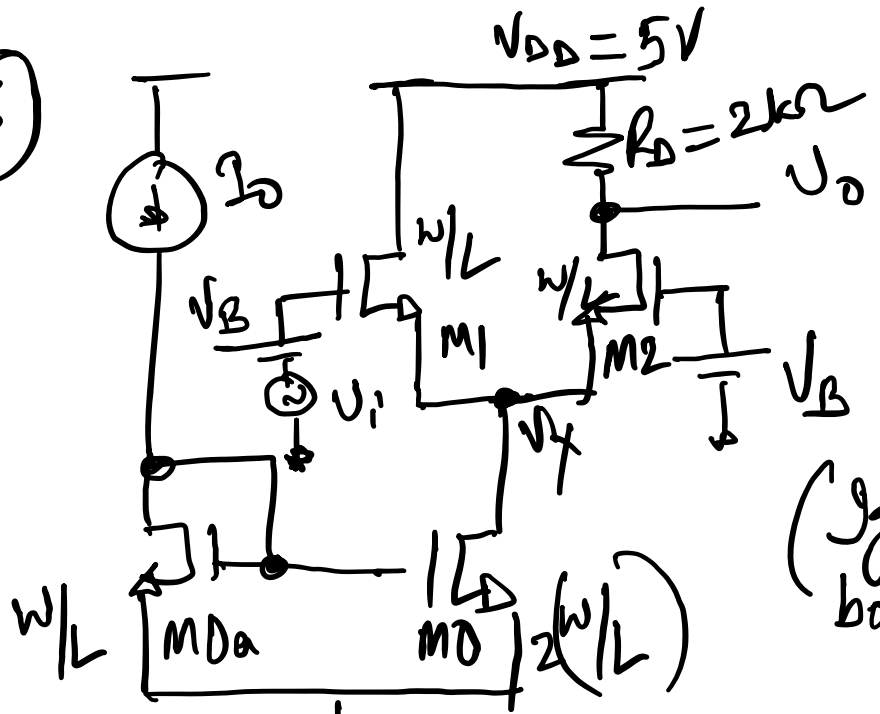
Size M2 and R_2 such that we can get max gain between V_o and V_i while keeping all transistors in saturation, and away from cutoff.

(5) Redo tutorial 6 using PMOSFETs.

You may assume $\mu_p C_{ox} = 100 \mu A/V^2$ for all transistors.

Also double the (W/L) for all transistors w.r.t tutorial 6.

(6)



(Ignore body effect)

$I_o = 1mA$ $\left(\frac{W}{L}\right) = 10$, $\mu_n C_{ox} = 0.2 mA/V^2$

$V_B = 3.5V$.

(a) Find the currents through all transistors.

(b) Neglecting CLM, find v_o/v_i, v_x/v_i.

(c) Find V_x.

(d) What happens if you reduce V_B? does the currents change

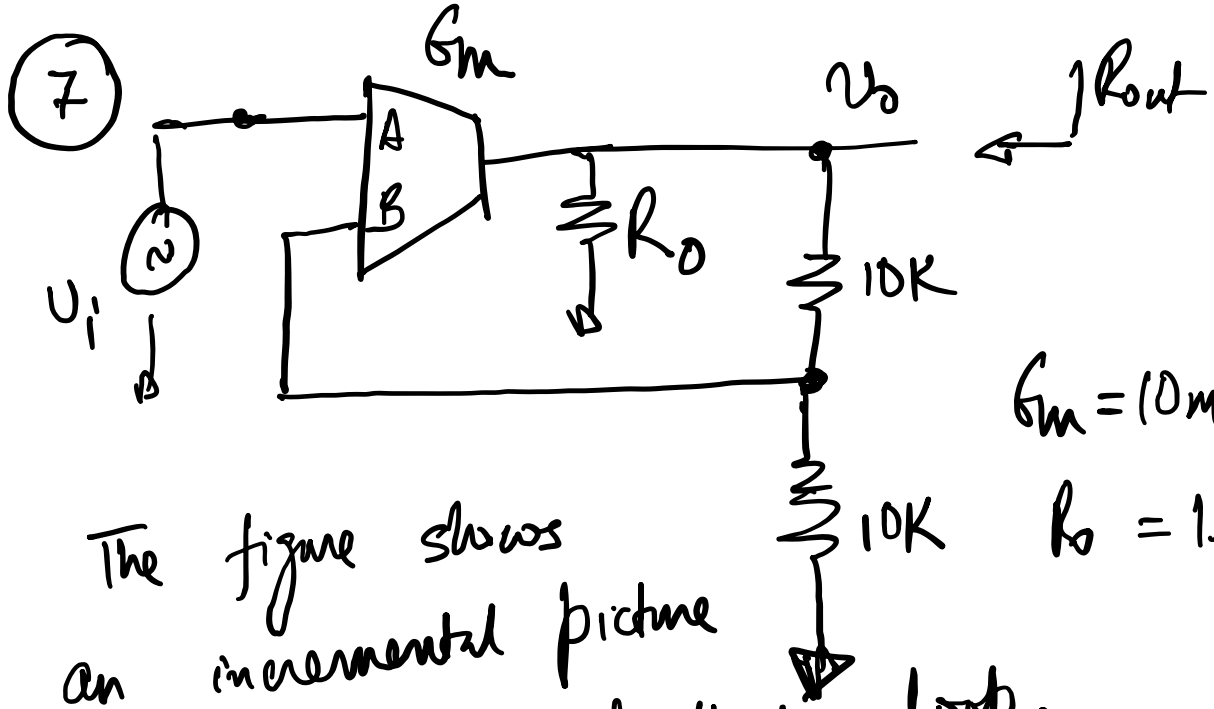
if you reduce V_B by 100mV? How low can V_B go before you start noticing any change in quiescent currents? Ignore CLM.

(e) Is there a $V_B(max)$ beyond which M1, M2 go out of saturation?

(f) If $v_i = V_p \sin(\omega t)$, find max V_p while keeping all transistors in saturation and away from cut-off.

(g) How does your analysis in (f) change if you $-V_i$ at the gate of M2 in addition to the existing input @ the gate of M1?

(7)



$G_m = 10mS$

$R_o = 1k\Omega$

The figure shows an incremental picture of a negative feedback loop.

(a) Find the +ve terminal of the G_m for the loop to be in negative feedback.

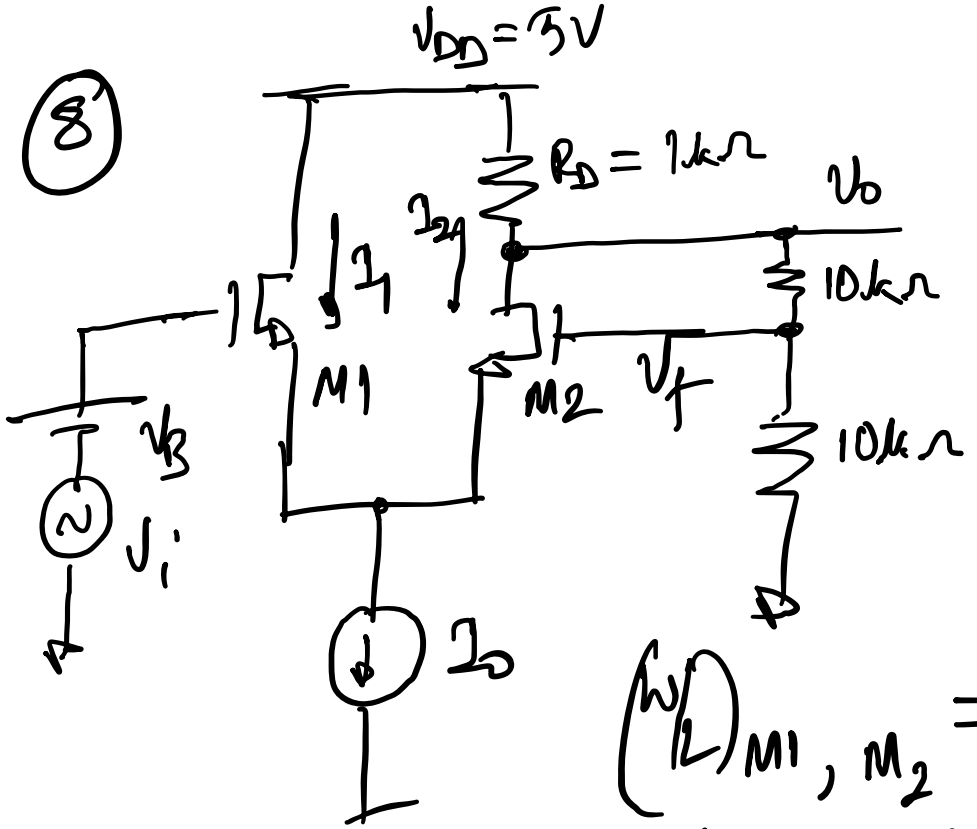
(b) Find V_o/V_i ?

(c) Find the loop gain. (Break @ the i/p of B)

(d) Find the steady state error if V_i is a step i/p of 10mV.

(e) Find R_{out} looking into the loop

as shown in the figure. Is Rout closer to R_D, or the fb resistors or $1/g_m$? Why?



$\left(\frac{W}{L}\right)_{M1,M2} = 640$

$I_D = 2mA$

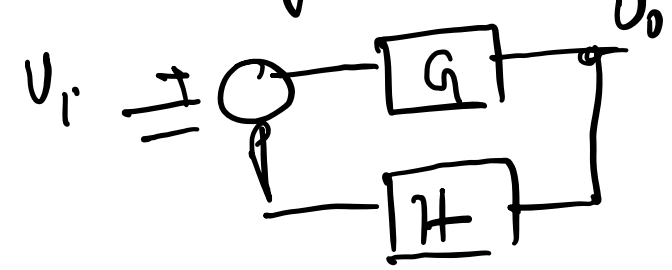
(a) Ignore CLM.

Find quiescent I_1 and I_2.

How close is I_1 and I_2 to $I_D/2$?

(b) Find the incremental loop gain of the fb loop. To do this, break the loop at the gate of M2, apply test voltage at the gate of M2 and observe the return voltage at the junction of the 10K resistors.

(c) If you model it as



what will G and H be?

(d) Find V_o/V_i from this model.