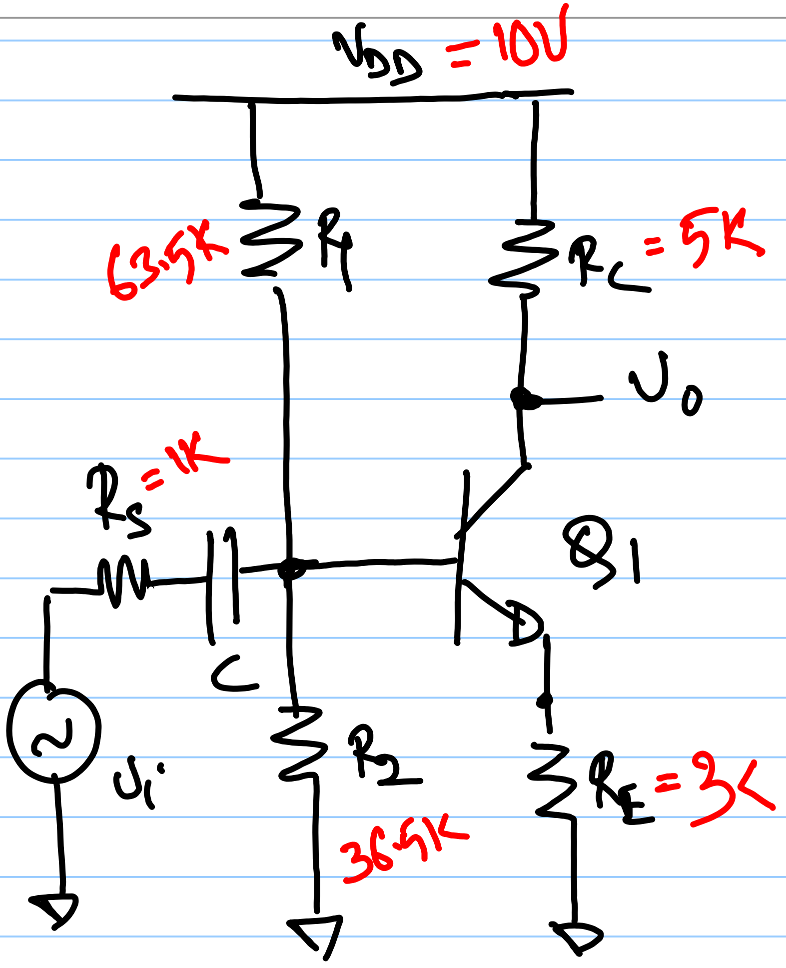
PROBLEM SET#9

①



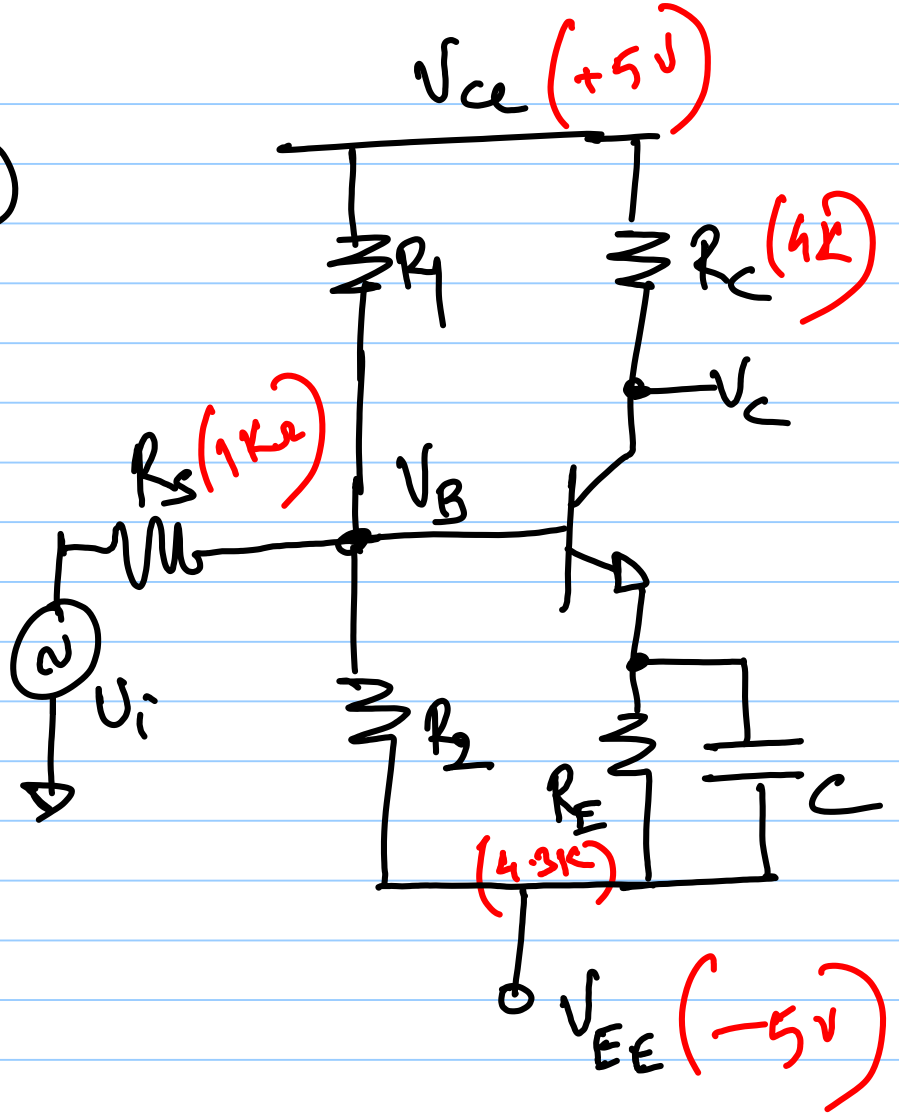
Q1 has a $\beta = 100$. (Assume $\beta = \infty$ for bias calculation) Assume $V_T = 25mV$, and C is large enough to be shorted at signal frequencies. (Assume $V_A = \infty$, and $V_{BE} = 0.65V$)

ⓐ Find v_o / v_i

ⓑ If $v_i = V_p \sin(\omega_0 t)$, find max V_p which keeps Q in active region and sufficiently on.

Use quiescent + Incremental model for your analysis.

②



$\beta = 100$, $V_T = 25\,mV$. Note that one terminal of the i/p source is grounded, but $V_{EE} = -5V$. (Assume $V_A = \infty$). Assume $\beta = \infty$ for biasing.

ⓐ Size R_1 and R_2 such that $V_{BQ} = 0V$, and $v_b \approx v_i$ for the following two cases.

ⓘ $C = 0$ ⓘⓘ $C = \infty$.

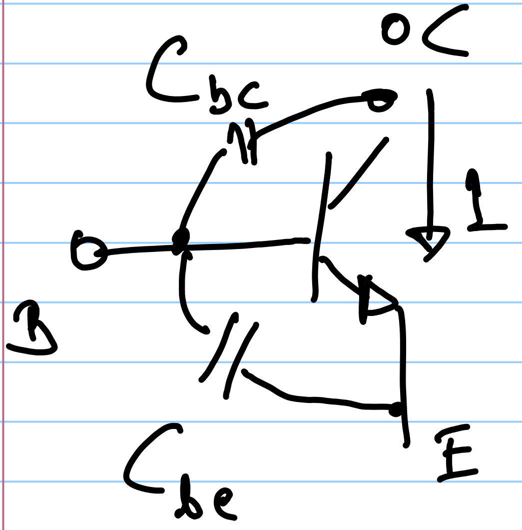
ⓑ Find the swing limits of v_i if $v_i = V_p \sin(\omega t)$.

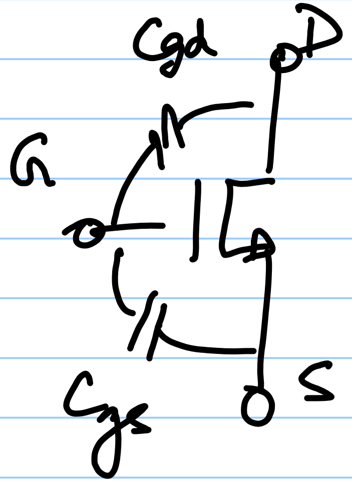
ⓒ What benifit does a -ve power supply have (like the case in the figure)?

ⓓ Find the time-constant associated with C.
How is it different from the expression that you get while using a MOSFET? What is the root cause behind it?

③ A diode has capacitances associated with its terminals.

∴ A BJT also has capacitances between its terminals.





BJT

$C_{be} = \frac{\tau_F I}{V_T}$

C_{bc} = depletion cap.

Generally

$C_{be} \gg C_{bc}$

(τ_F = Device constant)

MOSFET

$C_{gs} = \frac{2}{3} WL(V_{GS} - V_{tn})$ + Coverlap

C_{gd} = Coverlap.

Generally

$C_{gs} \gg C_{gd}$.

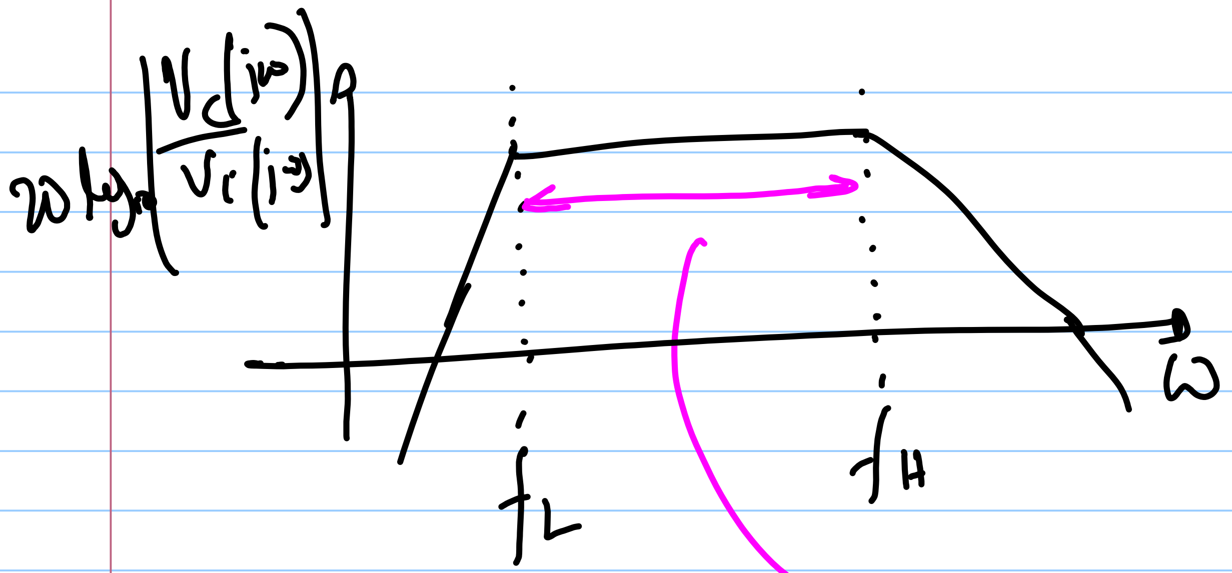
ⓐ Sketch the small signal model of a BJT with all the capacitances included.

ⓑ Find and sketch the frequency response of the amplifier in question 1; if a $C_L = 1pF$ is connected between V_C and ground.

Assume $C_{be} = 1pF$, and neglect C_{bc}.

Size C such that the lower cutoff frequency is 10X smaller than the higher cutoff frequency.

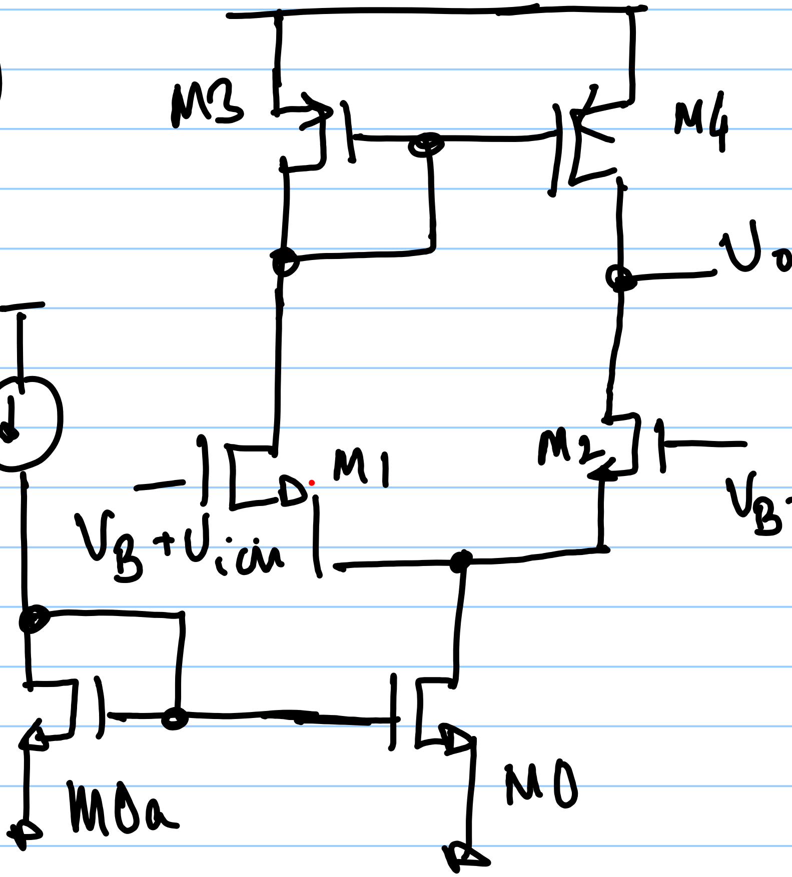
(fig. in next page)

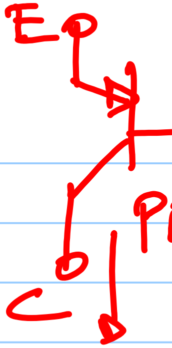


$f_L = f_H/10$

ⓒ What is the gain in the mid-band region, ie when $2\pi f_L \ll \omega_o \ll 2\pi f_H$?

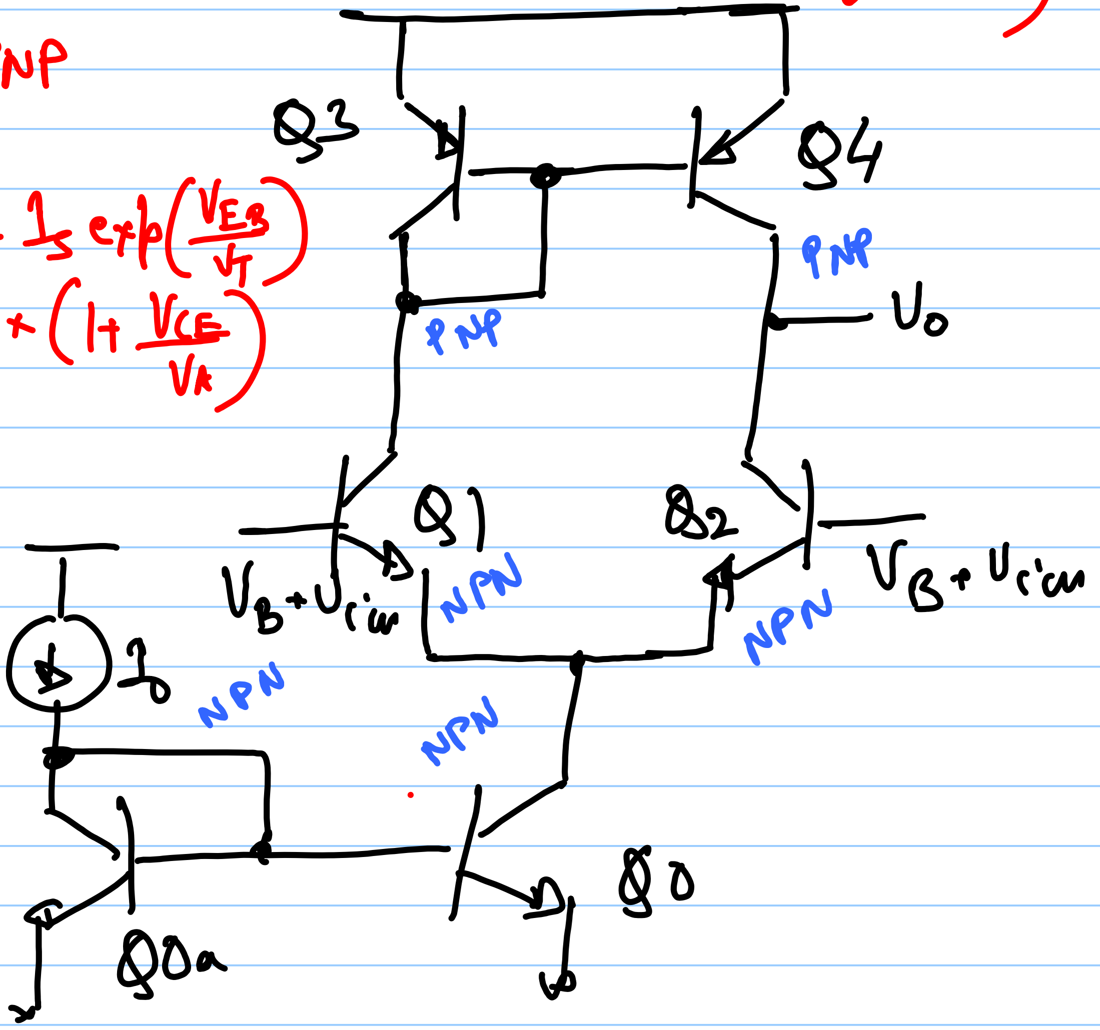
④





$\rightarrow I_B = \frac{I_C}{\beta}$ (Note the change in direction)

$$I_C = I_S \exp\left(\frac{V_{EB}}{V_T}\right) \times \left(1 + \frac{V_{CE}}{V_A}\right)$$



Assume all the MOSFETs and the BJTs are biased in saturation region and active region of operation respectively.

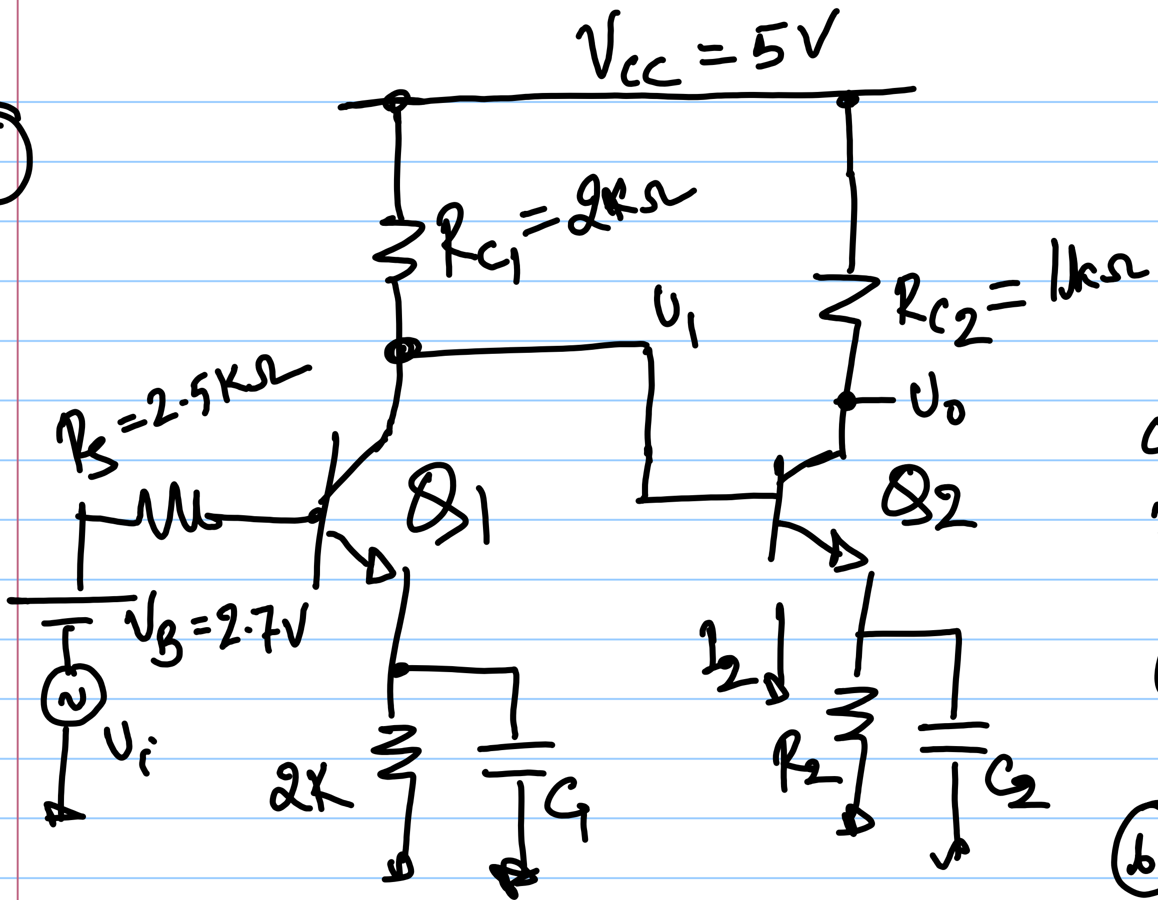
For MOSFETs neglect CLM for M1, M2, MOa, and consider CLM for all other transistors.

For BJTs assume $r_\pi = \infty$, (ie. $\beta = \infty$) for all transistors.

Neglect base width modulation (ie assume $V_A = \infty$) for Q1, Q2, QOa, and assume finite V_A for all other transistors.

Find v_o / v_{in}.

⑤



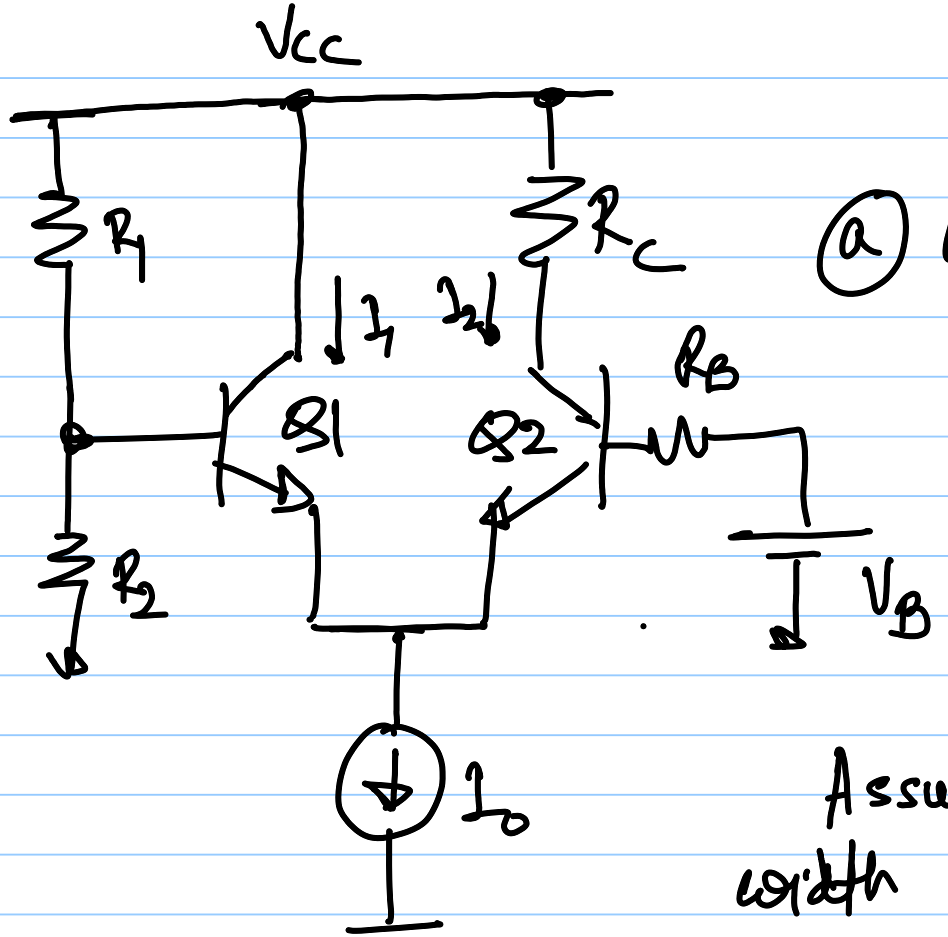
Assume $V_{BE} = 0.7V$ Neglect base current for Q-point calculation, but consider r_π in incremental model. Consider $\beta = 100$, $V_T = 25mV$

ⓐ Size R_2 such that $I_2 = 2mA$..

ⓑ Find v_o/v_i.

ⓒ If you don't want Q2 to load v_1, suggest necessary modifications to the network. (Think VCVS).

⑥



Q1 ≡ Q2.

ⓐ We want to ensure $I_1 = I_2$.

If $V_B = \frac{V_{cc} R_2}{R_1 + R_2}$

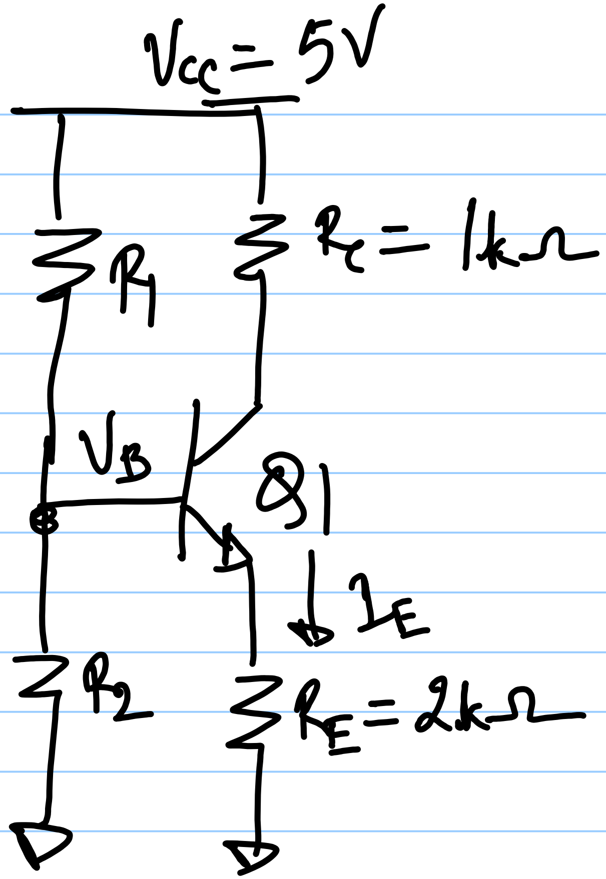
what value of R_B ensures

$I_1 = I_2 = I_o/2$?

Assume finite β, and neglect base width modulation. (i.e. $V_A = \infty$).

ⓑ Why does the answer make sense?

⑦

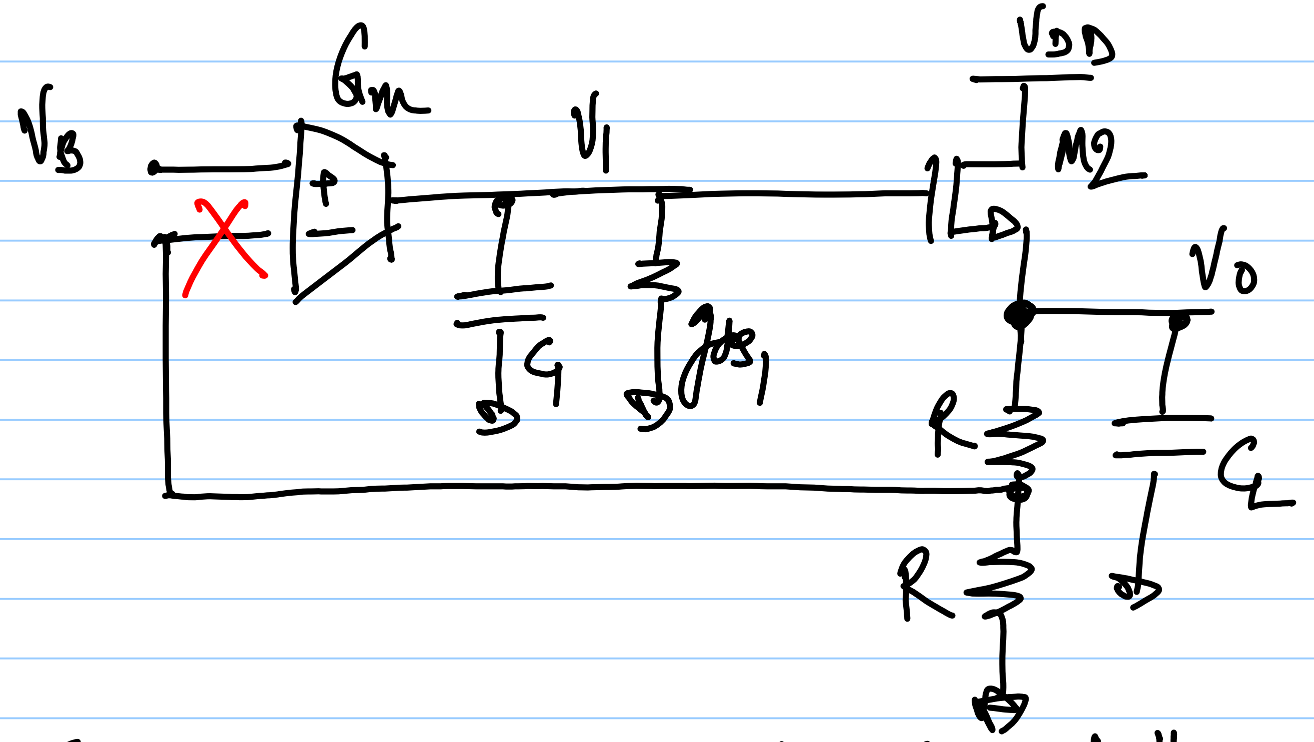


$\beta = 100$, $V_{BE} = 0.7V$.

ⓐ Find R_1, R_2 such that $I_E = 1mA$; and $r_\pi \gg (R_1 \| R_2)$.

Do not ignore base current for Q-point calculation.

⑧



$G_m / g_{ds1} = 100$, $G_m = 1mS$

$C_1 = 0.1\ pF$.

$R = 5k\Omega$.

Ignore CLM for M2.

$V_B = 1.5V$, $V_{DD} = 5V$

$V_{tn} = 500mV$

$\mu_n C_{ox} = 0.2 mA/V^2$.

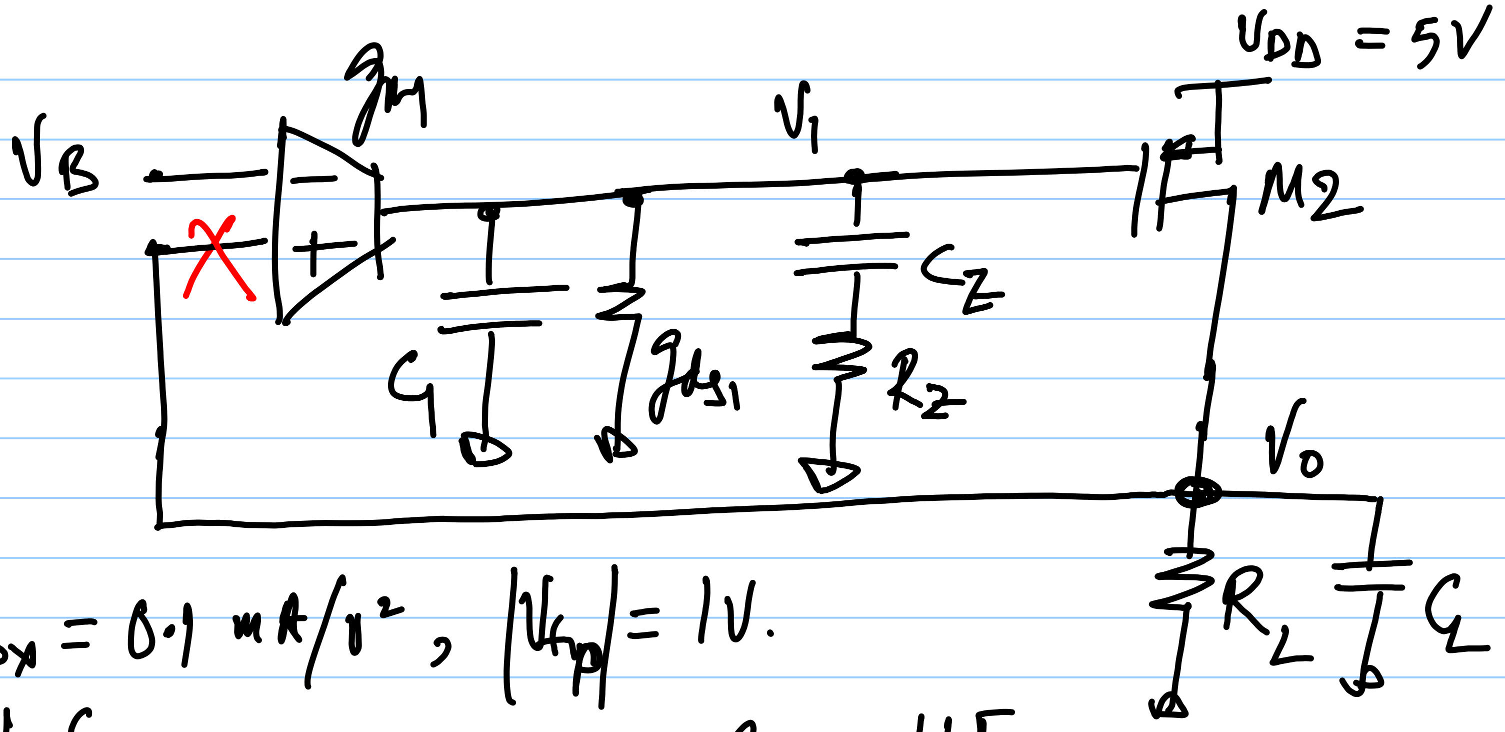
ⓐ What is the expected V_o if the loop has $L(0) \rightarrow \infty$

ⓑ Size M2 such that $V_1 = 4.5V$.

ⓒ What is the expression of the loop gain, $L(s)$. Break the loop @ X for your analysis

ⓓ What is the constraint on C_L, such that the $P_2 = 4\,\omega_{ugb}$, when ω_{ugb} = unity gain frequency of the loop, and P_2 is the pole associated with C_L. (Note that the loop needs to be broken at X for finding poles of the loop-gain).

⑨



$\mu_n C_{ox} = 0.1\ mA/V^2$, $|V_{tp}| = 1V$.

$g_{m1} = 1mS$

$g_{ds1} = 10\mu S$. $C_1 = 1pF$, $C_L = 1pF$,

$R_L = 1K\Omega$, $V_B = 4V$.

ⓐ Find the loop gain symbolically (Assume $g_{ds1} = 0$)

ⓑ Size M2 such that it is in saturation with a margin of 500mV.

ⓒ Size R_Z, C_Z such that the phase margin associated with the loop is 76°.
(Hint: Find all the poles and zeros of $L(s)$ explicitly, find ω_{ugb} from the loop gain and then calculate phase margin).