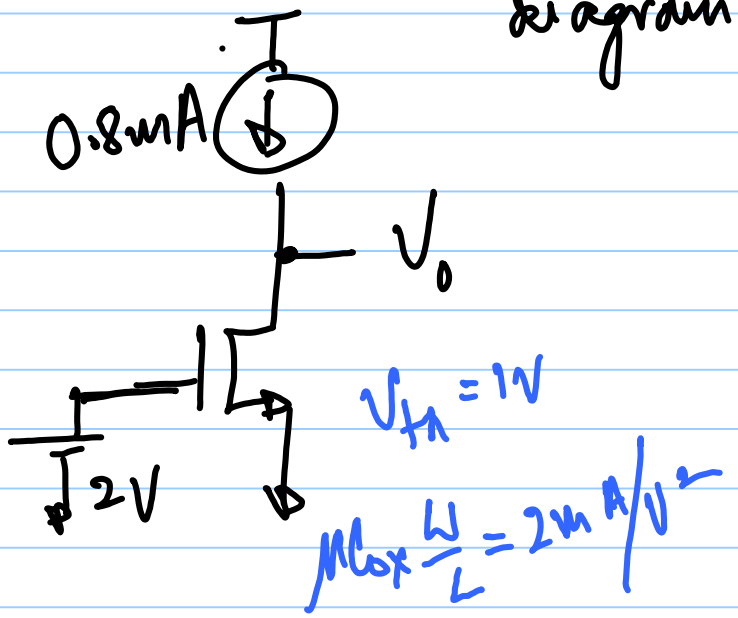
Home Assignment #2

Note Title 23-08-2022

(1) A designer decides to bias a transistor in the following manner. The transistor parameters are marked in the diagram.



(a) What is the region of operation?

(b) Find V_0.

(2) A MOS transistor is biased in saturation region. The designer observes that the g_m of the transistor increases linearly with W/L.

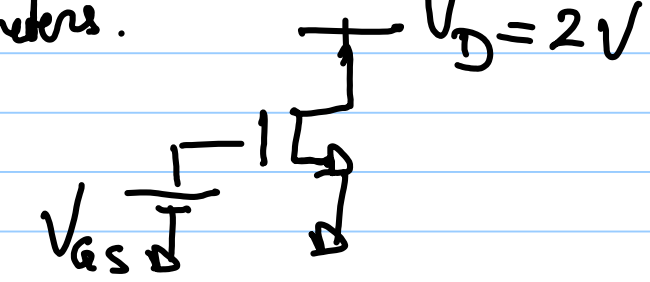
(#) Show a biasing scheme (with ideal voltages or current sources) which will lead to the above observation.

(3) Show a biasing scheme if the designer observes that $g_m \propto \sqrt{\frac{W}{L}}$

(4) A designer wants to increase the g_m of a transistor by 2× without changing the g_{ds}. Suggest a way of doing it. The transistor should be biased in saturation region of operation.

(5) A MOSFET has the following parameters.

$\mu C_{ox} \frac{W}{L} = 2\,mA/V^2$ $\quad V_{th} = 1V.$ $\quad \lambda = 0$

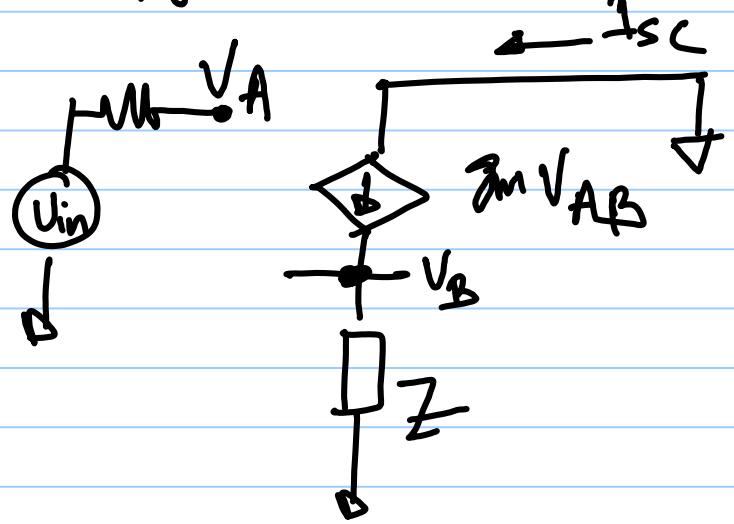


Plot g_m and g_{ds} wrt V_{GS} for $0 < V_{GS} < 4V$.

(6) A designer observes that the intrinsic gain (g_m/g_{ds}) decreases as she increases W/L. What is the biasing scheme that she is using? You can use ideal voltage and current sources if you find it necessary.

(7) Find the short-ckt currents for the following configurations.

(a)

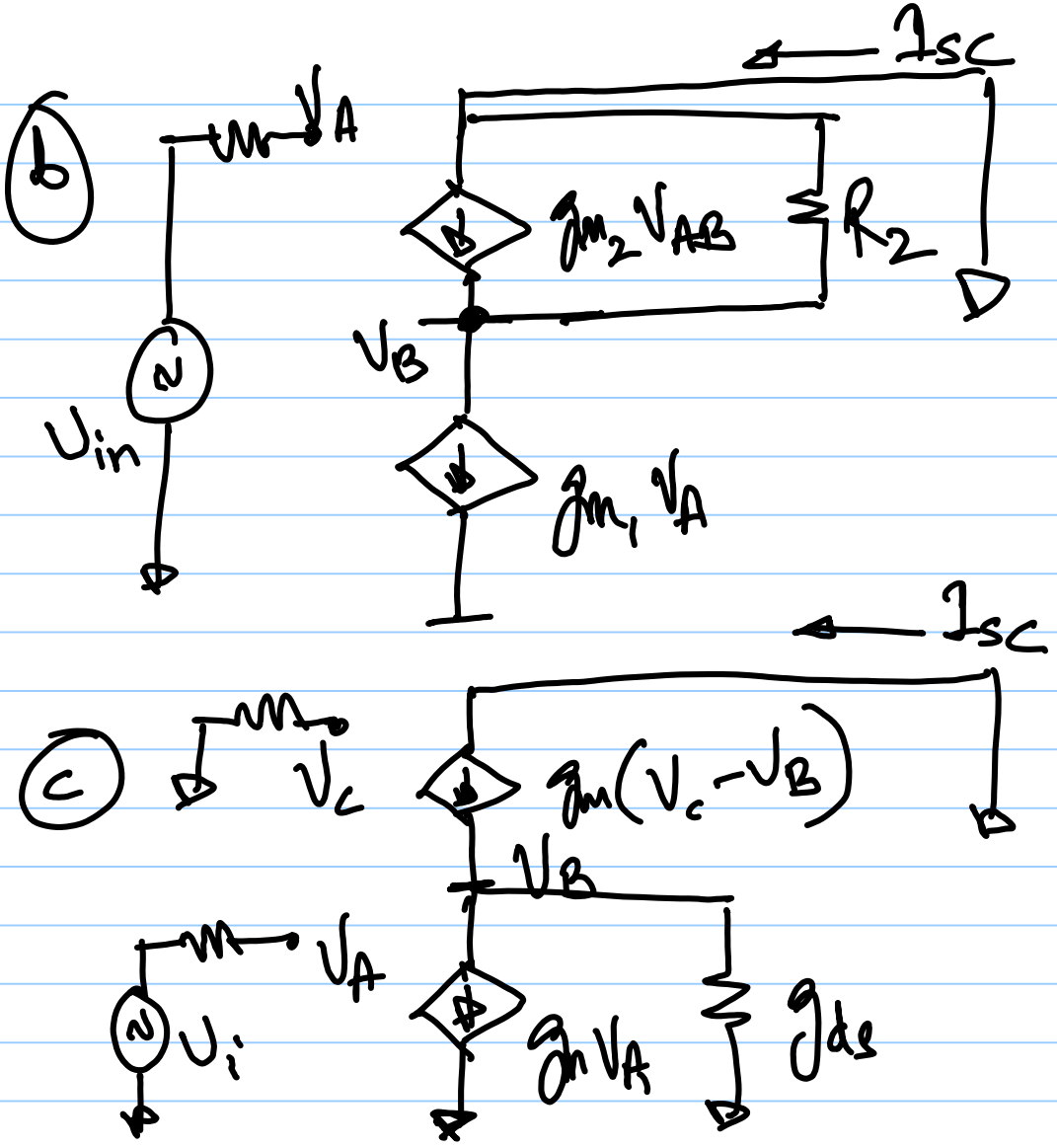


(i) $Z = R$

(ii) $Z = 1/sC$

(iii) Z is a parallel combination of R and C

(iv) Plot I_{sc} wrt ω for $0 \leq \omega \leq \infty$ using Bode approximation


b
V_A
I_{sc}
$g_{m_2} V_{AB}$
R_2
V_B
V_{in}
$g_{m_1} V_A$
c
V_c
I_{sc}
$g_m(V_c - V_B)$
V_B
V_A
V_i
$g_m V_A$
g_{ds}

8

: Consider a two port network as discussed in the class. Assume $I_1 = 0$, and $I_2 = \alpha(V_1 - V_{th})^n / V_A^n$ for $V_1 > V_{th}$ where α, V_{th} and V_A are positive constants and $n \geq 2$ is a positive integer and $I_2 = 0$ for $V_1 < V_{th}$. Assume that a resistance R_L is connected to port 2.

a) : Find the incremental voltage gain between ports 1 and 2.

b) : Find the second and third harmonic distortion at the output if an input $V_{th} + V_{ov} + V_p \sin(\omega t)$ is applied at port 1, where $V_p < V_{ov}$ and $V_{ov} > 0$.

c) : For identical linear voltage gains (same HD1), comment on the strengths of the distortion components as you increase n.

d) : To achieve identical HD1, comment on the quiescent voltage requirements at port 1 as you increase n.