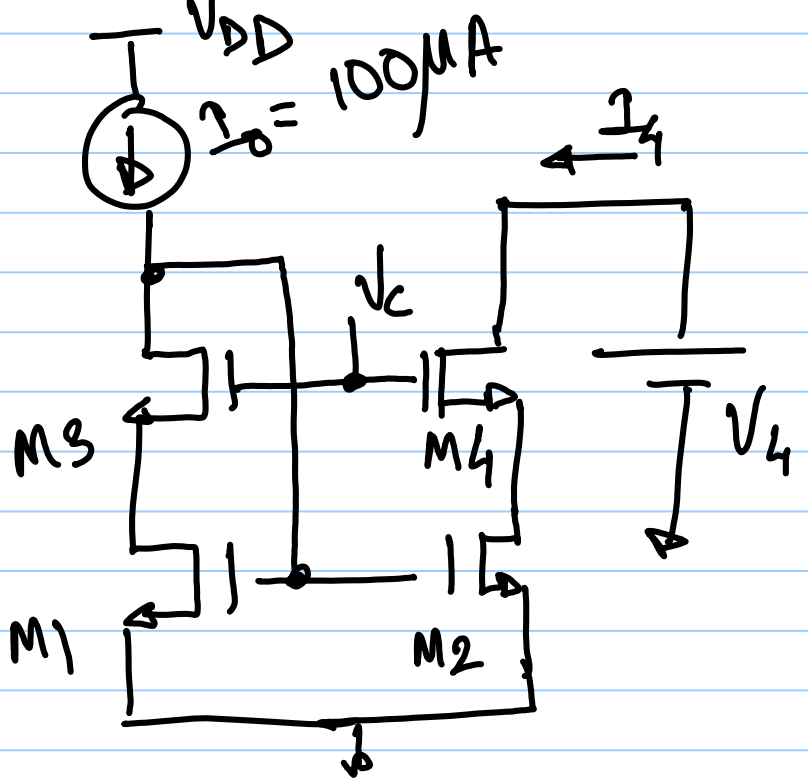
PROBLEM SET 4-(b)

Note Title 15-10-2022

(5) Simulate the following circuit using the 180nm PDK available on the course website. (Use LT-spice)



$V_{DD} = 1.8V$

$L = 180nm$ for all transistors.

Generate V_c using the method shown in the class.

Keep W identical for M1–M4.

(a) What is the minimum V_4 for which all transistors remain in saturation? Give reasons in your design as to why you cannot lower your V_4 beyond the value that you have mentioned above.

Tabulate the operating conditions for M1-M4 to support your claim

(b) Plot I_4 with respect to V_4 while varying V_4 between $V_{4(min)}$ to V_{DD}. What is the slope?

(c) Remove M3, M4 from the figure and repeat parts (a) and (b).

(d) How does the slope of I_4 vs. V_4 compare between the two configurations that you simulated. What are the theoretically calculated values of the same.

To find the theoretical values use the small signal parameters from the DC operating point. You don't need to extract the μC_{ox} parameters.